HIGH-VOLTAGE MIXED-SIGNAL IC

UC1611

160COM x 240SEG Matrix LCD Controller-Driver
w/ 16-shade per pixel

PP Specifications
Revision 0.81

June 17, 2003

ULTRACHIP

The Coolest LCD Driver. Ever.!!

TABLE OF CONTENT

UC1611

Single-Chip, Ultra-Low Power
160COM x 240SEG Matrix
Passive LCD Controller-Driver

INTRODUCTION

UC1611 is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images, with well balanced gray shades.

In addition to low power SEG and COM drivers, UC1611 contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation, and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, Smart Phones, PDA, and other battery-operated palmtop devices and/or portable instruments.

FEATURE HIGHLIGHTS

- Single-chip controller-driver supports 160x240 STN LCD, 16-shade-per-pixel with gamma compensated modulation, and hardware dither support for 64-shade image display.
- Soft-ICON: Partial scroll function to support programmable graphics ICON or scroll bar.
- Support both row ordered and column ordered display buffer RAM access
- Support industry standard parallel interface (8080 or 6800) in 8-bit and 4-bit mode.
- Support industry standard 3-wire SPI and 4-wire SPI serial interface.
- Special driver structure and gray shade modulation scheme produce near crosstalk free image, with low power consumption for all display patterns.
- Support the 80-80-80 partial display function on the SEG driver.
- Fully programmable Mux Rate, partial display window, Bias Ratio, and Line Rate allow many flexible power management options.
- Four software programmable frame rates (125Hz, 150Hz, 175Hz, 200Hz). Support the use of fast Liquid Crystal material for speedy LCD response.
- 4 software-programmable temperature compensation coefficients.
- On-chip Power-ON Reset and Software RESET command make RST pin optional.
- Self-configuring 10x charge pump with on-chip pumping capacitor requires only 5 external capacitors to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- V_{DD} (digital) range: 2.5V ~ 3.3V
  V_{DD} (analog) range: 2.5V ~ 3.3V
  LCD V_{OP} range: 6.5V ~ 16.5V
- Available in gold bump dies
  Bump pitch: 50μM min.
  Bump gap: 18μM min.

ORDERING INFORMATION

Product ID	Description
UC1611xGAB	Gold bumped die.
UC1611xFBB	COF. 140uM pitch.

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

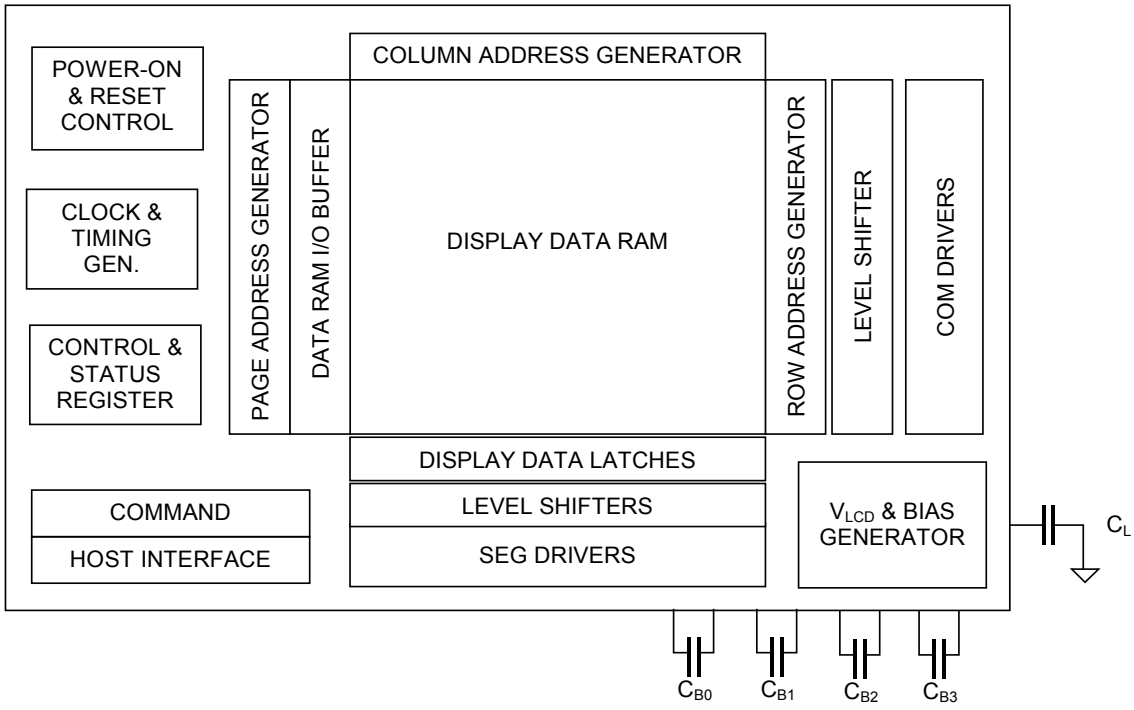
BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of UltraChip's delivery. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and quality their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Pins	Description
			MAIN POWER SUPPLY
V_{DD} V_{DD2} V_{DD3}	PWR		V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND		Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for V_{SS} and V_{SS2}.
			LCD POWER SUPPLY
V_{S1} V_{S2} V_{CM}	PWR		When two or more UC1611 chips are used in Master/Slave configuration, connect all chips' $V_{LCD-IN}/_{OUT}$ together, and connect their corresponding V_{S1} / V_{S2} / V_{CM} together. Leave these pins open when Master/Slave feature is not used.
V_{BIAS}	I		This is the reference voltage to generate the actual SEG driving voltage. V_{BIAS} can be used to fine tune VLCD by external variable resistors. Please refer to Application Note for such application. In COF application, connect a small bypass capacitor between V_{BIAS} and V_{SS} to reduce noise.
V_{B0+} V_{B0-} V_{B1+} V_{B1-} V_{B2+} V_{B2-} V_{B3+} V_{B3-}	PWR		LCD Bias Voltages. These are the voltage source to provide SEG driving current. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. The resistance of these four traces directly affects the SEG driving strength of the resulting LCD module. Minimize the trace resistance is critical in achieving high quality image.
S_{B0+} S_{B0-} S_{B1+} S_{B1-} S_{B2+} S_{B2-} S_{B3+} S_{B3-}	I		The sensor pins for C_{BX} capacitors. Connect these pins to proper C_{BX} pads. These signals each can tolerate input resistance of up to 2K Ohm, so, narrow ITO/COF traces can be used. The noise on these pins affects the accuracy of SEG driving voltage level. To minimize noise caused by V_{BX}-C_{BX} charging current, the trace resistance shared between $V_{BX+/-}$ and $S_{BX+/-}$ should be minimized.
V_{LCD-IN} $V_{LCD-OUT}$	PWR		High voltage LCD Power Supply. Connect these pins together. A bypass capacitor C_L should be connected between V_{LCD} and V_{SS}. Keep the trace resistance under 300 Ohm.

Note:

Recommended capacitor values:

C_B: ~100x LCD load capacitance or 5µF (2V), whichever is higher.

C_L: 0.1~0.5uF (20V) is appropriate for most applications.

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM[1:0]</td><td>I</td><td>2</td><td>Bus Mode: The interface bus mode is determined by BM[1:0] and D[7] by the following relationship:
<table>
<tr><th>BM[1:0]</th><th>D[7]</th><th>Mode</th></tr>
<tr><td>11</td><td>Data</td><td>6800/8-bit</td></tr>
<tr><td>10</td><td>Data</td><td>8080/8-bit</td></tr>
<tr><td>01</td><td>0</td><td>6800/4-bit</td></tr>
<tr><td>00</td><td>0</td><td>8080/4-bit</td></tr>
<tr><td>01</td><td>1</td><td>3-wire SPI (S9)</td></tr>
<tr><td>00</td><td>1</td><td>4-wire SPI (S8)</td></tr>
</table></td></tr>
<tr><td>CS1
CS0</td><td>I</td><td>2</td><td>Chip Selection. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, D[7:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td></td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1611 has built-in Power-ON Reset and a software Reset command, RST pin is not required for general chip operation.

When RST pin is used, insert a ~10K Ohm resistor to improve noise filtering (a small filter capacitor is provided on-chip). When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD</td><td>I</td><td></td><td>Control data or Display data Selection for read/write operation.
In S9 modes, CD pin is not used, connect CD pin to V_{SS}.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td></td><td>WR[1:0] controls the read/write operation of the host interface. See Host Interface section for more detail.

In parallel mode, WR[1:0] meaning depends on whether the interface is in 6800 mode or 8080 mode. In serial interface modes, these two pins are not used. Connect them to V_{SS}.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td></td><td>Bi-directional bus for both serial and parallel host interfaces.

In serial modes, connect D[0] to SCK, D[3] to SDA, and D[7] to V_{DD} or V_{SS}. When BM[1:0]=”LL”, the bus mode is defined by D[7]
<table>
<tr><th></th><th>BM=1x
(Parallel)</th><th>BM=0x
(Serial)</th></tr>
<tr><td>D0</td><td>D0</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td>–</td></tr>
<tr><td>D2</td><td>D2</td><td>–</td></tr>
<tr><td>D3</td><td>D3</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td>–</td></tr>
<tr><td>D5</td><td>D5</td><td>–</td></tr>
<tr><td>D6</td><td>D6</td><td>–</td></tr>
<tr><td>D7</td><td>D7</td><td>S8/S9</td></tr>
</table>
Connect unused pins to V_{SS}.</td></tr>
</table>

Name	Type	Pins	Description
HOST INTERFACE			
M/S	I		Master / Slave Mode Selection “H”: Slave configuration “L”: Master configuration, or Stand-alone
DISP_ON PUMP_DN SCLK	I/O		When multiple UC1611 chips are used in Master-Slave configuration, connect all chips’ DISP_ON / PUMP_DN / SCLK together. Leave these pins open circuit in other situations.
LCD DRIVER OUTPUT			
SEG1 ~ SEG240	HV		SEG (column) driver outputs. Support up to 240 columns. Leave unused drivers open-circuit.
COM1~ COM160	HV		COM (row) driver outputs. Support up to 160 rows. Leave unused drivers open-circuit.
MISC. PINS			
V_{DDX} V_{SSX}	O		Auxiliary V_{DD}, V_{SS}. These pins serve auxiliary functions such as providing mechanical balance, or to facilitate chip configurations in COF applications. These pins should not be used as main V_{DD}, V_{SS} connection for the chip. Connect V_{SSX} to the main V_{SS} externally is a good practice, but optional.
TST4	I		Test control. Connect to GND.
TST[2:1]	I/O		Test I/O pins. Leave these pins open during normal use.
TP[3:1]	I		Test control. Leave these pins open during normal use.

Note: Several control registers will specify “0-based index” for COM and SEG electrodes. In those situations, $COM_{\underline{X}}$ or $SEG_{\underline{X}}$ will correspond to index $\underline{X}$-1, and the value ranges for those index registers will be 0~159 for COM and 0~239 for SEG.

CONTROL REGISTERS

UC1611 contains registers that control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meaning and their default value. Commands supported by UC1611 will be described in the next two sections. A summary table comes first and then followed by a detailed instruction-by-instruction description.

Name: The symbolic reference of the register.
Note that, some symbol names refer to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	8	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value are between 0 (for no scrolling) and (159 – FL). Setting SL outside of this range causes undefined effect on the displayed image.
FL	4	0H	Fixed lines. The first (FLx2) lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two regions: one scrollable, one non-scrollable.
CR	8	0H	Return Column Address. Useful for cursor implementation.
CA	8	0H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	7	0H	Display Data RAM Page Address (Used in Host to Display Data RAM access)
BR	2	2H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 5 01b: 10 **10b: 11** 11b: 12
TC	2	0H	Temperature Compensation (per ^{o}C). **00b: -0.05%** 01b: -0.10% 10b: -0.15% 11b: -0.20%
GN	2	3H	Gain, coarse setting of V_{BIAS} and V_{LCD}
PM	6	10H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
OM	2	–	Operating Modes (Read Only) 10b: Sleep 11b: Normal 01b: (Not used) 00b: Reset
BZ	1	–	Busy with internal processes (reset, changing mode, etc.) OK for Display RAM read/write access.
RS	1	–	Reset in progress, Host Interface not ready
PC	4	DH	Pump Control and LCD panel loading. PC[1:0]: 00b: LCD: <20nF **01b: LCD: 20~28nF** 10b: LCD: 28~40nF 11b: LCD: 40~56nF PC[3:2]: 00b: External V_{LCD} 01b: Internal V_{LCD} (Low V_{LCD}, only use when BR=5) **11b: Internal V_{LCD}** (Standard)
APC0	8	FDH	Advanced Product Configuration. For UltraChip only. Please do not use.

Name	Bits	Default	Description
DC	5	0H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[4:2]: Display ON/OFF (Default **000**) Each bit controls a set of SEG (column) drivers (80-80-80). When DC[4:2] is set to "HLH", the chip is turned into a 160x160 controller-driver and the programmers' view of CA becomes 0~159. Setting DC[4:2] flag does not affect the content of display RAM.
AC	4	1H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default **1: ON**) AC[1]: Auto-Increment order **0: Column (CA) first** 1: Page (PA) first AC[2]: PID: PA (page address) auto increment direction (**0:+1** 1:-1) AC[3]: CUM: Cursor update mode, (Default: **0: OFF**) when CUM=1, CA increment on write only, wrap around suspended
MC	8	EFH	Max. CA. CA wrapping boundary: when CA+1 = MC, CA will be reset to 0. The proper value range for MC is 0~239 or 0~159, depends on the value of DC[4:2]. The chip's behavior is undefined when MC is out of these ranges.
CEN DST DEN	8 8 8	9FH 00H 9FH	COM scanning end (last COM with full line cycle, 0 based index). Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ⩾ DEN ⩾ DST+ 9
LC	10	0D0H	LCD Control: LC[0]: MSF: MSB First mapping Option (Default:: **OFF**) LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: **OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default:: **OFF**) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 20 Klps 01b: 24 Klps **10b: 28 Klps** 11b: 32 Klps (Frame-Rate = Line-Rate / Mux-Rate) LC[6:5]: Gray Scale selection 00b: black/white 01b: 8 gray scale **10b: 16 gray scale** 11b: 64 gray scale LC[7] : Reserved (Default:: 1b) LC[9:8] : Partial Display Control **0xb: Disable** Mux-rate = CEN+1 DST, DEN not used. 10b: Enable Mux-rate = CEN+1 11b: Enabled Mux-rate = DEN-DST+1

COMMAND TABLE

The following list of host commands is supported by UC1611

C/D: 0: Control 1: Data
W/R: 0: Write cycle 1: Read cycle

\# Effective Data bits
– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	BZ	MX	MY	RS	WA	DE	PM[7:6]		Get Status	N/A
4	Set Column Addr. LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Addr. MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5	Temp. Compensation.	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b: -0.05%/°C
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC [1:0]	01b: 20-28nF
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC [3:2]	11b
8	Set Adv. Control	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0] where R = 0 or 1	N/A
	(double byte command)	0	0	#	#	#	#	#	#	#	#		
9	Set Max CA	0	0	0	0	1	1	0	0	1	0	Set MC	239
	(double byte command)	0	0	#	#	#	#	#	#	#	#		
10	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0
11	Set Page Address LSB	0	0	0	1	1	0	#	#	#	#	Set PA[3:0]	0
	Set Page Address MSB	0	0	0	1	1	1	#	#	#	#	Set PA[7:4]	0
12	Set Gain and Potentiometer	0	0	1	0	0	0	0	0	0	1	Set {GN[1:0], PM[5:0]}	PM=16 GN=11b
	(double byte command)	0	0	#	#	#	#	#	#	#	#		
13	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	0: Disable
14	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
15	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
16	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
17	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
18	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
19	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	0
20	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
21	Set Gray Scale Mode	0	0	1	1	0	1	0	0	#	#	Set LC[6:5]	10b=16 shade
22	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
23	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
24	Set test control	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
25	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b: 11
26	Reset cursor update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	N/A
27	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	N/A
28	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[7:0]	159
		0	0	#	#	#	#	#	#	#	#		
29	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[7:0]	0
		0	0	#	#	#	#	#	#	#	#		
30	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[7:0]	159
		0	0	#	#	#	#	#	#	#	#		

* Other than commands listed above, all other bit patterns may result in undefined behavior.

COMMAND DESCRIPTIONS

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

Please refer to command (21) *Set Gray Scale Mode* for detail data write sequence.

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Write/Read Data Byte (command 1, 2) operation accesses display buffer RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will increase or decrease automatically after each bus cycle, depending on the setting of Access Control (AC) register. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of page (MC), and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches end of page, CA will be reset to 0 and PA will be increased or decreased by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 79), PA will be wrapped around to the other end of RAM and continue.

(3) GET STATUS SUMMARY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	BZ	MX	MY	RS	WA	DE	PM[7:6]	

Status flag definitions:

BZ: Busy with internal process. When BZ=1 host interface can access if RS=0.
MX: Status of register LC[1], mirror X.
MY: Status of register LC[2], mirror Y.
RS: Reset in progress. If RS=1, host interface will be inaccessible.
WA: Status of register AC[0] . Automatic column/page wrap around.
DE: Display Enable flag. DE=1 when display is enabled.
PM: Setting of V_{BIAS} potentiometer control register

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[4:7]	0	0	**0**	**0**	**0**	**1**	CA7	CA6	CA5	CA4

Set the SRAM column address for read/write access.

CA possible value: **0-239**

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Compensation TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} Temperature compensation coefficient (%-per-degree-C) for all 4 temperature compensation curves.

Temperature compensation curve definition:
00b= -0.05%/^{o}C 01b= -0.10%/^{o}C 10b= -0.15%/^{o}C 11b= -0.20%/^{o}C

(6) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition: 00b=<20nF **01b**=20~28nF 10b=28~40nF 11b=40-56nF

(7) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

00b=External V_{LCD} 01b= Internal V_{LCD} (only use when BR=5) **11b**= Internal V_{LCD} (standard)

(8) SET ADVANCED PRODUCT CONFIGURATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[1:0] (Double byte command)	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	R
	0	0	APC register parameter							

For UltraChip only. Please do NOT use.

(9) SET MAX COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MC[7:0] (Double-byte command)	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**0**
	0	0	MC[7:0]							

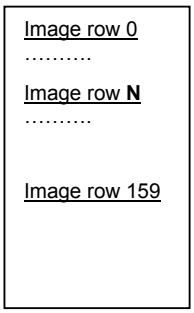
Set the wrap-around boundary of auto increment of column address. The RAM column address will reset to 0 (WA=1) or stop increment (WA=0) after column address reaches the value of MC[7:0]. The proper value range of MC is 0~159 for DC[4:2] = “101” and 0~239 for other DC[4:2] settings.

(10) SET SCROLL LINE

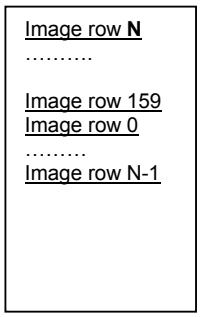
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[4:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[7:4]	0	0	**0**	**1**	**0**	**1**	SL7	SL6	SL5	SL4

Set the number of line to scroll. Possible value = **0** ~ (159-2xFL)

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and (159-2xFL). FL is the register value programmed with Set Fixed Lines command.



SL=0



SL=N

(11) SET PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address LSB PA [3:0]	0	0	**0**	**1**	**1**	**0**	PA3	PA2	PA1	PA0
Set Page Address MSB PA [6:4]	0	0	**0**	**1**	**1**	**1**	-	PA6	PA5	PA4

Set SRAM page address for read/write access.

Possible value = **0** ~ 79

(12) SET GAIN AND POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Gain and Potentiometer	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
GN [1:0] PM [5:0] (Double byte command)	0	0	GN1	GN0	PM5	PM4	PM3	PM2	PM1	PM0

Program Gain (GN[1:0]) and Potentiometer (PM[5:0]). See Section LCD Voltage Setting for detail information.

Effective range of GN = 0 ~ **3** PM value = **0 ~ 63**

(13) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Control LC [9:8]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	LC9	LC8

This command is used to control partial display function.

LC[8:7] : 0Xb: Disable Partial Display, Mux-Rate = CEN+1, (DST, DEN are not used.)
10b: Enable Partial Display, Mux-Rate = CEN+1
11b: Enable Partial Display, Mux-Rate = DEN-DST+1

(14) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or CA will increment by one step.

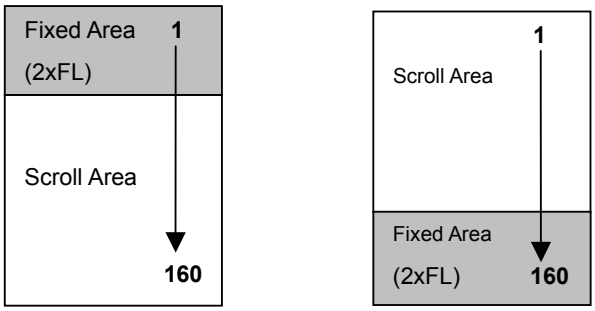
AC[1]: Auto-Increment order
0 : column (CA) increases (+1) first until CA reach CA boundary, then PA will increase by (+/-1).
1 : page (PA) increases (+/-1) first until PA reach PA boundary, then CA will increase by (+1).

AC[2]: PID, page address (PA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary(CA=MC), PID controls whether page address will be adjusted by increasing +1 or -1. If WA is 0, the column address will stay in MC value and the page address will stay unchanged.

(15) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines FL [3:0]	0	0	**1**	**0**	**0**	**1**	FL3	FL2	FL1	FL0

The Fixed Lines function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. Set Fixed Lines command will define the fixed area, which will not be affected by the SL scroll function. When MY= **0**, the fixed area covers the top 2xFL rows; when MY=1, the bottom 2xFL rows. One example of the visual effect on LCD is illustrated in the figure below.



(16) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate)

00b: 20.0KHz 01b: 23.2kHz **10b:** 27.2KHz 11b: 32.0KHz
(Klps: Kilo-line per second)

(17) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(18) SET INVERSE DISPLAY (PXV)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

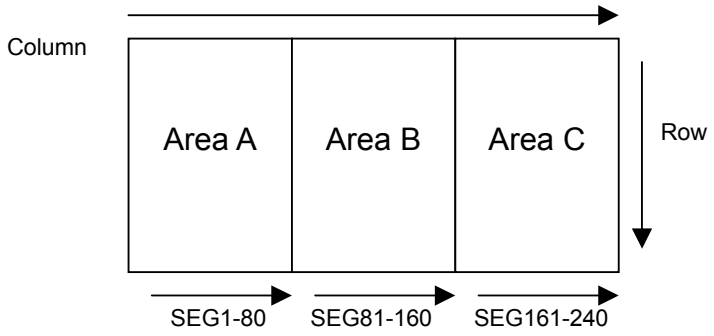
Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

(19) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC[4:2]	0	0	**1**	**0**	**1**	**0**	**1**	DC4	DC3	DC2

This command is for programming registers DC[4:2], which are used to control 3 sets of column (SEG) drivers.

DC[2] controls column drivers SEG1~SEG80 (area a), DC[3] controls column drivers SEG81~SEG160 (area b), and DC[4] controls column drivers SEG161~SEG240 (area c). When one or more bits of DC[4:2] are set to 1, UC1611 will first exit from Sleep mode, restore the power, and then turn on COM (row) drivers and corresponding SEG (column) drivers.



(20) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC[2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	MSF

Set LC[2:0] for COM (row) mirror (MY), SEG (column) mirror (MX) and MSB first or LSB first options (MSF).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

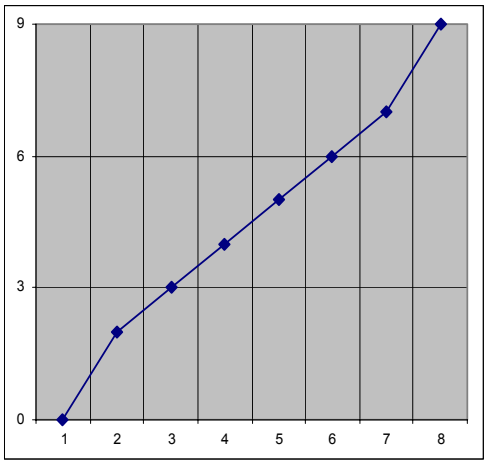
MX is implemented by selecting the CA or 239-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

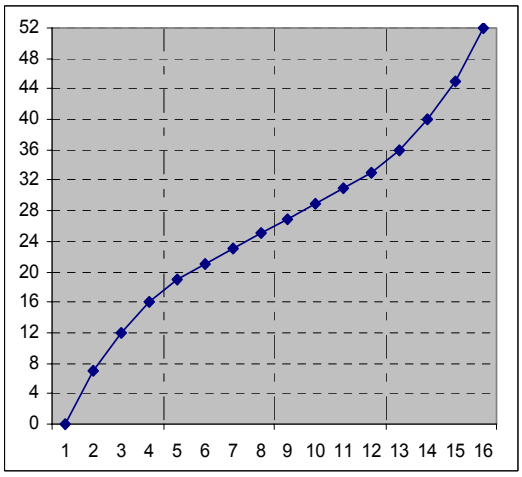
MSF is implemented by MSB-LSB swapping. The operation is determined by LC[6:5], as described in Set Gray Scale Mode command below.

(21) SET GRAY SCALE MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Gray Scale Control LC [6:5]	0	0	**1**	**1**	**0**	**1**	**0**	**0**	LC6	LC5

UC1611 has two gray shade modulation modes: an 8-shade mode and a 16-shade mode. The modulation curves are shown below. Horizontal axes are the gray shade data. The vertical axes are the ON-OFF ratio. 9/9 is 100% ON for 8-shade mode, 52/52 is 100% ON for 16-shade mode. Together with on-chip dithering and bit extension circuits, UC1611 supports 4 gray scale modes as described below





Depending on the setting of LC[6:5], UC1611 will convert one or two bytes of input data into a 8-bit buffer (B[7:0]) by dithering, 0-extension, or direct mapping. B[7:0] is then stored into display RAM depending on the setting of MSF (LC[0]) and will be used to control the gray shade of two pixels of neighboring pixel rows, one on each simultaneously.

LC[6:5]	Gray-Scale	Sequence	D7	D6	D5	D4	D3	D2	D1	D0
00	B/W	1 write	B[7:4]				B[3:0]			
01	8-gray	1 write	B[7:4]				B[3:0]			
10	16-gray	1 write	B[7:4]				B[3:0]			
11	64-gray	1st write	Dither mapping D[7:2] => B[7:4]						-	-
		2nd write	Dither mapping D[7:2] => B[3:0]						-	-

MSF	RAM_D[7:4]	RAM_D[3:0]
0	B[7:4]	B[3:0]
1	B[3:0]	B[7:4]

(22) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(23) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

(24) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT (Double byte command)	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
	0	0	Testing parameter							

This command is used for UltraChip production testing. For UltraChip only. Please do NOT use.

(25) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition: 00b= 5 01b=10 **10b**=11 11b=12

(26) RESET CURSOR MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Reset Cursor Update Mode AC[3]=0 CA=CR	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

This command is used to reset Cursor Update Mode function.

(27) SET CURSOR MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=1 CR=CA	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**

Set Cursor Mode command is used to turn on Cursor Update Mode function. AC[3] will be set to 1 and register CR will be set to the value of register CA

When AC[3]=1, column address (CA) will only increase with write RAM operation but not with read RAM operation. The address CA wrapping around will also be suspended no matter what WA setting is. The purpose of this combination of features is to support “Read-Modify-Write” for cursor implementation.

Reset Cursor Mode command will clear Cursor Update Mode flag (AC[3]=0). CA will be restored to previous CA value that is stored in CR, while CA and PA increment will return to its normal condition.

(28) SET COM END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN (Double byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
	0	0	*CEN* register parameter							

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD.

(29) SET DISPLAY START

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST (Double byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
	0	0	*DST* register parameter							

This command programs the starting COM electrode, which has been assigned a full scanning period, and which will output active COM scanning pulses.

(30) SET DISPLAY END

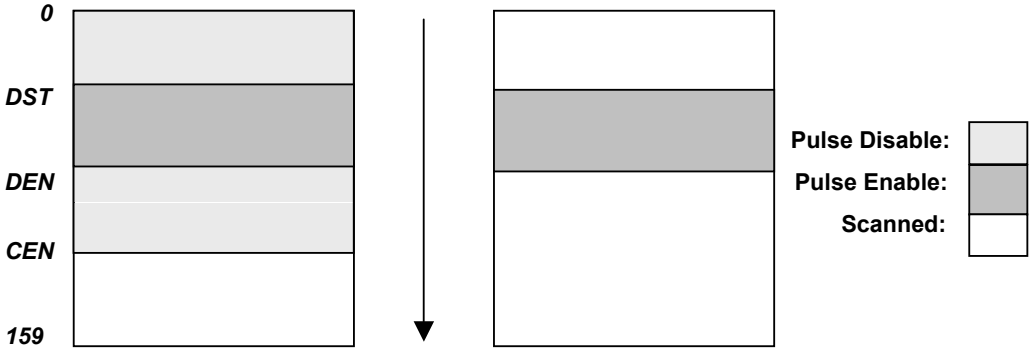
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(Double byte command)			*DEN* register parameter							

This command programs the ending COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse. CEN, DST, and DEN are 0-based indexes of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[9]=1, two partial display modes are possible with UC1611:

LC[8]=1: Ultra-low-power mode (if Mux-Rate ⩽ 32, set BR=5, PC[3:2]=01b).
Set up according to application preference - lower V_{LCD} consumes less power while higher V_{LCD} provides better vision quality.
LC[8]=0: Full gray shade low power mode (no change to BR and PM)

When LC[9:8]=11b, the Mux-Rate is narrowed down to just the range between DST and DEN. When Mux-Rate is under 32, set BR=5, PC[3:2]=01b, and adjust PM to reduce VLCD and achieve the lowest power consumption. When LC[9:8]=10b, the Mux-Rate is still CEN+1. This is achieved by suppressing only the scanning pulses, but not the scanning time slots, for COM electrodes that is outside of DST~DEN. Under this mode, the gray-scale quality of the display is preserved, while the power can be reduced significantly. In either case, DST/DEN defines a small subsection of the display that will remain active while shutting down all the rest of the display to conserve energy.



LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate (*MR*) is completely software programmable in UC1611 via the register CEN.

Combined with low power partial display mode and a low bias ratio of 5, UC1611 can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$BR = V_{LCD}/V_{BIAS}$,
where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=160), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally cannot maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1611 supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	5	10	11	12

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per °C	–0.05	–0.10	–0.15	–0.20

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2]. For good product reliability, it is recommended to keep V_{LCD} under 16.5V over the entire operating range.

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the BR register setting. The values are provided in the table in the next page,

PM is the numerical value of PM register,

T is the ambient temperature in °C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

Gray shade and color STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

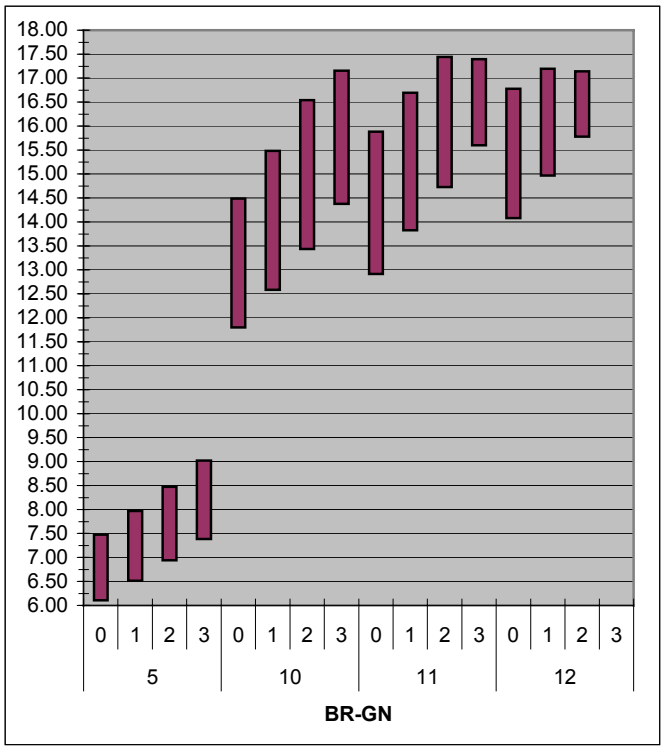
For best result, software-based approach for V_{LCD} adjustment is the recommended method for V_{LCD} fine-tuning.

For applications where mechanical manual fine-tuning of V_{LCD} becomes necessary, then V_{BIAS} pin may be used with an external trim pot to fine tune the V_{LCD}. Please refer to Application Notes for more detailed discussion on this subject.

LOAD DRIVING STRENGTH

UC1611's power supply circuits are designed to handle LCD panels with load capacitance up to 40nF at VLCD=15V when V_{DD2} = 2.8V. For larger LCD panels or higher VLCD use higher $V_{DD2/3}$.

V_{LCD} QUICK REFERENCE



BR	GN	CV0 (V)	CPM (mV)	VLCD Range (V)	
5	0	6.1008	21.80	6.1008	7.4742
	1	6.5108	23.10	6.5108	7.9661
	2	6.9417	24.30	6.9417	8.4726
	3	7.3814	26.00	7.3814	9.0194
10	0	11.8007	42.60	11.8007	14.4845
	1	12.5858	45.90	12.5858	15.4775
	2	13.4340	49.30	13.4340	16.5399
	3	14.3757	44.10	14.3757	17.1540
11	0	12.9139	47.10	12.9139	15.8812
	1	13.8279	45.50	13.8279	16.6944
	2	14.7246	43.10	14.7246	17.4399
	3	15.6002	28.50	15.6002	17.3957
12	0	14.0782	42.90	14.0782	16.7809
	1	14.9706	35.30	14.9706	17.1945
	2	15.7804	21.60	15.7804	17.1412
	~~3~~	~~16.2344~~	~~9.40~~	~~16.2344~~	~~16.8266~~

NOTE:

- For best product reliability, keep V_{LCD} under **16.5**V under all temperature and operating conditions, and avoid condition “BR=12 and GN=3”.
- For V_{LCD} under 15V (25°C), $V_{DD2/3}$ = 2.8V or higher is recommended.
  For V_{LCD} above 15V (25°C), $V_{DD2/3}$ = 3.0V or higher is recommended.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

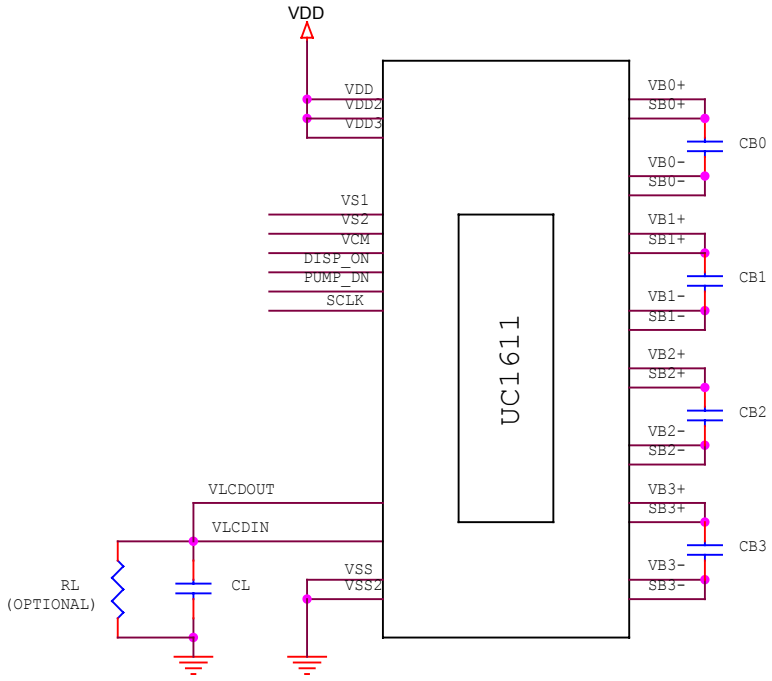


FIGURE 1: Reference circuit using internal Hi-V generator circuit

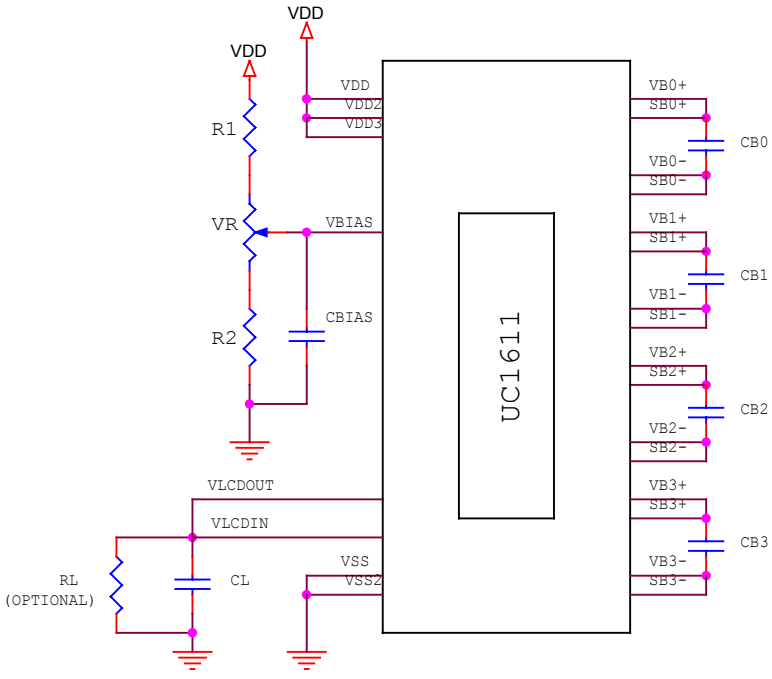


FIGURE 2: Reference circuit for VLCD fine tuning

Note

- Recommended component values:
  - C_B: ~100x LCD load capacitance or 5uF (2V), whichever is higher.
  - C_L: 0.1~0.5uF (20V) is appropriate for most applications.
  - R_L: 10M ohm. Acts as a draining circuit when the power is abnormally shut down.
- To ensure consistency of LCM contrast, VLCD fine tuning is highly recommended.
  C_{BIAS}: 0.1uF for noise filtering. Minimize wiring trace from this capacitor to UC1611.

  Since the value of R1/R2 depends strongly on the GN, PM, BR settings, and vary slightly depends on the value of V_{DD2}, each LCM design will need to be optimized individually.

  The following is the recommended procedures for selecting R1, R2 and VR values.

  Step 1: Adjust LCM for the best contrast with C_{BIAS}, but without R1, R2, VR.
  Step 2: Measure V_{BIAS} voltage
  Step 3: Select VR and R2 (recommend to start with VR=500K, R2=200K)
  Step 4: Calculate R1 by: R1 = R2 x (V_{DD2}/V_{BIAS} -1)
  Step 5: Install R1, R2, VR. The "neutral position" of VR is at V_{BIAS}/V_{DD2}.
  Step 6: Test the fine tuning range by adjusting VR over the full range.
  Step 7: If adjustment range is too narrow, reduce R2, … and vise versa.
  Step 8: Repeat from Step 4.
- Step 2, "Measure V_{BIAS}" is a very critical step. Since the purpose of this circuit is to maximize the contrast consistency of mass production units, please fine tuning GN, PM, BR across at least 150~200 LCM units (without the V_{LCD} adjustment circuit), before finalizing the values of PM, GN, BR. The average V_{BIAS} should be measured after PM, GN and BR is selected and finalized.
- Please note that, the "Neutral position" of the VR (the position with minimum VLCD adjustment) is located at V_{BIAS}/V_{DD2}, not the center. Relative to this "Neutral position", the circuit produced by above procedure will have equal V_{LCD} adjustment range of +N% ~ -N% for the average V_{LCD}.
- Please avoid situations where the adjustment of the VR can push UC1611 out of its safe V_{LCD} operation range. If this happens, then it will be possible for the MP operators to damage the LCM by adjusting the VR.
- Since the value of V_{DD2} can affect the adjustment of the VR, please apply V_{DD2} that is intended to be used in the final application during the mass production V_{LCD} tuning process.
- Due to its minor sensitivity to the value of V_{DD2}, this V_{LCD} tuning circuit may not be suitable for "standard product" where the actual V_{DD2} value can vary far over 5% from the design V_{DD2} value. For such applications, please use a Zener diode, such as Hitachi HZU3LL, to replace V_{DD2} as the power source for this V_{LCD} fine tuning circuit.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1611 contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 72, frame rate is calculated as:

Frame rate = Line-Rate / Mux-Rate.

When LC[9:0]=11b, and Mux-Rate is under 72 (or under 36), the system clock is automatically scaled down by 2 (or 4) to reduce power consumption.

Line rate will also automatically scale down by ~30% when switching from 64/16-gray-shade mode to 8-gray-shade mode.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Frame rate ⩾ 150Hz is recommended for 16-shade mode. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[4:2]). When SEG drivers are in idle mode, their outputs are high-impedance (open circuit). When COM drivers are in idle mode, their outputs are connected to V_{SS}.

DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where x = 1~160, refers to the COM driver for the x-th row of pixels on the LCD panel.
The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO), and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[4:2] via *Set Display ON* command.

- DC[2] controls column drivers SEG1~SEG80,
- DC[3] controls SEG81~SEG160, and
- DC[4] controls SEG161~SEG240.

When all 3 bits of DC[4:2] are set to OFF (logic “0”), both SEG and COM drivers will become idle and UC1611 will put itself into Sleep Mode to conserve power.

When one or more bits of DC[4:2] are set to ON, the DE flag will become “1”, and UC1611 will first exit from Sleep mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM drivers and proper SEG drivers.

160X160 CONFIGURATION

UC1611 can be used as a 160x160 controller-driver by setting DC[4:2] to “HLH”. When thus set, all resources for SEG81~SEG160, including RAM data corresponding to these SEG drivers, will be placed into idle and become inaccessible. This is particularly effective when using standard COF UC1611 in applications that require only 160 SEG drivers.

Setting of DC[4:2] does not affect the content of display RAM. To format the screen as 160x160 display, refresh the display RAM. The CA will automatically skip over 81~160 when DC[4:2] is set to HLH.

ALL PIXELS ON (APO)

When set, this flag will force all active SEG drivers to output On signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, active SEG drivers will output the inverse of the value it received from the display buffer RAM. This flag has no impact on data stored in RAM.

PARTIAL SCROLL

The control register FL specifies a region of rows those are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can be used to implement fixed region when the other part of the display is scrolled by SL.

GRAY SCALE CONTROL

Four (4) gray Scale options are supported by UC1611. System programmers may set the option via command *Set Gray Scale Mode*. Refer to the Command Descriptions section for details.

LAYOUT CONSIDERATIONS FOR COM SIGNALS

Under 16-gray-shade mode, the COM scanning pulses of UC1611 can be as short as 17µs. Since COM distortion can lead to reduction of effective duty factor of the LCM, it is critical to control the RC delay of COM signal to minimize distortion of COM scanning pulse.

For the best image quality, limit the worst case RC delay of COM signal as calculated below.

$$RC_{COM} = (R_{ROW} / 3 + R_{COM} + R_{OUT}) \times C_{ROW}$$
$$RC_{COM\text{-}MAX} \leqslant 1.2uS$$

where

- C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.
- R_{ROW}: ITO resistance over one row of pixels within the active area
- R_{COM}: COM routing resistance from IC to the active area (COF+ITO routing)
- R_{OUT}: COM driver output impedance

In case $RC_{COM\text{-}MAX}$ exceed the above constraint significantly, please make sure

$$| RC_{COM\text{-}MAX} - RC_{COM\text{-}MIN} | < 0.6uS$$

so that the COM scan pulse distortions from the top of the screen to the bottom of the screen are uniform.

For 8-gray-shade mode, the COM scanning pulse is about 35% slower than the 16-gray-shade mode. Therefore, the two constraints described above can be relaxed by 1/3 respectively to

$$RC_{COM} \leqslant 1.6uS$$
$$| RC_{COM\text{-}MAX} - RC_{COM\text{-}MIN} | < 0.8uS$$

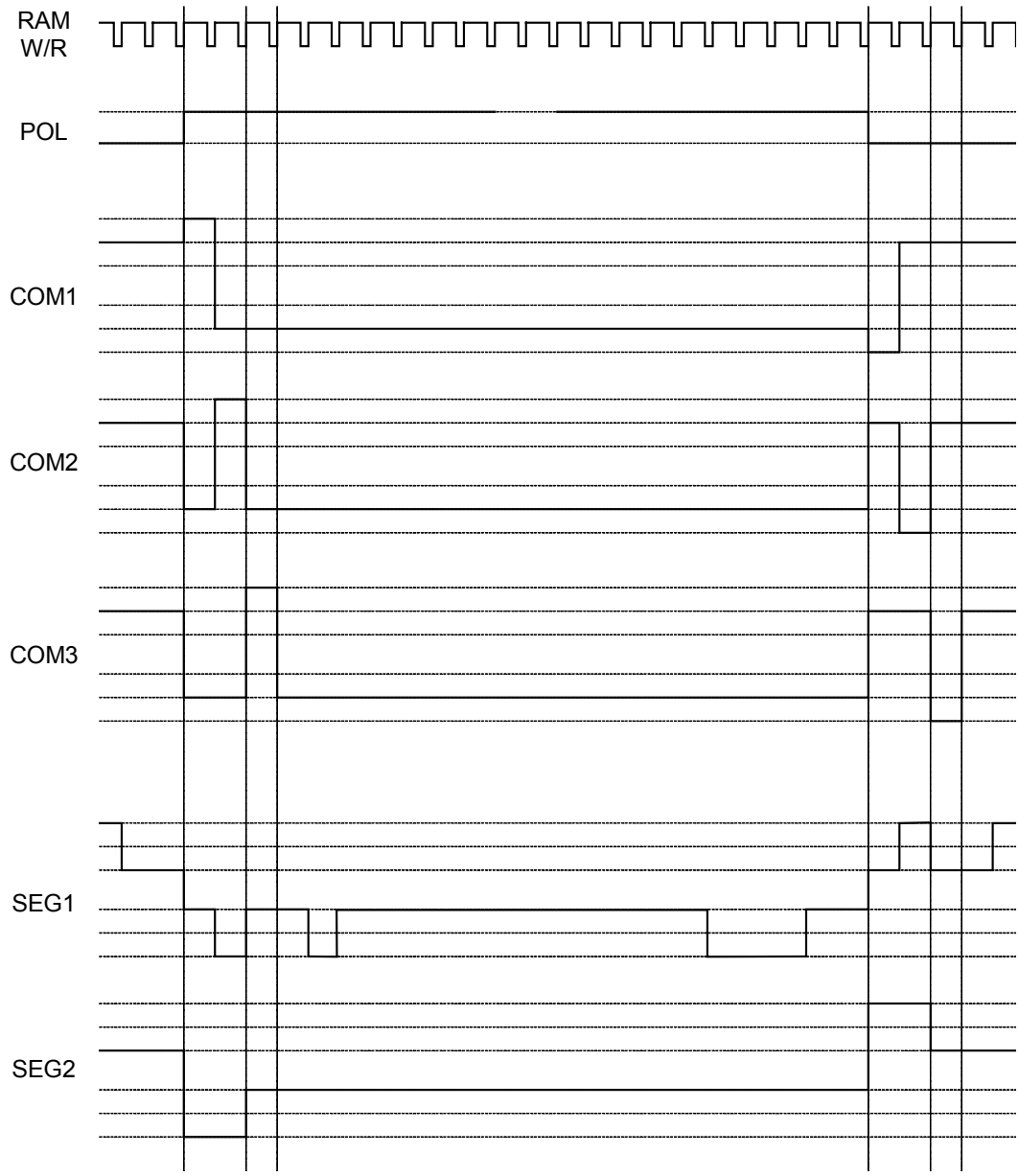


FIGURE 3: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1611 supports two parallel bus protocols, in either 8-bit of 4-bit bus width, and two serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

Bus Type		8080		6800		4wr SPI (S8)	3wr SPI (S9)
Width		8-bit	4-bit	8-bit	4-bit	Serial	
Access		Read/Write				Write Only	
Control & Data Pins	BM[1:0]	10	00	11	01	00	01
	D[7]	Data	0	Data	0	1	1
	CS[1:0]	Chip Select					
	CD	Control/Data				Control/Data	–
	WR0	$\overline{WR}$		R/$\overline{W}$		–	–
	WR1	$\overline{RD}$		EN		–	–
	D[6:4]	Data	–	Data	–	–	–
	D[3:0]	Data	Data	Data	Data	D0=SCK, D3=SDA	

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

Table 3: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1611 internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in 8-bit mode or 4-bit mode, by either *Set CA,* or *Set PA* command, a dummy read cycle needs to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

8-BIT & 4-BIT BUS OPERATION

UC1611 supports both 8-bit and 4-bit bus width. The bus width is determined by pin BM[1].

4-bit bus operation exactly doubles the clock cycles of 8-bit bus operation, MSB followed by LSB, including the dummy read, which also requires two clock cycles.

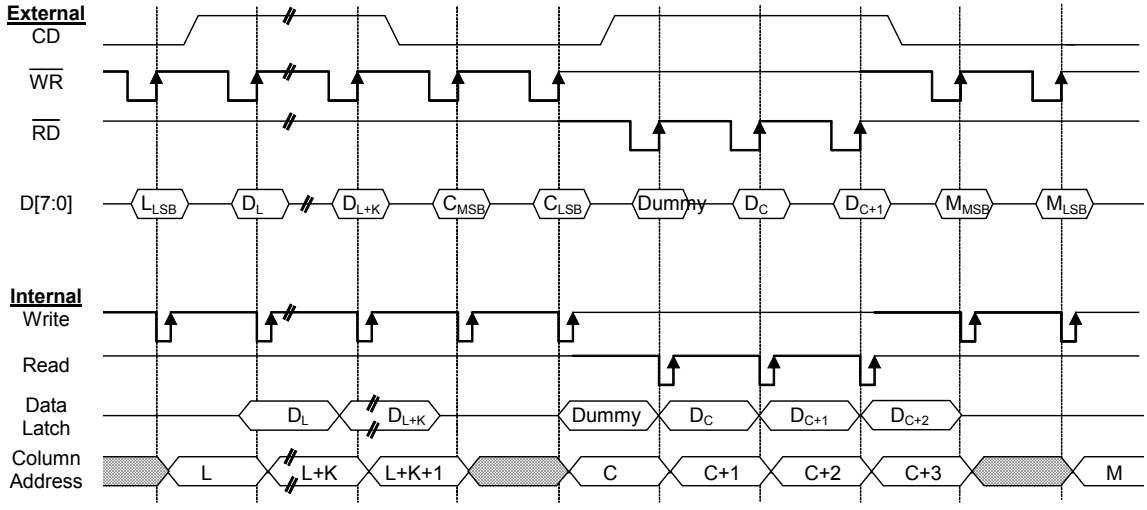


FIGURE 4: 8 bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1611 supports two serial modes, 4-wire SPI mode (S8), and 3-wire SPI mode (S9). Bus interface mode is determined by the wiring of the BM[1:0] and D7. See configuration table in the beginning of this section for more detail.

4-WIRE SERIAL INTERFACE (S8)

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse.

Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

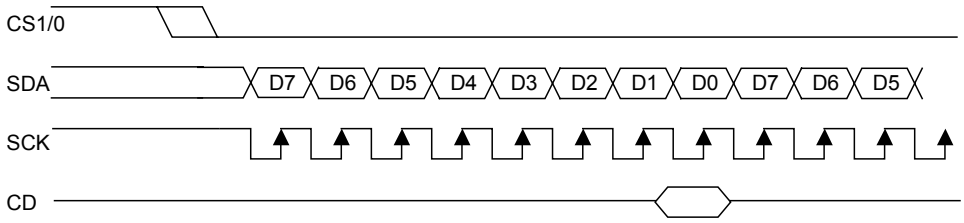


FIGURE 5.a: 4-wire Serial Interface (S8)

3-WIER SERIAL INTERFACE (S9)

Only write operations are supported in 3-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}.

The toggle of CS0 (or CS1) for each byte of data/command is recommended but optional.

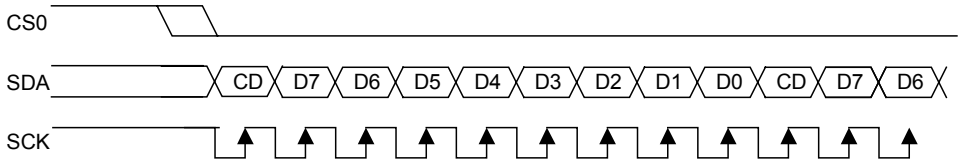


FIGURE 5.b: 3-wire Serial Interface (S9)

HOST INTERFACE REFERENCE CIRCUIT

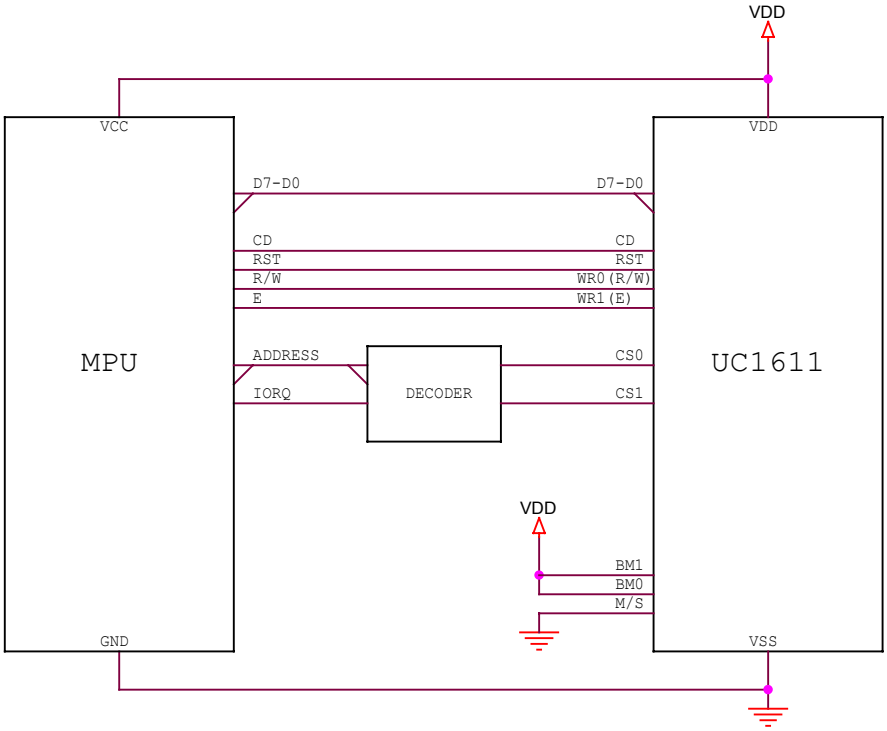


FIGURE 6: 6800/8bit parallel mode reference circuit

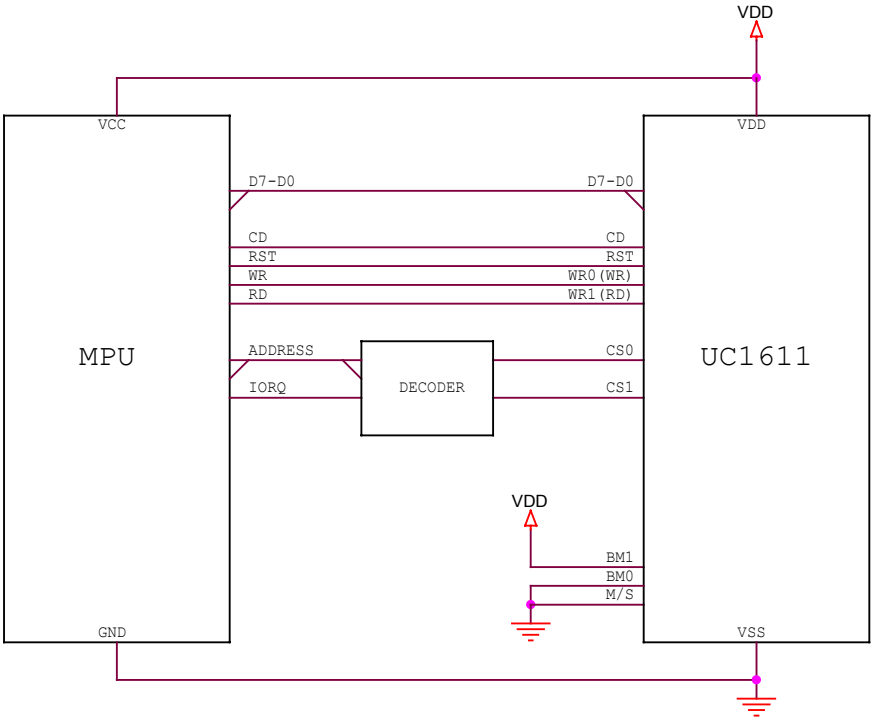


FIGURE 7: 8080/8bit parallel mode reference circuit

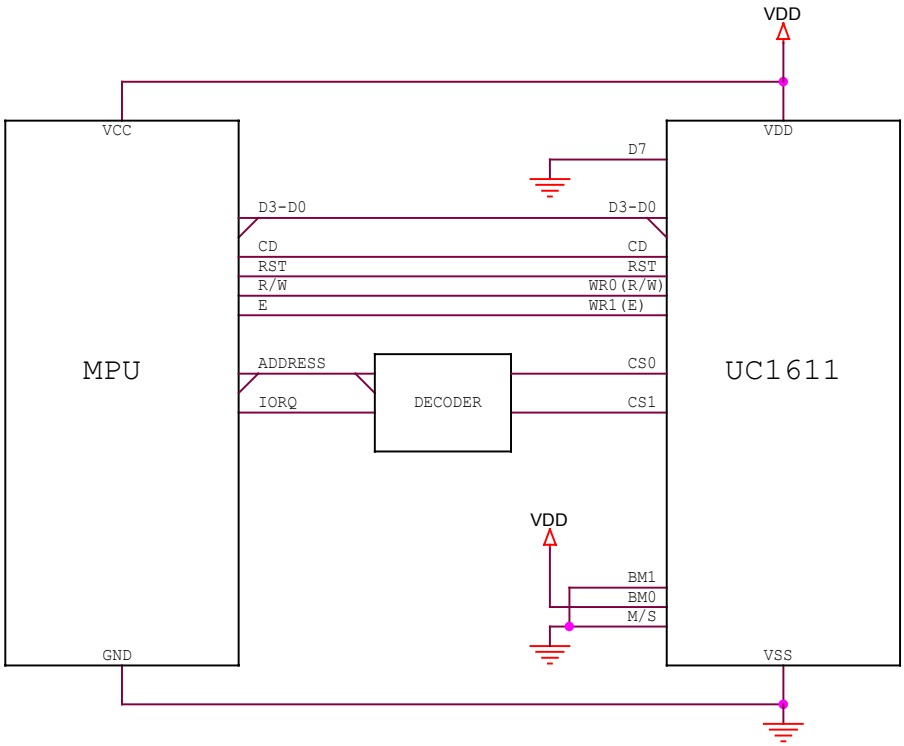


FIGURE 8: 6800/4bit parallel mode reference circuit

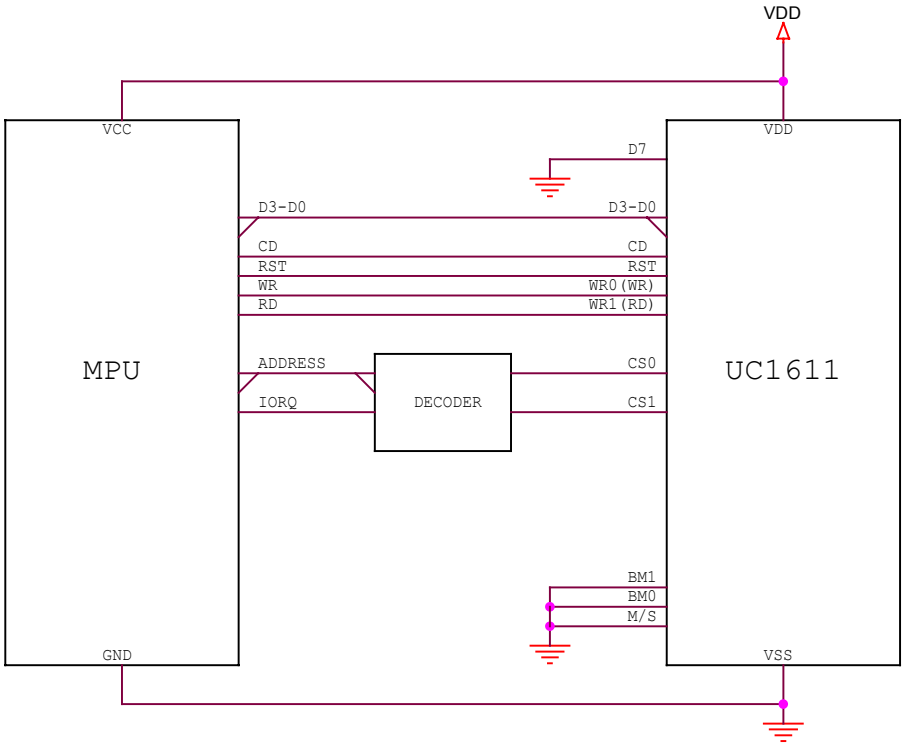


FIGURE 9: 8080/4bit parallel mode reference circuit

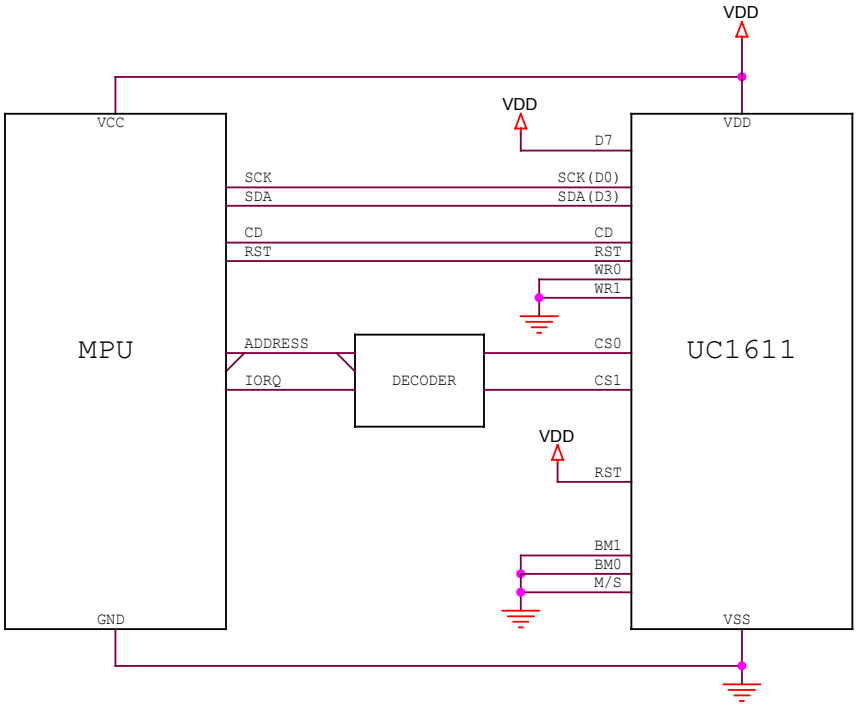


FIGURE 10: 4-Wires SPI (S8) serial mode reference circuit

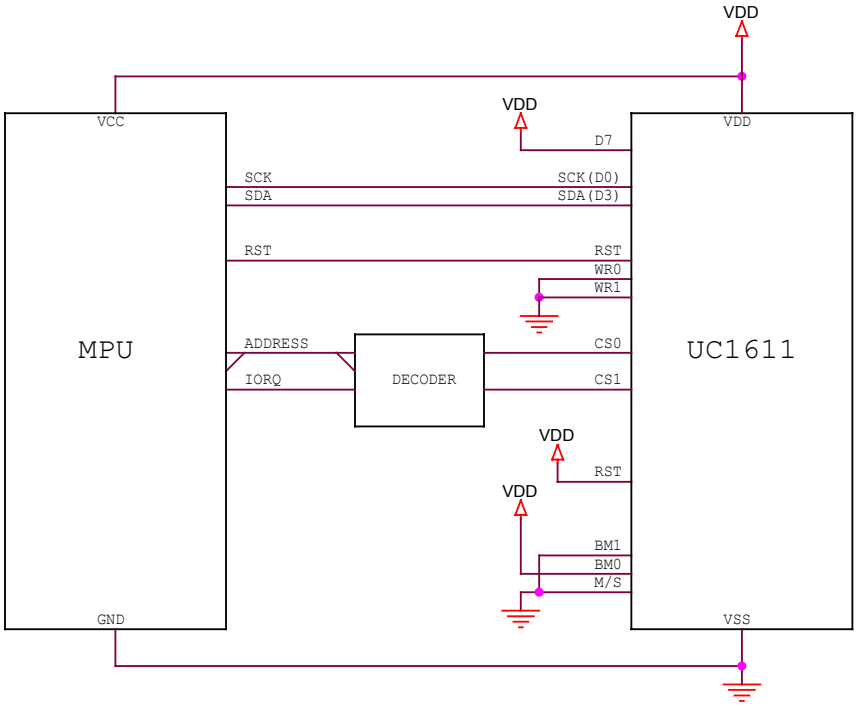


FIGURE 11 3-Wires SPI (S9) serial mode reference circuit

Note

RST pin is optional. When RST pin is not used, connect the pin to V_{DD}.

DISPLAY DATA RAM

DATA ORGANIZATION

The display data is 4-bit per pixel and stored in a dual port SRAM. The SRAM is organized as 160x 240x4.

After setting CA and PA, the next data write cycle will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page for the relation between the COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM that allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Page Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of page (MC), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increment or decrement, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 79), PA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (239–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

RAM ADDRESS GENERATION

The mapping of the data store in the display SRAM and the scanning electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FL=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*
Otherwise
Line = Mod (*Line* + 1, *160*)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches *160*. Effects such as page scrolling and page swapping can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL* + *MUX* - *1*, *160*)
where MUX is the mux rate
Otherwise
Line = Mod(*Line* - *1* , *160*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

MSF 0	MSF 1	Line Adderss	RAM	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
D3/0	D7/4	00H	Page 0	COM1	COM145	COM160	COM16
D7/4	D3/0	01H		COM2	COM146	COM159	COM15
D3/0	D7/4	02H	Page 1	COM3	COM147	COM158	COM14
D7/4	D3/0	03H		COM4	COM148	COM157	COM13
D3/0	D7/4	04H	Page 2	COM5	COM149	COM156	COM12
D7/4	D3/0	05H		COM6	COM150	COM155	COM11
D3/0	D7/4	06H	Page 3	COM7	COM151	COM154	COM10
D7/4	D3/0	07H		COM8	COM152	COM153	COM9
D3/0	D7/4	08H	Page 4	COM9	COM153	COM152	COM8
D7/4	D3/0	09H		COM10	COM154	COM151	COM7
D3/0	D7/4	0AH	Page 5	COM11	COM155	COM150	COM6
D7/4	D3/0	0BH		COM12	COM156	COM149	COM5
D3/0	D7/4	0CH	Page 6	COM13	COM157	COM148	COM4
D7/4	D3/0	0DH		COM14	COM158	COM147	COM3
D3/0	D7/4	0EH	Page 7	COM15	COM159	COM146	COM2
D7/4	D3/0	0FH		COM16	COM160	COM145	COM1
D3/0	D7/4	10H	Page 8	COM17	COM1		COM160
D7/4	D3/0	11H		COM18	COM2		COM159
D3/0	D7/4	12H	Page 9	COM19	COM3		COM158
D7/4	D3/0	13H		COM20	COM4		COM157
D3/0	D7/4	14H	Page 10	COM21	COM5		COM156
D7/4	D3/0	15H		COM22	COM6		COM155
D3/0	D7/4	16H	Page 11	COM23	COM7		COM154
D7/4	D3/0	17H		COM24	COM8		COM153
D3/0	D7/4	18H	Page 12	COM25	COM9		COM152
D7/4	D3/0	19H		COM26	COM10		COM151
D3/0	D7/4	1AH	Page 13	COM27	COM11		COM150
D7/4	D3/0	1BH		COM28	COM12		COM149
D3/0	D7/4	1CH	Page 14	COM29	COM13		COM148
D7/4	D3/0	1DH		COM30	COM14		COM147
D3/0	D7/4	1EH	Page 15	COM31	COM15		COM146
D7/4	D3/0	1FH		COM32	COM16		COM145
D3/0	D7/4	8CH	Page 70	COM141		COM20	
D7/4	D3/0	8DH		COM142		COM19	
D3/0	D7/4	8EH	Page 71	COM143		COM18	
D7/4	D3/0	8FH		COM144		COM17	
D3/0	D7/4	90H	Page 72	COM145		COM16	
D7/4	D3/0	91H		COM146		COM15	
D3/0	D7/4	92H	Page 73	COM147		COM14	
D7/4	D3/0	93H		COM148		COM13	
D3/0	D7/4	94H	Page 74	COM149		COM12	
D7/4	D3/0	95H		COM150		COM11	
D3/0	D7/4	96H	Page 75	COM151		COM10	
D7/4	D3/0	97H		COM152		COM9	
D3/0	D7/4	98H	Page 76	COM153		COM8	
D7/4	D3/0	99H		COM154		COM7	
D3/0	D7/4	9AH	Page 77	COM155		COM6	
D7/4	D3/0	9BH		COM156		COM5	
D3/0	D7/4	9CH	Page 78	COM157	COM141	COM4	COM20
D7/4	D3/0	9DH		COM158	COM142	COM3	COM19
D3/0	D7/4	9EH	Page 79	COM159	COM143	COM2	COM18
D7/4	D3/0	9FH		COM160	COM144	COM1	COM17

MX														
0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8		SEG236	SEG237	SEG238	SEG239	SEG240
1	SEG240	SEG239	SEG238	SEG237	SEG236	SEG235	SEG234	SEG233		SEG5	SEG4	SEG3	SEG2	SEG1

Example for memory mapping: let MX = 0, MY = 0, SL = 0, MSF = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1: 00001111b
⇒ Page 0 SEG 2: 11110000b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1611 has two different types of Reset:
Power-ON-Reset and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about 5~10mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1611 enters RESET sequence:

- Operation mode will be "Reset"
- System Status bits RS and BZ will stay as "1" until the Reset process is completed. When RS=1, the IC will only respond to *Read Status* command. All other commands are ignored.
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1611 has three operating modes (OM):
Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	OFF	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[4:2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

For maximum energy utilization, Sleep mode is designed to retain charges stored in external capacitors C_{B0}, C_{B1}, C_{B2}, C_{B3} and C_{LCD}. To drain these capacitors, use Reset command to activate the on-chip draining circuit.

Action	Mode	OM
Set Driver Enable to "000"	Sleep	10
Set Driver Enable to "111"	Normal	11
Reset command RST_ pin pulled "L" Power-ON-Reset	Reset	00

Table 5: OM changes

Even though UC1611 consumes very little energy in Sleep mode (typically 5uA or less), however, since all capacitors are still charged, the leakage through COM drivers may damage the LCD over the long term. It is therefore recommended to use Sleep mode only for brief Display OFF operations, such as full-frame screen updates, and to use RESET for extended screen OFF operations.

EXITING SLEEP MODE

UC1611 contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset Mode, COM and SEG drivers will not be activated until UC1611 internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1611 power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 5~ 10 ms before the CPU starting to issue commands to UC1611. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands. However, while turning on VDD, Vdd2/3 should be started not later than Vdd.

Delay allowance between Vdd and Vdd2/3 is illustrated as Figure 12-1.

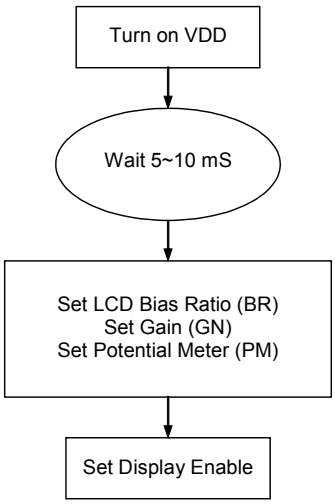


FIGURE 12: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+}, C_{BX-}, and C_L from damaging the LCD when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K Ohm for both V_{LCD} and V_{B+}. It is recommended to wait *3* x *RC* for V_{LCD} and *1.5 x RC* for V_{B+}. For example, if C_L is 33nF, then the draining time required for V_{LCD} is 0.5~1mS.

When internal V_{LCD} is not used, UC1611 will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

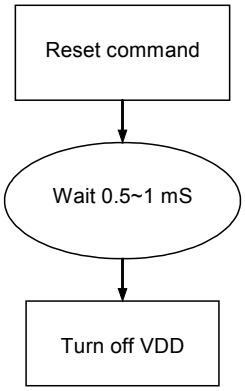


FIGURE 13: Reference Power-Down Sequence

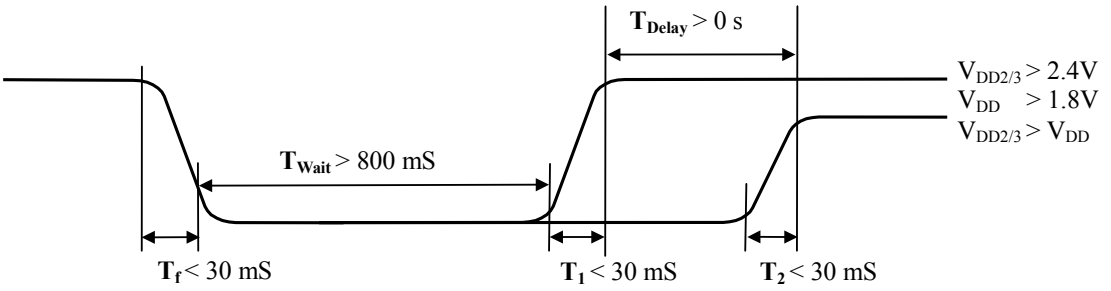
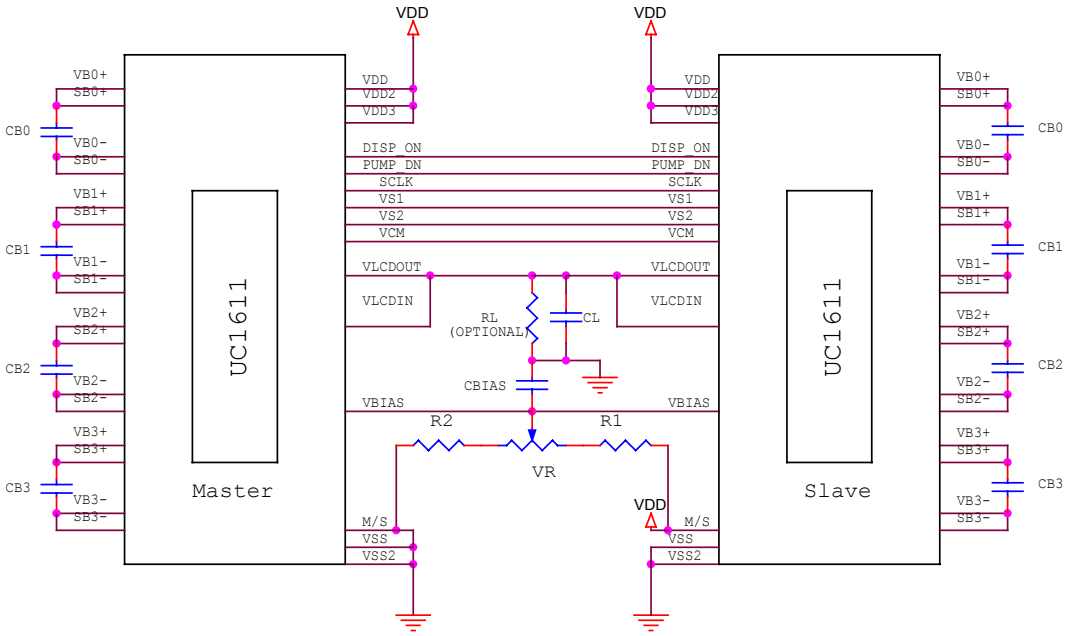


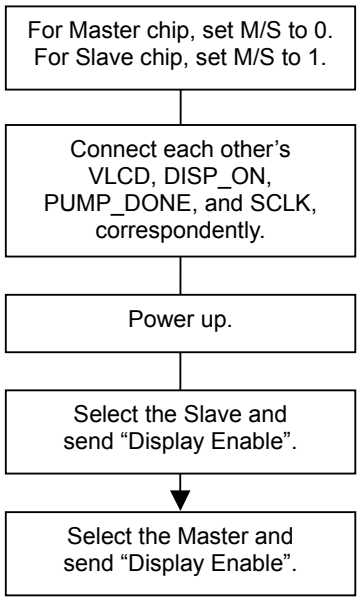
Figure 12-1: Delay allowance between V_{DD} and V_{DD23}

MASTER / SLAVE OPERATION



Master/Slave mode initialization steps:

1. Set one chip to be master mode (M/S=0) and the other chip slave mode (M/S=1).
2. Connect VLCD, DISP_ON, PUMP_DONE, and SCLK between the master chip and the slave chip.
3. Power up.
4. Select the slave chip and send “display enable” command set to it. Ensure you always do this step prior to step 5.
5. Select the master chip and send “display enable” command set to it.



SAMPLE COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type Required: These items are required
Customer: These items are not necessary, if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of data-flow of the cycle. It can be either Write (0) or Read (1).

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait ~10ms after V_{DD} is ON
C	0	0	0	0	1	0	0	1	#	#	(5) Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	(20) Set LCD Mapping Control	
A	0	0	1	0	1	0	0	0	#	#	(16) Set Line Rate	Fine tune for power, flicker, contrast, and shading.
A	0	0	1	1	0	1	0	0	#	#	(21) Set Gray Scale Mode	
C	0	0	1	1	1	0	1	0	#	#	(25) Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	(12) Set Gain and PM	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	(1) Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	(19) Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(22) System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1ms before V_{DD} OFF

BRIEF DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	0	0	0	(19) Set Display Disable	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	(1) Write display RAM	Set up display image. (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	(19) Set Display Enable	

* This is only recommended for very brief display OFF (under 10mS).
If image becomes unstable use the *Extended Display OFF* approach shown below.

EXTENDED DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(22) System Reset.	C_{B1}, C_{B1}, C_{LCD} discharged.
–	–	–	–	–	–	–	–	–	–	–		Extended display OFF *Z z z z . . .*
–	–	–	–	–	–	–	–	–	–	–		System waking up
R											Repeat power-up sequence	Repeat power up register setting sequence
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	(1) Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the RESET state.)
R	0	0	1	0	1	0	1	1	1	1	(19) Set Display Enable	

* The sequence is basically the same as the power up sequence, except *Power-ON RESET* is replaced by *System RESET* command, and an extended idle time in between.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
V_{LCD}	LCD Generated voltage ($-30^{O}C \sim +80^{O}C$)	-0.3	+18.0	V
V_{IN}	Digital input voltage	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Note:
1. V_{DD} based on V_{SS} = 0V
2. Stress above values listed may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		2.5		3.3	V
V_{DD2}	Supply for bias & pump		2.5		3.3	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant 2.5V$, 25°C		15	16.5	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant 2.5V$, 25°C			1.75	V
V_{IL}	Input logic LOW				$0.15V_{DD}$	V
V_{IH}	Input logic HIGH		$0.85V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
C_{IN}	Input capacitance			5	10	pF
C_{OUT}	Output capacitance			5	10	pF
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 15V		1.2	2.5	kΩ
$R_{0(COM)}$	COM output impedance	V_{LCD} = 15V		1.2	2.5	kΩ
f_{LINE}	Average Line rate	LC[4:3] = 11b	29.44	32	35.84	kHz

POWER CONSUMPTION

VDD = 2.8, Bias Ratio = 12, Gain = 01b, PM = 3, Line Rate = 32Klps, PL = 40~56nF, MR = 160, Bus mode = 6800, C_L = 1uF, CB = 1uF. All outputs are open circuit.

Display Pattern	Conditions	Typ.	Max.
All-OFF	Bus = idle	2836	4200
2-pixel checker	Bus = idle	3242	4200
-	Bus = idle (standby current)	-	5 μA

AC CHARACTERISTICS

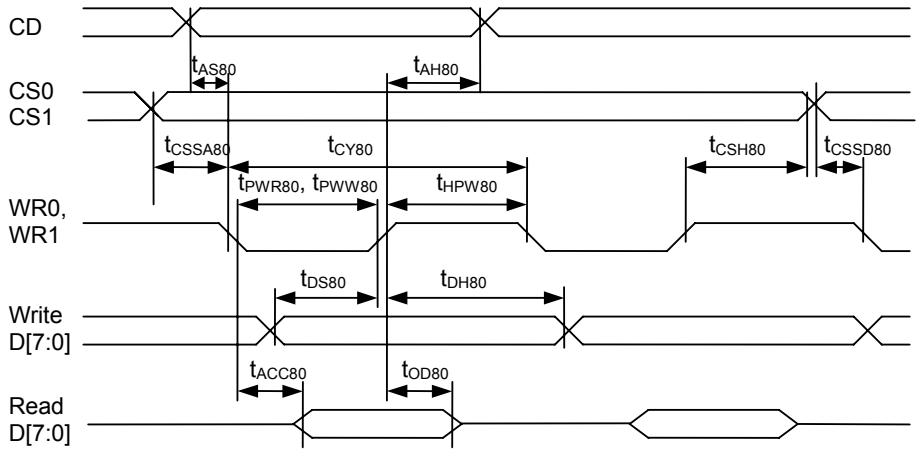


FIGURE 14: Parallel Bus Timing Characteristics (for 8080 MCU)

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 20	–	ns
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	ns
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		65 65	–	ns
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		35 35	–	ns
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 65 35 65 35	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 15	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 12	60 20	ns
t_{SSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		ns

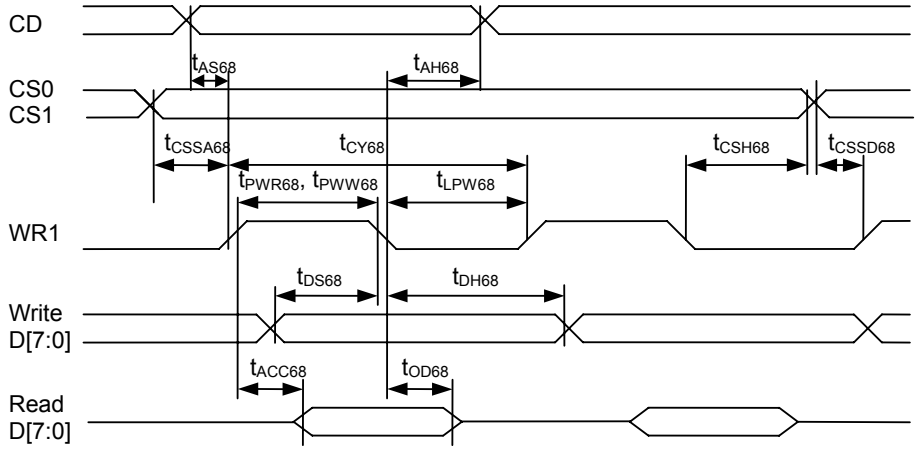


FIGURE 15: Parallel Bus Timing Characteristics (for 6800 MCU)

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 20	–	ns
T_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	ns
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		65 65	–	ns
t_{PWW68}		Pulse width 8 bits (write) 4 bits		35 35	–	ns
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 65 35 65 35	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 15	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 12	60 20	ns
t_{CSSA68} t_{CSSD68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		ns

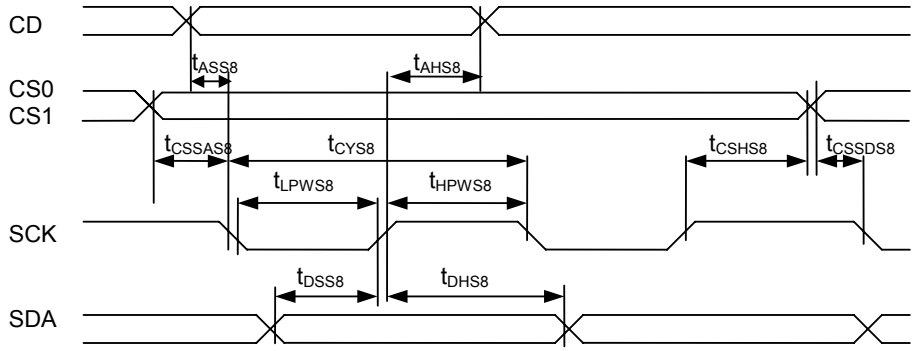


FIGURE 16: Serial Bus Timing Characteristics

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	ns
t_{AHS8}		Address hold time		20	–	ns
t_{CYS8}	SCK	System cycle time		80	–	ns
t_{LPWS8}		Low pulse width		40	–	ns
t_{HPWS8}		High pulse width		40	–	ns
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 15	–	ns
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10 20		ns

FIGURE 17: Reset Characteristics

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		1000	–	ns

PHYSICAL DIMENSIONS

DIE SIZE:

17.119 mm X 1.637 mm

DIE THICKNESS:

0.5 mm

AU BUMP HEIGHT:

17 μm ±1 μm (within die)

AU BUMP PITCH:

50 μm (Typ.)

AU BUMP SIZE:

85 X 32 μm (Typ.)

DUMMY BUMP SIZE:

85 X 50 μm (Typ.)

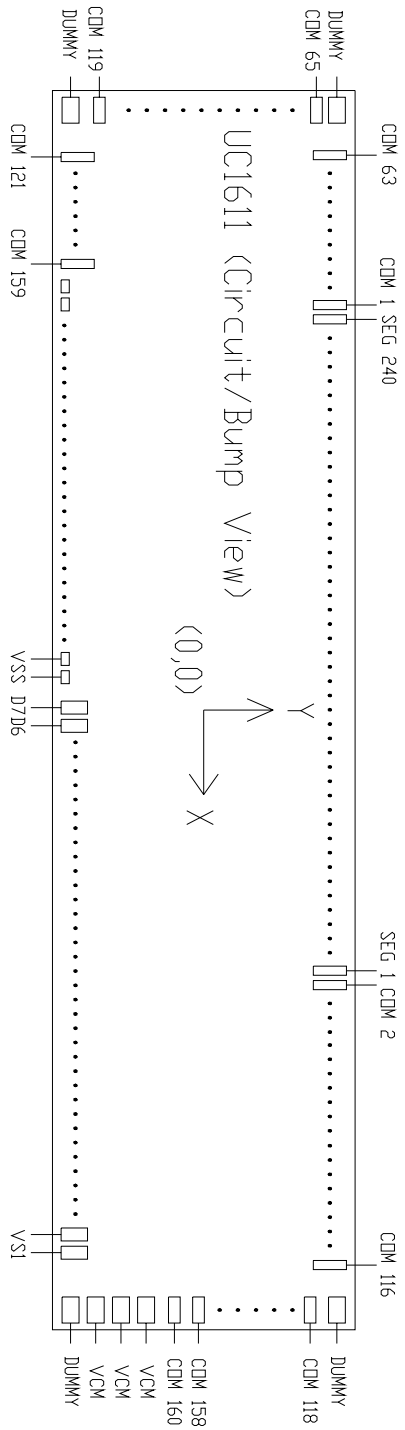
PAD COORDINATES:

Pad center

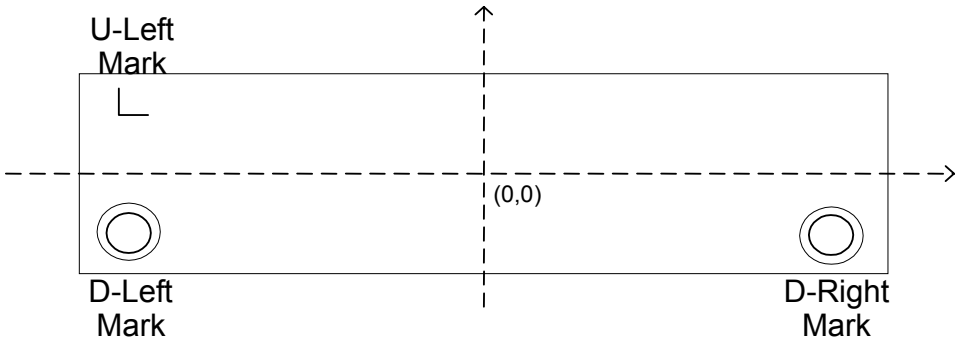
PAD ORIGIN:

Chip center

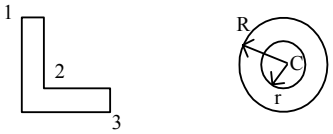
(Drawings and coordinates are in the circuit/bump view)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment mark is on Metal3 under Passivation.

COORDINATES:

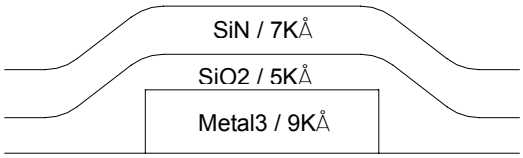
U-Left Mark		
	X	Y
1	-8372.3	771.0
2	-8356.7	739.1
3	-8325.4	723.6

D-Left Mark Center		D-Right Mark Center	
X	Y	X	Y
-8351.2	-746.9	8340.4	-746.9

SIZE:

R: 27.5 μm; r: 16.6 μm

TOP METAL AND PASSIVATION:



FOR NON-OTP PROCESS CROSS-SECTION

PAD COORDINATES

#	Pad name	X	Y	W	H
1	DUMMY	-8456.2	744.4	85	50
2	COM65	-8456.2	678.6	85	32
3	COM67	-8456.2	628.6	85	32
4	COM69	-8456.2	578.6	85	32
5	COM71	-8456.2	528.6	85	32
6	COM73	-8456.2	478.6	85	32
7	COM75	-8456.2	428.6	85	32
8	COM77	-8456.2	378.6	85	32
9	COM79	-8456.2	328.6	85	32
10	COM81	-8456.2	278.6	85	32
11	COM83	-8456.2	228.6	85	32
12	COM85	-8456.2	178.6	85	32
13	COM87	-8456.2	128.6	85	32
14	COM89	-8456.2	78.6	85	32
15	COM91	-8456.2	28.6	85	32
16	COM93	-8456.2	-21.5	85	32
17	COM95	-8456.2	-71.5	85	32
18	COM97	-8456.2	-121.5	85	32
19	COM99	-8456.2	-171.5	85	32
20	COM101	-8456.2	-221.5	85	32
21	COM103	-8456.2	-271.5	85	32
22	COM105	-8456.2	-321.5	85	32
23	COM107	-8456.2	-371.5	85	32
24	COM109	-8456.2	-421.5	85	32
25	COM111	-8456.2	-471.5	85	32
26	COM113	-8456.2	-521.5	85	32
27	COM115	-8456.2	-571.5	85	32
28	COM117	-8456.2	-621.5	85	32
29	COM119	-8456.2	-671.5	85	32
30	DUMMY2	-8456.2	-744.4	85	50
31	COM121	-8280.0	-730.0	32	85
32	COM123	-8230.0	-730.0	32	85
33	COM125	-8180.0	-730.0	32	85
34	COM127	-8130.0	-730.0	32	85
35	COM129	-8080.0	-730.0	32	85
36	COM131	-8030.0	-730.0	32	85
37	COM133	-7980.0	-730.0	32	85
38	COM135	-7930.0	-730.0	32	85
39	COM137	-7880.0	-730.0	32	85
40	COM139	-7830.0	-730.0	32	85
41	COM141	-7780.0	-730.0	32	85
42	COM143	-7730.0	-730.0	32	85
43	COM145	-7680.0	-730.0	32	85
44	COM147	-7630.0	-730.0	32	85
45	COM149	-7580.0	-730.0	32	85
46	COM151	-7530.0	-730.0	32	85
47	COM153	-7480.0	-730.0	32	85
48	COM155	-7430.0	-730.0	32	85
49	COM157	-7380.0	-730.0	32	85
50	COM159	-7330.0	-730.0	32	85
51	VSS	-7093.2	-755.6	83.1	29.2
52	VSS	-6991.4	-755.6	83.1	29.2
53	VSS	-6863.2	-755.6	83.1	29.2
54	VSS	-6761.4	-755.6	83.1	29.2

#	Pad name	X	Y	W	H
55	VSS	-6633.2	-755.6	83.1	29.2
56	VSS	-6531.4	-755.6	83.1	29.2
57	VSS	-6403.2	-755.6	83.1	29.2
58	VSS	-6301.4	-755.6	83.1	29.2
59	VSS	-6173.2	-755.6	83.1	29.2
60	VSS	-6071.4	-755.6	83.1	29.2
61	VSS	-5943.2	-755.6	83.1	29.2
62	VSS	-5841.4	-755.6	83.1	29.2
63	VSS	-5713.2	-755.6	83.1	29.2
64	VSS	-5611.4	-755.6	83.1	29.2
65	VSS	-5483.2	-755.6	83.1	29.2
66	VSS	-5381.4	-755.6	83.1	29.2
67	VSS	-5253.2	-755.6	83.1	29.2
68	VSS	-5151.4	-755.6	83.1	29.2
69	VSS	-5023.2	-755.6	83.1	29.2
70	VSS	-4921.4	-755.6	83.1	29.2
71	VSS	-4793.2	-755.6	83.1	29.2
72	VSS	-4691.4	-755.6	83.1	29.2
73	VSS	-4563.2	-755.6	83.1	29.2
74	VSS	-4461.4	-755.6	83.1	29.2
75	VSS	-4333.2	-755.6	83.1	29.2
76	VSS	-4231.4	-755.6	83.1	29.2
77	VSS	-4103.2	-755.6	83.1	29.2
78	VSS	-4001.4	-755.6	83.1	29.2
79	VSS	-3873.2	-755.6	83.1	29.2
80	VSS	-3771.4	-755.6	83.1	29.2
81	VSS	-3643.2	-755.6	83.1	29.2
82	VSS	-3541.4	-755.6	83.1	29.2
83	VSS	-3413.2	-755.6	83.1	29.2
84	VSS	-3311.4	-755.6	83.1	29.2
85	VSS	-3183.2	-755.6	83.1	29.2
86	VSS	-3081.4	-755.6	83.1	29.2
87	VSS	-2953.2	-755.6	83.1	29.2
88	VSS	-2851.4	-755.6	83.1	29.2
89	VSS	-2723.2	-755.6	83.1	29.2
90	VSS	-2621.4	-755.6	83.1	29.2
91	VSS	-2354.5	-756.5	70	30.9
92	VSS	-2259.0	-756.5	70	30.9
93	VSS	-2163.4	-756.5	70	30.9
94	VSS	-2067.9	-756.5	70	30.9
95	VSS	-1972.3	-756.5	70	30.9
96	VSS	-1876.8	-756.5	70	30.9
97	VSS	-1781.2	-756.5	70	30.9
98	VSS	-1685.7	-756.5	70	30.9
99	VSS	-1590.1	-756.5	70	30.9
100	VSS	-1494.6	-756.5	70	30.9
101	VSS	-1399.0	-756.5	70	30.9
102	VSS	-1303.5	-756.5	70	30.9
103	VSS	-1207.9	-756.5	70	30.9
104	VSS	-1112.4	-756.5	70	30.9
105	VSS	-1016.8	-756.5	70	30.9
106	VSS	-921.3	-756.5	70	30.9
107	VSS	-825.7	-756.5	70	30.9
108	VSS	-730.2	-756.5	70	30.9

#	Pad name	X	Y	W	H
109	VSS	-634.6	-756.5	70	30.9
110	VSS	-539.0	-756.5	70	30.9
111	VSS	-443.5	-756.5	70	30.9
112	VSS	-348.0	-756.5	70	30.9
113	VSS	-252.4	-756.5	70	30.9
114	VSS	-156.9	-756.5	70	30.9
115	VSS	-61.3	-756.5	70	30.9
116	VSS	34.3	-756.5	70	30.9
117	VSS	129.8	-756.5	70	30.9
118	VSS	225.4	-756.5	70	30.9
119	VSS	320.9	-756.5	70	30.9
120	VSS	416.5	-756.5	70	30.9
121	VSS	512.0	-756.5	70	30.9
122	VSS	607.6	-756.5	70	30.9
123	VSS	703.1	-756.5	70	30.9
124	VSS	798.7	-756.5	70	30.9
125	VSS	894.2	-756.5	70	30.9
126	VSS	989.8	-756.5	70	30.9
127	VSS	1085.3	-756.5	70	30.9
128	VSS	1180.9	-756.5	70	30.9
129	VSS	1276.4	-756.5	70	30.9
130	VSS	1372.0	-756.5	70	30.9
131	VSS	1467.5	-756.5	70	30.9
132	VSS	1563.1	-756.5	70	30.9
133	VSS	1658.6	-756.5	70	30.9
134	VSS	1754.2	-756.5	70	30.9
135	VSS	1849.7	-756.5	70	30.9
136	VSS	1945.3	-756.5	70	30.9
137	VSS	2040.8	-756.5	70	30.9
138	VSS	2136.4	-756.5	70	30.9
139	VSS	2231.9	-756.5	70	30.9
140	VSS	2327.5	-756.5	70	30.9
141	VSS	2423.0	-756.5	70	30.9
142	VSS	2518.6	-756.5	70	30.9
143	VSS	2614.1	-756.5	70	30.9
144	VSS	2709.7	-756.5	70	30.9
145	VSS	2805.2	-756.5	70	30.9
146	VSS	2900.8	-756.5	70	30.9
147	VSS	2996.3	-756.5	70	30.9
148	DATA7	3134.1	-732.5	50	80
149	DATA6	3204.1	-732.5	50	80
150	DATA5	3274.1	-732.5	50	80
151	DATA4	3344.1	-732.5	50	80
152	DATA3	3414.1	-732.5	50	80
153	DATA2	3484.1	-732.5	50	80
154	DATA1	3554.1	-732.5	50	80
155	DATA0	3624.1	-732.5	50	80
156	M/S	3718.1	-732.5	50	80
157	SCLK	3805.7	-732.5	50	80
158	DISP_ON	3875.7	-732.5	50	80
159	INIT_DO	3945.7	-732.5	50	80
160	RST_	4030.4	-732.5	50	80
161	CS0	4108.5	-732.5	50	80
162	CS1	4184.9	-732.5	50	80
163	CD	4271.2	-732.5	50	80
164	WR0	4359.7	-732.5	50	80

#	Pad name	X	Y	W	H
165	WR1	4446.0	-732.5	50	80
166	BM1	4534.5	-732.5	50	80
167	BM0	4620.8	-732.5	50	80
168	TST4	4709.3	-732.5	50	80
169	VSS	4788.5	-732.5	50	80
170	VSS	4858.5	-732.5	50	80
171	VSS2	4928.5	-732.5	50	80
172	VSS2	4998.5	-732.5	50	80
173	VDD2	5068.5	-732.5	50	80
174	VDD2	5138.5	-732.5	50	80
175	VDD3	5208.5	-732.5	50	80
176	VDD	5278.5	-732.5	50	80
177	VDD	5348.5	-732.5	50	80
178	VBIAS	5433.9	-732.5	50	80
179	TST2	5542.5	-732.5	50	80
180	TST1	5639.8	-732.5	50	80
181	TP3	5733.4	-732.5	50	80
182	TP2	5803.4	-732.5	50	80
183	TP1	5873.4	-732.5	50	80
184	VLCDIN	5943.4	-732.5	50	80
185	VLCDIN	6013.1	-732.5	50	80
186	VLCDOUT	6083.4	-732.5	50	80
187	VLCDOUT	6153.4	-732.5	50	80
188	SB2N	6223.4	-732.5	50	80
189	VB2N	6293.4	-732.5	50	80
190	VB2N	6362.9	-732.5	50	80
191	SB3N	6433.2	-732.5	50	80
192	VB3N	6503.2	-732.5	50	80
193	VB3N	6572.7	-732.5	50	80
194	SB3P	6643.0	-732.5	50	80
195	VB3P	6713.0	-732.5	50	80
196	VB3P	6782.5	-732.5	50	80
197	SB2P	6852.8	-732.5	50	80
198	VB2P	6922.8	-732.5	50	80
199	VB2P	6992.3	-732.5	50	80
200	SB0N	7062.6	-732.5	50	80
201	VB0N	7132.6	-732.5	50	80
202	VB0N	7202.1	-732.5	50	80
203	SB1N	7272.4	-732.5	50	80
204	VB1N	7342.4	-732.5	50	80
205	VB1N	7411.9	-732.5	50	80
206	SB1P	7482.2	-732.5	50	80
207	VB1P	7552.0	-732.5	50	80
208	VB1P	7621.7	-732.5	50	80
209	SB0P	7692.0	-732.5	50	80
210	VB0P	7762.0	-732.5	50	80
211	VB0P	7831.5	-732.5	50	80
212	VS1	7903.4	-732.5	50	80
213	VS1	7973.4	-732.5	50	80
214	VS1	8043.4	-732.5	50	80
215	VS2	8113.4	-732.5	50	80
216	VS2	8183.4	-732.5	50	80
217	VS2	8253.4	-732.5	50	80
218	DUMMY	8456.2	-744.4	85	50
219	VCM	8458.7	-621.9	80	50
220	VCM	8458.7	-551.9	80	50

#	Pad name	X	Y	W	H
221	VCM	8458.7	-481.9	80	50
222	COM160	8456.2	-405.0	85	32
223	COM158	8456.2	-355.0	85	32
224	COM156	8456.2	-305.0	85	32
225	COM154	8456.2	-255.0	85	32
226	COM152	8456.2	-205.0	85	32
227	COM150	8456.2	-155.0	85	32
228	COM148	8456.2	-105.0	85	32
229	COM146	8456.2	-55.0	85	32
230	COM144	8456.2	-5.0	85	32
231	COM142	8456.2	45.0	85	32
232	COM140	8456.2	95.0	85	32
233	COM138	8456.2	145.0	85	32
234	COM136	8456.2	195.0	85	32
235	COM134	8456.2	245.0	85	32
236	COM132	8456.2	295.0	85	32
237	COM130	8456.2	345.0	85	32
238	COM128	8456.2	395.0	85	32
239	COM126	8456.2	445.0	85	32
240	COM124	8456.2	495.0	85	32
241	COM122	8456.2	545.0	85	32
242	COM120	8456.2	595.0	85	32
243	COM118	8456.2	645.0	85	32
244	DUMMY	8456.2	744.1	85	50
245	COM116	8170.0	730.0	32	85
246	COM114	8120.0	730.0	32	85
247	COM112	8070.0	730.0	32	85
248	COM110	8020.0	730.0	32	85
249	COM108	7970.0	730.0	32	85
250	COM106	7920.0	730.0	32	85
251	COM104	7870.0	730.0	32	85
252	COM102	7820.0	730.0	32	85
253	COM100	7770.0	730.0	32	85
254	COM98	7720.0	730.0	32	85
255	COM96	7670.0	730.0	32	85
256	COM94	7620.0	730.0	32	85
257	COM92	7570.0	730.0	32	85
258	COM90	7520.0	730.0	32	85
259	COM88	7470.0	730.0	32	85
260	COM86	7420.0	730.0	32	85
261	COM84	7370.0	730.0	32	85
262	COM82	7320.0	730.0	32	85
263	COM80	7270.0	730.0	32	85
264	COM78	7220.0	730.0	32	85
265	COM76	7170.0	730.0	32	85
266	COM74	7120.0	730.0	32	85
267	COM72	7070.0	730.0	32	85
268	COM70	7020.0	730.0	32	85
269	COM68	6970.0	730.0	32	85
270	COM66	6920.0	730.0	32	85
271	COM64	6870.0	730.0	32	85
272	COM62	6820.0	730.0	32	85
273	COM60	6770.0	730.0	32	85
274	COM58	6720.0	730.0	32	85
275	COM56	6670.0	730.0	32	85
276	COM54	6620.0	730.0	32	85

#	Pad name	X	Y	W	H
277	COM52	6570.0	730.0	32	85
278	COM50	6520.0	730.0	32	85
279	COM48	6470.0	730.0	32	85
280	COM46	6420.0	730.0	32	85
281	COM44	6370.0	730.0	32	85
282	COM42	6320.0	730.0	32	85
283	COM40	6270.0	730.0	32	85
284	COM38	6220.0	730.0	32	85
285	COM36	6170.0	730.0	32	85
286	COM34	6120.0	730.0	32	85
287	COM32	6070.0	730.0	32	85
288	COM30	6020.0	730.0	32	85
289	COM28	5970.0	730.0	32	85
290	COM26	5920.0	730.0	32	85
291	COM24	5870.0	730.0	32	85
292	COM22	5820.0	730.0	32	85
293	COM20	5770.0	730.0	32	85
294	COM18	5720.0	730.0	32	85
295	COM16	5670.0	730.0	32	85
296	COM14	5620.0	730.0	32	85
297	COM12	5570.0	730.0	32	85
298	COM10	5520.0	730.0	32	85
299	COM8	5470.0	730.0	32	85
300	COM6	5420.0	730.0	32	85
301	COM4	5370.0	730.0	32	85
302	COM2	5320.0	730.0	32	85
303	SEG1	5270.0	730.0	32	85
304	SEG2	5220.0	730.0	32	85
305	SEG3	5170.0	730.0	32	85
306	SEG4	5120.0	730.0	32	85
307	SEG5	5070.0	730.0	32	85
308	SEG6	5020.0	730.0	32	85
309	SEG7	4970.0	730.0	32	85
310	SEG8	4920.0	730.0	32	85
311	SEG9	4870.0	730.0	32	85
312	SEG10	4820.0	730.0	32	85
313	SEG11	4770.0	730.0	32	85
314	SEG12	4720.0	730.0	32	85
315	SEG13	4670.0	730.0	32	85
316	SEG14	4620.0	730.0	32	85
317	SEG15	4570.0	730.0	32	85
318	SEG16	4520.0	730.0	32	85
319	SEG17	4470.0	730.0	32	85
320	SEG18	4420.0	730.0	32	85
321	SEG19	4370.0	730.0	32	85
322	SEG20	4320.0	730.0	32	85
323	SEG21	4270.0	730.0	32	85
324	SEG22	4220.0	730.0	32	85
325	SEG23	4170.0	730.0	32	85
326	SEG24	4120.0	730.0	32	85
327	SEG25	4070.0	730.0	32	85
328	SEG26	4020.0	730.0	32	85
329	SEG27	3970.0	730.0	32	85
330	SEG28	3920.0	730.0	32	85
331	SEG29	3870.0	730.0	32	85
332	SEG30	3820.0	730.0	32	85

#	Pad name	X	Y	W	H
333	SEG31	3770.0	730.0	32	85
334	SEG32	3720.0	730.0	32	85
335	SEG33	3670.0	730.0	32	85
336	SEG34	3620.0	730.0	32	85
337	SEG35	3570.0	730.0	32	85
338	SEG36	3520.0	730.0	32	85
339	SEG37	3470.0	730.0	32	85
340	SEG38	3420.0	730.0	32	85
341	SEG39	3370.0	730.0	32	85
342	SEG40	3320.0	730.0	32	85
343	SEG41	3270.0	730.0	32	85
344	SEG42	3220.0	730.0	32	85
345	SEG43	3170.0	730.0	32	85
346	SEG44	3120.0	730.0	32	85
347	SEG45	3070.0	730.0	32	85
348	SEG46	3020.0	730.0	32	85
349	SEG47	2970.0	730.0	32	85
350	SEG48	2920.0	730.0	32	85
351	SEG49	2870.0	730.0	32	85
352	SEG50	2820.0	730.0	32	85
353	SEG51	2770.0	730.0	32	85
354	SEG52	2720.0	730.0	32	85
355	SEG53	2670.0	730.0	32	85
356	SEG54	2620.0	730.0	32	85
357	SEG55	2570.0	730.0	32	85
358	SEG56	2520.0	730.0	32	85
359	SEG57	2470.0	730.0	32	85
360	SEG58	2420.0	730.0	32	85
361	SEG59	2370.0	730.0	32	85
362	SEG60	2320.0	730.0	32	85
363	SEG61	2270.0	730.0	32	85
364	SEG62	2220.0	730.0	32	85
365	SEG63	2170.0	730.0	32	85
366	SEG64	2120.0	730.0	32	85
367	SEG65	2070.0	730.0	32	85
368	SEG66	2020.0	730.0	32	85
369	SEG67	1970.0	730.0	32	85
370	SEG68	1920.0	730.0	32	85
371	SEG69	1870.0	730.0	32	85
372	SEG70	1820.0	730.0	32	85
373	SEG71	1770.0	730.0	32	85
374	SEG72	1720.0	730.0	32	85
375	SEG73	1670.0	730.0	32	85
376	SEG74	1620.0	730.0	32	85
377	SEG75	1570.0	730.0	32	85
378	SEG76	1520.0	730.0	32	85
379	SEG77	1470.0	730.0	32	85
380	SEG78	1420.0	730.0	32	85
381	SEG79	1370.0	730.0	32	85
382	SEG80	1320.0	730.0	32	85
383	SEG81	1270.0	730.0	32	85
384	SEG82	1220.0	730.0	32	85
385	SEG83	1170.0	730.0	32	85
386	SEG84	1120.0	730.0	32	85
387	SEG85	1070.0	730.0	32	85
388	SEG86	1020.0	730.0	32	85

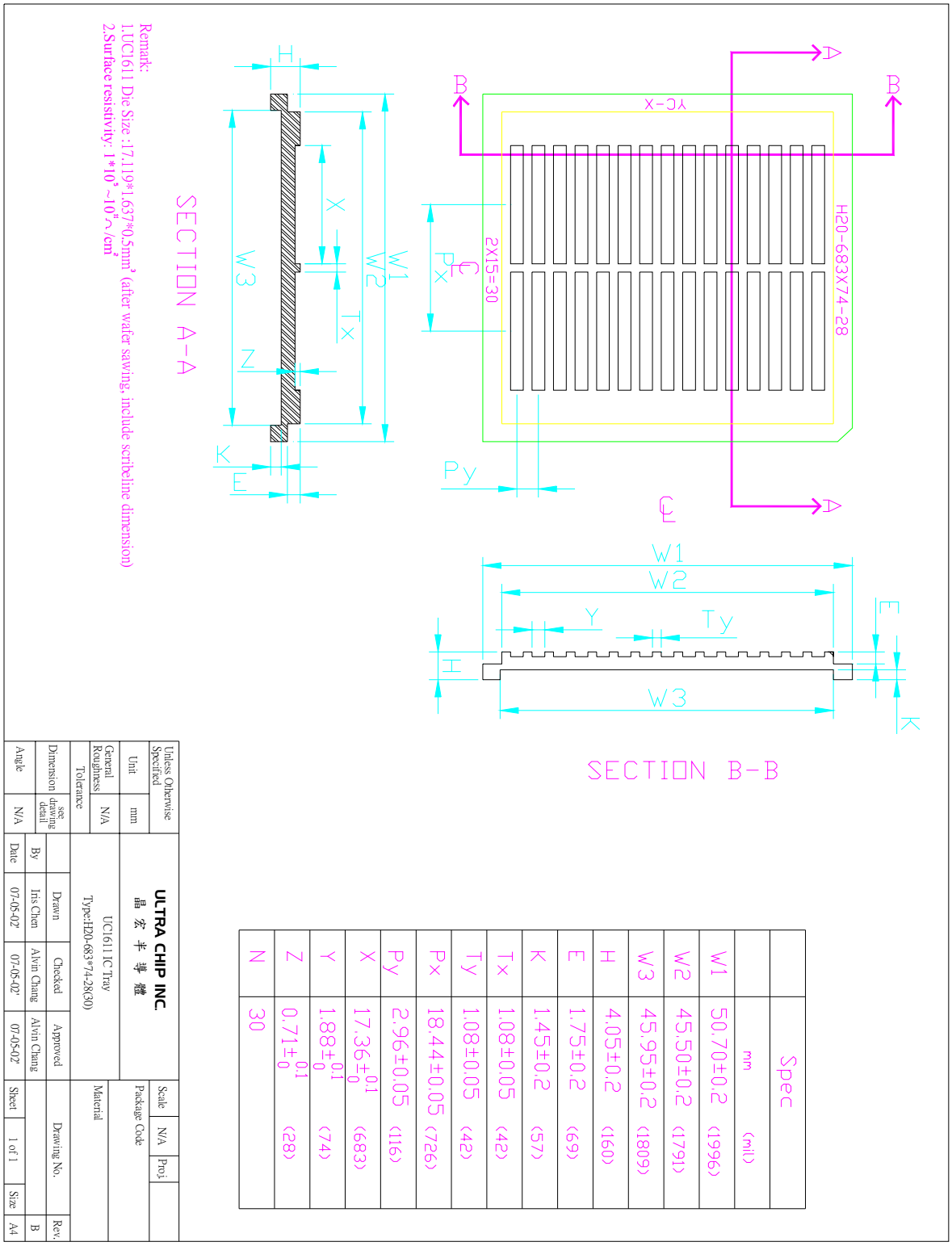
#	Pad name	X	Y	W	H
389	SEG87	970.0	730.0	32	85
390	SEG88	920.0	730.0	32	85
391	SEG89	870.0	730.0	32	85
392	SEG90	820.0	730.0	32	85
393	SEG91	770.0	730.0	32	85
394	SEG92	720.0	730.0	32	85
395	SEG93	670.0	730.0	32	85
396	SEG94	620.0	730.0	32	85
397	SEG95	570.0	730.0	32	85
398	SEG96	520.0	730.0	32	85
399	SEG97	470.0	730.0	32	85
400	SEG98	420.0	730.0	32	85
401	SEG99	370.0	730.0	32	85
402	SEG100	320.0	730.0	32	85
403	SEG101	270.0	730.0	32	85
404	SEG102	220.0	730.0	32	85
405	SEG103	170.0	730.0	32	85
406	SEG104	120.0	730.0	32	85
407	SEG105	70.0	730.0	32	85
408	SEG106	20.0	730.0	32	85
409	SEG107	-30.0	730.0	32	85
410	SEG108	-80.0	730.0	32	85
411	SEG109	-130.0	730.0	32	85
412	SEG110	-180.0	730.0	32	85
413	SEG111	-230.0	730.0	32	85
414	SEG112	-280.0	730.0	32	85
415	SEG113	-330.0	730.0	32	85
416	SEG114	-380.0	730.0	32	85
417	SEG115	-430.0	730.0	32	85
418	SEG116	-480.0	730.0	32	85
419	SEG117	-530.0	730.0	32	85
420	SEG118	-580.0	730.0	32	85
421	SEG119	-630.0	730.0	32	85
422	SEG120	-680.0	730.0	32	85
423	SEG121	-730.0	730.0	32	85
424	SEG122	-780.0	730.0	32	85
425	SEG123	-830.0	730.0	32	85
426	SEG124	-880.0	730.0	32	85
427	SEG125	-930.0	730.0	32	85
428	SEG126	-980.0	730.0	32	85
429	SEG127	-1030.0	730.0	32	85
430	SEG128	-1080.0	730.0	32	85
431	SEG129	-1130.0	730.0	32	85
432	SEG130	-1180.0	730.0	32	85
433	SEG131	-1230.0	730.0	32	85
434	SEG132	-1280.0	730.0	32	85
435	SEG133	-1330.0	730.0	32	85
436	SEG134	-1380.0	730.0	32	85
437	SEG135	-1430.0	730.0	32	85
438	SEG136	-1480.0	730.0	32	85
439	SEG137	-1530.0	730.0	32	85
440	SEG138	-1580.0	730.0	32	85
441	SEG139	-1630.0	730.0	32	85
442	SEG140	-1680.0	730.0	32	85
443	SEG141	-1730.0	730.0	32	85
444	SEG142	-1780.0	730.0	32	85

#	Pad name	X	Y	W	H
445	SEG143	-1830.0	730.0	32	85
446	SEG144	-1880.0	730.0	32	85
447	SEG145	-1930.0	730.0	32	85
448	SEG146	-1980.0	730.0	32	85
449	SEG147	-2030.0	730.0	32	85
450	SEG148	-2080.0	730.0	32	85
451	SEG149	-2130.0	730.0	32	85
452	SEG150	-2180.0	730.0	32	85
453	SEG151	-2230.0	730.0	32	85
454	SEG152	-2280.0	730.0	32	85
455	SEG153	-2330.0	730.0	32	85
456	SEG154	-2380.0	730.0	32	85
457	SEG155	-2430.0	730.0	32	85
458	SEG156	-2480.0	730.0	32	85
459	SEG157	-2530.0	730.0	32	85
460	SEG158	-2580.0	730.0	32	85
461	SEG159	-2630.0	730.0	32	85
462	SEG160	-2680.0	730.0	32	85
463	SEG161	-2730.0	730.0	32	85
464	SEG162	-2780.0	730.0	32	85
465	SEG163	-2830.0	730.0	32	85
466	SEG164	-2880.0	730.0	32	85
467	SEG165	-2930.0	730.0	32	85
468	SEG166	-2980.0	730.0	32	85
469	SEG167	-3030.0	730.0	32	85
470	SEG168	-3080.0	730.0	32	85
471	SEG169	-3130.0	730.0	32	85
472	SEG170	-3180.0	730.0	32	85
473	SEG171	-3230.0	730.0	32	85
474	SEG172	-3280.0	730.0	32	85
475	SEG173	-3330.0	730.0	32	85
476	SEG174	-3380.0	730.0	32	85
477	SEG175	-3430.0	730.0	32	85
478	SEG176	-3480.0	730.0	32	85
479	SEG177	-3530.0	730.0	32	85
480	SEG178	-3580.0	730.0	32	85
481	SEG179	-3630.0	730.0	32	85
482	SEG180	-3680.0	730.0	32	85
483	SEG181	-3730.0	730.0	32	85
484	SEG182	-3780.0	730.0	32	85
485	SEG183	-3830.0	730.0	32	85
486	SEG184	-3880.0	730.0	32	85
487	SEG185	-3930.0	730.0	32	85
488	SEG186	-3980.0	730.0	32	85
489	SEG187	-4030.0	730.0	32	85
490	SEG188	-4080.0	730.0	32	85
491	SEG189	-4130.0	730.0	32	85
492	SEG190	-4180.0	730.0	32	85
493	SEG191	-4230.0	730.0	32	85
494	SEG192	-4280.0	730.0	32	85
495	SEG193	-4330.0	730.0	32	85
496	SEG194	-4380.0	730.0	32	85
497	SEG195	-4430.0	730.0	32	85
498	SEG196	-4480.0	730.0	32	85
499	SEG197	-4530.0	730.0	32	85
500	SEG198	-4580.0	730.0	32	85

#	Pad name	X	Y	W	H
501	SEG199	-4630.0	730.0	32	85
502	SEG200	-4680.0	730.0	32	85
503	SEG201	-4730.0	730.0	32	85
504	SEG202	-4780.0	730.0	32	85
505	SEG203	-4830.0	730.0	32	85
506	SEG204	-4880.0	730.0	32	85
507	SEG205	-4930.0	730.0	32	85
508	SEG206	-4980.0	730.0	32	85
509	SEG207	-5030.0	730.0	32	85
510	SEG208	-5080.0	730.0	32	85
511	SEG209	-5130.0	730.0	32	85
512	SEG210	-5180.0	730.0	32	85
513	SEG211	-5230.0	730.0	32	85
514	SEG212	-5280.0	730.0	32	85
515	SEG213	-5330.0	730.0	32	85
516	SEG214	-5380.0	730.0	32	85
517	SEG215	-5430.0	730.0	32	85
518	SEG216	-5480.0	730.0	32	85
519	SEG217	-5530.0	730.0	32	85
520	SEG218	-5580.0	730.0	32	85
521	SEG219	-5630.0	730.0	32	85
522	SEG220	-5680.0	730.0	32	85
523	SEG221	-5730.0	730.0	32	85
524	SEG222	-5780.0	730.0	32	85
525	SEG223	-5830.0	730.0	32	85
526	SEG224	-5880.0	730.0	32	85
527	SEG225	-5930.0	730.0	32	85
528	SEG226	-5980.0	730.0	32	85
529	SEG227	-6030.0	730.0	32	85
530	SEG228	-6080.0	730.0	32	85
531	SEG229	-6130.0	730.0	32	85
532	SEG230	-6180.0	730.0	32	85
533	SEG231	-6230.0	730.0	32	85
534	SEG232	-6280.0	730.0	32	85
535	SEG233	-6330.0	730.0	32	85
536	SEG234	-6380.0	730.0	32	85
537	SEG235	-6430.0	730.0	32	85
538	SEG236	-6480.0	730.0	32	85
539	SEG237	-6530.0	730.0	32	85
540	SEG238	-6580.0	730.0	32	85
541	SEG239	-6630.0	730.0	32	85
542	SEG240	-6680.0	730.0	32	85
543	COM1	-6730.0	730.0	32	85
544	COM3	-6780.0	730.0	32	85
545	COM5	-6830.0	730.0	32	85
546	COM7	-6880.0	730.0	32	85
547	COM9	-6930.0	730.0	32	85
548	COM11	-6980.0	730.0	32	85
549	COM13	-7030.0	730.0	32	85
550	COM15	-7080.0	730.0	32	85
551	COM17	-7130.0	730.0	32	85
552	COM19	-7180.0	730.0	32	85
553	COM21	-7230.0	730.0	32	85
554	COM23	-7280.0	730.0	32	85
555	COM25	-7330.0	730.0	32	85
556	COM27	-7380.0	730.0	32	85

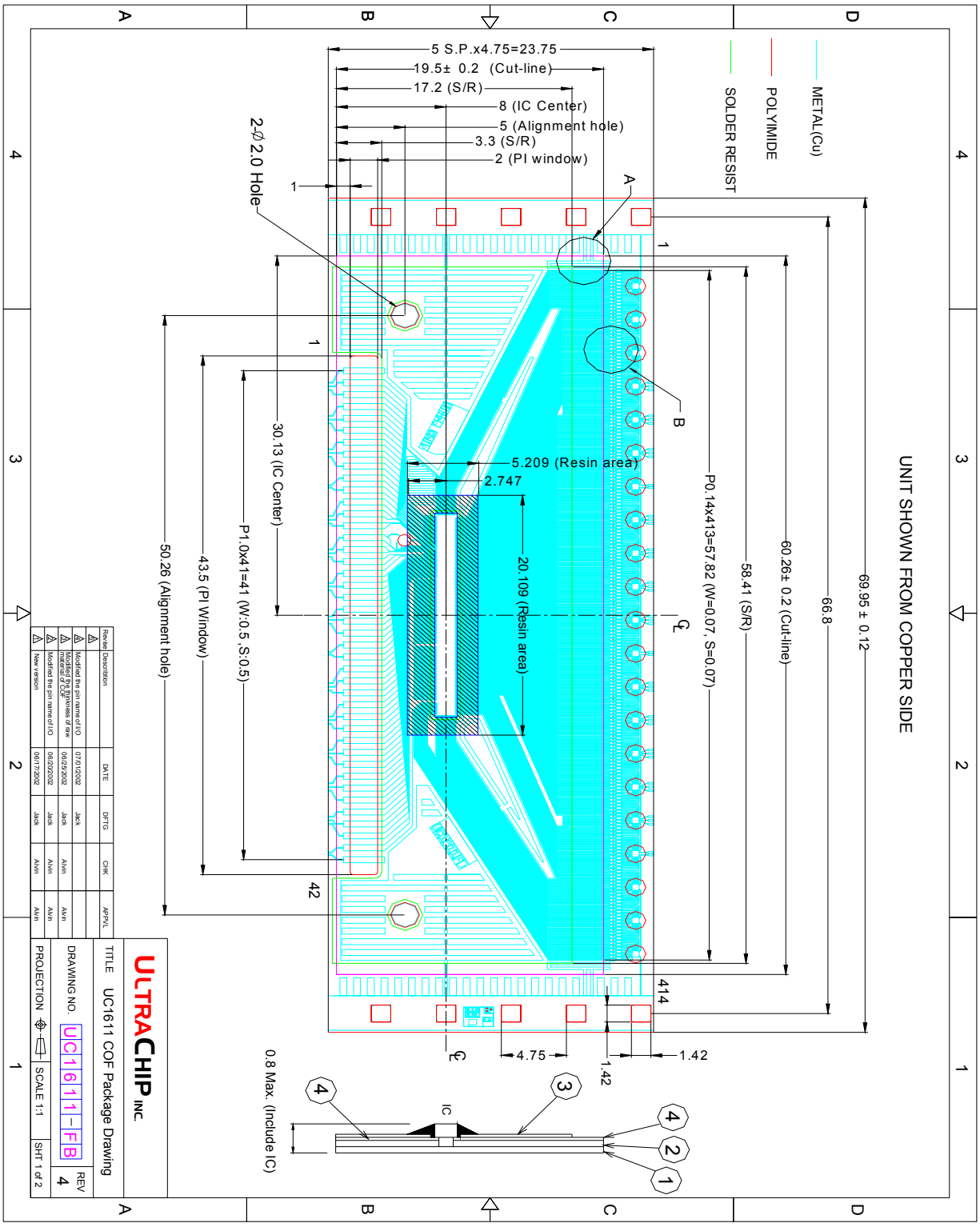
#	Pad name	X	Y	W	H
557	COM29	-7430.0	730.0	32	85
558	COM31	-7480.0	730.0	32	85
559	COM33	-7530.0	730.0	32	85
560	COM35	-7580.0	730.0	32	85
561	COM37	-7630.0	730.0	32	85
562	COM39	-7680.0	730.0	32	85
563	COM41	-7730.0	730.0	32	85
564	COM43	-7780.0	730.0	32	85
565	COM45	-7830.0	730.0	32	85
566	COM47	-7880.0	730.0	32	85
567	COM49	-7930.0	730.0	32	85
568	COM51	-7980.0	730.0	32	85
569	COM53	-8030.0	730.0	32	85
570	COM55	-8080.0	730.0	32	85
571	COM57	-8130.0	730.0	32	85
572	COM59	-8180.0	730.0	32	85
573	COM61	-8230.0	730.0	32	85
574	COM63	-8280.0	730.0	32	85

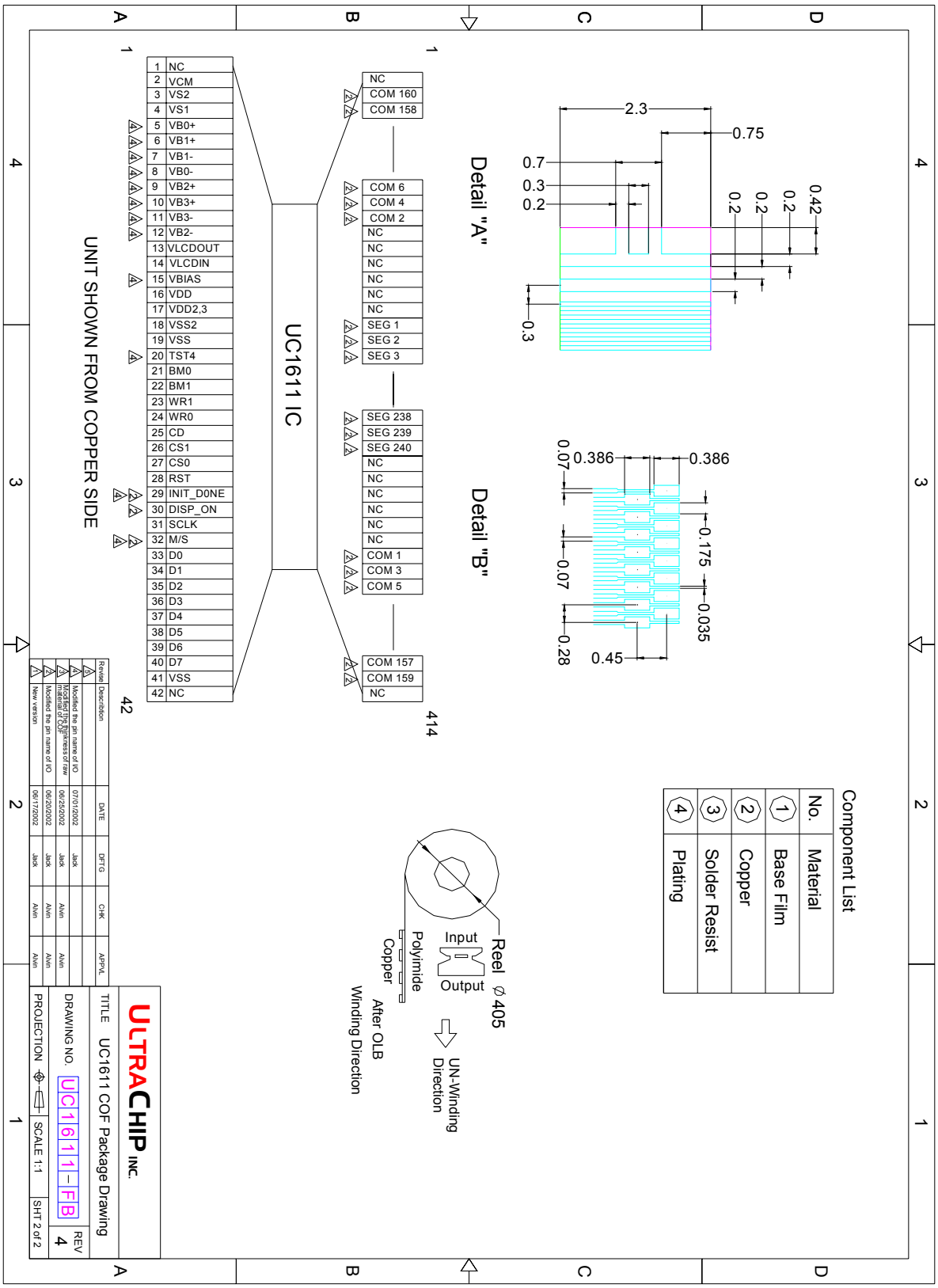
TRAY INFORMATION



	Spec
	mm (mil)
W1	50.70±0.2 (1996)
W2	45.50±0.2 (1791)
W3	45.95±0.2 (1809)
H	4.05±0.2 (160)
E	1.75±0.2 (69)
K	1.45±0.2 (57)
Tx	1.08±0.05 (42)
Ty	1.08±0.05 (42)
Px	18.44±0.05 (726)
Py	2.96±0.05 (116)
X	$17.36^{+0.1}_{0}$ (683)
Y	$1.88^{+0.1}_{0}$ (74)
Z	$0.71^{+0.1}_{0}$ (28)
N	30

COF INFORMATION




UNIT SHOWN FROM COPPER SIDE
UC1611 IC
1 NC
2 VCM
3 VS2
4 VS1
5 VB0+
6 VB1+
7 VB1-
8 VB0-
9 VB2+
10 VB3+
11 VB3-
12 VB2-
13 VLCDOUT
14 VLCDIN
15 VBIAS
16 VDD
17 VDD2,3
18 VSS2
19 VSS
20 TST4
21 BM0
22 BM1
23 WR1
24 WR0
25 CD
26 CS1
27 CS0
28 RST
29 INIT_D0NE
30 DISP_ON
31 SCLK
32 M/S
33 D0
34 D1
35 D2
36 D3
37 D4
38 D5
39 D6
40 D7
41 VSS
42 NC
42
NC
COM 160
COM 158
COM 6
COM 4
COM 2
NC
NC
NC
NC
NC
NC
SEG 1
SEG 2
SEG 3
SEG 238
SEG 239
SEG 240
NC
NC
NC
NC
NC
NC
COM 1
COM 3
COM 5
COM 157
COM 159
NC
414
Detail "A"
2.3
0.75
0.7
0.3
0.2
0.2
0.2
0.2
0.42
0.3
Detail "B"
0.07
0.386
0.386
0.175
0.07
0.035
0.28
0.45
Component List
No. Material
1 Base Film
2 Copper
3 Solder Resist
4 Plating
Reel ø405
Input
Output
Polyimide
Copper
After OLB
Winding Direction
UN-Winding Direction
Revision Description DATE DFTG CHK APPVL
New version 06/17/2002 Jack Alvin Alvin
Modified the pin name of IO 06/20/2002 Jack Alvin Alvin
Modified the pin name of IO, Thickness of raw material of COF 06/25/2002 Jack Alvin Alvin
Modified the pin name of IO 07/01/2002 Jack Alvin Alvin
ULTRACHIP INC.
TITLE UC1611 COF Package Drawing
DRAWING NO. UC1611-FB
REV 4
PROJECTION
SCALE 1:1
SHT 2 of 2

REVISION HISTORY

Version	Contents	Date of revision
0.2	First release	Jun. 10, 2002
0.21	(1) Signal labels in Figure 14 and Figure 15 are updated. (page 39, 41)	Aug. 20, 2002
	(2) COF Information is presented. (Page 54, 55)	
	(3) Symbol name V_{DD1} is changed to V_{DD}. (Page 37)	
	(4) More information is added for pin description D0~D7. (Page 6)	
	(5) Pad name for pin 173 is changed to VDD2. (Page 48)	
	(6) Application circuits are added. (Page 22, 27~29)	
	(7) Alignment Mark Information is presented (Page 46)	
	(8) Tray Information is presented. (Page 53)	
0.3	(1) The range of V_{DD} is updated as following: 2.0V to 3.3V (Overall)	Dec. 5, 2002
	(2) Die size is updated. (Page 45)	
	(3) Alignment Mark Information is updated. (Page 46)	
	(4) COF Information is updated. (Page 54)	
0.31	(1) Power consumption table is added. (Page 38)	March 7, 2003
	(2) Alignment Mark Information is updated. (Page 46)	
	(3) The value of D2 in table (21) Set Gray Scale Mode is changed from 1 to 0. (Page 17)	
	(4) Master / Slave Operation (Page 34) - The VCM VS1 and VS2 are removed and the external V_{BIAS} adjustment circuit is added.	
	(5) Figure 12-1 is added for Delay Allowance between V_{DD} and $V_{DD2/3}$ (Page 33)	
0.4	(1) Product Version is changed to 1611, revision 0.4.	March 20, 2003
	(2) Master / Slave Operation Chart (Page 34)	
	(3) Power consumption table is filled with tested values. (Page 38)	

Version	Contents	Date of revision
0.8	(1) The range of Vdd/Vdd2/Vdd3 value is modified to 2.5V ~ 3.3V, mainly in the table on page 38.	April 11, 2003
	(2) The values are changed in the “Min” column of the table on page 39. Also in this DC Characteristic table, the minimum and maximum values are given for f_{LINE}.	
	(3) The table is deleted which was marked “(V_{DD}=2.0V to 2.5V, Ta=-30 to +85^{o}C)” on page 40.	
	(4) The values are changed in the “Min” column of the table on page 41.	
	(5) The table is removed which was marked “(V_{DD}=2.0V to 2.5V, Ta=-30 to +85^{o}C)” on page 42.	
	(6) The values are changed in the “Min” column of the table on page 43.	
	(7) The table is erased which was marked “(V_{DD}=2.0V to 2.5V, Ta=-30 to +85^{o}C)” on page 43.	
	(8) The table mark is modified as “(V_{DD}=2.5V to 3.3, Ta=-30 to +85^{o}C)” on page 44.	
	(9) All the data are renewed in the section V_{LCD} Quick Reference due to a equation adjustment. (Page 21)	
	(10) Figure 12-1 Delay Allowance is maintained. (Page 34)	
	(11) Some new simulation results are used to replace the old ones: $t_{ACC68/80}$: 60ns (Max.) (Pages 40 and 42) $t_{OD68/80}$: 12ns (Min); 20ns (Max.) (Pages 40 and 42) $t_{AH68/80}$: 20nx (Pages 40, 42, and 44)	
	(12) The “Action” column for “(13) Set Partial Display Control” entry is corrected as “Set LC[9:8]”. (Page 12 Command Table)	

Version	Contents	Date of revision
0.81	(1) Product name is switched from “1611C” back to “1611”.	June 17, 2003
	(2) Section “Table of Revision History” is renamed as “Revision History” and moved to the rear of the datasheet.	
	(3) A typo error is corrected from for chip serial C to for B. (Section “Ordering Information”, Page 2)	
	(4) C_L is adjusted in Note paragraphs: 2nF~50nF → 33~330nF (Section “Pin Description”, Page 4; “V_{LCD} Quick Reference”, page 21)	
	(5) The line below is erased from the description of entry “D0~D7”: D[7]: “L”: S8 (4-wire SPI) “H”: S9 (3-wire SPI) (Section “Pin Description”, Page 5)	
	(6) Description for LC[8]=1 is modified to avoid calling “ON-OFF” mode. (Section “Command Description” – (30) Set Display End, Page 17)	
	(7) BR values are corrected: BR: 9,10,11,12 → 5,10,11,12 (Section “Control Registers”, Page 7; “V_{LCD} Quick Reference”, Page 19)	
	(8) Some changes are made into the bar chart and the table to suggest the exclusion of condition “BR=3 and GN=3”. Besides, the notes are updated. (Section “V_{LCD} Quick Reference”, Page 19)	
	(9) The notes are renewed, and some recommended values are changed: R1: 300K R2: 100K VR: 200K (Section “V_{LCD} Quick Reference”, Page 21)	
	(10) Access right for 3-wire and 4-wire is corrected from “Read Only” to “Write Only” in Table “Host interfaces Choices”. (Section “Host interfaces”, Page 25)	
	(11) Figure “Delay allowance between V_{DD} and V_{DD23}” is refined. (Section “Reset & Power Management”, Page 33)	
	(12) The timing figure and table for 8080, 6800, and S8 are updated. (Section “AC Characteristics”, Pp 39-41)	