凌陽科技
SUNPLUS

DATA SHEET

SPLC780A1

16COM/40SEG Controller/Driver

JUL. 09, 2002

Version 1.5

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16COM/40SEG CONTROLLER/DRIVER

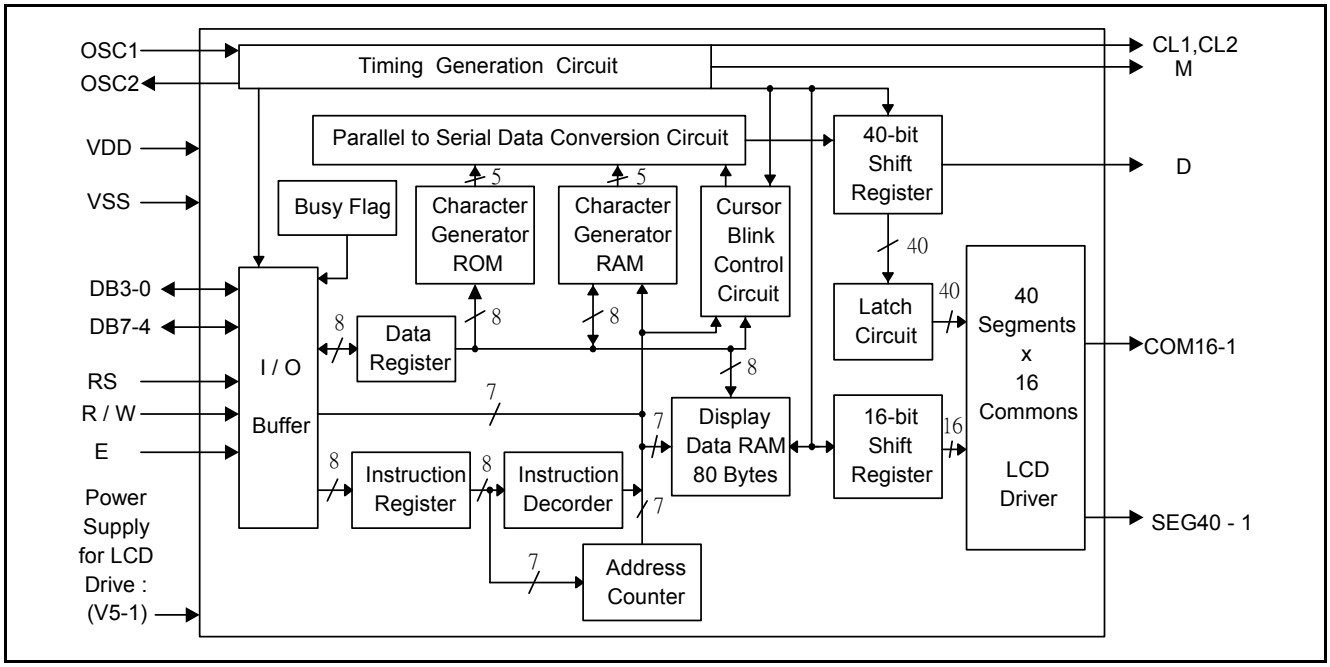
1. GENERAL DESCRIPTION

The SPLC780A1, a dot-matrix LCD controller and driver from SUNPLUS, is a unique design for displaying alpha-numeric, Japanese-Kana characters and symbols. The SPLC780A1 provides two types of interfaces to MPU: 4-bit and 8-bit interfaces. The transferring speed of 8-bit is twice faster than 4-bit. A single SPLC780A1 is able to display up to two 8-character lines. By cascading with SPLC100 or SPLC063, the display capability can be extended. The CMOS technology ensures the power saves in the most efficient way and the performance keeps in the highest rank.

2. FEATURES

- Character generator ROM: 7200 bits
  - Character font 5 x 7 dots: 160 characters
  - Character font 5 x 10 dots: 32 characters
- Character generator RAM: 512 bits
  - Character font 5 x 7 dots: 8 characters
  - Character font 5 x 10 dots: 4 characters
- Provide connecting to 4-bit or 8-bit MPU
- Direct driver for LCD: 16 COMs x 40 SEGs
- Duty factor (selected by program):
  - 1/8 duty: 1 line of 5 x 7 dots
  - 1/11 duty: 1 line of 5 x 10 dots
  - 1/16 duty: 2 lines of 5 x 7 dots / line
- Built-in power on automatic reset circuit
- Built-in oscillator circuit (with external resistor)
- Support external clock operation
- Package form: 80 QFP or bare chip available

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	PAD No.	Type	Description
VDD	10	I	Power input
VSS	80	I	Ground
OSC1 OSC2	1 2	-	Both OSC1 and OSC2 are connected to resistor for internal oscillator circuit. For external clock operation, the clock is input to OSC1.
V5 - 1	7 - 3	I	Supply voltage for LCD driving.
E	15	I	It is a start signal to read data or write data.
R / W	14	I	It is a signal to select read or write. 1: Read, 0: Write.
RS	13	I	It is a signal to select register. 1: Data register (for read and write) 0: Instruction register (for write), Busy flag -- address counter (for read).
DB3 - 0	19 - 16	I/O	Low-order 4 data bits
DB7 - 4	23 - 20	I/O	High-order 4 data bits
CL1	8	O	Clock to latch serial data D.
CL2	9	O	Clock to shift serial data D.
M	11	O	Switch signal to convert LCD waveform to AC.
D	12	O	Sends character pattern data corresponding to each common signal serially. 1: Selection, 0: Non-selection.
SEG40 - 1	40 - 79	O	Segment signals for LCD.
COM16 - 1	39 - 24	O	Common signals for LCD.

5. FUNCTIONAL DESCRIPTIONS

5.1. Oscillator

SPLC780A1 has a good oscillator that supports not only the internal oscillator operation but also the external clock operation.

5.2. Control and Display Instructions

Control and display instructions will show in details as following:

5.2.1. Clear display

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

It clears the whole display and sets display data RAM′s address 0 in address counter.

5.2.2. Return home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

X: Do not care (0 or 1)

It sets display data RAM′s address 0 in address counter and display returns to its original position. The cursor or blink goes to the left edge of the display (to the 1st line if 2 lines are displayed). The contents of the Display Data RAM do not change.

5.2.3. Entry mode set

During writing and reading data, it sets cursor move direction and shifts the display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I / D	S

I / D = 1: Increment, I / D = 0: Decrement.

S = 1: The display shift, S = 0: The display does not shift.

S = 1	I / D = 1	It shifts the display to the left
S = 1	I / D = 0	It shifts the display to the right

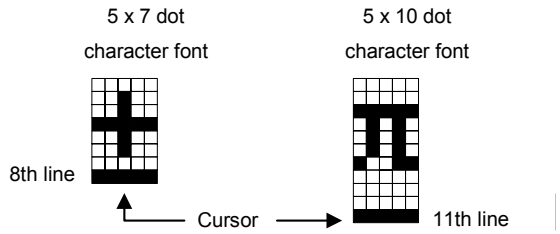
5.2.4. Display ON/OFF control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

D = 1: Display on, D = 0: Display off

C = 1: Cursor on, C = 0: Cursor off

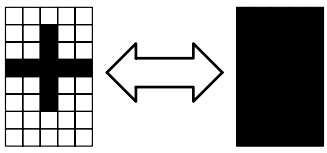
B = 1: Blinks on, B = 0: Blinks off



5.2.5. Cursor or display shift

Without changing DD RAM′s datas, it can move cursor and shift display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X



Blink display alternately

S/C	R/L	Description	Address Counter
0	0	Shift cursor to the left	AC = AC - 1
0	1	Shift cursor to the right	AC = AC + 1
1	0	Shift display to the left. Cursor follows the display shift	AC = AC
1	1	Shift display to the right. Cursor follows the display shift	AC = AC

5.2.6. Function set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

X: Do not care (0 or 1)

DL: It sets interface data length.

DL = 1: Datas are transferred with 8-bit lengths (DB7 - 0).

DL = 0: Datas are transferred with 4-bit lengths (DB7 - 4).

(It needs two times to transfer datas)

N: It sets the number of the display line.

N = 0: One-line display.

N = 1: Two-line display.

F: It sets the character font.

F = 0: 5 x 7 dots character font.

F = 1: 5 x 10 dots character font.

N	F	No. of Display Lines	Character Font	Duty Factor
0	0	1	5 X 7 dots	1 / 8
0	1	1	5 x 10 dots	1 / 11
1	X	2	5 x 7 dots	1 / 16

It cannot display two lines with 5 x 10 dot character font.

5.2.7. Set character generator RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	a	a	a	a	a	a

It sets character generator RAM address $(aaaaaa)_2$ to the address counter. Character generator RAM data can read or write after this setting.

5.2.8. Set display data RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	a	a	a	a	a	a	a

It sets display data RAM address $(aaaaaaa)_2$ to the address counter. Display data RAM can read or write after this setting.

In one-line display (N = 0), $(aaaaaaa)_{2:}$ $(00)_{16}$ - $(4F)_{16.}$

In two-line display (N = 1), $(aaaaaaa)_{2:}$ $(00)_{16}$ - $(27)_{16}$ for the first line, $(aaaaaaa)_{2:}$ $(40)_{16}$ - $(67)_{16}$ for the second line.

5.2.9. Read busy flag and address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	a	a	a	a	a	a	a

When (BF = 1) indicates that the system is busy now, it will not accept any instruction until no busy (BF = 0). At the same time, the address counter ccontents's $(aaaaaaa)_2$ is read out.

5.2.10. Write data to character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	d	d	d	d	d	d	d	d

It writes data $(dddddddd)_2$ to character generator RAM or display data RAM.

5.2.11. Read data from character generator RAM or Display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	d	d	d	d	d	d	d	d

It reads data $(dddddddd)_2$ from character generator RAM or display data RAM. To get the correct data readout is shown belows:

1). Set the address of the character generator RAM or display data RAM or shift the cursor instruction.

2). Send the " Read " instruction.

5.3. Instruction Table

Instruction	Instruction Code										Description	Execution time (F_{osc} = 270KHz)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display	38μs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	38μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	38μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F: 5x10 dots/5x8 dots)	38μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	38μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in counter	38μs
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	38μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	38μs

* "-": don't care

5.4. 8-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on . (SPLC780A1 starts initializing)		Power on reset . No display .
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 X X		Set to 8-bit operation and select 1-line display line and character font .
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on . Cursor appear .
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one . It will shift the cursor to the right when writing to the DD RAM / CG RAM . Now the display has no shift .
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W " . The cursor is incremented by one and shifted to the right .
6	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WE_	Write " E " . The cursor is incremented by one and shifted to the right .
7	⋮	⋮	
8	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E " . The cursor is incremented by one and shifted to the right .
9	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME_	Set mode for display shift when writing
10	Write data to CG RAM / DD RAM 1 0 0 0 1 0 0 0 0 0	ELCOME _	Write " "(space) . The cursor is incremented by one and shifted to the right .
11	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 1 1	LCOME C_	Write " C " . The cursor is incremented by one and shifted to the right .
12	⋮	⋮	

No.	Instruction	Display	Operation
13	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	COMPAMY _	Write " Y " . The cursor is incremented by one and shifted to the right .
14	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY	Only shift the cursor's position to the left (Y) .
15	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY	Only shift the cursor's position to the left (M) .
16	Write data to CG RAM / DD RAM 1 0 0 1 0 0 1 1 1 0	OMPANY	Write " N " . The display moves to the left .
17	Cursor or display shift 0 0 0 0 0 1 1 1 X X	COMPANY	Shift the display and the cursor's position to the right .
18	Cursor or display shift 0 0 0 0 0 1 0 1 X X	COMPANY _	Shift the display and the cursor's position to the right .
19	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 0 0	OMPANY _	Write " " (space) . The cursor is incremented by one and shifted to the right .
20	⋮	⋮	
21	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME	Both the display and the cursor return to the original position (address 0) .

5.5. 4-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on . (SPLC780A1 starts initializing)		Power on reset . No display .
2	Function set RS R/W DB7 DB6 DB5 DB4 0 0 0 0 1 0		Set to 4-bit operation .
3	Function set 0 0 0 0 1 0 0 0 0 0 X X		Set to 4-bit operation and select 1-line display line and character font .
4	Display on / off control 0 0 0 0 0 0 0 0 1 1 1 0	_	Display on . Cursor appears .
5	Entry mode set 0 0 0 0 0 0 0 0 0 1 1 0	_	Increase address by one . It will shift the cursor to the right when writing to the DD RAM / CG RAM . Now the display has no shift .
6	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1 1 1	W_	Write " W " . The cursor is incremented by one and shifted to the right .

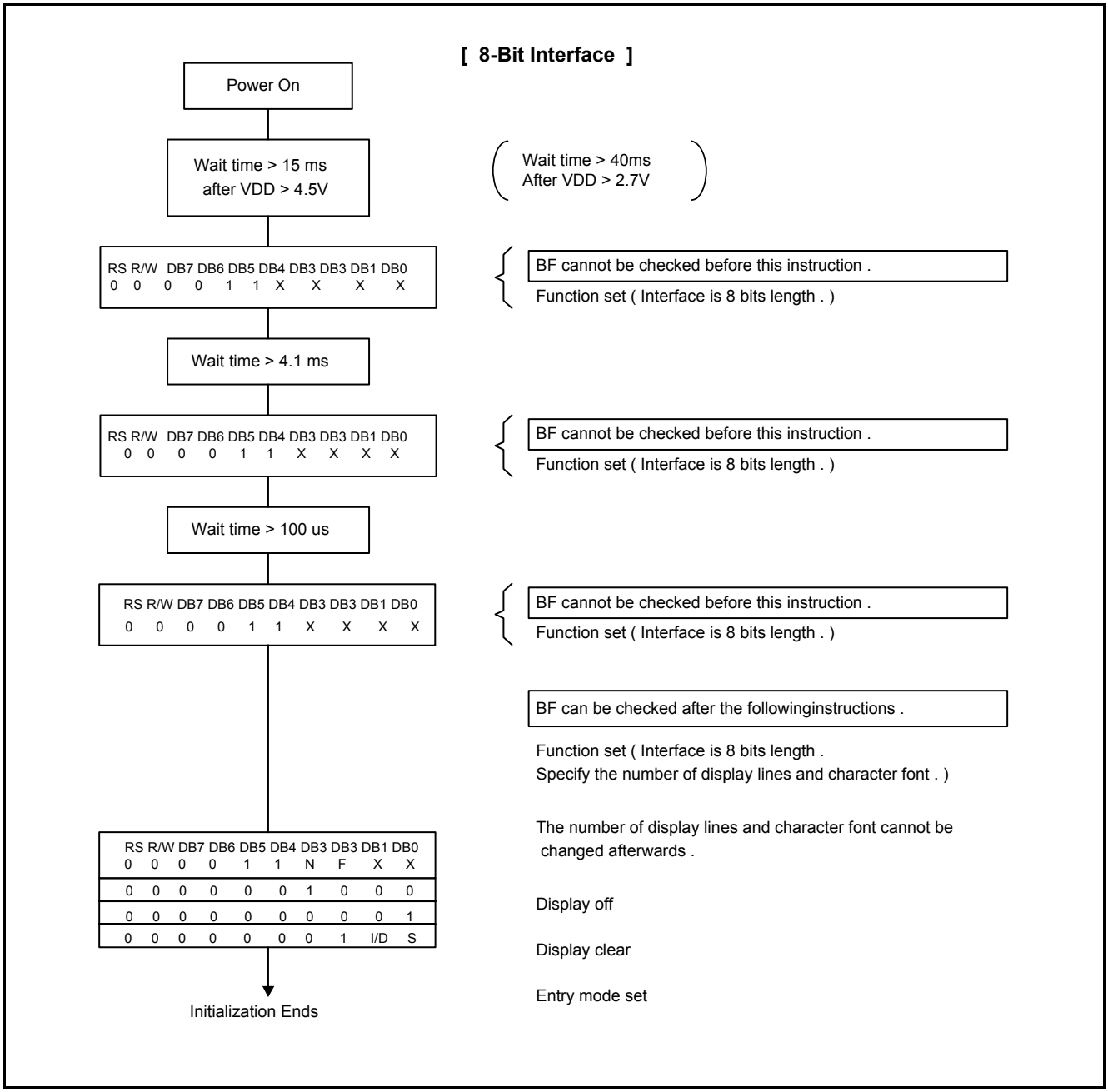
5.6. 8-Bit Operation and 8-Digit 2-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on . (SPLC780A1 starts initializing)		Power on reset . No display .
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 X X		Set to 8-bit operation and select 2-line display line and 5 x 7 dot character font .
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on . Cursor appear .
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one . It will shift the cursor to the right when writing to the DD RAM / CG RAM . Now the display has no shift .
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W " . The cursor is incremented by one and shifted to the right .
6	⋮	⋮	
7	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E " . The cursor is incremented by one and shifted to the right .
8	Set DD RAM address 0 0 1 1 0 0 0 0 0 0	WELCOME _	It sets DD RAM's address . The cursor is moved to the beginning position of the 2nd line .
9	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME T_	Write " T " . The cursor is incremented by one and shifted to the right .
10	⋮	⋮	
11	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME TO PART_	Write " T " . The cursor is incremented by one and shifted to the right .
12	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME TO PART_	When writing , it sets mode for the display shift .
13	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	ELCOME O PARTY_	Write " Y " . The cursor is incremented by one and shifted to the right .
14	⋮	⋮	
15	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME TO PARTY	Both the display and the cursor return to the original position (address 0) .

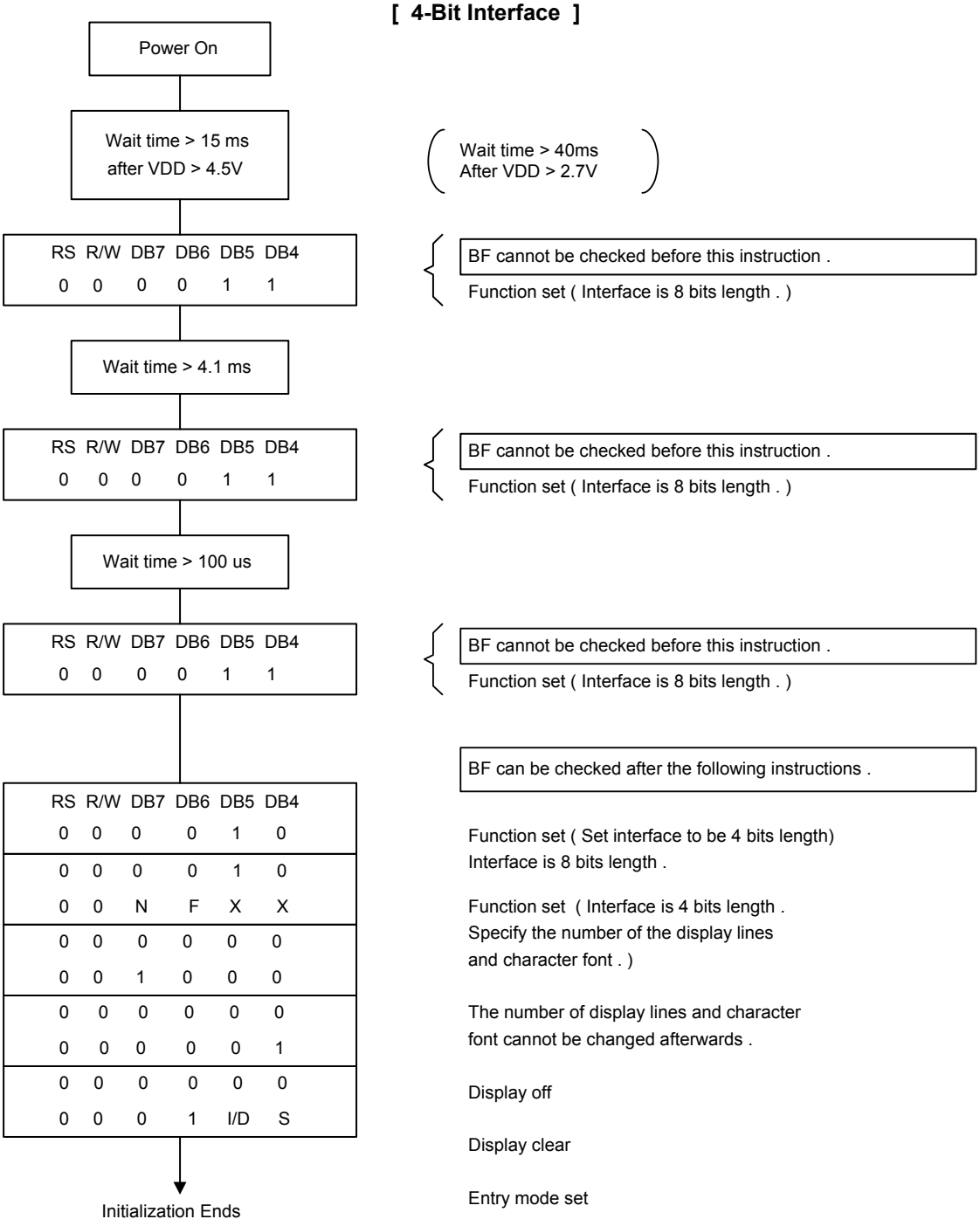
5.7. Reset Function

At power on, it starts the internal auto-reset circuit and executes the initial instructions.

There are the initial procedures shown as belows:

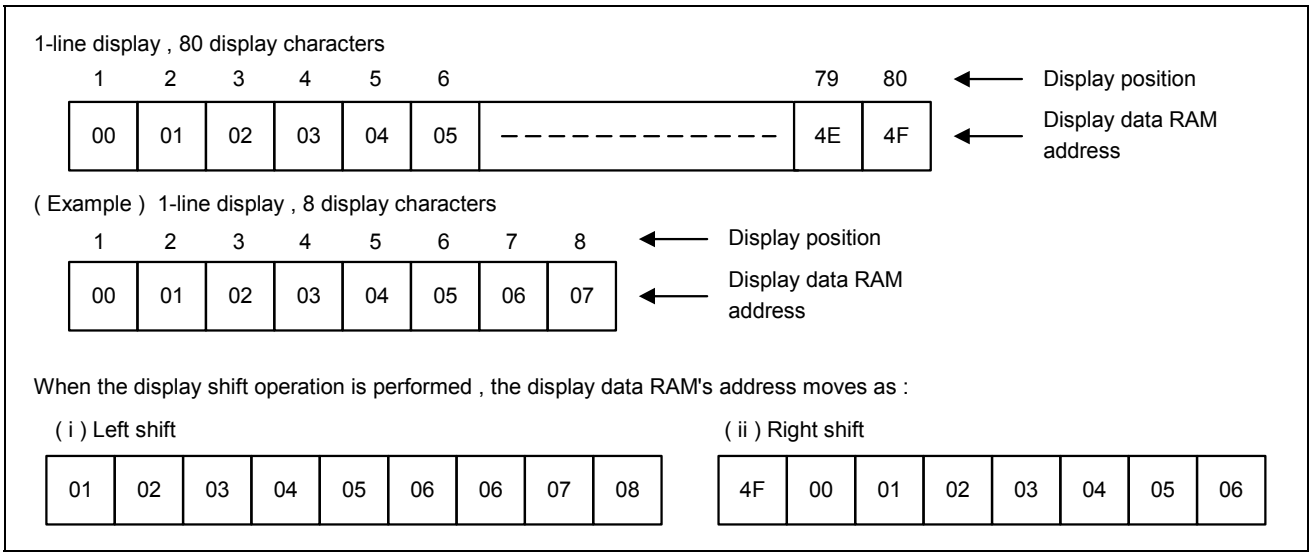


[4-Bit Interface]



5.8. Display Data RAM (DD RAM)

The DD RAM stores display data and its RAM size is 80 bytes. The area in DD RAM that is not used for display can be used as a general data RAM. Its address is set in the address counter. There are the relations between the display data RAM's address and the LCD's position shown belows.



5.9. Character Generator ROM (CG ROM)

Using 8-bit character code, the character generator ROM generates 5 x 7 dot or 5 x 10 dot character patterns. It also can generate 160 5 x 7 dot character patterns and 32 5 x 10 dot character patterns.

5.10. Character Generator RAM (CG RAM)

Using the programs, users can easily change the character patterns in the character generator RAM. It can be written with 5 x 7 dots, 8 character patterns or written with 5 x 10 dots, 4 character patterns.

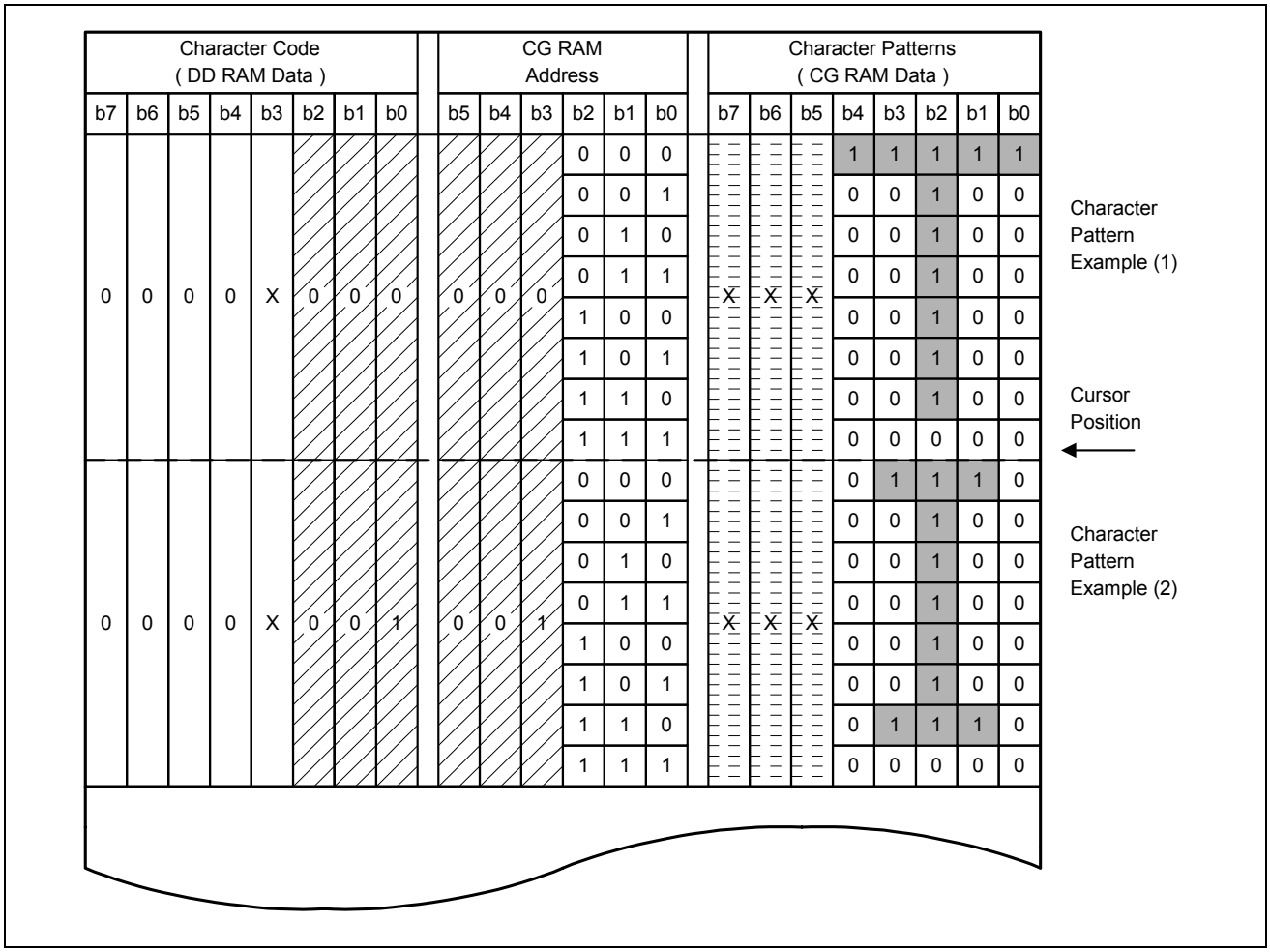
Here are the SPLC780A1's character patterns shown as belows:

Correspondence between Character Codes and Character Patterns

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)												
		0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
	0000	CG RAM (1)												
	0001	CG RAM (2)												
	0010	CG RAM (3)												
	0011	CG RAM (4)												
	0100	CG RAM (5)												
	0101	CG RAM (6)												
	0110	CG RAM (7)												
	0111	CG RAM (8)												
	1000	CG RAM (1)												
	1001	CG RAM (2)												
	1010	CG RAM (3)												
	1011	CG RAM (4)												
	1100	CG RAM (5)												
	1101	CG RAM (6)												
	1110	CG RAM (7)												
	1111	CG RAM (8)												

There are the relations between character generator RAM addresses, character generator RAM datas (character patterns) and character codes shown as belows:

5.10.1. 5 x 7 dot character patterns



Note1: ▨ It means that the bit0-2 of the character code correspond to the bit3-5 of the CG RAM address.

Note2: ▤ These areas are not used for display, but can be used for the general data RAM.

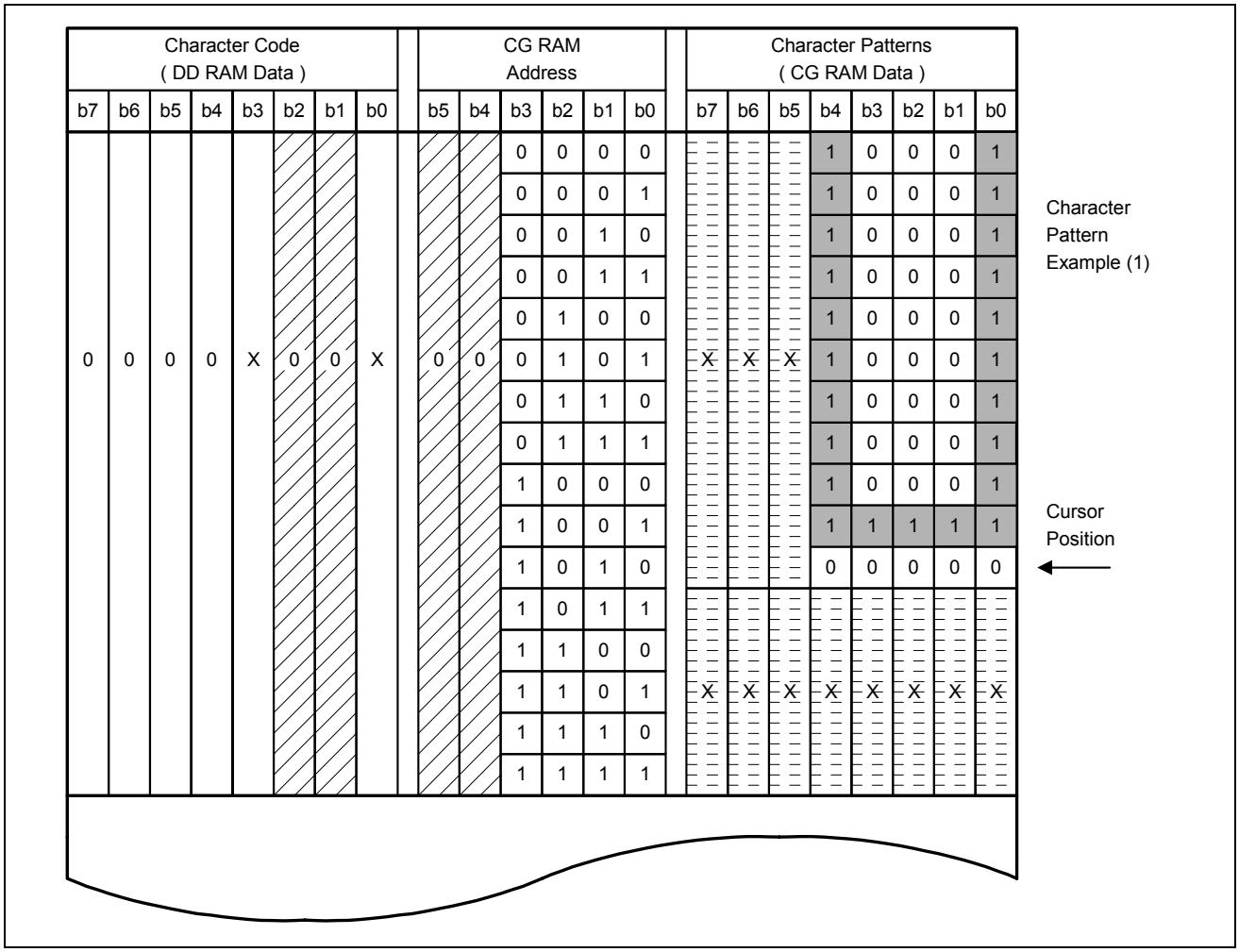
Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

Note4: "1": Selected, "0": No selected, "X": Do not care (0 or 1).

Note5: For example (1), to set character code (b2 = b1 = b0 = 0, b3 = 0 or 1, b7 - b4 = 0) is to display "T". That means character code $(00)_{16}$, and $(08)_{16}$ can display "T" character.

Note6: The bits 0-2 of the character code RAM is character pattern line position. The 8^{th} line is the cursor position and display is formed by logical OR with the cursor.

5.10.2. 5 x 10 dot character patterns



Note1: ▨ It means that the bit1-2 of the character code correspond to the bit4-5 of the CG RAM address.

Note2: ▤ These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

Note4: "1": Selected, "0": No selected, "X": Do not care (0 or 1).

Note5: For example (1), to set character code (b2 = b1 = 0, b3 = b0 = 0 or 1, b7-b4 = 0) is to display " U ". That means all of the character codes $(00)_{16}$, $(01)_{16}$, $(08)_{16}$, and $(09)_{16}$ can display " U " character.

Note6: The bits 0-3 of the character code RAM is character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.

5.11. Timing Generation Circuit

The timing generation circuit can generate needed timing signals to the internal circuits. In order to prevent the internal timing interface, the MPU access timing and the RAM access timing are separately generated.

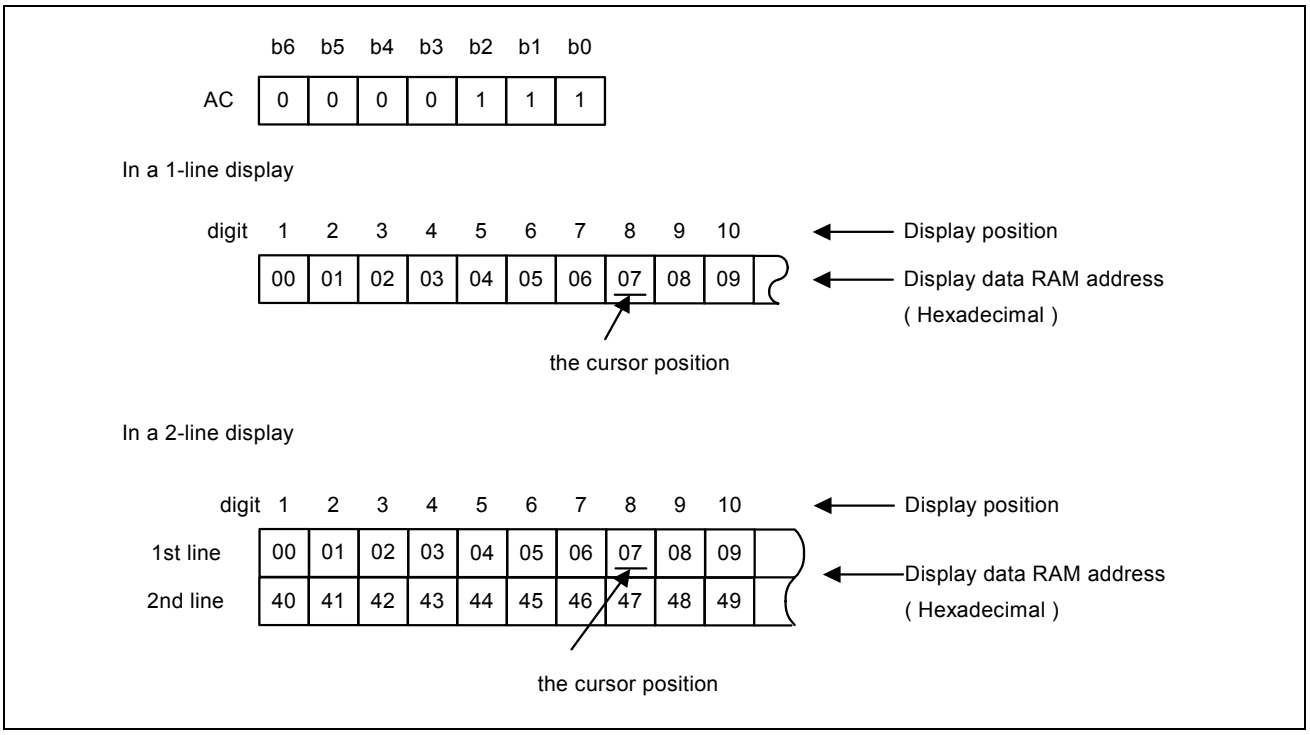
5.12. LCD Driver Circuit

There are 16 commons x 40 segments signal drivers in the LCD driver circuit. When a program specifies the character fonts and line numbers, the corresponding common signals will output drive waveforms and the others still output unselected waveforms.

5.13. Cursor / Blink Control Circuit

It can generate the cursor or blink in the cursor / blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

When the address counter is $(07)_{16}$, the cursor's position is shown as belows:



5.14. Interfacing to MPU

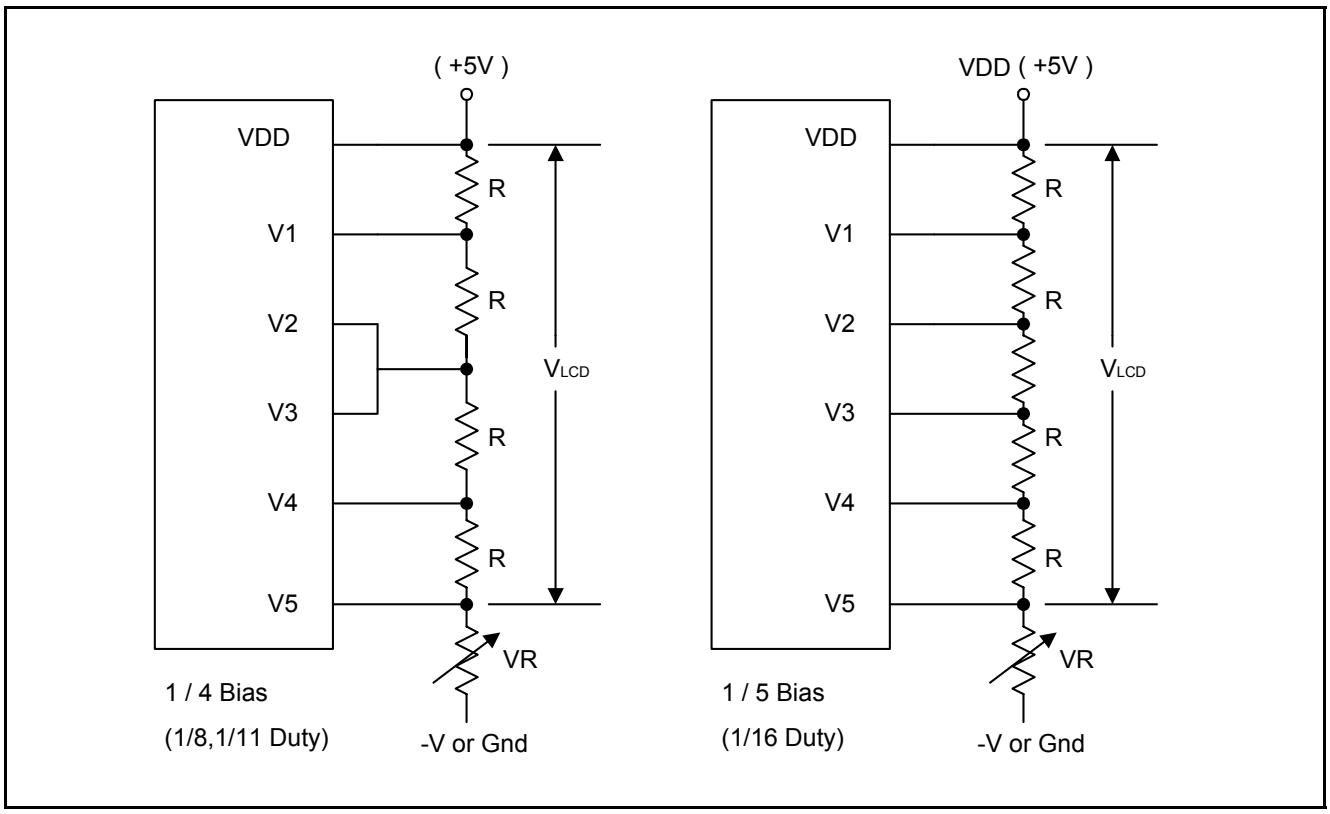
There are two kinds of data operations - one is 4-bit operations, the other is 8-bit operations. Using 4-bit MPU, the interfacing 4-bit datas are transferred by 4-busline (for 8-bit operation, DB7 to DB4). DB3 - 0 buslines are not used. Using 4-bit MPU to interface 8-bit datas needs two times. First, the higher order 4-bit datas are transferred by 4-busline (for 8-bit operation, DB7 to DB4). Secondly, the lower order 4-bit datas are transferred by 4-busline (for 8-bit operation, DB3 to DB0). Using 8-bit MPU, the interfacing 8-bit datas are transferred by 8-buslines (DB7 - 0).

5.15. Supply Voltage for LCD Drive

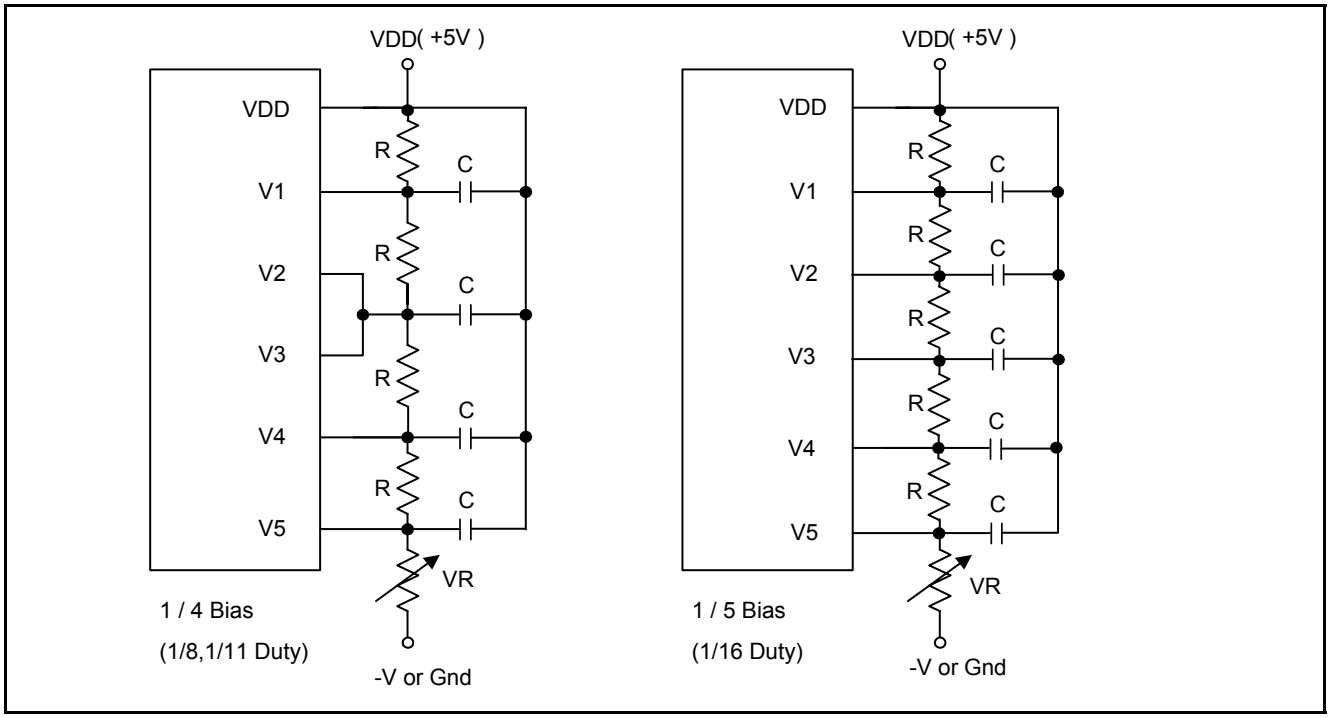
There are different voltages that supply to SPLC780A1's pins (V5 - 1) to obtain LCD drive waveform. The relations of the bias, duty factor and supply voltages are shown as belows:

Duty Factor / Supply Voltage \ Bias	1 / 8 , 1 / 11	1 / 16
	1 / 4	1 / 5
V1	VDD - 1/4 V_{LCD}	VDD - 1/5 V_{LCD}
V2	VDD - 1/2 V_{LCD}	VDD - 2/5 V_{LCD}
V3	VDD - 1/2 V_{LCD}	VDD - 3/5 V_{LCD}
V4	VDD - 3/4 V_{LCD}	VDD - 4/5 V_{LCD}
V5	VDD - V_{LCD}	VDD - V_{LCD}

The power connections for LCD (1/4 bias, 1/5 bias) are shown belows:



The bypass-capacitor can improve the LCD display's quality.



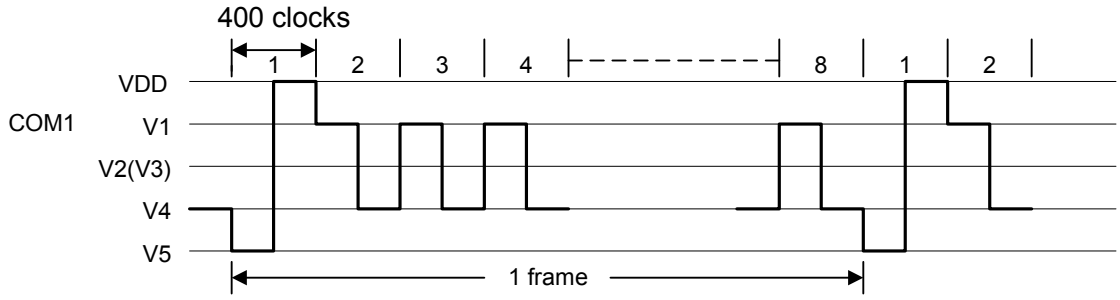
The bias voltage must have the following relations:

VDD > V1 > V2 ≧ V3 > V4 > V5.

5.15.1. The relations between LCD frame's frequency and oscillator's frequency

(Assume the oscillation frequency is 250.0KHz, 1 clock cycle time = 4.0μs)

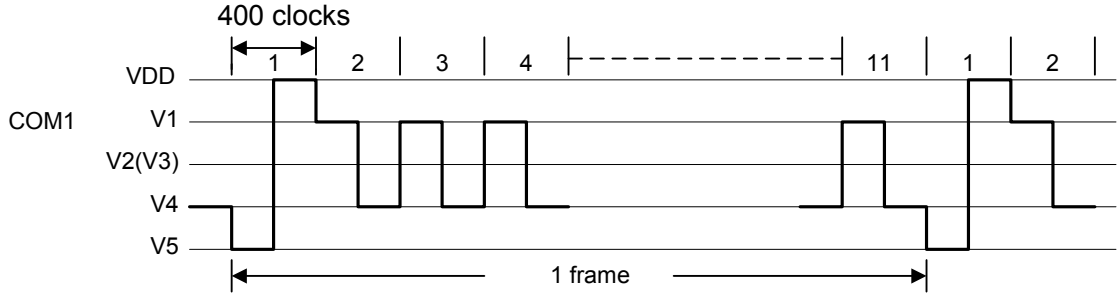
1. 1 / 8 Duty



1 frame = 4 (μs) x 400 x 8 = 12800 (μs) = 12.8 ms

Frame frequency = $\frac{1}{12.8\ (ms)}$ = 78.1 (Hz)

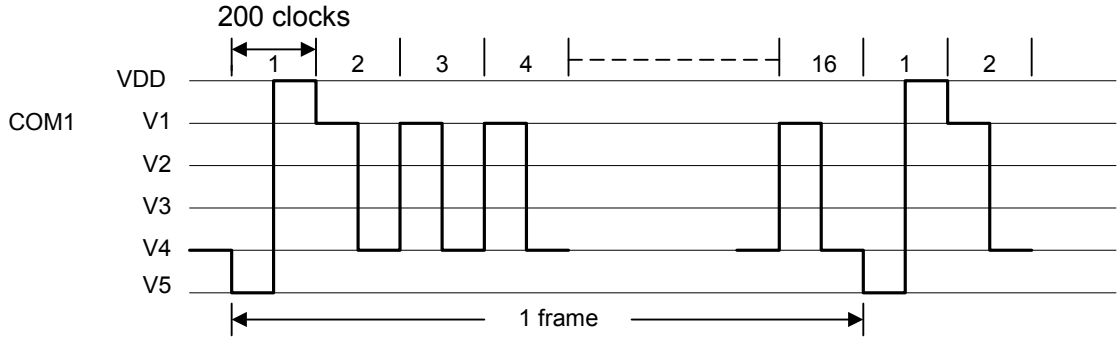
2. 1 / 11 Duty



1 frame = 4 (μs) x 400 x 11 = 17600 (μs) = 17.6 ms

Frame frequency = $\frac{1}{17.6\ (ms)}$ = 56.8 (Hz)

3. 1 / 16 Duty



1 frame = 4 (μs) x 200 x 16 = 12800 (μs) = 12.8 ms

Frame frequency = $\frac{1}{12.8\ (ms)}$ = 78.1 (Hz)

5.16. Register --- IR (Instruction Register) and DR (Data Register)

SPLC780A1 has two 8-bit registers - IR (instruction register) and DR (data register). In the followings, we can use the combinations of the RS pin and the R/W pin to select the IR and DR.

RS	R/W	Operation
0	0	IR write(Display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB6 - 0)
1	0	DR write (DR to Display data RAM or Character generator RAM)
1	1	DR read (Display data RAM or Character generator RAM to DR)

The IR can be written from the MPU but cannot read by the MPU.

5.17. Busy Flag (BF)

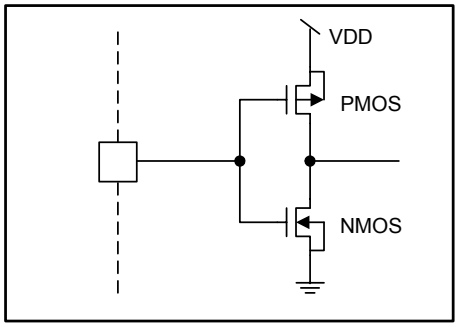
When RS = 0 and R/W = 1, the busy flag is output to DB7.
As the busy flag =1, SPLC780A1 is in busy state and does not accept any instructions until the busy flag = 0.

5.18. Address Counter (AC)

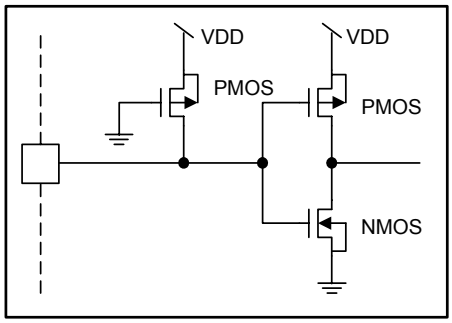
The address counter assigns addresses to display data RAM and character generator RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. After writing into (or reading from) display data RAM or character generator RAM, AC is automatically incremented by+1 (or decremented by -1). AC contents are output to DB6 - DB0 when RS = 0 and R/W = 1.

5.19. I/O Port Configuration

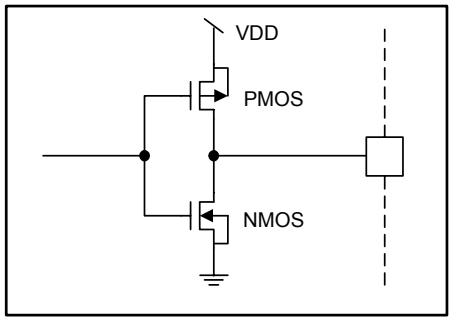
Input port : E



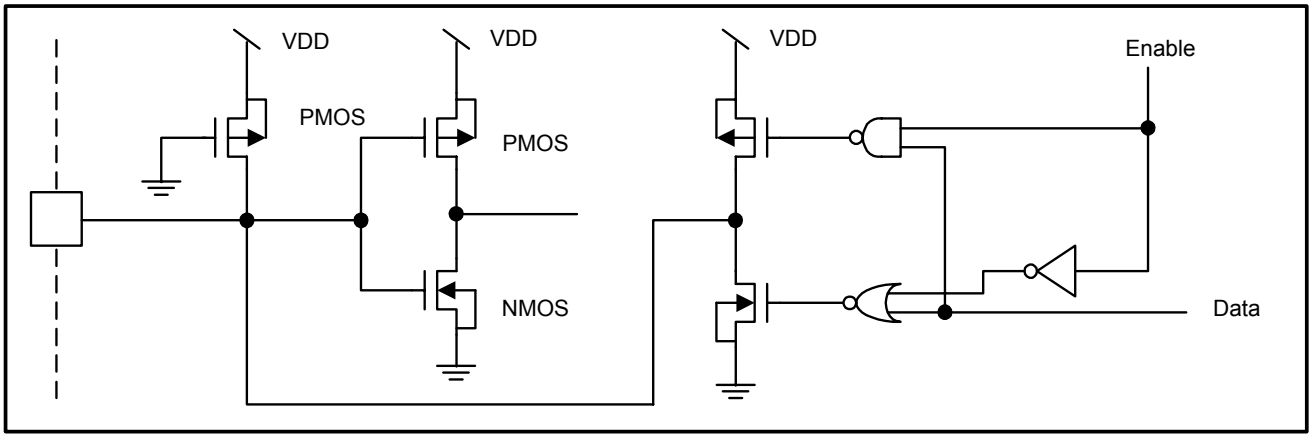
Input port : R / W , RS



Output port : CL1 , CL2 , M , D



Input / Output port : DB7 - 0



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD	-0.3V to +7.0V
Driver Supply Voltage	V_{LCD}	VDD-12V to VDD+0.3V
Input Voltage Range	V_{IN}	-0.3V to VDD + 0.3V
Operating Temperature	T_A	-25℃ to +75℃
Storage Temperature	T_{STO}	-55℃ to +125℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 2.7V to 4.5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	IDD	-	0.2	0.4	mA	External clock (Note)
Input High Voltage	V_{IH1}	0.7VDD	-	VDD	V	Pins:(E, RS, R/W, DB7 - 0)
Input Low Voltage	V_{IL1}	-0.3	-	0.55	V	
Input High Voltage	V_{IH2}	0.7VDD	-	VDD	V	Pin OSC1
Input Low Voltage	V_{IL2}	-0.2	-	0.2VDD	V	
Input High Current	I_{IH}	-1.0	-	1.0	μA	Pins: (RS, R/W, DB7 - 0)
Input Low Current	I_{IL}	-5.0	-15.0	-30.0	μA	VDD = 3.0V
Output High Voltage (TTL)	V_{OH1}	0.75VDD	-	-	V	I_{OH} = - 0.1mA Pins: DB7 - 0
Output Low Voltage (TTL)	V_{OL1}	-	-	0.2VDD	V	I_{OL} = 0.1mA Pins: DB7 - 0
Output High Voltage (CMOS)	V_{OH2}	0.8VDD	-	-	V	I_{OH} = - 40.0μA, Pins: CL1, CL2, M, D
Output Low Voltage (CMOS)	V_{OL2}	-	-	0.2VDD	V	I_{OL} = 40.0μA, Pins: CL1, CL2, M, D
Driver ON Resistance (COM)	R_{COM}	-	-	20.0	KΩ	I_O = ±50.0μA, V_{LCD} = 4.0V Pins: COM16 - 1
Driver ON Resistance (SEG)	R_{SEG}	-	-	30.0	KΩ	I_O = ±50.0μA, V_{LCD} = 4.0V Pins: SEG40 - 1
LCD Voltage	V_{LCD}	3.0	-	11.0	V	VDD-V5, 1/4 bias or 1/5 bias

Note: F_{OSC} = 250.0KHz, VDD = 3.0V, pin E = "L", RS, R/W, DB7 - 0 are open, all outputs are no loads.

6.3. AC Characteristics (VDD = 2.7V to 4.5V, T_A = 25℃)

6.3.1. Internal clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC1}	190.0	270.0	350.0	KHz	VDD = 3.0V R_f = 75.0KΩ±2%

6.3.2. External clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
External Frequency	F_{OSC2}	125.0	250.0	350.0	KHz	
Duty Cycle		45.0	50.0	55.0	%	
Rise/Fall Time	t_r, t_f	-	-	0.2	μs	

6.3.3. Write mode (Writing data from MPU to SPLC780A1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1000.0	-	-	ns	Pin E
E Pulse Width	t_{PW}	450.0	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25.0	ns	Pin E
Address Setup Time	t_{SP1}	60.0	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20.0	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	195.0	-	-	ns	Pins: DB7 - 0
Data Hold Time	t_{HD2}	10.0	-	-	ns	Pins: DB7 - 0

6.3.4. Read mode (Reading data from SPLC780A1 to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1000.0	-	-	ns	Pin E
E Pulse Width	t_W	450.0	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25.0	ns	Pin E
Address Setup Time	t_{SP1}	60.0	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20.0	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	360.0	ns	Pins: DB7 - 0
Data hold time	t_{HD2}	5.0	-	-	ns	Pin DB7 - 0

6.4. DC Characteristics (VDD = 4.5V to 5.5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	IDD	-	0.55	0.8	mA	External clock (Note)
Input High Voltage	V_{IH1}	2.2	-	VDD	V	Pins:(E, RS, R/W, DB7 - 0)
Input Low Voltage	V_{IL1}	-0.3	-	0.6	V	
Input High Voltage	V_{IH2}	VDD-1	-	VDD	V	Pin OSC1
Input Low Voltage	V_{IL2}	-0.2	-	1.0	V	Pin OSC1
Input High Current	I_{IH}	-2.0	-	2.0	μA	Pins: (RS, R/W, DB7 - 0)
Input Low Current	I_{IL}	-20.0	-50.0	-100.0	μA	VDD = 5.0V
Output High Voltage (TTL)	V_{OH1}	2.4	-	VDD	V	I_{OH} = - 0.1mA Pins: DB7 - 0
Output Low Voltage (TTL)	V_{OL1}	-	-	0.4	V	I_{OL} = 0.1mA Pins: DB7 - 0
Output High Voltage (CMOS)	V_{OH2}	0.9VDD	-	VDD	V	I_{OH} = - 40.0μA, Pins: CL1, CL2, M, D
Output Low Voltage (CMOS)	V_{OL2}	-	-	0.1VDD	V	I_{OL} = 40.0μA, Pins: CL1, CL2, M, D
Driver ON Resistance (COM)	R_{COM}	-	-	20.0	KΩ	I_O = ±50.0μA, V_{LCD} = 4.0V Pins: COM16 - 1
Driver ON Resistance (SEG)	R_{SEG}	-	-	30.0	KΩ	I_O = ±50.0μA, V_{LCD} = 4.0V Pins: SEG40 - 1
LCD Voltage	V_{LCD}	3.0	-	11.0	V	VDD - V5, 1/4 bias or 1/5 bias

Note: F_{OSC} = 250.0KHz, VDD = 5.0V, pin E = "L", RS, R/W, DB7 - 0 are open, all outputs are no loads.

6.5. AC Characteristics (VDD = 4.5V to 5.5V, T_A = 25℃)

6.5.1. Internal clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC1}	190.0	270.0	350.0	KHz	VDD = 5.0V Rf = 91.0KΩ±2%

6.5.2. External clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
External Frequency	F_{OSC2}	125.0	250.0	350.0	KHz	
Duty Cycle		45.0	50.0	55.0	%	
Rise/Fall Time	t_r, t_f	-	-	0.2	μs	

6.5.3. Write mode (Writing data from MPU to SPLC780A1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	400.0	-	-	ns	Pin E
E Pulse Width	t_{PW}	150.0	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25.0	ns	Pin E
Address Setup Time	t_{SP1}	30.0	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10.0	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	40.0	-	-	ns	Pins: DB7 - 0
Data Hold Time	t_{HD2}	10.0	-	-	ns	Pins: DB7 - 0

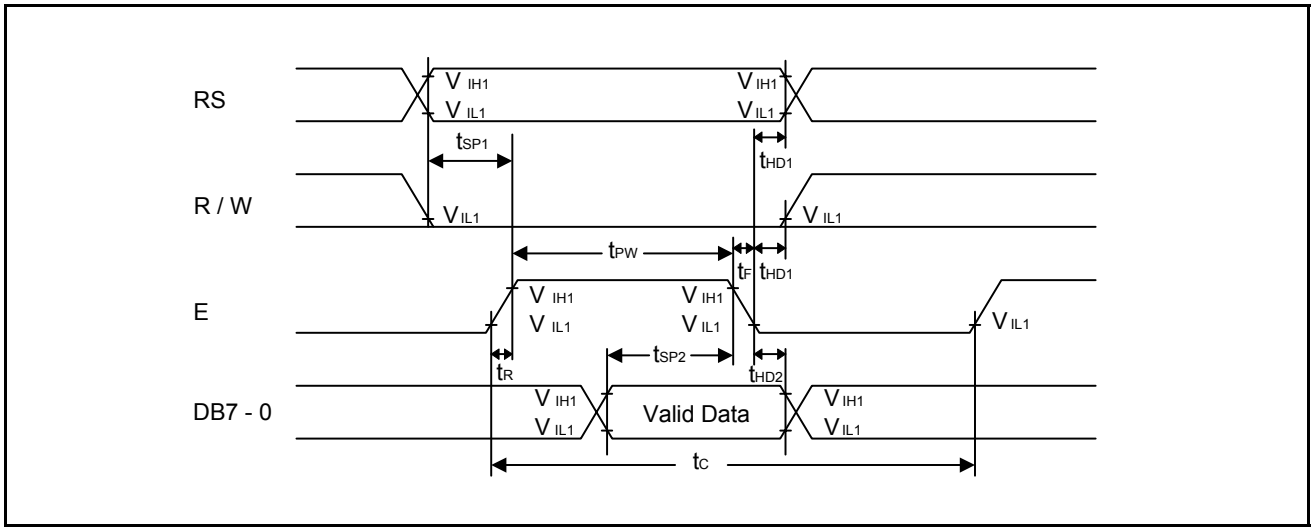
6.5.4. Read mode (Reading data from SPLC780A1 to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	400.0	-	-	ns	Pin E
E Pulse Width	t_W	150.0	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25.0	ns	Pin E
Address Setup Time	t_{SP1}	30.0	-	-	ns	Pins: RS, R/W,E
Address Hold Time	t_{HD1}	10.0	-	-	ns	Pins: RS, R/W,E
Data Output Delay Time	t_D	-	-	100.0	ns	Pins: DB7 - 0
Data hold time	t_{HD2}	20.0	-	-	ns	Pin DB7 - 0

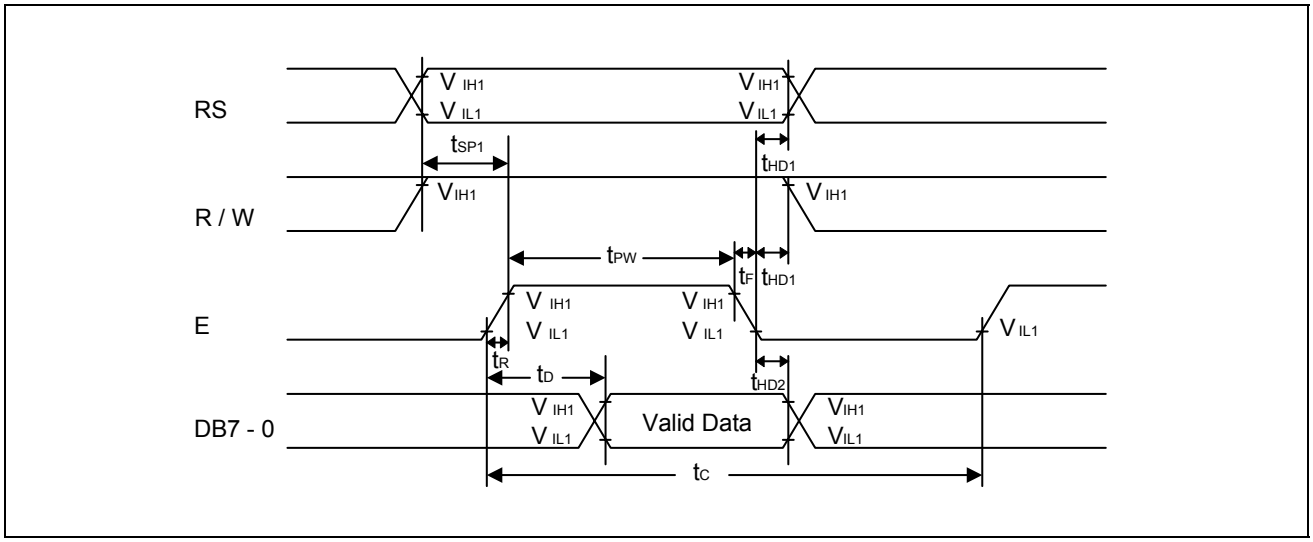
6.5.5. Interface mode with LCD driver (SPLC100A1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Clock pulse width high	t_{PWH}	800.0	-	-	ns	Pins: CL1, CL2
Clock pulse width low	t_{PWL}	800.0	-	-	ns	Pins: CL1, CL2
Clock setup time	t_{CSP}	500.0	-	-	ns	Pins: CL1, CL2
Data setup time	t_{DSP}	300.0	-	-	ns	Pins: D
Data hold time	t_{HD}	300.0	-	-	ns	Pins: D
M delay time	t_D	-1000.0	-	1000.0	ns	Pins: M

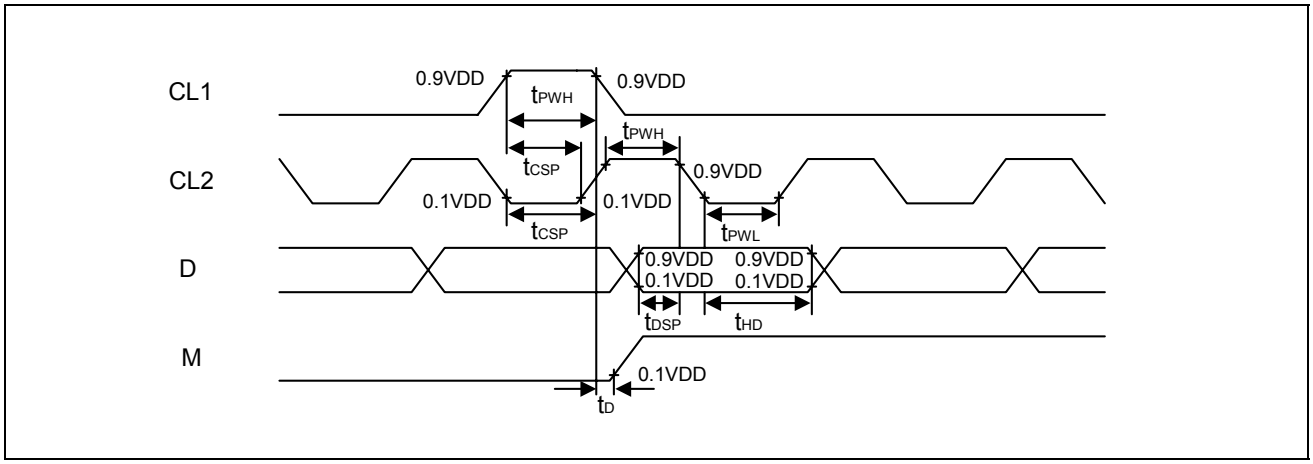
6.6. Write Mode Timing Diagram (Writing Data from MPU to SPLC780A1)



6.7. Read Mode Timing Diagram (Reading Data from SPLC780A1 to MPU)



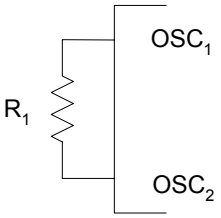
6.8. Interface Mode with SPLC100A1 Timing Diagram



7. APPLICATION CIRCUITS

7.1. R-oscillator

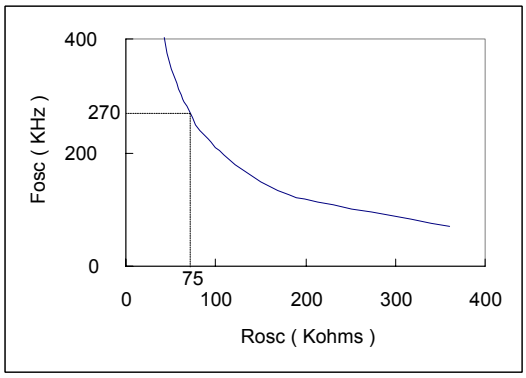
The oscillation resistor R_f is used only for the internal oscillaotr operation mode.



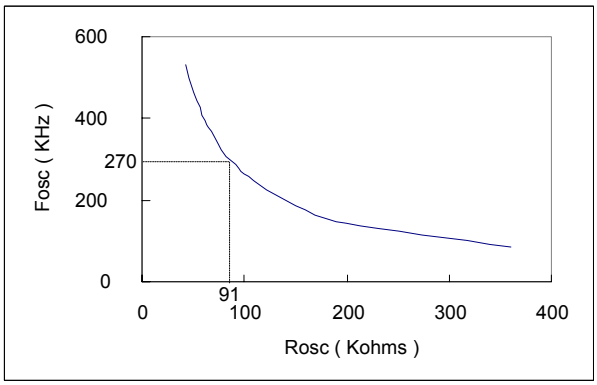
R_f : 75KΩ ±2% (when VDD = 3.0V)

R_f : 91KΩ ± 2% (when VDD = 5.0V)

Since the oscillation frequency varies depending on the OSC_1 and OSC_2 pin capacitance, the wiring length to these pins should be minimized.

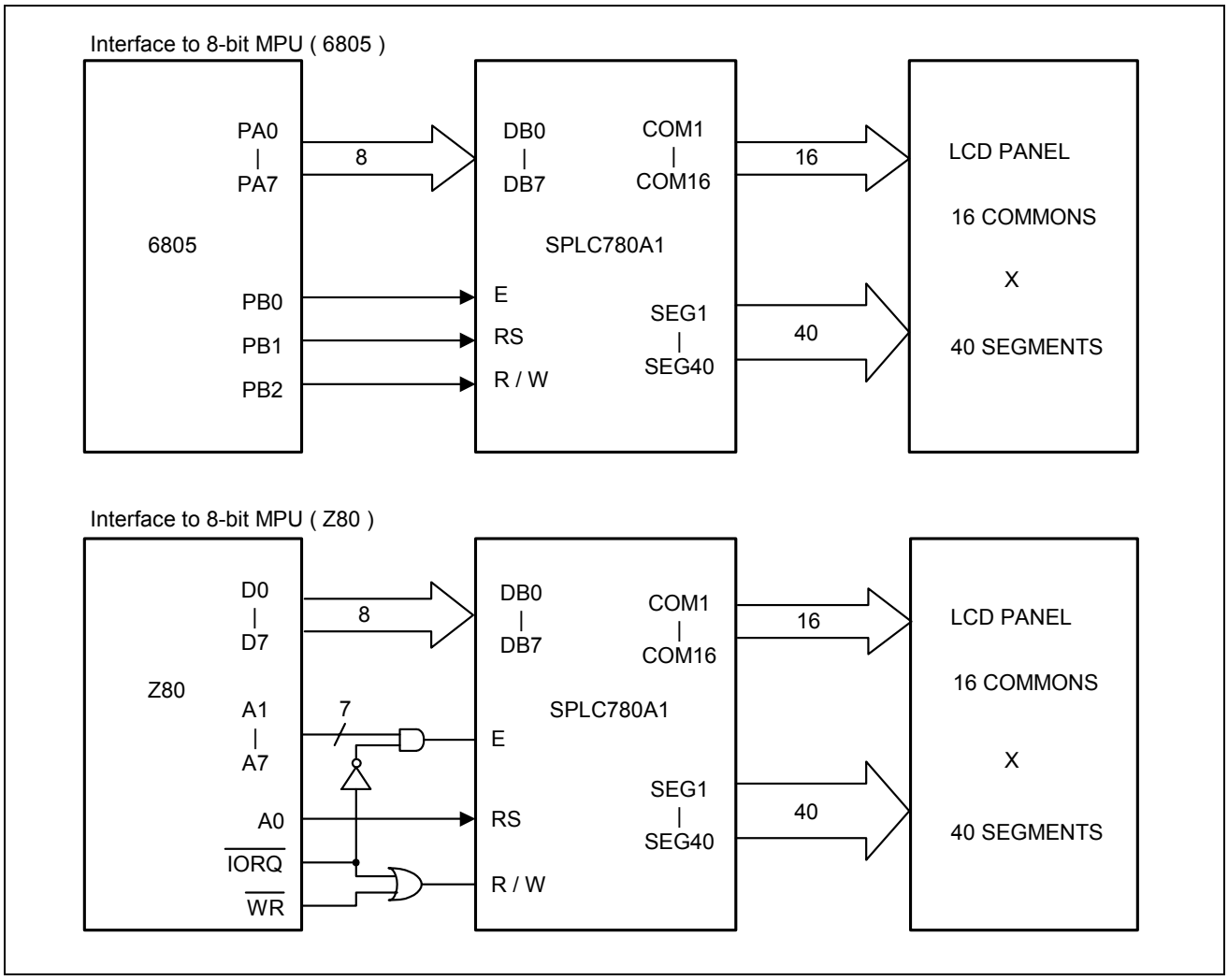


VDD = 3.0V

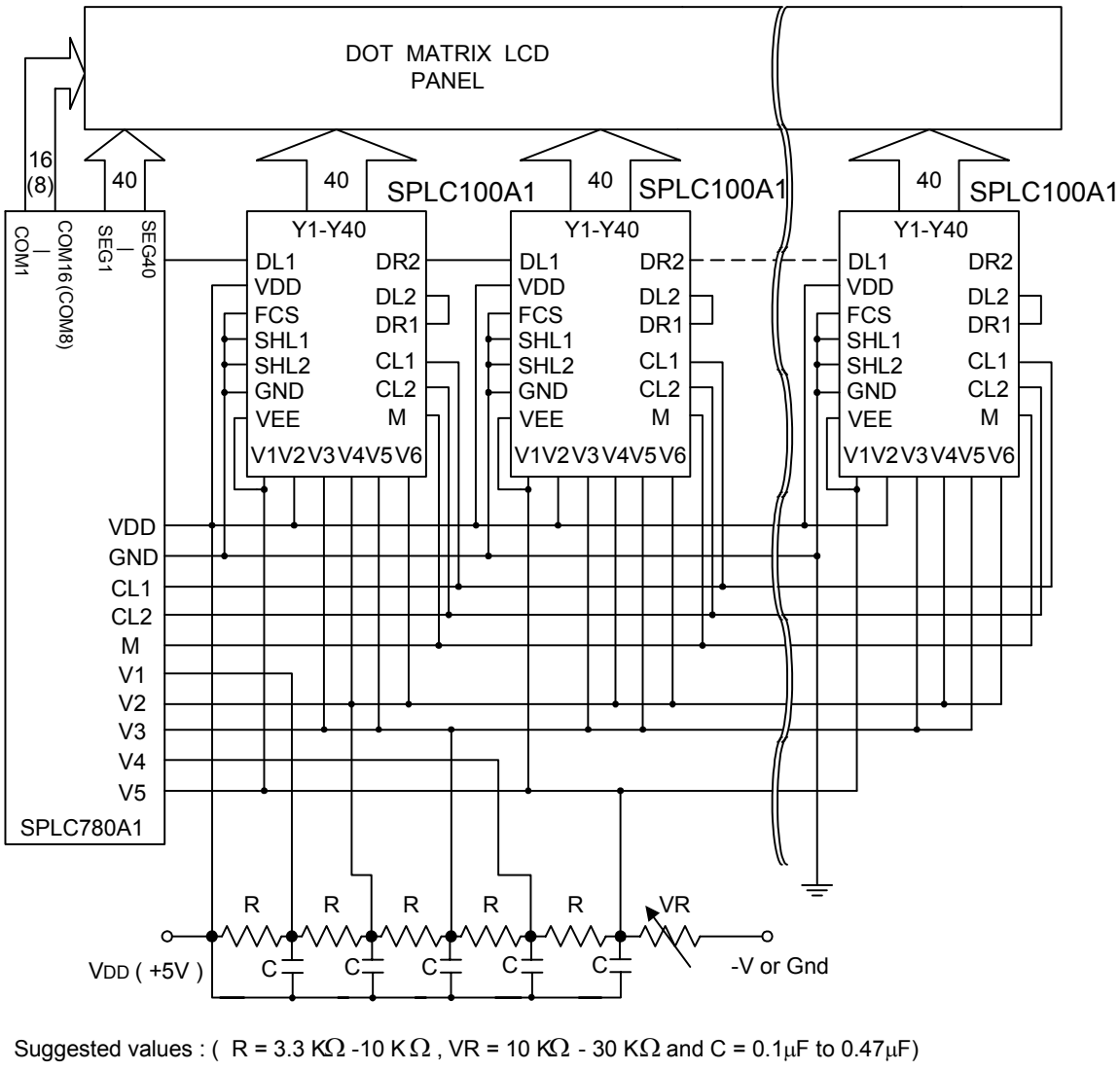


VDD = 5.0V

7.2. Interface to MPU

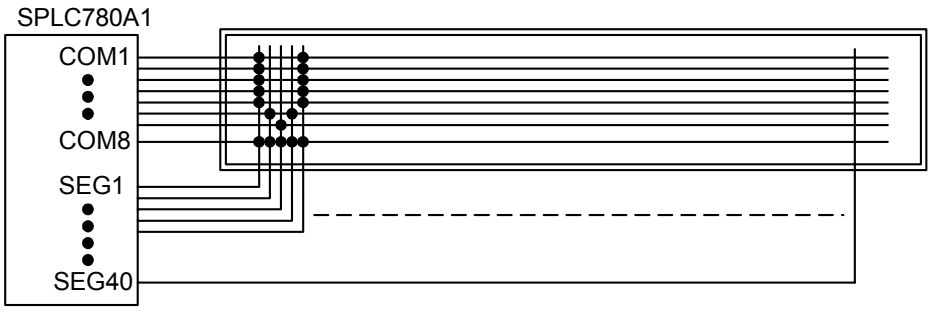


7.3. SPLC780A1 Application Circuit

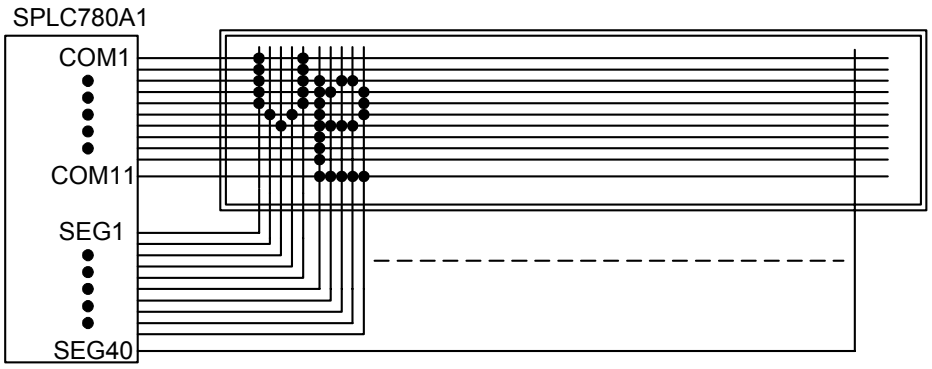


Suggested values : (R = 3.3 KΩ -10 KΩ , VR = 10 KΩ - 30 KΩ and C = 0.1μF to 0.47μF)

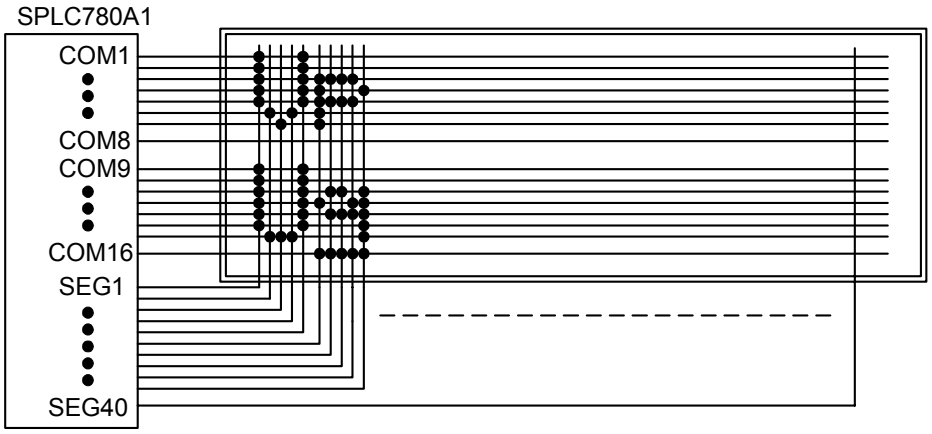
7.4. Applications for LCD



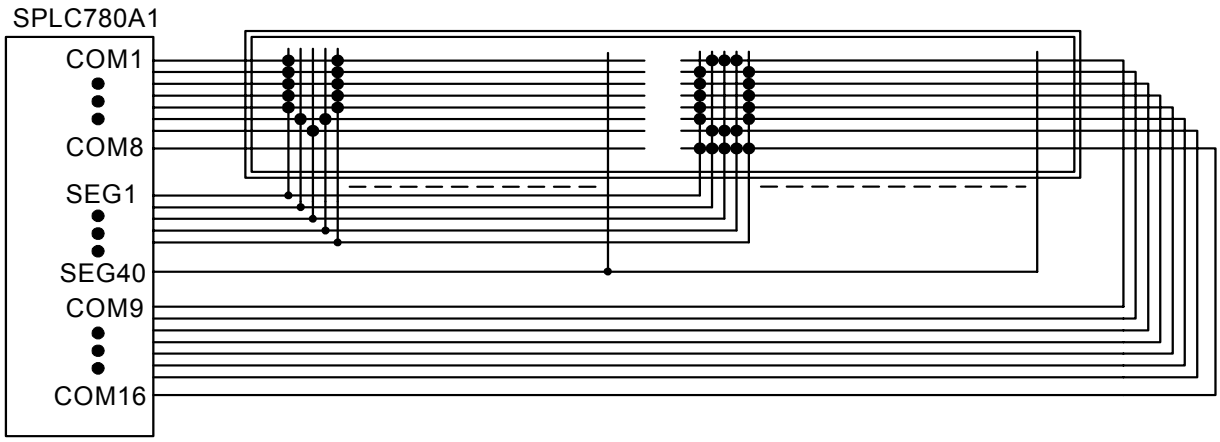
(Example 1) : 5 x 7 dots , 8 characters x 1 line [1 / 4 Bias , 1 / 8 Duty]



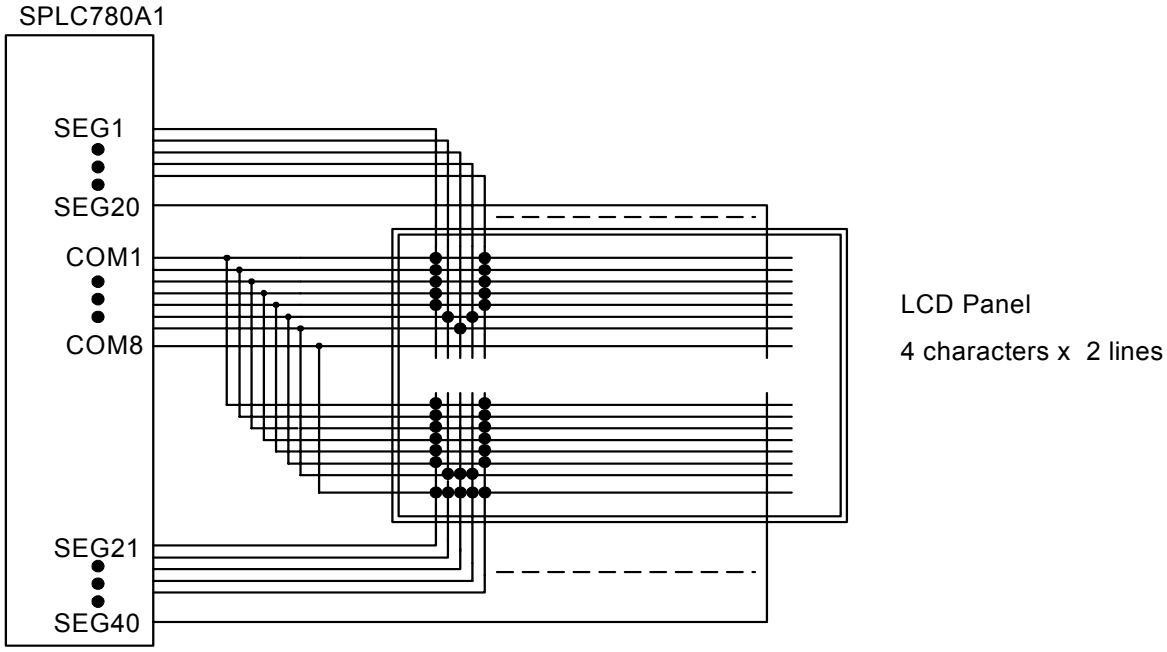
(Example 2) : 5 x 10 dots , 8 characters x 1 line [1 / 4 Bias , 1 / 11 Duty]



(Example 3) : 5 x 7 dots , 8 characters x 2 lines [1 / 5 Bias , 1 / 16 Duty]



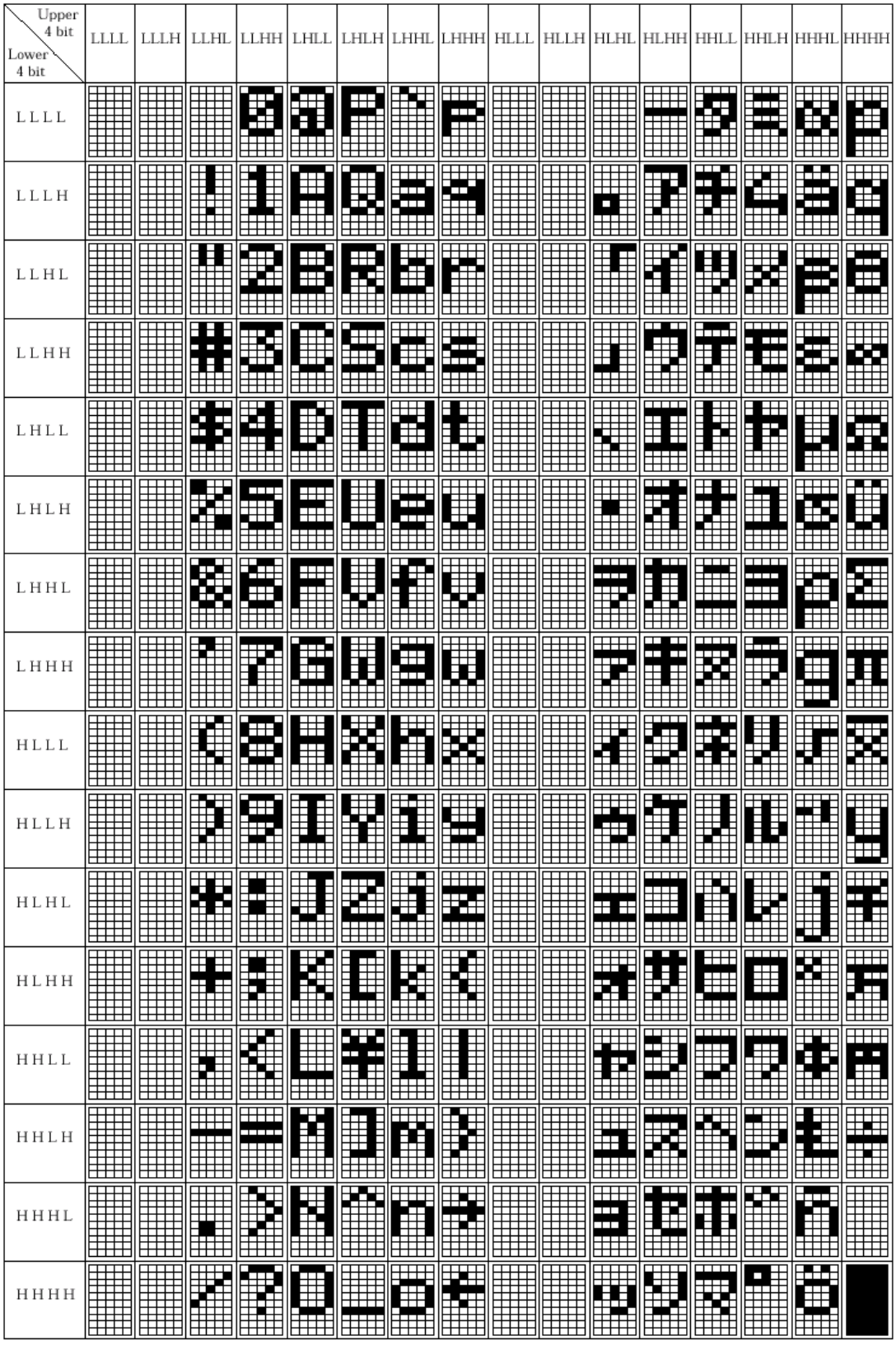
(Example 4) : 5 x 7 dots , 16 characters x 1 line [1 / 5 Bias , 1 / 16 Duty]



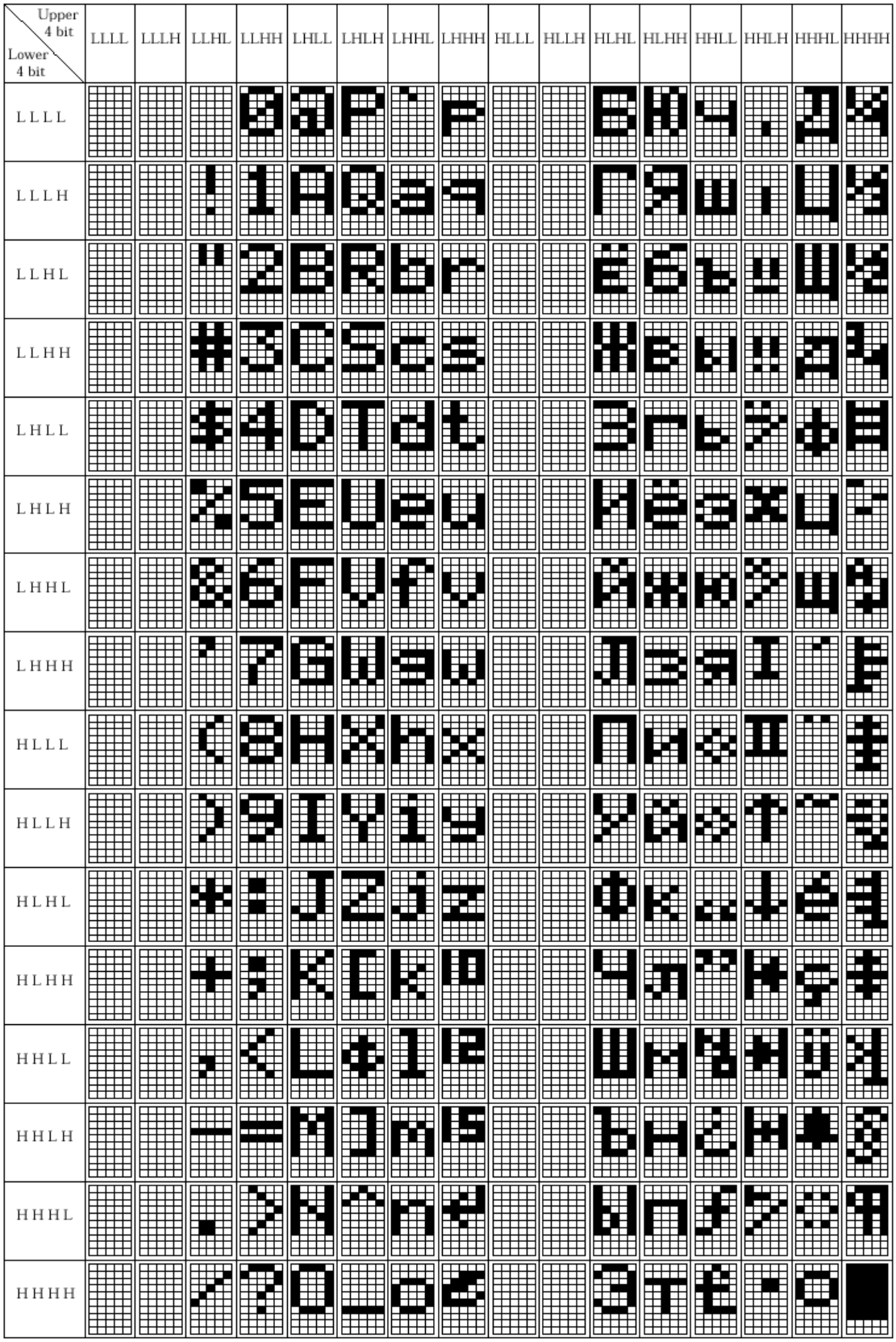
(Example 5) : 5 x 7 dots , 4 characters x 2 lines [1 / 4 Bias , 1 / 8 Duty]

8. CHARACTER GENERATOR ROM

8.1. SPLC780A1 - 01

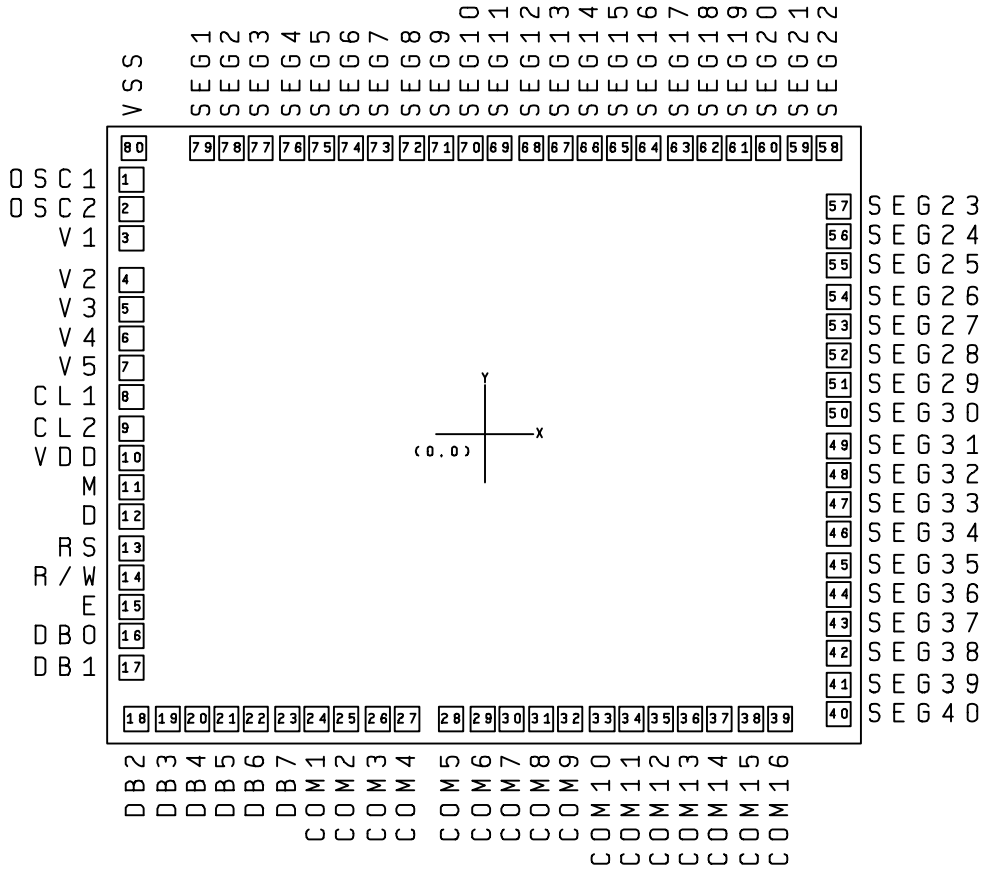


8.2. SPLC780A1 - 02



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 3840μm x 3170μm

PAD Size: 100μm x 100μm

This IC substrate should be connected to VDD

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPLC780A1-nnnnV-C	Chip form
SPLC780A1-nnnnV-PQ05	Package form - QFP 80L

Note1: Code number (nnnnV) is assigned for customer.

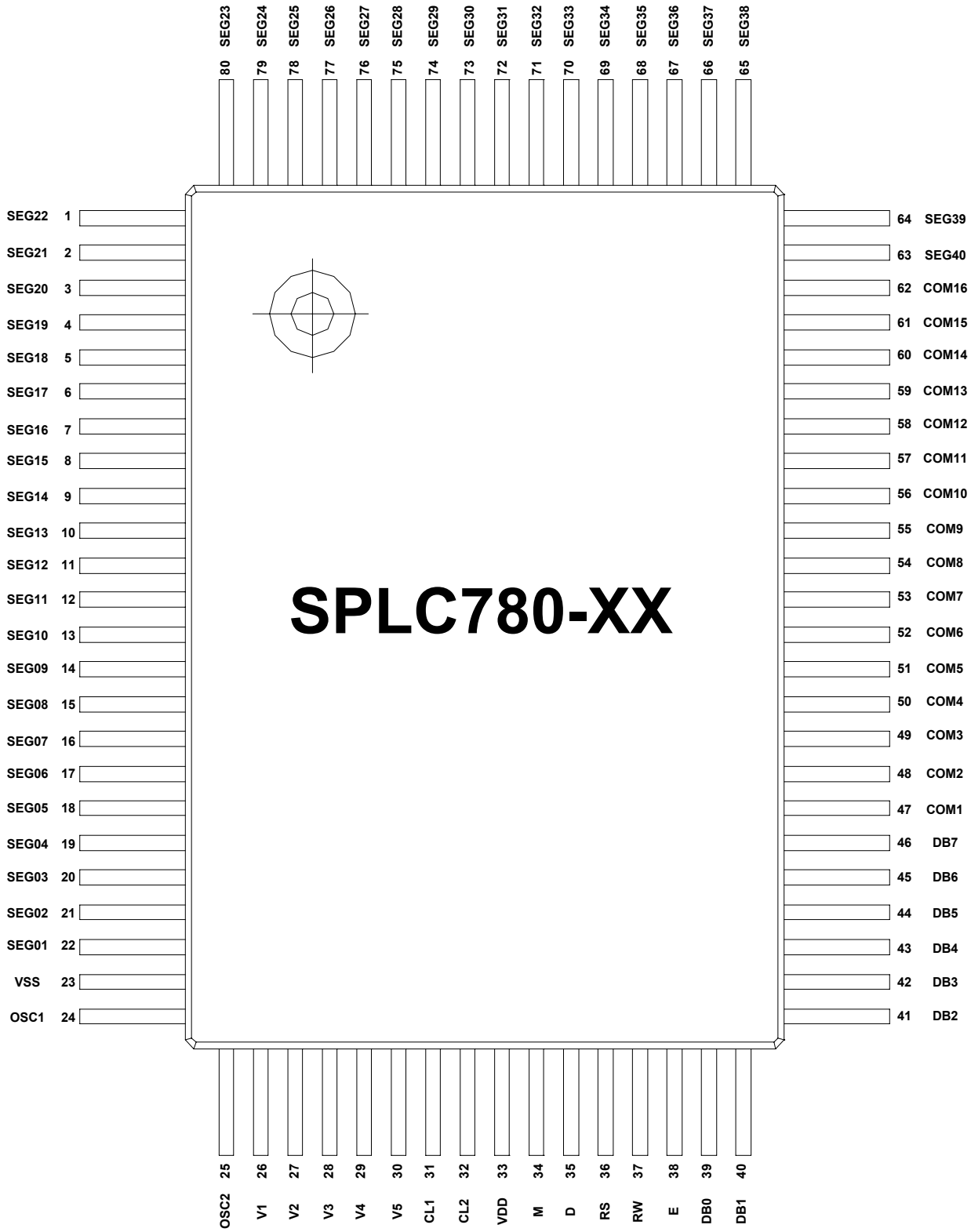
Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	OSC1	-1738	1256	41	SEG39	1744	-1226
2	OSC2	-1738	1110	42	SEG38	1744	-1078
3	V1	-1738	963	43	SEG37	1744	-932
4	V2	-1738	765	44	SEG36	1744	-786
5	V3	-1738	619	45	SEG35	1744	-638
6	V4	-1738	472	46	SEG34	1744	-492
7	V5	-1738	325	47	SEG33	1744	-345
8	CL1	-1738	178	48	SEG32	1744	-199
9	CL2	-1738	32	49	SEG31	1744	-51
10	VDD	-1738	-115	50	SEG30	1744	94
11	M	-1738	-261	51	SEG29	1744	241
12	D	-1738	-408	52	SEG28	1744	388
13	RS	-1738	-554	53	SEG27	1744	535
14	R / W	-1738	-702	54	SEG26	1744	681
15	E	-1738	-848	55	SEG25	1744	829
16	DB0	-1738	-994	56	SEG24	1744	975
17	DB1	-1738	-1142	57	SEG23	1744	1122
18	DB2	-1705	-1404	58	SEG22	1695	1406
19	DB3	-1558	-1404	59	SEG21	1549	1406
20	DB4	-1411	-1404	60	SEG20	1402	1406
21	DB5	-1264	-1404	61	SEG19	1255	1406
22	DB6	-1118	-1404	62	SEG18	1108	1406
23	DB7	-970	-1404	63	SEG17	962	1406
24	COM1	-819	-1404	64	SEG16	814	1406
25	COM2	-673	-1404	65	SEG15	668	1406
26	COM3	-526	-1404	66	SEG14	522	1406
27	COM4	-379	-1404	67	SEG13	374	1406
28	COM5	-158	-1404	68	SEG12	228	1406
29	COM6	-12	-1404	69	SEG11	81	1406
30	COM7	135	-1404	70	SEG10	-64	1406
31	COM8	282	-1404	71	SEG9	-212	1406
32	COM9	428	-1404	72	SEG8	-358	1406
33	COM10	576	-1404	73	SEG7	-505	1406
34	COM11	722	-1404	74	SEG6	-652	1406
35	COM12	868	-1404	75	SEG5	-799	1406
36	COM13	1015	-1404	76	SEG4	-945	1406
37	COM14	1162	-1404	77	SEG3	-1093	1406
38	COM15	1309	-1404	78	SEG2	-1239	1406
39	COM16	1455	-1404	79	SEG1	-1386	1406
40	SEG40	1744	-1372	80	VSS	-1719	1402

9.4. Package Configuration

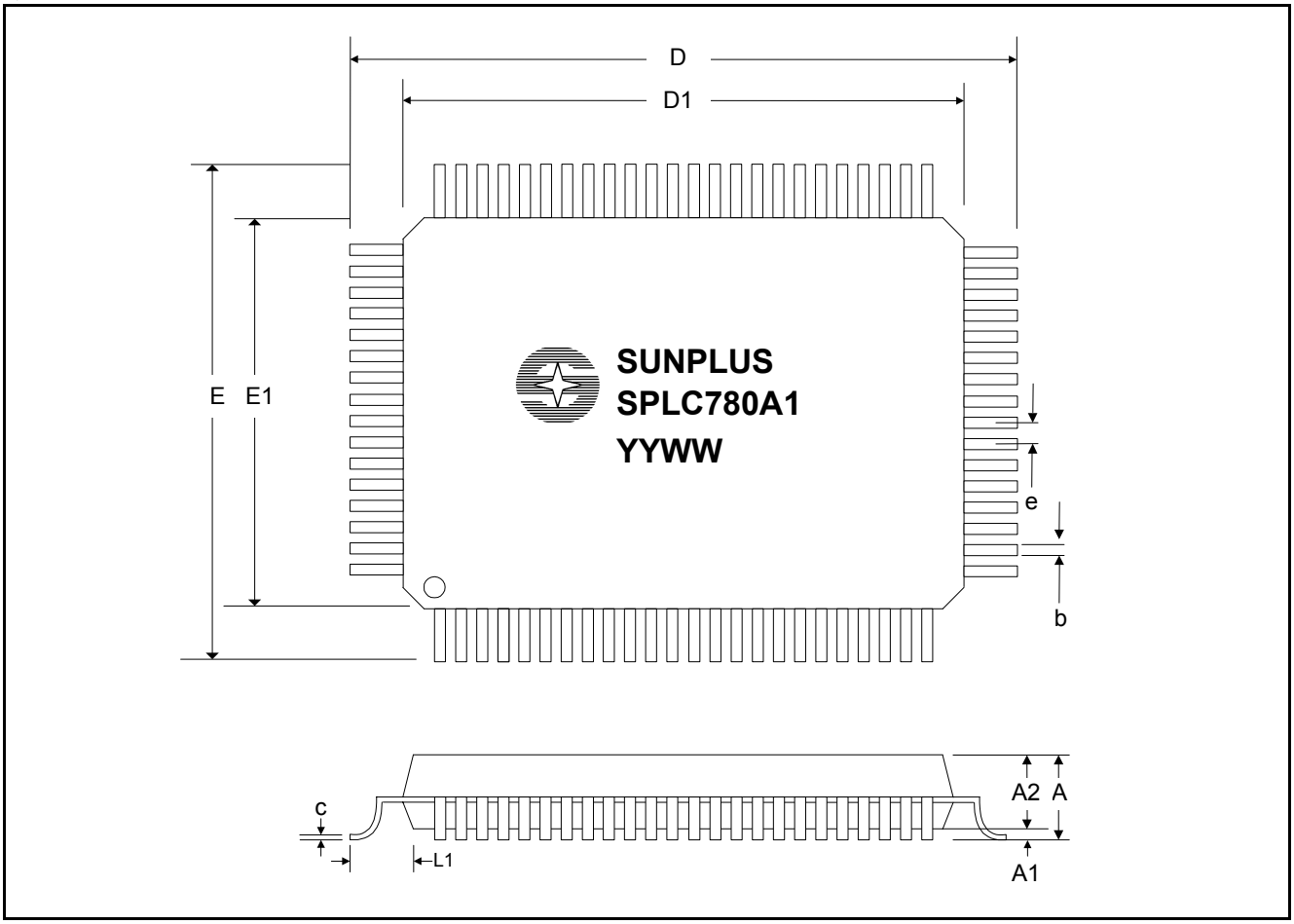
QFP 80L Top View



9.5. Package Information

QFP 80L Outline Dimensions

Unit: Millimeter



Symbol	Min.	Nom.	Max.	Unit
D		23.20 REF		Millimeter
D1		20.00 REF		Millimeter
E		17.20 REF		Millimeter
E1		14.00 REF		Millimeter
e		0.80 REF		Millimeter
b	0.30	0.35	0.45	Millimeter
A	-	-	3.40	Millimeter
A1	0.25	-	-	Millimeter
A2	2.50	2.72	2.90	Millimeter
c	0.11	0.15	0.23	Millimeter
L1		1.60 REF		Millimeter

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
FEB. 26, 1999	1.0	Original	
DEC. 03, 1999	1.1	Modify format	
MAY. 05, 2000	1.2	1. I_{IL}: -10μA ~ -12μA -> I_{IL}: -5μA ~ -30μA 2. I_{IL}: -50μA ~ -250μA -> I_{IL}: -20μA ~ -100μA 3. Add "*PACKAGE CONFIGURATION*" and "*PACKAGE INFORMATION*"	23 25 36 - 38
OCT. 25, 2000	1.3	1. Add "*INSTRUCTION TABLE*" 2. Power on reset flow chart is for 4.5V only. Add "Wait time > 40ms" followed by the description of VDD > 2.7V 3. Modify the pin sequence of COM/SEG in application circuit to the same as the LCD panel sequence. 4. Modify ROM code to the grid format by ROM code editor to ensure the font correspondence and reconfirmation. 5. Add PAD size description 6. Correct "PACKAGE INFORMATION" outline drawing: 64 PIN QFP -> 80 PIN QFP	6 11 - 12 30-31 34 - 35 36 40-41
APR. 04, 2001	1.4	1. Modify "Operating Temperature" vaule from "-20℃ to +75℃" to "-25℃ to +75℃" in the "*6.1 Absolute Maximum Ratings*" 2. Correct chip size: 3810μm X 3140μ-> 3840μm X 3170μm 3. Add Note2 in the "*9.1 PAD Assignment*" 4. Add "*11. REVISION HISTORY*" 5. Renew to a new document format	23 35 35 40
JUL. 09, 2002	1.5	1. Add Package Information in the "*9.2 Ordering Information*" 2. Add Note1 in the "*9.1 PAD Assignment*" 3. Update "*9.5 Package Information*" 4. Renew to a new document format	35 35 38