



SOLOMON SYSTECH SEMICONDUCTOR TECHNICAL DATA

Advanced Information

LCD Segment / Common Driver with Controller

CMOS

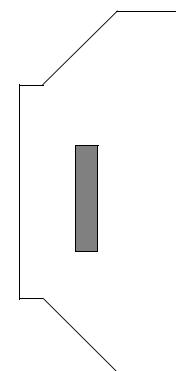
SSD1815 is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix graphic display system. It consists of 197 high voltage driving output pins for driving 132 Segments, 64 Commons and 1 icon driving-Common.

SSD1815 displays data directly from its internal 132 X 65 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through a software selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

SSD1815 embeds a DC-DC Converter, an On-Chip Bias Divider and an On-Chip Oscillator which reduce the number of external components. With the special design on minimizing power consumption and die/package layout, SSD1815 is suitable for any portable battery-driven applications requiring a long operation period and a compact size.

- Single Supply Operation, 1.8 V - 3.5V
- Minimum -12.0V LCD Driving Output Voltage
- Low Current Sleep Mode
- On-Chip Voltage Generator / External Power Supply
- 2X / 3X / 4X On-Chip DC-DC Converter
- On-Chip Oscillator
- Programmable Multiplex ratio (2Mux ~ 65Mux)
- On-Chip Bias Divider
- Programmable bias ratio
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface and Serial Peripheral Interface
- On-Chip 132 X 65 Graphic Display Data RAM
- Re-mapping of Row and Column Drivers
- Vertical Scrolling
- Display Offset Control
- 64 Level Internal Contrast Control
- External Contrast Control
- Programmable LCD Driving Voltage Temperature Coefficients
- Available in Gold Bump Die and TAB (Tape Automated Bonding) Package

SSD1815



TAB

Gold Bump Die

ORDERING INFORMATION

| | |
|------------|---------------|
| SSD1815Z | Gold Bump Die |
| SSD1815TR | TAB |
| SSD1815T1R | TAB |
| SSD1815T2R | TAB |
| SSD1815T3R | TAB |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Block Diagram

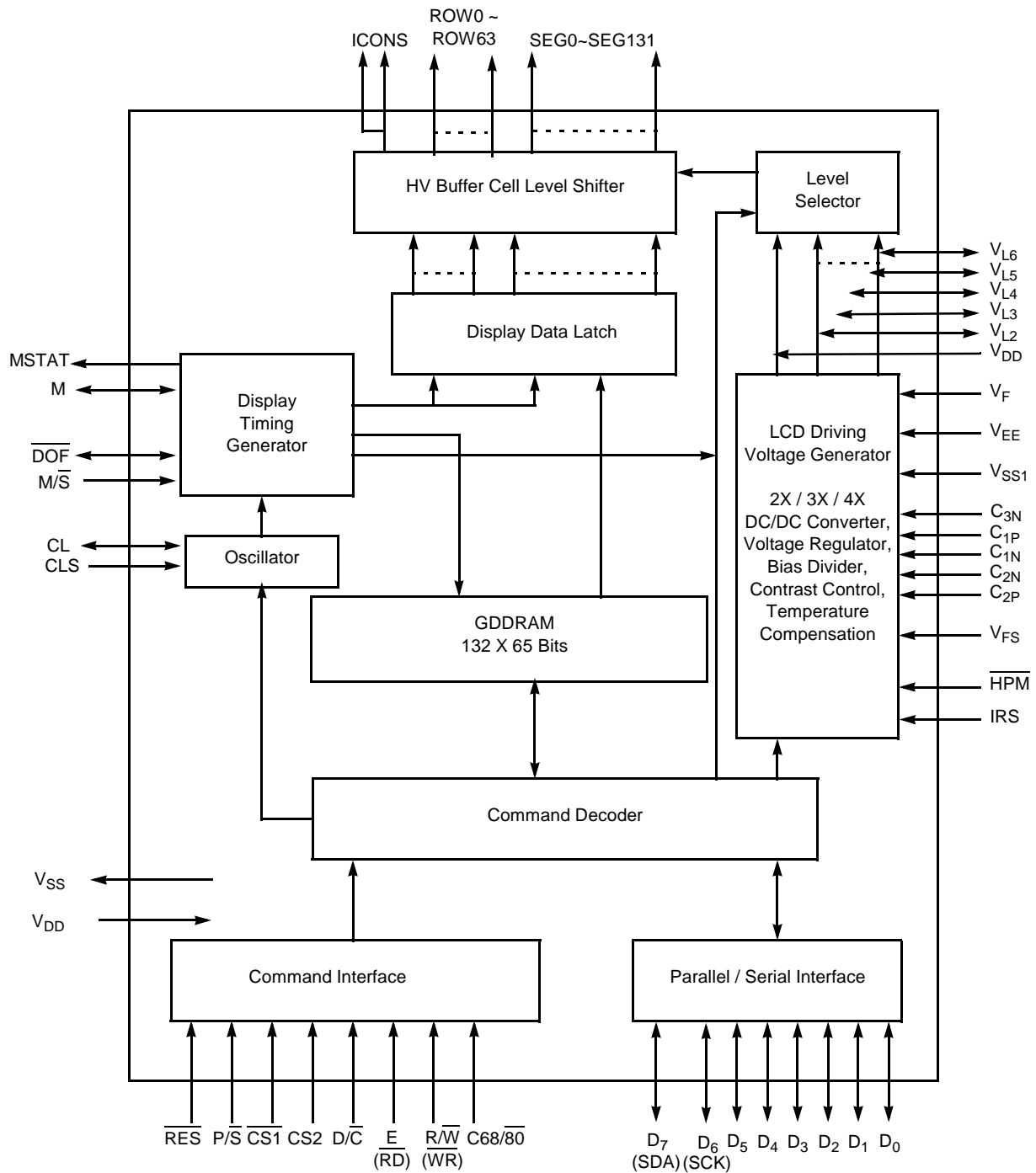
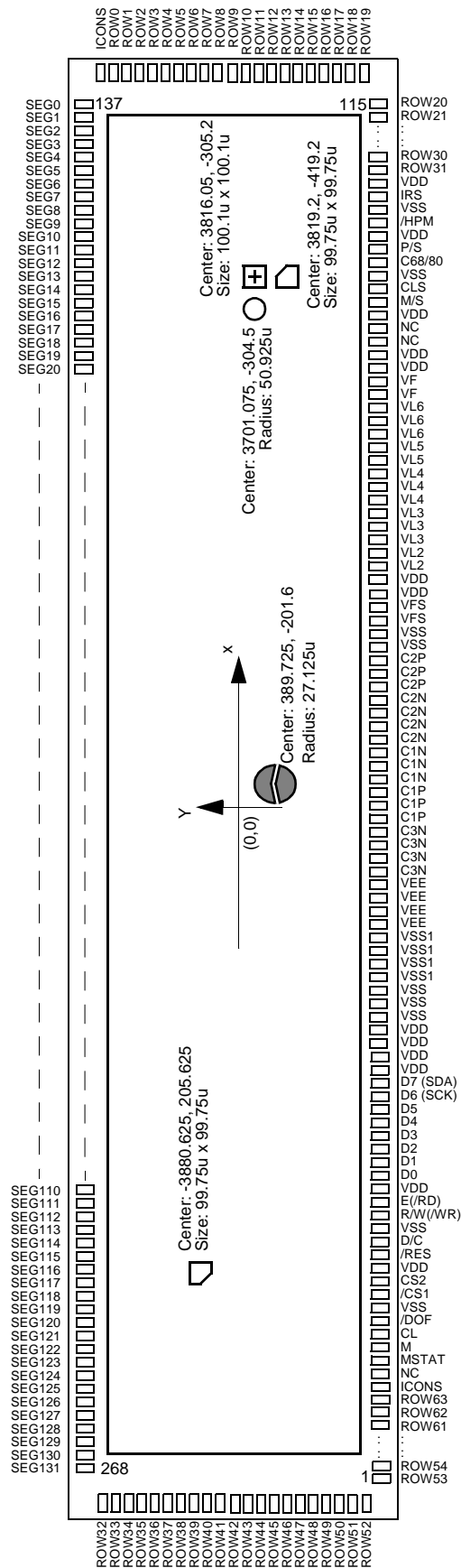


Figure 1 - Block Diagram of SSD1815



Gold Bump Alignment Mark

This alignment mark contains gold nump for IC bumping process alignment and IC identifications. No conductive tracks should be laid underneath this mark to avoid short circuit.

Note:

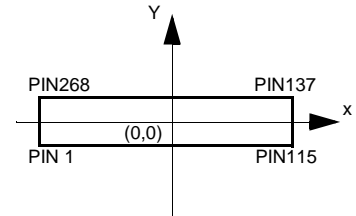
1. This diagram showing Die Face Up view.
2. Coordinates and Size of all alignment marks are in unit μm and w.r.t. center of the chip.

Die Size: 10.977mm X 1.912mm
 Die Thickness: 533 +/-25 μm
 Bump Pitch: 76.2 μm [Min]
 Bump Height: Nominal 18 μm
 Tolerance <4 μm within die
 <8 μm within lot

Figure 2 - SSD1815Z Die Pin Assignment

Table 1 - SSD1815Z Die Pad Coordinates

| PAD # | NAME | X | Y | PAD # | NAME | X | Y | PAD # | NAME | X | Y |
|-------|-------|----------|---------|-------|--------|---------|---------|-------|-------|---------|---------|
| 1 | ROW53 | -4958.45 | -751.98 | 61 | C2N | 266.70 | -771.93 | 116 | ROW19 | 5285.18 | -768.78 |
| 2 | ROW54 | -4882.15 | -751.98 | 62 | C2N | 355.60 | -771.93 | 117 | ROW18 | 5285.18 | -692.48 |
| 3 | ROW55 | -4805.85 | -751.98 | 63 | C2N | 444.50 | -771.93 | 118 | ROW17 | 5285.18 | -616.18 |
| 4 | ROW56 | -4729.55 | -751.98 | 64 | C2N | 533.40 | -771.93 | 119 | ROW16 | 5285.18 | -539.88 |
| 5 | ROW57 | -4653.25 | -751.98 | 65 | C2P | 622.30 | -771.93 | 120 | ROW15 | 5285.18 | -463.58 |
| 6 | ROW58 | -4576.95 | -751.98 | 66 | C2P | 711.20 | -771.93 | 121 | ROW14 | 5285.18 | -387.28 |
| 7 | ROW59 | -4500.65 | -751.98 | 67 | C2P | 800.10 | -771.93 | 122 | ROW13 | 5285.18 | -310.98 |
| 8 | ROW60 | -4424.35 | -751.98 | 68 | VSS | 889.00 | -771.93 | 123 | ROW12 | 5285.18 | -234.68 |
| 9 | ROW61 | -4348.05 | -751.98 | 69 | VSS | 977.90 | -771.93 | 124 | ROW11 | 5285.18 | -158.38 |
| 10 | ROW62 | -4271.75 | -751.98 | 70 | VFS | 1066.80 | -771.93 | 125 | ROW10 | 5285.18 | -82.08 |
| 11 | ROW63 | -4195.45 | -751.98 | 71 | VFS | 1155.70 | -771.93 | 126 | ROW9 | 5285.18 | -5.78 |
| 12 | ICONS | -4119.15 | -751.98 | 72 | VDD | 1244.60 | -771.93 | 127 | ROW8 | 5285.18 | 70.53 |
| 13 | NC | -4000.50 | -771.93 | 73 | VDD | 1333.50 | -771.93 | 128 | ROW7 | 5285.18 | 146.83 |
| 14 | MSTAT | -3911.60 | -771.93 | 74 | VL2 | 1422.40 | -771.93 | 129 | ROW6 | 5285.18 | 223.13 |
| 15 | M | -3822.70 | -771.93 | 75 | VL2 | 1511.30 | -771.93 | 130 | ROW5 | 5285.18 | 299.43 |
| 16 | CL | -3733.80 | -771.93 | 76 | VL3 | 1600.20 | -771.93 | 131 | ROW4 | 5285.18 | 375.73 |
| 17 | /DOF | -3644.90 | -771.93 | 77 | VL3 | 1689.10 | -771.93 | 132 | ROW3 | 5285.18 | 452.03 |
| 18 | VSS | -3556.00 | -771.93 | 78 | VL3 | 1778.00 | -771.93 | 133 | ROW2 | 5285.18 | 528.33 |
| 19 | /CS1 | -3467.10 | -771.93 | 79 | VL4 | 1866.90 | -771.93 | 134 | ROW1 | 5285.18 | 604.63 |
| 20 | CS2 | -3378.20 | -771.93 | 80 | VL4 | 1955.80 | -771.93 | 135 | ROW0 | 5285.18 | 680.93 |
| 21 | VDD | -3289.30 | -771.93 | 81 | VL4 | 2044.70 | -771.93 | 136 | ICONS | 5285.18 | 757.23 |
| 22 | /RES | -3200.40 | -771.93 | 82 | VL5 | 2133.60 | -771.93 | | | | |
| 23 | D/C | -3111.50 | -771.93 | 83 | VL5 | 2222.50 | -771.93 | | | | |
| 24 | VSS | -3022.60 | -771.93 | 84 | VL6 | 2311.40 | -771.93 | | | | |
| 25 | R/W | -2933.70 | -771.93 | 85 | VL6 | 2400.30 | -771.93 | | | | |
| 26 | E/RD | -2844.80 | -771.93 | 86 | VL6 | 2489.20 | -771.93 | | | | |
| 27 | VDD | -2755.90 | -771.93 | 87 | VF | 2578.10 | -771.93 | | | | |
| 28 | D 0 | -2667.00 | -771.93 | 88 | VF | 2667.00 | -771.93 | | | | |
| 29 | D 1 | -2578.10 | -771.93 | 89 | VDD | 2755.90 | -771.93 | | | | |
| 30 | D 2 | -2489.20 | -771.93 | 90 | VDD | 2844.80 | -771.93 | | | | |
| 31 | D 3 | -2400.30 | -771.93 | 91 | NC | 2933.70 | -771.93 | | | | |
| 32 | D 4 | -2311.40 | -771.93 | 92 | NC | 3022.60 | -771.93 | | | | |
| 33 | D 5 | -2222.50 | -771.93 | 93 | VDD | 3111.50 | -771.93 | | | | |
| 34 | D 6 | -2133.60 | -771.93 | 94 | M/S | 3200.40 | -771.93 | | | | |
| 35 | D 7 | -2044.70 | -771.93 | 95 | CLS | 3289.30 | -771.93 | | | | |
| 36 | VDD | -1955.80 | -771.93 | 96 | VSS | 3378.20 | -771.93 | | | | |
| 37 | VDD | -1866.90 | -771.93 | 97 | C68/80 | 3467.10 | -771.93 | | | | |
| 38 | VDD | -1778.00 | -771.93 | 98 | P/S | 3556.00 | -771.93 | | | | |
| 39 | VDD | -1689.10 | -771.93 | 99 | VDD | 3644.90 | -771.93 | | | | |
| 40 | VSS | -1600.20 | -771.93 | 100 | /HPM | 3733.80 | -771.93 | | | | |
| 41 | VSS | -1511.30 | -771.93 | 101 | VSS | 3822.70 | -771.93 | | | | |
| 42 | VSS | -1422.40 | -771.93 | 102 | IRS | 3911.60 | -771.93 | | | | |
| 43 | VSS1 | -1333.50 | -771.93 | 103 | VDD | 4000.50 | -771.93 | | | | |
| 44 | VSS1 | -1244.60 | -771.93 | 104 | ROW31 | 4119.15 | -751.98 | | | | |
| 45 | VSS1 | -1155.70 | -771.93 | 105 | ROW30 | 4195.45 | -751.98 | | | | |
| 46 | VSS1 | -1066.80 | -771.93 | 106 | ROW29 | 4271.75 | -751.98 | | | | |
| 47 | VEE | -977.90 | -771.93 | 107 | ROW28 | 4348.05 | -751.98 | | | | |
| 48 | VEE | -889.00 | -771.93 | 108 | ROW27 | 4424.35 | -751.98 | | | | |
| 49 | VEE | -800.10 | -771.93 | 109 | ROW26 | 4500.65 | -751.98 | | | | |
| 50 | VEE | -711.20 | -771.93 | 110 | ROW25 | 4576.95 | -751.98 | | | | |
| 51 | C3N | -622.30 | -771.93 | 111 | ROW24 | 4653.25 | -751.98 | | | | |
| 52 | C3N | -533.40 | -771.93 | 112 | ROW23 | 4729.55 | -751.98 | | | | |
| 53 | C3N | -444.50 | -771.93 | 113 | ROW22 | 4805.85 | -751.98 | | | | |
| 54 | C3N | -355.60 | -771.93 | 114 | ROW21 | 4882.15 | -751.98 | | | | |
| 55 | C1P | -266.70 | -771.93 | 115 | ROW20 | 4958.45 | -751.98 | | | | |
| 56 | C1P | -177.80 | -771.93 | | | | | | | | |
| 57 | C1P | -88.90 | -771.93 | | | | | | | | |
| 58 | C1N | 0.00 | -771.93 | | | | | | | | |
| 59 | C1N | 88.90 | -771.93 | | | | | | | | |
| 60 | C1N | 177.80 | -771.93 | | | | | | | | |



Die Size: 10.977mm X 1.912mm
 Bump Height:
 - nominal: 18um
 - tolerance:<4um (within die)
 <6um (within wafer)
 <8um (within lot)
 Unit in um unless otherwise specified.

Die Size: 10.977mm X 1.912mm
 Bump Size:

| Pad # | X [um] | Y [um] | Pad # | X [um] | Y [um] | Pad # | X [um] | Y [um] | Pad # | X [um] | Y [um] |
|-----------|--------|--------|-------------------------------------|--------|--------|-----------|--------|--------|-----------|--------|--------|
| 1 - 12 | 43.5 | 101.6 | 116 - 136 | 101.6 | 43.5 | 137 - 268 | 43.5 | 101.6 | 269 - 289 | 101.6 | 43.5 |
| 13 - 103 | 61.7 | 61.7 | Gold bump size tolerance: +/-1.5um. | | | | | | | | |
| 104 - 115 | 43.5 | 101.6 | | | | | | | | | |

| PAD # | NAME | X | Y | PAD # | NAME | X | Y | PAD # | NAME | X | Y |
|-------|-------|---------|--------|-------|--------|----------|--------|-------|-------|----------|---------|
| 137 | SEG0 | 4997.65 | 751.98 | 203 | SEG66 | -38.15 | 751.98 | 269 | ROW32 | -5285.18 | 757.23 |
| 138 | SEG1 | 4921.35 | 751.98 | 204 | SEG67 | -114.45 | 751.98 | 270 | ROW33 | -5285.18 | 680.93 |
| 139 | SEG2 | 4845.05 | 751.98 | 205 | SEG68 | -190.75 | 751.98 | 271 | ROW34 | -5285.18 | 604.63 |
| 140 | SEG3 | 4768.75 | 751.98 | 206 | SEG69 | -267.05 | 751.98 | 272 | ROW35 | -5285.18 | 528.33 |
| 141 | SEG4 | 4692.45 | 751.98 | 207 | SEG70 | -343.35 | 751.98 | 273 | ROW36 | -5285.18 | 452.03 |
| 142 | SEG5 | 4616.15 | 751.98 | 208 | SEG71 | -419.65 | 751.98 | 274 | ROW37 | -5285.18 | 375.73 |
| 143 | SEG6 | 4539.85 | 751.98 | 209 | SEG72 | -495.95 | 751.98 | 275 | ROW38 | -5285.18 | 299.43 |
| 144 | SEG7 | 4463.55 | 751.98 | 210 | SEG73 | -572.25 | 751.98 | 276 | ROW39 | -5285.18 | 223.13 |
| 145 | SEG8 | 4387.25 | 751.98 | 211 | SEG74 | -648.55 | 751.98 | 277 | ROW40 | -5285.18 | 146.83 |
| 146 | SEG9 | 4310.95 | 751.98 | 212 | SEG75 | -724.85 | 751.98 | 278 | ROW41 | -5285.18 | 70.53 |
| 147 | SEG10 | 4234.65 | 751.98 | 213 | SEG76 | -801.15 | 751.98 | 279 | ROW42 | -5285.18 | -5.78 |
| 148 | SEG11 | 4158.35 | 751.98 | 214 | SEG77 | -877.45 | 751.98 | 280 | ROW43 | -5285.18 | -82.08 |
| 149 | SEG12 | 4082.05 | 751.98 | 215 | SEG78 | -953.75 | 751.98 | 281 | ROW44 | -5285.18 | -158.38 |
| 150 | SEG13 | 4005.75 | 751.98 | 216 | SEG79 | -1030.05 | 751.98 | 282 | ROW45 | -5285.18 | -234.68 |
| 151 | SEG14 | 3929.45 | 751.98 | 217 | SEG80 | -1106.35 | 751.98 | 283 | ROW46 | -5285.18 | -310.98 |
| 152 | SEG15 | 3853.15 | 751.98 | 218 | SEG81 | -1182.65 | 751.98 | 284 | ROW47 | -5285.18 | -387.28 |
| 153 | SEG16 | 3776.85 | 751.98 | 219 | SEG82 | -1258.95 | 751.98 | 285 | ROW48 | -5285.18 | -463.58 |
| 154 | SEG17 | 3700.55 | 751.98 | 220 | SEG83 | -1335.25 | 751.98 | 286 | ROW49 | -5285.18 | -539.88 |
| 155 | SEG18 | 3624.25 | 751.98 | 221 | SEG84 | -1411.55 | 751.98 | 287 | ROW50 | -5285.18 | -616.18 |
| 156 | SEG19 | 3547.95 | 751.98 | 222 | SEG85 | -1487.85 | 751.98 | 288 | ROW51 | -5285.18 | -692.48 |
| 157 | SEG20 | 3471.65 | 751.98 | 223 | SEG86 | -1564.15 | 751.98 | 289 | ROW52 | -5285.18 | -768.78 |
| 158 | SEG21 | 3395.35 | 751.98 | 224 | SEG87 | -1640.45 | 751.98 | | | | |
| 159 | SEG22 | 3319.05 | 751.98 | 225 | SEG88 | -1716.75 | 751.98 | | | | |
| 160 | SEG23 | 3242.75 | 751.98 | 226 | SEG89 | -1793.05 | 751.98 | | | | |
| 161 | SEG24 | 3166.45 | 751.98 | 227 | SEG90 | -1869.35 | 751.98 | | | | |
| 162 | SEG25 | 3090.15 | 751.98 | 228 | SEG91 | -1945.65 | 751.98 | | | | |
| 163 | SEG26 | 3013.85 | 751.98 | 229 | SEG92 | -2021.95 | 751.98 | | | | |
| 164 | SEG27 | 2937.55 | 751.98 | 230 | SEG93 | -2098.25 | 751.98 | | | | |
| 165 | SEG28 | 2861.25 | 751.98 | 231 | SEG94 | -2174.55 | 751.98 | | | | |
| 166 | SEG29 | 2784.95 | 751.98 | 232 | SEG95 | -2250.85 | 751.98 | | | | |
| 167 | SEG30 | 2708.65 | 751.98 | 233 | SEG96 | -2327.15 | 751.98 | | | | |
| 168 | SEG31 | 2632.35 | 751.98 | 234 | SEG97 | -2403.45 | 751.98 | | | | |
| 169 | SEG32 | 2556.05 | 751.98 | 235 | SEG98 | -2479.75 | 751.98 | | | | |
| 170 | SEG33 | 2479.75 | 751.98 | 236 | SEG99 | -2556.05 | 751.98 | | | | |
| 171 | SEG34 | 2403.45 | 751.98 | 237 | SEG100 | -2632.35 | 751.98 | | | | |
| 172 | SEG35 | 2327.15 | 751.98 | 238 | SEG101 | -2708.65 | 751.98 | | | | |
| 173 | SEG36 | 2250.85 | 751.98 | 239 | SEG102 | -2784.95 | 751.98 | | | | |
| 174 | SEG37 | 2174.55 | 751.98 | 240 | SEG103 | -2861.25 | 751.98 | | | | |
| 175 | SEG38 | 2098.25 | 751.98 | 241 | SEG104 | -2937.55 | 751.98 | | | | |
| 176 | SEG39 | 2021.95 | 751.98 | 242 | SEG105 | -3013.85 | 751.98 | | | | |
| 177 | SEG40 | 1945.65 | 751.98 | 243 | SEG106 | -3090.15 | 751.98 | | | | |
| 178 | SEG41 | 1869.35 | 751.98 | 244 | SEG107 | -3166.45 | 751.98 | | | | |
| 179 | SEG42 | 1793.05 | 751.98 | 245 | SEG108 | -3242.75 | 751.98 | | | | |
| 180 | SEG43 | 1716.75 | 751.98 | 246 | SEG109 | -3319.05 | 751.98 | | | | |
| 181 | SEG44 | 1640.45 | 751.98 | 247 | SEG110 | -3395.35 | 751.98 | | | | |
| 182 | SEG45 | 1564.15 | 751.98 | 248 | SEG111 | -3471.65 | 751.98 | | | | |
| 183 | SEG46 | 1487.85 | 751.98 | 249 | SEG112 | -3547.95 | 751.98 | | | | |
| 184 | SEG47 | 1411.55 | 751.98 | 250 | SEG113 | -3624.25 | 751.98 | | | | |
| 185 | SEG48 | 1335.25 | 751.98 | 251 | SEG114 | -3700.55 | 751.98 | | | | |
| 186 | SEG49 | 1258.95 | 751.98 | 252 | SEG115 | -3776.85 | 751.98 | | | | |
| 187 | SEG50 | 1182.65 | 751.98 | 253 | SEG116 | -3853.15 | 751.98 | | | | |
| 188 | SEG51 | 1106.35 | 751.98 | 254 | SEG117 | -3929.45 | 751.98 | | | | |
| 189 | SEG52 | 1030.05 | 751.98 | 255 | SEG118 | -4005.75 | 751.98 | | | | |
| 190 | SEG53 | 953.75 | 751.98 | 256 | SEG119 | -4082.05 | 751.98 | | | | |
| 191 | SEG54 | 877.45 | 751.98 | 257 | SEG120 | -4158.35 | 751.98 | | | | |
| 192 | SEG55 | 801.15 | 751.98 | 258 | SEG121 | -4234.65 | 751.98 | | | | |
| 193 | SEG56 | 724.85 | 751.98 | 259 | SEG122 | -4310.95 | 751.98 | | | | |
| 194 | SEG57 | 648.55 | 751.98 | 260 | SEG123 | -4387.25 | 751.98 | | | | |
| 195 | SEG58 | 572.25 | 751.98 | 261 | SEG124 | -4463.55 | 751.98 | | | | |
| 196 | SEG59 | 495.95 | 751.98 | 262 | SEG125 | -4539.85 | 751.98 | | | | |
| 197 | SEG60 | 419.65 | 751.98 | 263 | SEG126 | -4616.15 | 751.98 | | | | |
| 198 | SEG61 | 343.35 | 751.98 | 264 | SEG127 | -4692.45 | 751.98 | | | | |
| 199 | SEG62 | 267.05 | 751.98 | 265 | SEG128 | -4768.75 | 751.98 | | | | |
| 200 | SEG63 | 190.75 | 751.98 | 266 | SEG129 | -4845.05 | 751.98 | | | | |
| 201 | SEG64 | 114.45 | 751.98 | 267 | SEG130 | -4921.35 | 751.98 | | | | |
| 202 | SEG65 | 38.15 | 751.98 | 268 | SEG131 | -4997.65 | 751.98 | | | | |

PIN DESCRIPTIONS

MSTAT

This pin is the static indicator driving output. It is only active in master operation. The frame signal output pin, M, should be used as the back plane signal for the static indicator.

The duration of overlapping could be programmable. See Extended Command Table for details.

This pin becomes high impedance if the chip is operating in slave mode.

M

This pin is the frame signal input/output. In master mode, the pin supplies frame signal to slave devices while in slave mode, the pin receives frame signal from the master device.

CL

This pin is the display clock input/output. In master mode, the pin supplies display clock signal to slave devices while in slave mode, the pin receives display clock signal from the master device.

DOF

This pin is display blanking control between master and slave devices. In master mode, this pin supplies on/off signal to slave devices. In slave mode, this pin receives on/off signal from the master device.

CS1, CS2

These pins are the chip select inputs. The chip is enabled for MCP communication only when both CS1 is pulled low and CS2 is pulled high.

RES

This pin is reset signal input. Initialization of the chip is started once this pin is pulled low. Minimum pulse width for completing the reset is 1us.

D/C

This pin is Data/Command control pin. When the pin is pulled high, the data at D₇-D₀ is treated as display data. When the pin is pulled low, the data at D₇-D₀ will be transferred to the command register.

R/W(WR)

This pin is microprocessor interface input. When interfacing to an 6800-series microprocessor, this pin will be used as R/W signal input. Read mode will be carried out when this pin is pulled high and write mode when low.

When interfacing to an 8080-microprocessor, this pin will be the WR input. Data write operation is initiated when this pin is pulled low when the chip is selected.

E(RD)

This pin is microprocessor interface input. When interfacing to an 6800-series microprocessor, this pin will be used as the enable signal, E. Read/write operation is initiated when this pin is pulled high when the chip is selected.

When interfacing to an 8080-microprocessor, this pin receives the RD signal. Data read operation is initiated when this pin is pulled low when the chip is selected.

D₇-D₀

These pins are the 8-bit bi-directional data bus to be connected to the microprocessor in parallel interface mode. D₇ is the MSB while D₀ is the LSB.

When serial mode is selected, D₇ is the serial data input (SDA) and D₆ is the serial clock input (SCK).

V_{DD}

Power supply pin.

V_{SS}

Ground.

V_{SS1}

Reference voltage input for internal DC-DC converter. The voltage of generated, V_{EE}, equals to the multiple factor times the potential different between this pin, V_{SS1}, and V_{DD}. The multiple factor, 2X, 3X or 4X, is selected by different external capacitor connections. All voltage levels are referenced to V_{DD}.

Note: the potential at this input pin must lower than or equal to V_{SS}.

V_{EE}

This is the most negative voltage supply pin of the chip. It can be supplied externally or generated by the internal DC-DC converter.

When using internal DC-DC converter as generator, voltage at this pin is for internal reference only. It CANNOT be used for driving external circuitries.

C_{3N}, C_{1P}, C_{1N}, C_{2N} and C_{2P}

When internal DC-DC voltage converter is used, external capacitor(s) is/are connected between these pins. Different connection will result in different DC-DC converter multiple factor, 2X, 3X or 4X. Details please refer to voltage converter section in the block diagram description.

V_{FS}

This is an input pin to provide an external voltage reference for the internal voltage regulator. The function of this pin is only enabled for the External Input chip models which are required special ordering. For normal chip model, please leave this pin NC.

V_{L2}, V_{L3}, V_{L4} and V_{L5} (Voltages referenced to V_{DD})

LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:

$$V_{DD} > V_{L2} > V_{L3} > V_{L4} > V_{L5} > V_{L6}$$

| | 1:7 bias | 1:9 bias (default) |
|-----------------|---------------------|---------------------|
| V _{L2} | 1/7*V _{L6} | 1/9*V _{L6} |
| V _{L3} | 2/7*V _{L6} | 2/9*V _{L6} |
| V _{L4} | 5/7*V _{L6} | 7/9*V _{L6} |
| V _{L5} | 6/7*V _{L6} | 8/9*V _{L6} |

V_{L6}

This pin is the most negative LCD driving voltage. It can be supplied externally or generated by the internal regulator.

V_F

This pin is the input of the built-in voltage regulator. When external resistor network is selected to generate the LCD driving level, V_{L6} , two external resistors, R_1 and R_2 , are connected between V_{DD} and V_F , and V_F and V_{L6} , respectively (see application circuit).

M/ \overline{S}

This pin is the master/slave mode selection input. When this pin is pulled high, master mode is selected, which CL, M, MSTAT and DOF signals will be output for slave devices. When this pin is pulled low, slave mode is selected, which CL, M, DOF are required to be input from master device and MSTAT is high impedance.

CLS

This pin is the internal clock enable pin. When this pin is pulled high, internal clock is enabled. The internal clock will be disabled when it is pulled low, an external clock source should be input to CL pin.

C68/ $\overline{80}$

This pin is microprocessor interface selection input. When the pin is pulled high, 6800 series interface is selected and when the pin is pulled low, 8080 series MCU interface is selected.

P/ \overline{S}

This pin is serial/parallel interface selection input. When this pin is pulled high, parallel mode is selected. When it is pulled low, serial interface will be selected. Read back operation is only available in parallel mode.

 \overline{HPM}

This pin is the control input of High Power Current Mode. The function of this pin is only enabled for High Power model which required special ordering.

For normal models, High Power Mode is disabled and the LCD driving characteristics are the same no matter this pin is pulled High or Low.

Note: This pin must be pulled to either High or Low. Leaving this pin floating is prohibited.

IRS

This is the input pin to enable the internal resistors network for the voltage regulator. When this pin is pulled high the internal resistors will be enabled, and when it is low, the external resistors, R_1 and R_2 , should be connected to V_{DD} and V_F , and V_F and V_{L6} , respectively (see application circuits).

ROW0 - ROW63

These pins provide the row driving signal COM0 - COM63 to the LCD panel. See Table.1 about the COM signal mapping in different multiplex ratio N.

SEG0 - SEG131

These pins provide the LCD column driving signals. Their output voltage level is V_{DD} during sleep mode and standby mode.

ICONS

There are two ICONS pins (pin12 and 136) on the chip. Both pins output exactly the same signal. The reason for duplicating the pin is to enhance the flexibility of the LCD layout.

NC

These are the No Connection pins. Nothing should be connected to these pins, nor they are connected together. These pins should be left open individually.

Table 2 - ROW pins assignment for COM signals in different Programmable Multiplex Ratio
 [After power-on-reset, SSD1815 is set to 64 Multiplex]

| Die Pad Name | 64 Mux Com Signal Output | 54 Mux Com Signal Output | 53 Mux Com Signal Output | 52 Mux Com Signal Output | 49 Mux Com Signal Output | 48 Mux Com Signal Output | 34 Mux Com Signal Output | 33 Mux Com Signal Output | 32 Mux Com Signal Output |
|--------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| ROW0 | COM0 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW1 | COM1 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW2 | COM2 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW3 | COM3 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW4 | COM4 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW5 | COM5 | COM0 | COM0 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW6 | COM6 | COM1 | COM1 | COM0 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW7 | COM7 | COM2 | COM2 | COM1 | COM0 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW8 | COM8 | COM3 | COM3 | COM2 | COM1 | COM0 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW9 | COM9 | COM4 | COM4 | COM3 | COM2 | COM1 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW10 | COM10 | COM5 | COM5 | COM4 | COM3 | COM2 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW11 | COM11 | COM6 | COM6 | COM5 | COM4 | COM3 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW12 | COM12 | COM7 | COM7 | COM6 | COM5 | COM4 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW13 | COM13 | COM8 | COM8 | COM7 | COM6 | COM5 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW14 | COM14 | COM9 | COM9 | COM8 | COM7 | COM6 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW15 | COM15 | COM10 | COM10 | COM9 | COM8 | COM7 | COM0 | COM0 | NON-SELECT* |
| ROW16 | COM16 | COM11 | COM11 | COM10 | COM9 | COM8 | COM1 | COM1 | COM0 |
| ROW17 | COM17 | COM12 | COM12 | COM11 | COM10 | COM9 | COM2 | COM2 | COM1 |
| ROW18 | COM18 | COM13 | COM13 | COM12 | COM11 | COM10 | COM3 | COM3 | COM2 |
| ROW19 | COM19 | COM14 | COM14 | COM13 | COM12 | COM11 | COM4 | COM4 | COM3 |
| ROW20 | COM20 | COM15 | COM15 | COM14 | COM13 | COM12 | COM5 | COM5 | COM4 |
| ROW21 | COM21 | COM16 | COM16 | COM15 | COM14 | COM13 | COM6 | COM6 | COM5 |
| ROW22 | COM22 | COM17 | COM17 | COM16 | COM15 | COM14 | COM7 | COM7 | COM6 |
| ROW23 | COM23 | COM18 | COM18 | COM17 | COM16 | COM15 | COM8 | COM8 | COM7 |
| ROW24 | COM24 | COM19 | COM19 | COM18 | COM17 | COM16 | COM9 | COM9 | COM8 |
| ROW25 | COM25 | COM20 | COM20 | COM19 | COM18 | COM17 | COM10 | COM10 | COM9 |
| ROW26 | COM26 | COM21 | COM21 | COM20 | COM19 | COM18 | COM11 | COM11 | COM10 |
| ROW27 | COM27 | COM22 | COM22 | COM21 | COM20 | COM19 | COM12 | COM12 | COM11 |
| ROW28 | COM28 | COM23 | COM23 | COM22 | COM21 | COM20 | COM13 | COM13 | COM12 |
| ROW29 | COM29 | COM24 | COM24 | COM23 | COM22 | COM21 | COM14 | COM14 | COM13 |
| ROW30 | COM30 | COM25 | COM25 | COM24 | COM23 | COM22 | COM15 | COM15 | COM14 |
| ROW31 | COM31 | COM26 | COM26 | COM25 | COM24 | COM23 | COM16 | COM16 | COM15 |
| ROW32 | COM32 | COM27 | COM27 | COM26 | COM25 | COM24 | COM17 | COM17 | COM16 |
| ROW33 | COM33 | COM28 | COM28 | COM27 | COM26 | COM25 | COM18 | COM18 | COM17 |
| ROW34 | COM34 | COM29 | COM29 | COM28 | COM27 | COM26 | COM19 | COM19 | COM18 |
| ROW35 | COM35 | COM30 | COM30 | COM29 | COM28 | COM27 | COM20 | COM20 | COM19 |
| ROW36 | COM36 | COM31 | COM31 | COM30 | COM29 | COM28 | COM21 | COM21 | COM20 |
| ROW37 | COM37 | COM32 | COM32 | COM31 | COM30 | COM29 | COM22 | COM22 | COM21 |
| ROW38 | COM38 | COM33 | COM33 | COM32 | COM31 | COM30 | COM23 | COM23 | COM22 |
| ROW39 | COM39 | COM34 | COM34 | COM33 | COM32 | COM31 | COM24 | COM24 | COM23 |
| ROW40 | COM40 | COM35 | COM35 | COM34 | COM33 | COM32 | COM25 | COM25 | COM24 |
| ROW41 | COM41 | COM36 | COM36 | COM35 | COM34 | COM33 | COM26 | COM26 | COM25 |
| ROW42 | COM42 | COM37 | COM37 | COM36 | COM35 | COM34 | COM27 | COM27 | COM26 |
| ROW43 | COM43 | COM38 | COM38 | COM37 | COM36 | COM35 | COM28 | COM28 | COM27 |
| ROW44 | COM44 | COM39 | COM39 | COM38 | COM37 | COM36 | COM29 | COM29 | COM28 |
| ROW45 | COM45 | COM40 | COM40 | COM39 | COM38 | COM37 | COM30 | COM30 | COM29 |
| ROW46 | COM46 | COM41 | COM41 | COM40 | COM39 | COM38 | COM31 | COM31 | COM30 |
| ROW47 | COM47 | COM42 | COM42 | COM41 | COM40 | COM39 | COM32 | COM32 | COM31 |
| ROW48 | COM48 | COM43 | COM43 | COM42 | COM41 | COM40 | COM33 | NON-SELECT* | NON-SELECT* |
| ROW49 | COM49 | COM44 | COM44 | COM43 | COM42 | COM41 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW50 | COM50 | COM45 | COM45 | COM44 | COM43 | COM42 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW51 | COM51 | COM46 | COM46 | COM45 | COM44 | COM43 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW52 | COM52 | COM47 | COM47 | COM46 | COM45 | COM44 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW53 | COM53 | COM48 | COM48 | COM47 | COM46 | COM45 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW54 | COM54 | COM49 | COM49 | COM48 | COM47 | COM46 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW55 | COM55 | COM50 | COM50 | COM49 | COM48 | COM47 | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW56 | COM56 | COM51 | COM51 | COM50 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW57 | COM57 | COM52 | COM52 | COM51 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW58 | COM58 | COM53 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW59 | COM59 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW60 | COM60 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW61 | COM61 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW62 | COM62 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |
| ROW63 | COM63 | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* | NON-SELECT* |

Remark:

* The ROW will output a Non-Select COM signal.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/C pin. If D/C is high, data is written to Graphic Display Data RAM (GDDRAM). If D/C is low, the input at D₇-D₀ is interpreted as a Command and it will be decoded and be written to the corresponding command register.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D₇-D₀), R/W(WR), D/C, E(RD), CS1 and CS2. R/W(WR) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W(WR) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The E(RD) input serves as data latch signal (clock) when high provided that CS1 and CS2 are low and high respectively. Refer to Figure 9 for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3 below.

MPU Parallel 8080-series interface

The parallel interface consists of 8 bi-directional data pins (D₇-D₀), E(RD), R/W(WR), D/C, CS1 and CS2. E(RD) input serves as data read latch signal (clock) when low provided that CS1 and CS2 are low and high respectively. Whether it is display data or status register read is controlled by D/C. R/W(WR) input serves as data write latch signal(clock) when high provided that CS1 and CS2 are low and high respectively. Whether it is display data or command register write is controlled by D/C. Refer to Figure 10 for Parallel Interface Timing Diagram of 8080-series microprocessor.

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial interface

The serial interface consists of serial clock SCK (D₆), serial data SDA (D₇), D/C, CS1 and CS2. SDA is shifted into a 8-bit shift register on every rising edge of SCL in the order of D₇, D₆,... D₀. D/C is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock.

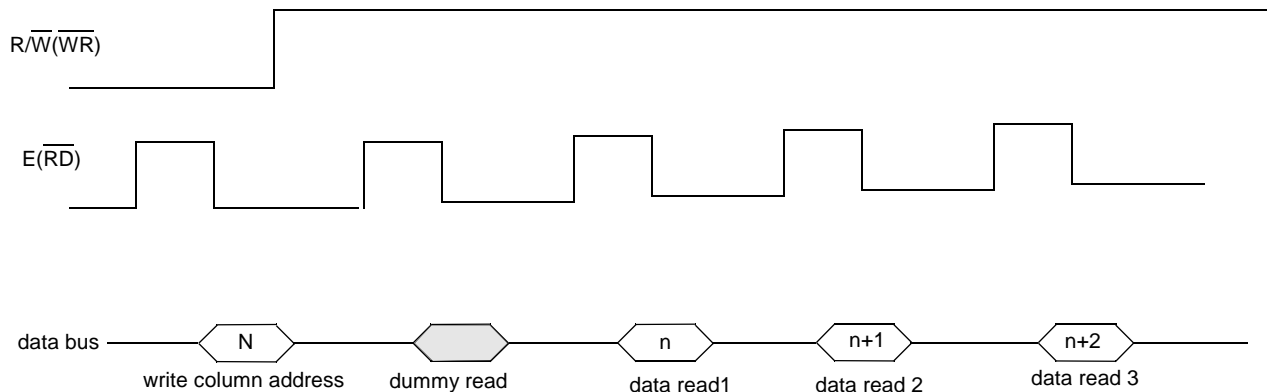


Figure 3 - Display data read with the insertion of dummy read

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 4). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

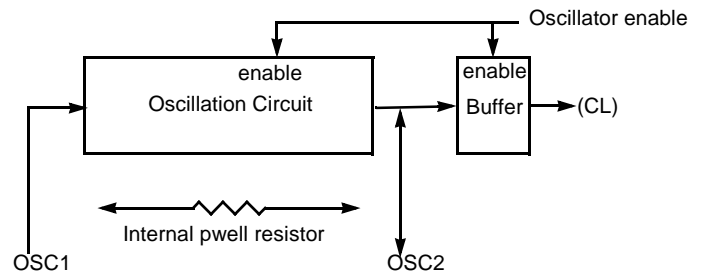
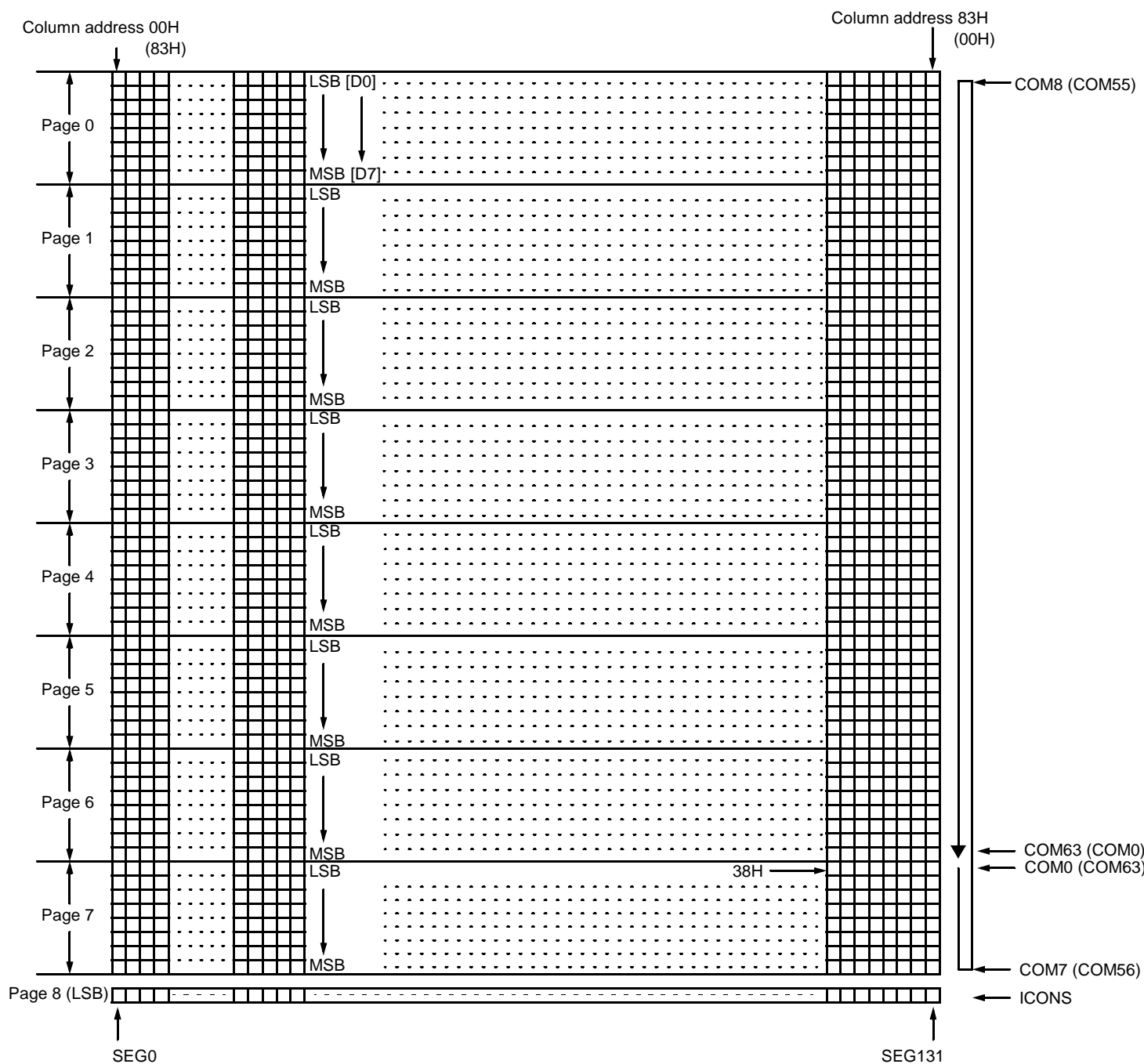


Figure 4 - Oscillator Circuitry

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 X 65= 8580 bits. Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs can be

selected by software. For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display. Figure 5 shows the case in which the display start line register is set to 38h.



Note: The configuration in parentheses represent the remapped values of Rows and Columns

**Figure 5. Graphic Display Data RAM (GDDRAM) Address Map (with display start line at 38H)
For 132 X 64 Graphic Display Mode with separated Icon Line**

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage required for display driving output. It takes a single supply input and generate necessary voltage levels. This block consists of:

1. 2X, 3X and 4X DC-DC voltage converter

The built-in DC-DC voltage converter is use to generate large negative LCD driving voltage with reference to V_{DD} from the voltage input (V_{SS1}). For SSD1815, it is possible to produce 2X, 3X or 4X boosting from the potential different between $V_{SS1} - V_{DD}$.

Detail configurations of the DC-DC converter for different boosting multiples are given in Figure 6 at the right.

2. Voltage Regulator (Voltages referenced to V_{DD})

The feedback gain control for LCD driving contrast curves can be selected by IRS pin to either internal (IRS pin = H) or external (IRS pin = L).

For internal resistor network is enabled, there are eight setting can be set by software.

If external control is selected, external resistors are required to be connected between V_{DD} and V_F (R1), and between V_F and V_{L6} (R2).

3. Contrast Control (Voltages referenced to V_{DD})

Software control of the 64 contrast voltage levels at each voltage regulator feedback gain. The equation of calculating the LCD driving voltage is given as:

$$V_{L6} - V_{DD} = Gain * (1 + \frac{Contrast}{b}) * V_{ref}$$

$$V_{ref} = (\frac{V_{BE} + R * (V_{DD} - V_{SS})}{1 + R})$$

where

| Int. Reg. Resistor Ratio Setting | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | Ext. Resistor |
|----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|--------------------------------------|
| Gain | -3.29 | -3.76 | -4.29 | -4.82 | -5.39 | -5.76 | -6.40 | -6.95 | -(1+R ₂ /R ₁) |
| β | 92.59 | 91.86 | 91.12 | 90.40 | 89.67 | 89.18 | 88.29 | 87.49 | 96.68 |

and

| TC | 0 (-0.01%/°C) | 2 (-0.10%/°C) | 4 (-0.18%/°C) | 7 (-0.25%/°C) |
|----------|------------------|------------------|------------------|------------------|
| V_{BE} | 0.025 | 0.523 | 0.520 | 0.517 |
| R | 0.72 | 0.423 | 0.272 | 0.121 |

4. Bias Divider

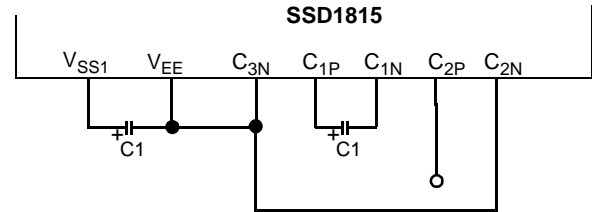
Divide the regulator output to give the LCD driving voltages ($V_{L2} - V_{L5}$). A low power consumption circuit design in this bias divider saves most of the display current comparing to traditional design.

5. Bias Ratio Selection circuitry

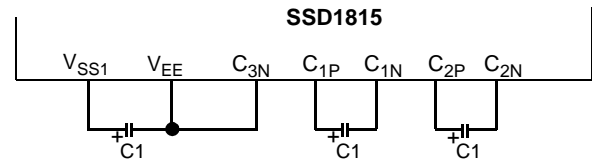
Software control of 1/7 and 1/9 bias ratio to match the characteristic of LCD panel. In addition, 1/4, 1/5, 1/6 and 1/8 bias ratios are also software selectable using the extended command for any mux application.

6. Self adjust temperature compensation circuitry

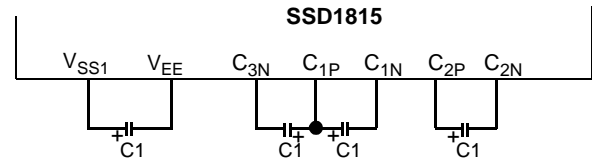
This block provides 4 different compensation settings to satisfy various liquid crystal temperature gradings by software control. Default temperature coefficient (TC) setting is TC0.



2X Boosting Configuration



3X Boosting Configuration



4X Boosting Configuration

Remarks:

1. $C1 = 0.47 - 1.0\mu F$
2. Boosting input from V_{SS1} .
3. V_{SS1} should be lower potential than or equal to V_{SS}
4. All voltages are referenced to V_{DD}

Figure 6 - Configurations for DC-DC Converter

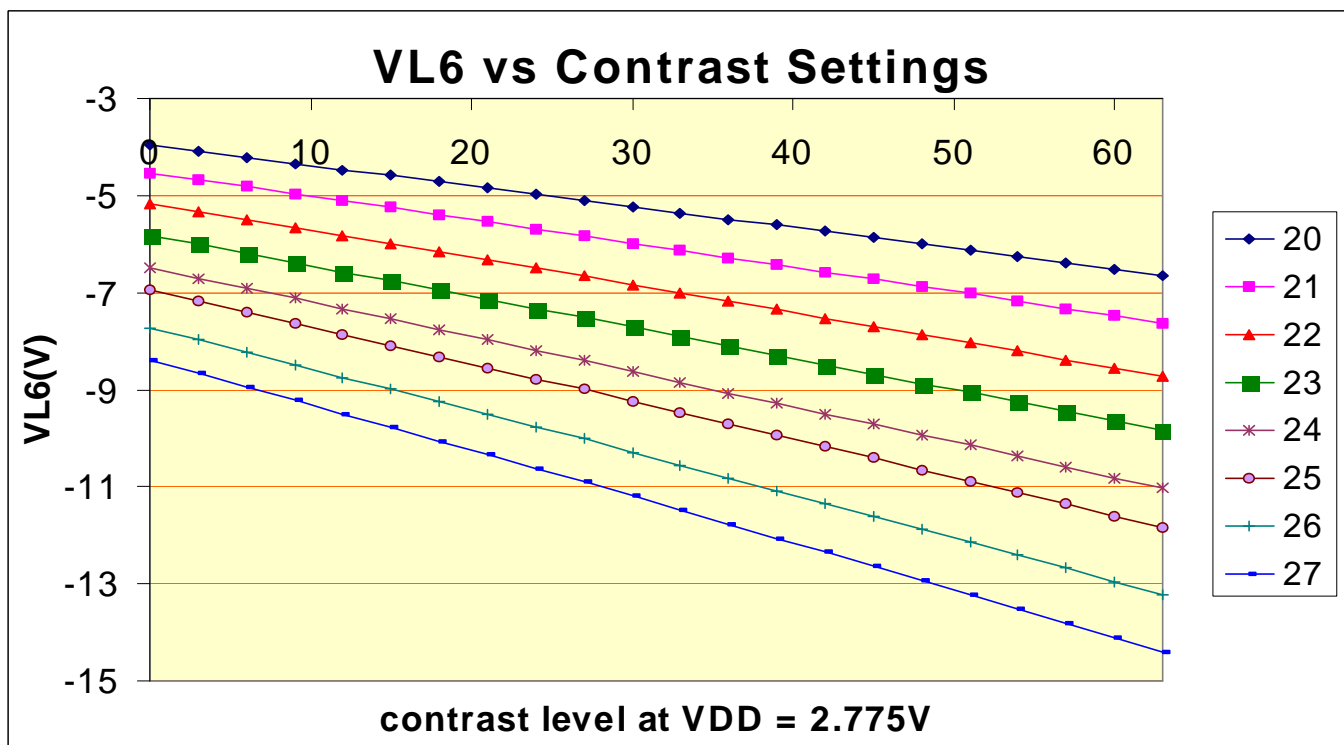


Figure 7 - Contrast Curves at Different Internal Feedback Resistor Ratio Settings

Reset Circuit

This block includes Power On Reset circuitry and the Reset pin, RES. Both of these having the same reset function. Once RES receives a negative reset pulse, all internal circuitry will start to initialize. Minimum pulse width for completing the reset sequence is 1 μ s. The status of the chip after reset is given by:

1. Display is turned OFF
2. 132X64 Display Display Mode with separated Icon Line
3. Normal segment and display data column address mapping (SEG0 mapped to address 00h)
4. Read-modify-write mode is OFF
5. Power control register is set to 000b
6. Shift register data clear in serial interface
7. Bias ratio is set to 1/9
8. Static indicator is turned OFF
9. Display start line is set to display RAM column address 0
10. Column address counter is set to 0
11. Page address is set to 0
12. Normal scan direction of the COM outputs
13. Contrast control register is set to 20h
14. Test mode is turned OFF

Display Data Latch

A series of registers carrying the display signal information. For SSD1815, there are 197 latches (132 + 65) for holding the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

Level Selector

Level Selector is a control of the display synchronization. Display

voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

HV Buffer Cell (Level Shifter)

HV Buffer Cell work as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

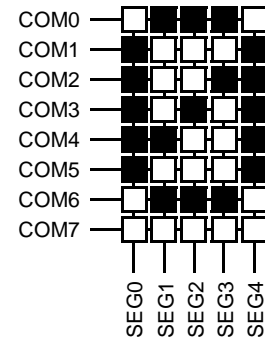
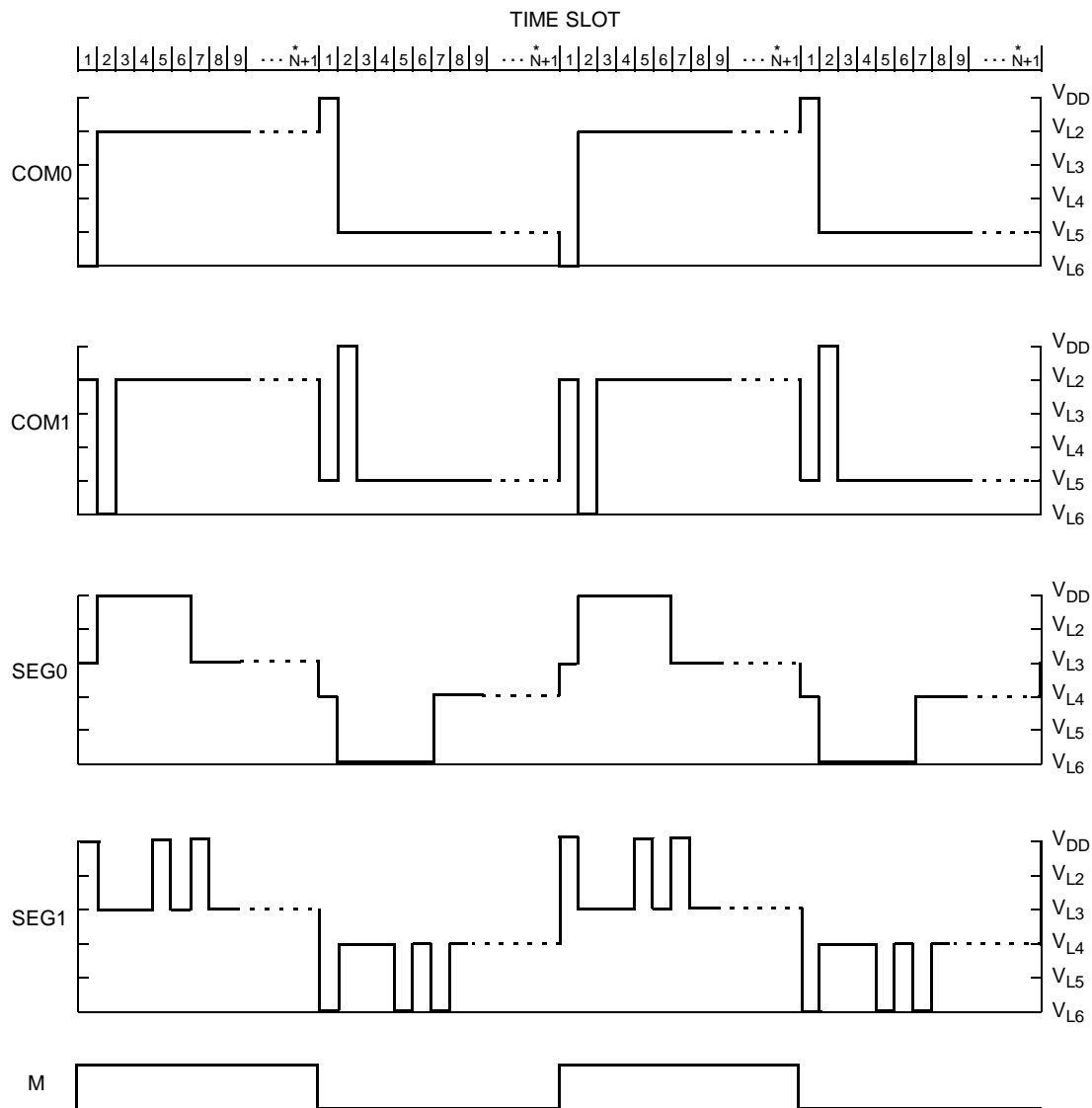


Figure 8a. LCD Display Example "0"



* Note : N is the number of multiplex ratio not included Icon, N is equal to 64 on POR.

Figure 8b - LCD Driving Waveform

COMMAND TABLE

| Bit Pattern | Write Command (D/C=0, R/W(WR)=0, E(RD)=1) | Comment |
|---|---|--|
| 0000X ₃ X ₂ X ₁ X ₀ | Set Lower Column Address | Set the lower nibble of the columne address register using X ₃ X ₂ X ₁ X ₀ as data bits. The initial display line register is reset to 0000b during POR. |
| 0001X ₃ X ₂ X ₁ X ₀ | Set Higher Column Address | Set the higher nibble of the columne address register using X ₃ X ₂ X ₁ X ₀ as data bits. The initial display line register is reset to 0000b during POR. |
| 00100X ₂ X ₁ X ₀ | Set Internal Regulator Resistor Ratio | Internal regulator gain increases as X ₂ X ₁ X ₀ increased from 000b to 111b. At POR, X ₂ X ₁ X ₀ = 100b. |
| 00101X ₂ X ₁ X ₀ | Set Power Control Register | X ₀ =0: turns off the output op-amp buffer (POR) X ₀ =1: turns on the output op-amp buffer X ₁ =0: turns off the internal regulator (POR) X ₁ =1: turns on the internal regulator X ₂ =0: turns off the internal voltage booster (POR) X ₂ =1: turns on the internal voltage booster |
| 01X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ | Set Display Start Line | Set display RAM display start line register from 0-63 using X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ . Display start line register is reset to 000000 during POR. |
| 10000001 * * X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ | Set Contrast Control Register | Set Contrast level from 64 contrast steps. Contrast increases (V _{L6} decreases) as X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ is increased. X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ = 100000b (POR) |
| 1010000X ₀ | Set Segment Re-map | X ₀ =0: column address 00h is mapped to SEG0 (POR) X ₀ =1: column address 83h is mapped to SEG0 Refer to Figure 5 for example. |
| 1010001X ₀ | Set LCD Bias | X ₀ =0: 1/9 bias (POR) X ₀ =1: 1/7 bias For setting bias ratio to 1/4, 1/5, 1/6 or 1/8, see Extended Command Table. |
| 1010010X ₀ | Set Entire Display On/Off | X ₀ =0: normal display (POR) X ₀ =1: entire display on |
| 1010011X ₀ | Set Normal/Reverse Display | X ₀ =0: normal display (POR) X ₀ =1: reverse display |
| 1010111X ₀ | Set Display On/Off | X ₀ =0: turns off LCD panel (POR) X ₀ =1: turns on LCD panel |
| 1011X ₃ X ₂ X ₁ X ₀ | Set Page Address | Set GDDRAM Page Address (0-8) using X ₃ X ₂ X ₁ X ₀ |
| 1100X ₃ * * * | Set COM Output Scan Direction | X ₃ =0: normal mode (POR) X ₃ =1: remapped mode, COM0 to COM[N-1] becomes COM[N-1] to COM0 when Multiplex ratio is equal to N. See Figure 5 as an example for N equal to 64. |
| 11100000 | Set Read-Modify-Write Mode | Read-modify-write mode will be entered in which the column address will not be incremented during display data read. At POR, Read-modify-write mode is turned OFF. |
| 11100010 | Software Reset | Initialize the internal status register. |
| 11101110 | Set End of Read-Modify-Write Mode | Exit Read-modify-write mode. Column address before entering the mode will be restored. At POR, Read-modify-write mode is OFF. |
| 1010110X ₀ * * * * * X ₁ X ₀ | Set Indicator On/Off Indicator Display Mode, This second byte command is required ONLY when "Set Indicator On" command is sent. | X ₀ = 0: indicator off (POR, no need of second command byte) X ₀ = 1: indicator on (second command byte required) X ₁ X ₀ = 00: indicator off X ₁ X ₀ = 01: indicator on and blinking at ~1 second interval X ₁ X ₀ = 10: indicator on and blinking at ~1/2 second interval X ₁ X ₀ = 11: indicator on constantly |
| 11100011 | NOP | Command for No Operation |
| 11110000 | Test Mode Reset | Reserved for IC testing. Do NOT use. |
| 1111 * * * * | Set Test Mode | Reserved for IC testing. Do NOT use. |
| * * * * * * | Set Power Save Mode | Standby or sleep mode will be entered with compound commands |

| Bit Pattern | Read Command (D/C=0, R/W(WR)=1, E(RD)=0) | Comment |
|---|---|---|
| D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀ (Data Read Back from the driver) | Status Register Read | D ₇ =0: indicates an internal operation is completed. D ₇ =1: indicates an internal operation is in progress. D ₆ =0: indicates reverse segment mapping with column address D ₆ =1: indicates normal segment mapping with column address D ₅ =0: indicates the display is ON D ₅ =1: indicates the display is OFF D ₄ =0: initialization is not in progress D ₄ =1: initialization is in progress after $\overline{\text{RES}}$ or software reset D ₃ D ₂ D ₁ D ₀ = 1010, these 4-bit is fixed to 1010 which could be used to identify as Solomon Systech Device. |

EXTENDED COMMAND TABLE

| Bit Pattern | Command | Comment |
|---|---|--|
| 10101000 00X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ | X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ : Set Multiplex Ratio | To select multiplex ratio N from 2 to 65 [Included Icon Line]. N = X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ + 2, eg. N = 111111b + 2 = 65 (POR) |
| 10101001 X ₇ X ₆ X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ | X ₁ X ₀ : Set Bias Ratio X ₄ X ₃ X ₂ : Set TC Value X ₇ X ₆ X ₅ : Modify Osc. Freq. | X ₁ X ₀ = 00: 1/8, 1/6 X ₁ X ₀ = 01: 1/6, 1/5 X ₁ X ₀ = 10: 1/9, 1/7 (POR) X ₁ X ₀ = 11: Prohibited X ₄ X ₃ X ₂ = 000: -0.01%/C (TC0, POR) X ₄ X ₃ X ₂ = 010: -0.10%/C (TC2) X ₄ X ₃ X ₂ = 100: -0.18%/C (TC4) X ₄ X ₃ X ₂ = 111: -0.25%/C (TC7) X ₄ X ₃ X ₂ = 001, 011, 101, 110: Reserved Increase the value of X ₇ X ₆ X ₅ will increase the oscillator frequency and vice versa. This command is not recommended to be used. X ₇ X ₆ X ₅ = 011(POR) |
| 1010101X ₀ | X ₀ : Set 1/4 Bias Ratio | X ₀ = 0: use Normal Setting (POR) X ₀ = 1: fixed at 1/4 Bias |
| 11010010 0X ₆ X ₅ 00010 | X ₆ X ₅ : Set Total Frame Phases | The On/Off of the Static Icon is given by 3 phases/1 phase overlapping of the M and MSTAT signals. This command set how many phases of dividing the M/MSTAT signals for each frame. The more the phases, the less the overlapping and thus the lower the effective driving voltage. X ₆ X ₅ = 00: 3 phases X ₆ X ₅ = 01: 5 phases X ₆ X ₅ = 10: 7 phases (POR) X ₆ X ₅ = 11: 16 phases |
| 11010011 00X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ | X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ : Set Display Offset (for mux ratio has been set less than 64 only) | After POR, X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ = 0 After setting mux ratio less than 64, data will be displayed at Center of matrix. See Table 1. To move display towards Row 0 by L, X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ = L To move display away from Row 0 by L, X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ = 64-L Note: max. value of L = (64 - display mux)/2 |

Note: Patterns other than that given in Command Table and Extended Command Table are prohibited to enter to the chip as a command. Otherwise, unexpected result will occurs.

Data Read / Write

To read data from the GDDRAM, input High to $\overline{R/W(WR)}$ pin and $\overline{D/C}$ pin for 6800-series parallel mode, Low to $\overline{E(RD)}$ pin and High to $\overline{D/C}$ pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read. However, no automatic increase will be performed in read-modify-write mode. Also, a dummy read is required before the first data read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to $\overline{R/W(WR)}$ pin and High to $\overline{D/C}$ pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

Address Increment Table (Automatic)

| D/C | R/W(WR) | Comment | Address Increment | Remarks |
|-----|---------|---------------|-------------------|---------|
| 0 | 0 | Write Command | No | |
| 0 | 1 | Read Status | No | |
| 1 | 0 | Write Data | Yes | |
| 1 | 1 | Read Data | Yes | *1 |

Address Increment is done automatically after data read/write. The column address pointer of GDDRAM*² is affected.

Remarks: 1. If read data is issued in read-modify-write mode, address will NOT be increased.
2. Column Address will NOT wrap round to zero when overflow.

Commands Required for $\overline{R/W(WR)}$ Actions on RAM

| R/W(WR) Actions on RAMs | Commands Required | |
|-------------------------------------|--|--|
| Read/Write Data from/to GDDRAM. | Set GDDRAM Page Address | (1011X ₃ X ₂ X ₁ X ₀)* |
| | Set GDDRAM Column Address | (0001X ₃ X ₂ X ₁ X ₀)* |
| | Read/Write Data | (0000X ₃ X ₂ X ₁ X ₀) (X ₇ X ₆ X ₅ X ₄ X ₃ X ₂ X ₁ X ₀) |
| Save/Restore GDDRAM Column Address. | Save GDDRAM Column Address by read-modify-write mode | (11100000) |
| | Restore GDDRAM Column Address by end of read-modify-write mode | (11101110) |

Note: 1. No need to resend the command again if it is set previously.
2. The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed or not.

Command Description

Set Lower Column Address

This command specifies the lower nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

Set Higher Column Address

This command specifies the higher nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

Set Internal Regulator Resistors Ratio

This command is to enable any one of the eight internal resistor sets for different regulator gain when using internal regulator resistor network (IRS pin pulled high). Please refer to Block Diagram Description section for detail calculation of the LCD driving voltage.

Set Power Control Register

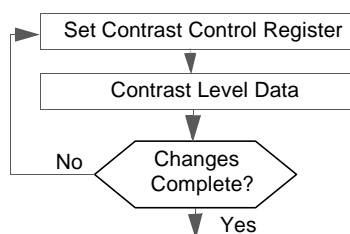
This command turns on/off the various power circuits associated with the chip.

Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0. The display start line values of 0 to 63 are assigned to Page 0 to 7.

Set Contrast Control Register

This commands adjusts the contrast of the LCD panel by changing V_{L6} of the LCD drive voltage provided by the On-Chip power circuits. V_{L6} is set with 64 steps (6-bit) contrast control register. It is a compound commands:



Set Segment Re-map

This commands changes the mapping between the display data column address and segment driver. It allows flexibility in layout during LCD module assembly. Refer to Figure 5 for example.

Set LCD Bias

This command selects a suitable bias ratio (1/7 or 1/9) required for driving the particular LCD panel in use. The POR default for SSD1815 is set to 1/9 bias. For setting 1/4, 1/5, 1/6 and 1/8 bias, an extended compound command should be

used.

Set Entire Display On/Off

This command forces the entire display, including the icon row, to be "ON" regardless of the contents of the display data RAM. This command has priority over normal/reverse display. This command will be used with "Set Display Display ON/OFF" command to form a compound command for entering power save mode. See "Set Power Save Mode".

Set Normal/Reverse Display

This command sets the display to be either normal/reverse. In normal display, a RAM data of 1 indicates an "ON" pixel while in reverse display, a RAM data of 0 indicates an "ON" pixel. In icon mode, the icon line is not reversed by this command.

Set Display On/Off

This command alternatively turns the display on and off. When display off is issued with entire display on, power save mode will be entered. See "Set Power Save Mode" for details.

Set Page Address

This command positions the page address from 0 to 8 possible positions in GDDRAM. Refer to Figure 5 for mapping.

Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly.

Set Read-Modify-Write Mode

This command puts the chip in read-modify-write mode in which:

1. the column address is saved before entering the mode
2. the column address is incremented by display data write but not by display data read

Software Reset

This command causes some of the internal status registers of the chip to be initialized:

1. Static indicator is turned OFF
2. Display start line register is set to 0
3. Column address counter is set to 0
4. Page address is set to 0
5. Normal scan direction of the COM outputs
6. Contrast control register is set to 0
7. Test mode is turned OFF

Set End of Read-Modify-Write Mode

This command relieves the chip from read-modify-write mode. The column address that is saved before entering read-modify-write mode will be restored.

Set Indicator On/Off

This command turns on and off the static drive indicators. It also controls whether standby mode or sleep mode will be

entered after the power save compound command. See "Set Power Save Mode".

When the "Set Indicator On" command is sent, the "Indicator Display Mode" must be followed in the next command. The "Set Indicator Off" command is a single byte command and no following command is required.

NOP

A command causing No Operation.

Set Test Mode

This command force the driver chip into its test mode for internal testing of the chip. Under normal operation, user should NOT use this command.

Set Power Save Mode

To enter Standby or Sleep Mode, it should be done by using a compound command composed of "Set Display ON/OFF" and "Set Entire Display ON/OFF" commands. When "Set Entire Display ON" is issued when display is OFF, either Standby Mode or Sleep Mode will be entered.

The status of the Static Indicator will determine which power save mode is entered. If static indicator is off, the Sleep Mode will be entered:

1. Internal oscillator and LCD power supply circuits are stopped
2. Segment and Common drivers output V_{DD} level
3. The display data and operation mode before sleep are held
4. Internal display RAM can still be accessed

If the static indicator is on, the chip enters Standby Mode which is similar to sleep mode except:

1. Internal oscillator is on
2. Static drive system is on

Note also that if the software reset command is issued during Standby Mode, Sleep Mode will be entered. Both power save modes can be exited by the issue of a new software command or by pulling Low at hardware pin \overline{RES} .

Status register Read

This command is issued by pulling $\overline{D/C}$ Low during a data read (refer to Figure 9 and 10 for parallel interface waveforms). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to trigger the enhanced features, on top of general ones, designed for the chip.

Set Multiplex Ratio

This command switches default 64 multiplex mode to any multiplex mode from 2 to 64. The chip pads ROW0-ROW63 will be switched to corresponding COM signal output, see Table 1 for examples of different multiplex settings.

Set Bias Ratio

Except the 1/4 bias, all the available bias ratios (1/5, 1/6, 1/7, 1/8 and 1/9) could be set using this command plus the Set LCD Bias. When changing the display multiplex ratio, the bias ratio also need to be adjusted to make display contrast consistent.

Set Temperature Coefficient (TC) Value

4 different temperature coefficient settings is selected by this command in order to match various liquid crystal temperature grades.

Modify Oscillator Frequency

The oscillator frequency can be fine tuned by applying this command. Since the oscillator frequency will be affected by some other factors, this command is not recommended for general usage. Please contact our application engineer for more detail explanation on this command.

Set 1/4 Bias Ratio

This command sets the bias ratio directly to 1/4 bias. This ratio is especially for use in under 12mux display.

In order to restore to other bias ratio, this command must be executed, with LSB=0, before the "Set Multiplex ratio" or "Set LCD Bias" command is sent.

Set Total Frame Phases

The total number of phases for one display frame is set by this command.

The Static Icon is generated by the overlapping of the M and MSTAT signals. To turn on the Static Icon, 3 phases overlapping will be applied to these signals, while 1 phase overlapping will be given to the Off status.

The more the total number of phases in one frame, the less the overlapping time and thus the lower the effective driving voltage at the Static Icon on the LCD panel.

Set Display Offset

This command should be sent ONLY when the multiplex ratio is set less than 64.

When the multiplex ratio less than 64 is set, the display will be mapped in the middle (y-direction) of the LCD, see Table 1. Use this command could move the display vertically within the 64 commons.

To make the Reduced-Mux Com 0 (Com 0 after reducing the multiplex ratio) towards the Row 0 direction for L lines, the 6-bit data in second command should be given by L.

To move in the other direction by L lines, the 6-bit data should be given by 64-L.

Please note that the display is confined within the un-reduced 64 mux. That is maximum value of L is given by the half of 64 minus the reduced-multiplex ratio. For an odd display mux after reduction, moving away from Row 0 direction will have 1 more step.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|-----------|---|------------------------------|------|
| V_{DD} | Supply Voltage | -0.3 to +4.0 | V |
| V_{EE} | | 0 to -12.0 | V |
| V_{in} | Input Voltage | $V_{SS}-0.3$ to $V_{DD}+0.3$ | V |
| I | Current Drain Per Pin Excluding V_{DD} and V_{SS} | 25 | mA |
| T_A | Operating Temperature | -30 to +85 | °C |
| T_{stg} | Storage Temperature Range | -65 to +150 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

DC CHARACTERISTICS (Unless otherwise specified, Voltage Referenced to V_{SS} , $V_{DD} = 2.4$ to $3.5V$, $T_A = -30$ to $85^\circ C$.)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|-------------|--|--|--------------------|----------|--------------------|---------|
| V_{DD} | Logic Circuit Supply Voltage Range | Recommend Operating Voltage Possible Operating Voltage | 2.4 1.8 | 2.7 - | 3.5 3.5 | V V |
| I_{AC} | Access Mode Supply Current Drain (V_{DD} Pins) | $V_{DD} = 2.7V$, Voltage Generator On, 4X DC-DC Converter Enabled, Write accessing, $T_{cyc} = 3.3MHz$, Osc. Freq.=17kHz, Display On. | - | 300 | 600 | μA |
| I_{DP1} | Display Mode Supply Current Drain (V_{DD} Pins) | $V_{DD} = 2.7V$, $V_{EE} = -8.1V$, Voltage Generator Disabled, R/W(WR) Halt, Osc. Freq. = 17kHz, Display On, $V_{L6} - V_{DD} = -8.1V$. | - | 60 | 100 | μA |
| I_{DP2} | Display Mode Supply Current Drain (V_{DD} Pins) | $V_{DD} = 2.7V$, $V_{EE} = -8.1V$, Voltage Generator On, 4x DC-DC Converter Enabled, R/W(WR) Halt, Osc. Freq. = 17kHz, Display On, $V_{L6} - V_{DD} = -8.1V$. | - | 150 | 200 | μA |
| I_{SB} | Standby Mode Supply Current Drain (V_{DD} Pins) | $V_{DD}=2.7V$, LCD Driving Waveform Off, Osc. Freq. = 17kHz, R/W(WR) halt. | - | 3.5 | 10 | μA |
| I_{SLEEP} | Sleep Mode Supply Current Drain (V_{DD} Pins) | $V_{DD} = 2.7V$, LCD Driving Waveform Off, Oscillator Off, R/W(WR) halt. | - | 0.2 | 5 | μA |
| V_{EE} | LCD Driving Voltage Generator Output (V_{EE} Pin) | Display On, Voltage Generator Enabled, DC/DC Converter Enabled, Osc. Freq.=17kHz, Regulator Enabled, Divider Enabled. | -12.0 | - | -1.8 | V |
| V_{LCD} | LCD Driving Voltage Input (V_{EE} Pin) | Voltage Generator Disabled. | -12.0 | - | -1.8 | V |
| V_{OH1} | Logic High Output Voltage | $I_{out}=100\mu A$ | $0.9 \cdot V_{DD}$ | - | V_{DD} | V |
| V_{OL1} | Logic Low Output Voltage | $I_{out}=100\mu A$ | 0 | - | $0.1 \cdot V_{DD}$ | V |
| V_{L6} | LCD Driving Voltage Source (V_{L6} Pin) | Regulator Enabled (V_{L6} voltage depends on Int/Ext Contrast Control) | $V_{EE}-0.5$ | - | V_{DD} | V |
| V_{L6} | LCD Driving Voltage Source (V_{L6} Pin) | Regulator Disable | - | Floating | - | V |
| V_{IH1} | Logic High Input voltage | | $0.8 \cdot V_{DD}$ | - | V_{DD} | V |
| V_{IL1} | Logic Low Input voltage | | 0 | - | $0.2 \cdot V_{DD}$ | V |

| | | | | | | |
|---|--|--|--|---|---|--------------------------|
| V _{L2} V _{L3} V _{L4} V _{L5} V _{L6} | LCD Display Voltage Output (V _{L2} , V _{L3} , V _{L4} , V _{L5} , V _{L6} Pins) | Voltage reference to V _{DD} , Bias Divider Enabled, 1:7 bias ratio | - - - - - | 1/7*V _{L6} 2/7*V _{L6} 5/7*V _{L6} 6/7*V _{L6} V _{L6} | - - - - - | V V V V V |
| V _{L2} V _{L3} V _{L4} V _{L5} V _{L6} | LCD Display Voltage Output (V _{L2} , V _{L3} , V _{L4} , V _{L5} , V _{L6} Pins) | Voltage reference to V _{DD} , Bias Divider Enabled, 1:9 bias ratio | - - - - - | 1/9*V _{L6} 2/9*V _{L6} 7/9*V _{L6} 8/9*V _{L6} V _{L6} | - - - - - | V V V V V |
| V _{L2} V _{L3} V _{L4} V _{L5} V _{L6} | LCD Display Voltage Input (V _{L2} , V _{L3} , V _{L4} , V _{L5} , V _{L6} Pins) | Voltage reference to V _{DD} , External Voltage Generator, Bias Divider Disabled | V _{L3} V _{L4} V _{L5} V _{L6} -12V | - - - - - | V _{DD} V _{L2} V _{L3} V _{L4} V _{L5} | V V V V V |
| I _{OH} | Logic High Output Current Source | V _{out} = V _{DD} -0.4V | 50 | - | - | μA |
| I _{OL} | Logic Low Output Current Drain | V _{out} = 0.4V | - | - | -50 | μA |
| I _{OZ} | Logic Output Tri-state Current Drain Source | | -1 | - | 1 | μA |
| I _{IL} /I _{IH} | Logic Input Current | | -1 | - | 1 | μA |
| C _{IN} | Logic Pins Input Capacitance | | - | 5 | 7.5 | pF |
| ΔV _{L6} | Variation of V _{L6} Output (V _{DD} is fixed) | Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0 | - | ± 3 | - | % |
| PTC0 PTC2 PTC4 PTC7 | Temperature Coefficient Compensation Flat Temperature Coefficient (POR) Temperature Coefficient 2* Temperature Coefficient 4* Temperature Coefficient 7* | Voltage Regulator Enabled Voltage Regulator Enabled Voltage Regulator Enabled Voltage Regulator Enabled | 0 -0.075 -0.15 -0.20 | -0.01 -0.10 -0.18 -0.25 | -0.075 -0.15 -0.20 - | %/C %/C %/C %/C |

* The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{ref} \text{ at } 50^{\circ}\text{C} - V_{ref} \text{ at } 0^{\circ}\text{C}}{50^{\circ}\text{C} - 0^{\circ}\text{C}} \times \frac{1}{V_{ref} \text{ at } 25^{\circ}\text{C}} \times 100\%$$

AC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = -30 to 85°C.)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|------------------|---|---|-----|-------------------------------|-----|------|
| F _{OSC} | Oscillation Frequency of Display Timing Generator | Internal Oscillator Enabled, V _{DD} = 2.7V | 15 | 17 | 19 | kHz |
| F _{FRM} | Frame Frequency | Display ON, Set 132 X 64 Graphic Display Mode | - | $\frac{F_{OSC}}{4 \times 65}$ | - | Hz |

TABLE 3. 6800-Series MPU Parallel Interface Timing Characteristics ($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = -30$ to $85^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--------------------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 0 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| PW_{CSL} | Chip Select Low Pulse Width (read) | 120 | - | - | ns |
| | Chip Select Low Pulse Width (write) | 60 | - | - | ns |
| PW_{CSH} | Chip Select High Pulse Width (read) | 60 | - | - | ns |
| | Chip Select High Pulse Width (write) | 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

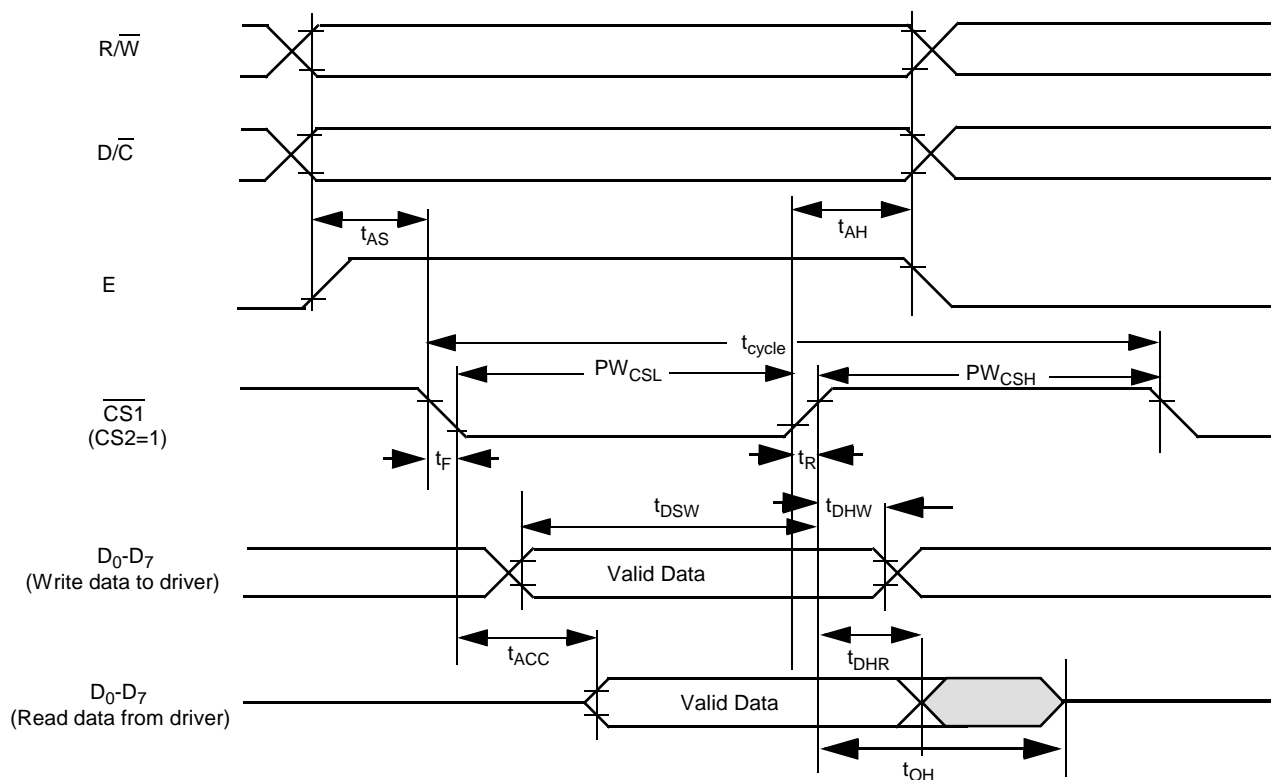


Figure 9 - 6800-series MPU Parallel Interface Characteristics

TABLE 4. 8080-Series MPU Parallel Interface Timing Characteristics ($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = -30$ to $85^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--------------------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 0 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| PW_{CSL} | Chip Select Low Pulse Width (read) | 120 | - | - | ns |
| | Chip Select Low Pulse Width (write) | 60 | - | - | ns |
| PW_{CSH} | Chip Select High Pulse Width (read) | 60 | - | - | ns |
| | Chip Select High Pulse Width (write) | 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

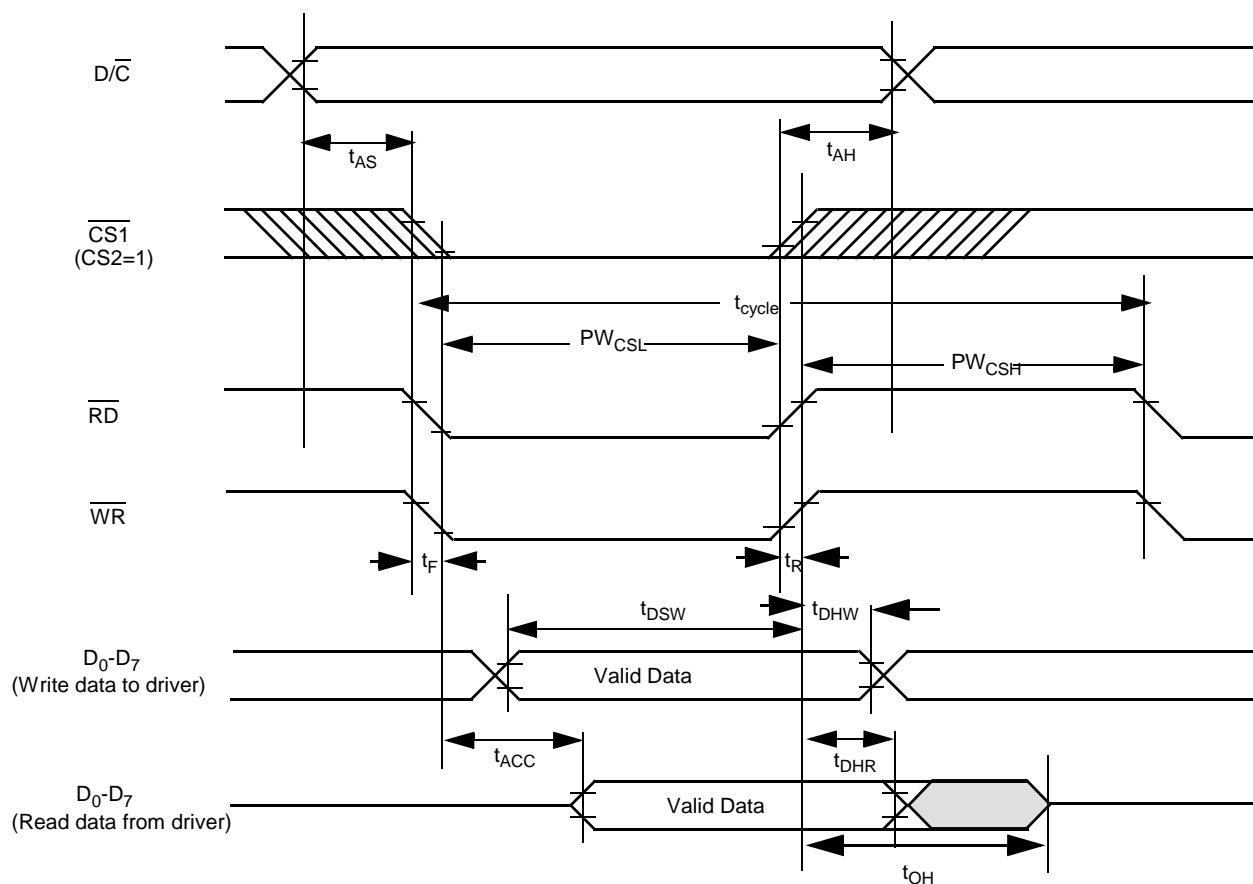


Figure 10 - 8080-series MPU Parallel Interface Characteristics

TABLE 5. Serial Interface Timing Characteristics ($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = -30$ to $85^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 250 | - | - | ns |
| t_{AS} | Address Setup Time | 150 | - | - | ns |
| t_{AH} | Address Hold Time | 150 | - | - | ns |
| t_{CSS} | Chip Select Setup Time (for D_7 input) | 120 | - | - | ns |
| t_{CSH} | Chip Select Hold Time (for D_0 input) | 60 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 100 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 100 | - | - | ns |
| t_{CLKL} | Clock Low Time | 100 | - | - | ns |
| t_{CLKH} | Clock High Time | 100 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

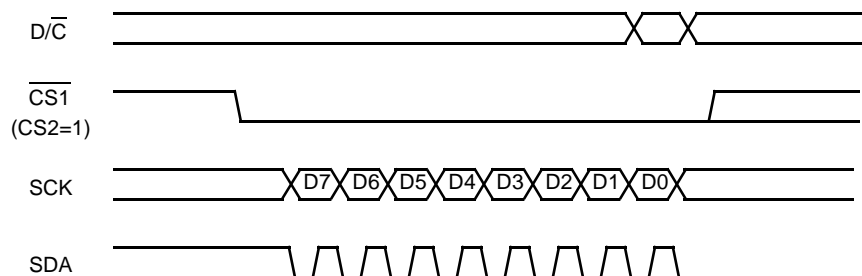
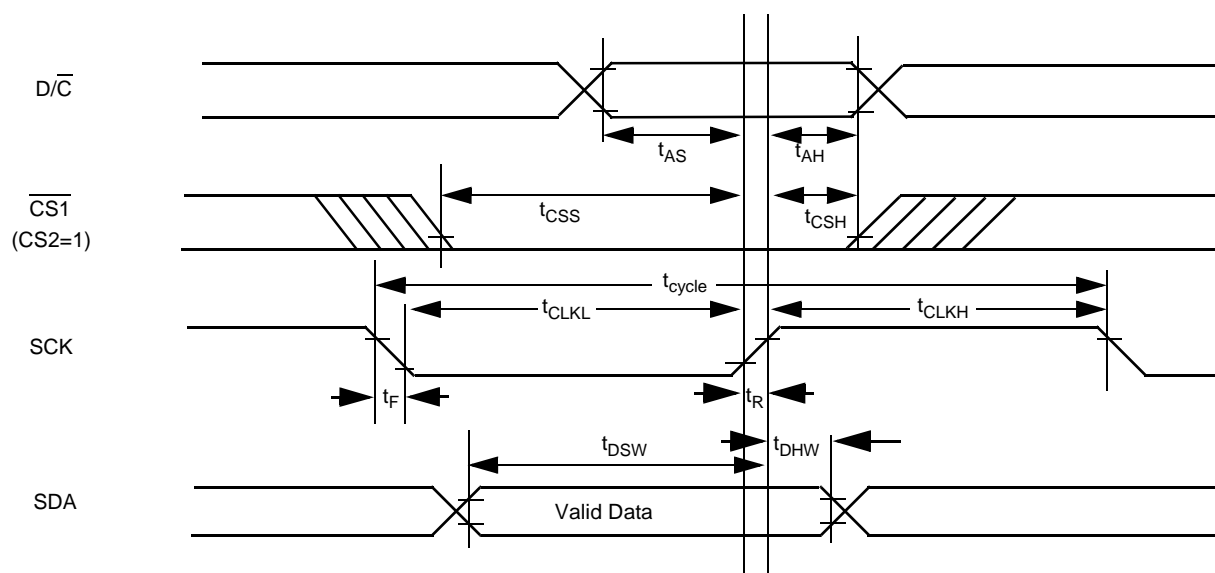
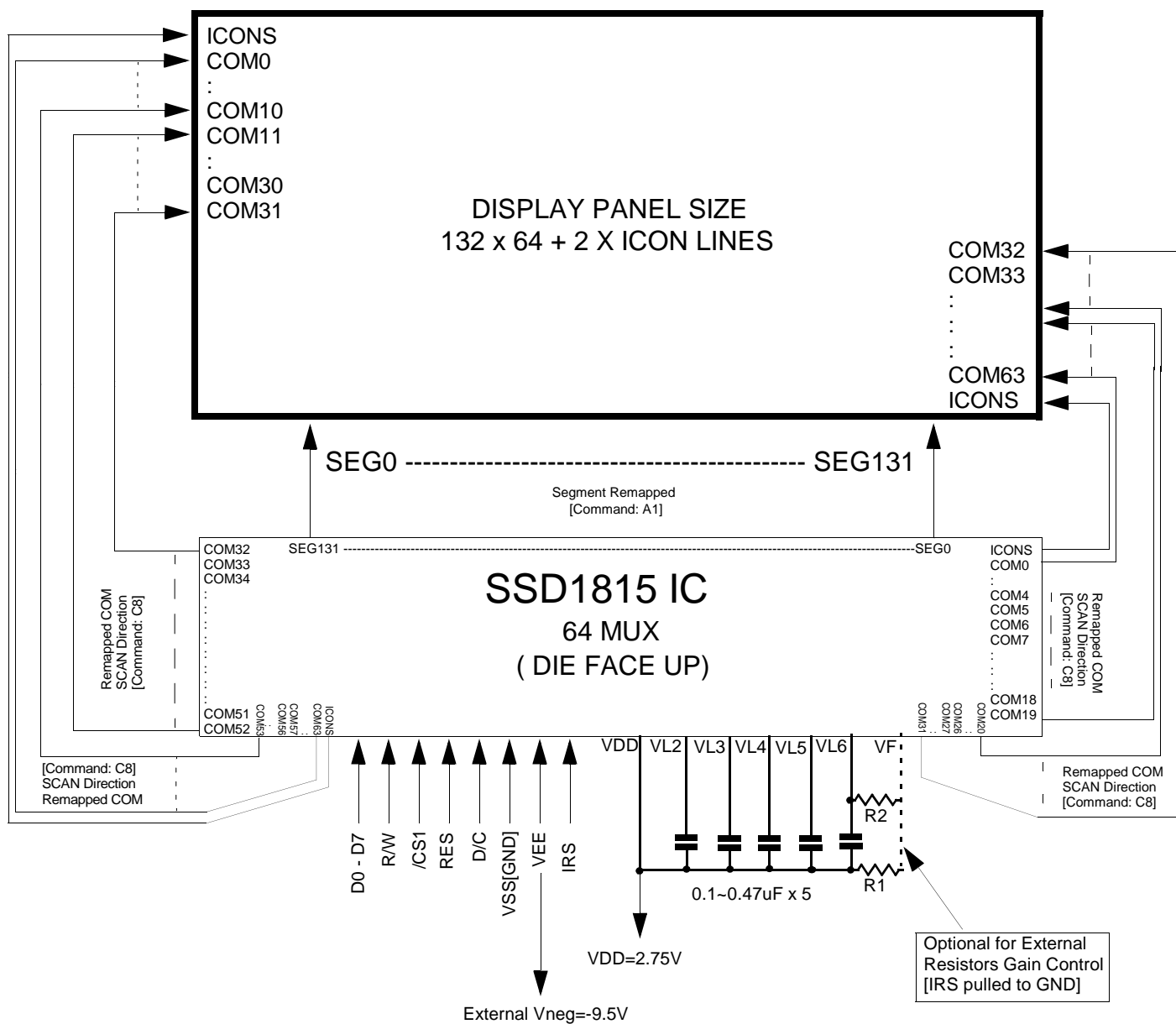


Figure 11 - Serial Interface Characteristics

Figure 12 - Application Circuit: External VEE with internal regulator and divider mode [Command: 2B] in 64 Mux.



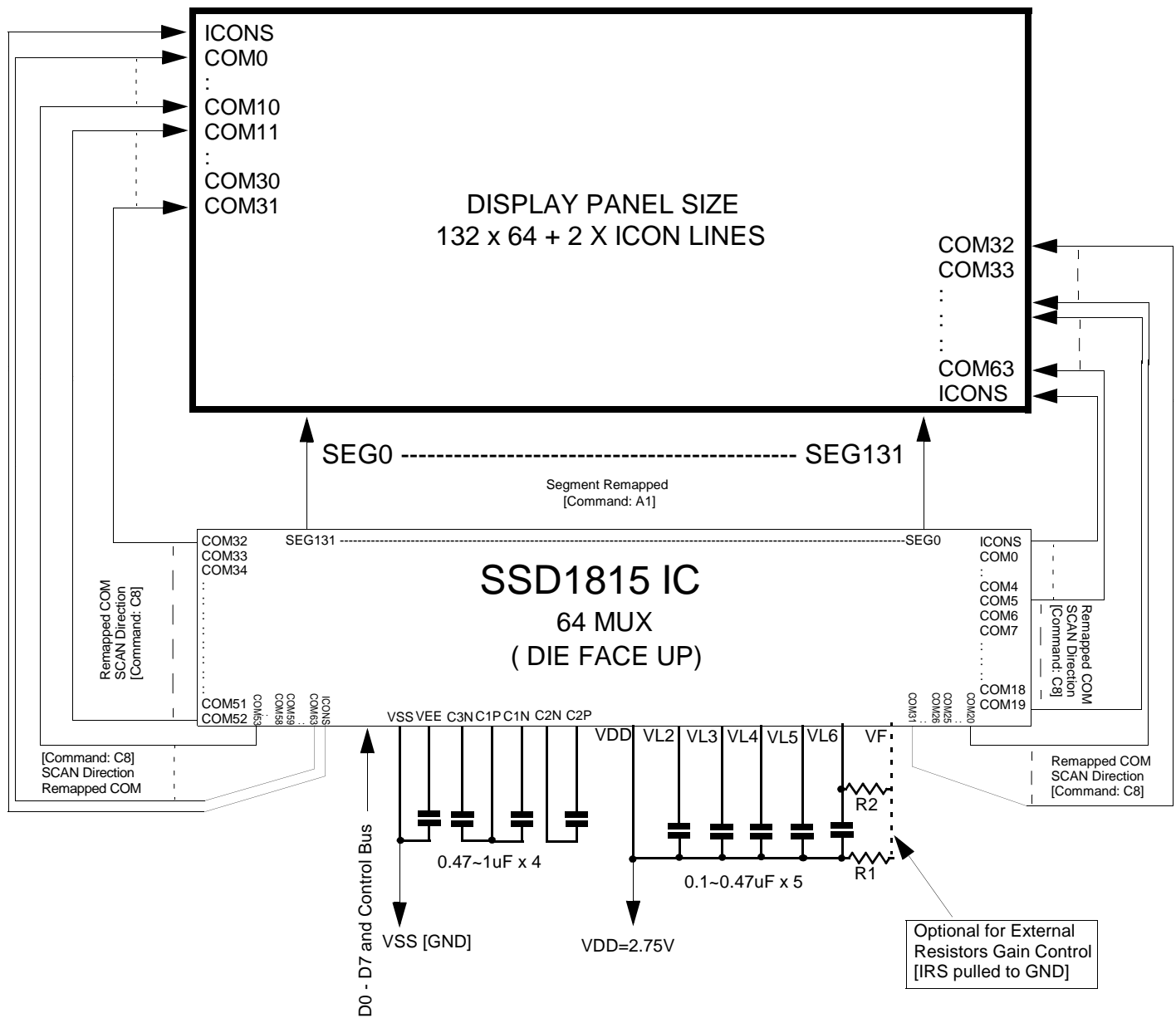
Logic pin connections not specified above:

Pins connected to V_{DD} : CS2, \overline{RD} , M/\overline{S} , CLS, C68/80, P/\overline{S} , \overline{HPM}

Pins connected to V_{SS}: V_{SS1}

Pins floating: $\overline{\text{DOF}}$, CL, V_{FS}

Figure 13 - Application Circuit: ALL internal power mode [Command: 2F] in 64 Mux.



Logic pin connections not specified above:

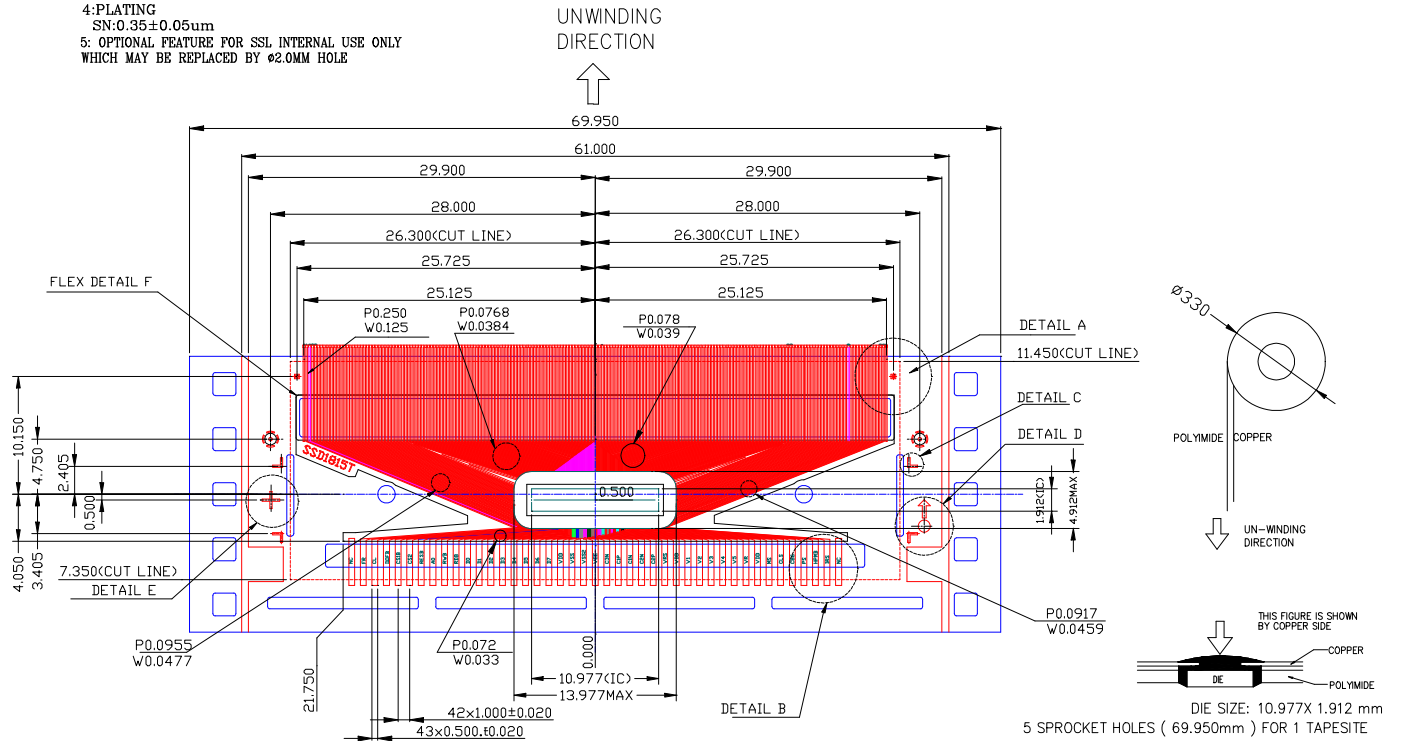
Pins connected to V_{DD} : CS2, \overline{RD} , M/ \overline{S} , CLS, C68/80, P/ \overline{S} , \overline{HPM}

Pins connected to V_{SS} : V_{SS1}

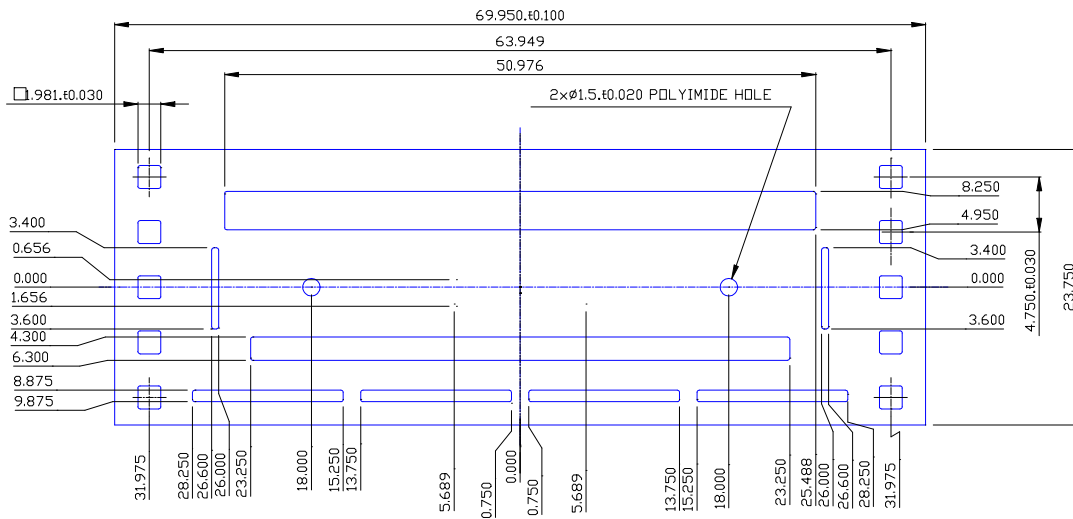
Pins floating: $\overline{\text{DOF}}$, $\overline{\text{CL}}$, $\overline{V_{FS}}$

APPENDIX A0-1. SDD1815T TAB Drawing

- 1:GENERAL TOLERANCE : $\pm 0.050\text{MM}$
- 2:ALL CHAMFER IS R0.20
- 3:MATERIAL
PI :UPILEX-S 75um ± 6 THICKNESS
CU :ED-SLP 25um
SOLDER RESIST: 26 ± 14 um
- 4:PLATING
SN:0.35 ± 0.05 um
- 5: OPTIONAL FEATURE FOR SSL INTERNAL USE ONLY
WHICH MAY BE REPLACED BY $\phi 2.0\text{MM}$ HOLE



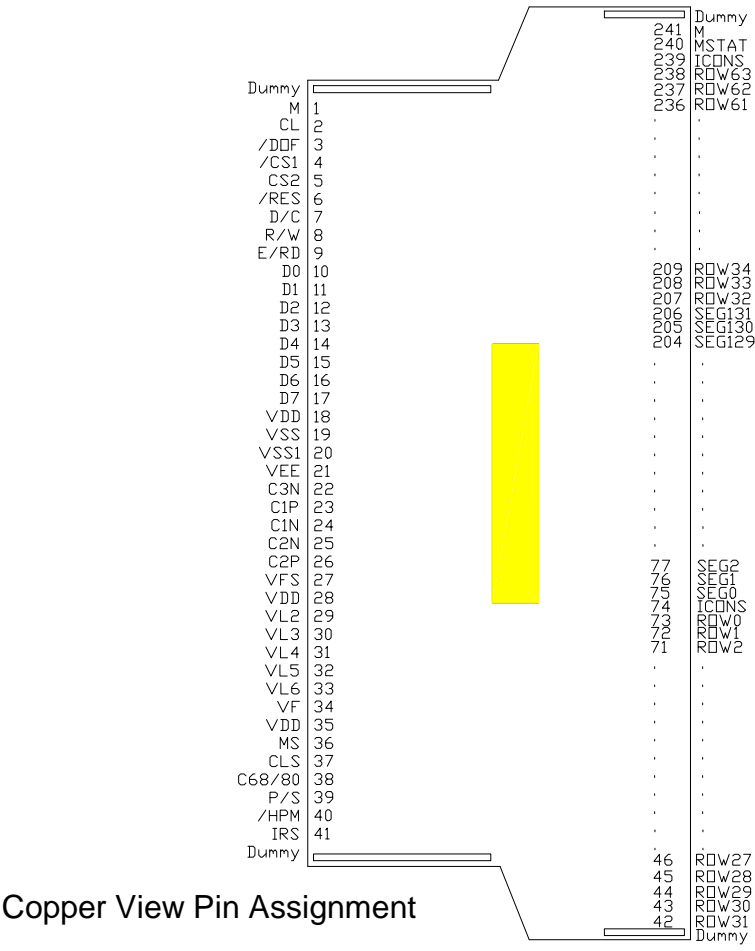
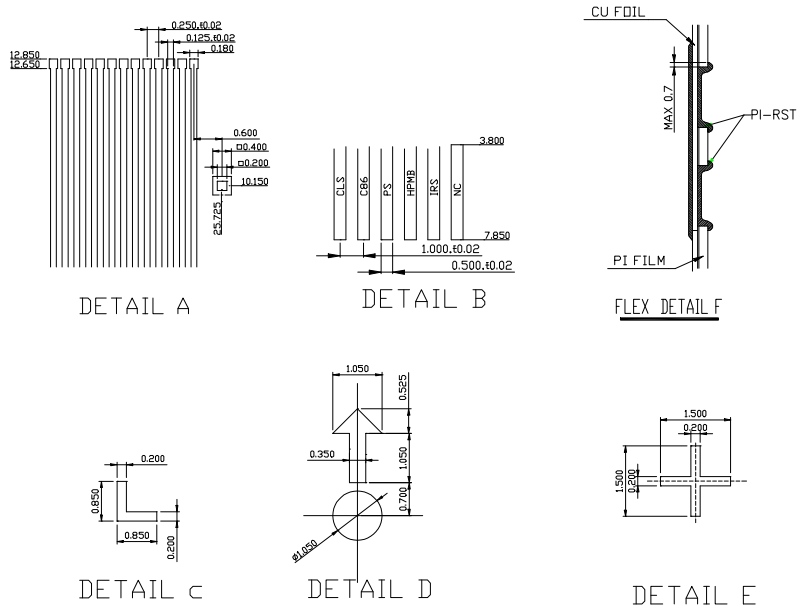
COPPER VIEW



| MATERIAL | UPILEX-S | PI FILM | 75um ± 6 um |
|-----------|----------------|--------------|------------------|
| HARD TOOL | YES | Adhesive | 12 um ± 2 um |
| | NO | PROTECT FILM | 20 um |
| HOLE | HOLE DIMENSION | NUMBER | |
| SQUARE | 1.981X1.981 | 10 | |
| | 11.378X2.312 | 1 | |
| | 50.976X3.300 | 1 | |
| | 13.000X1.000 | 4 | |
| | 7.000X0.600 | 2 | |
| | 46.500X2.500 | 1 | |
| CIRCLE | $\phi 1.500$ | 2 | |
| ELLIPSE | | | |

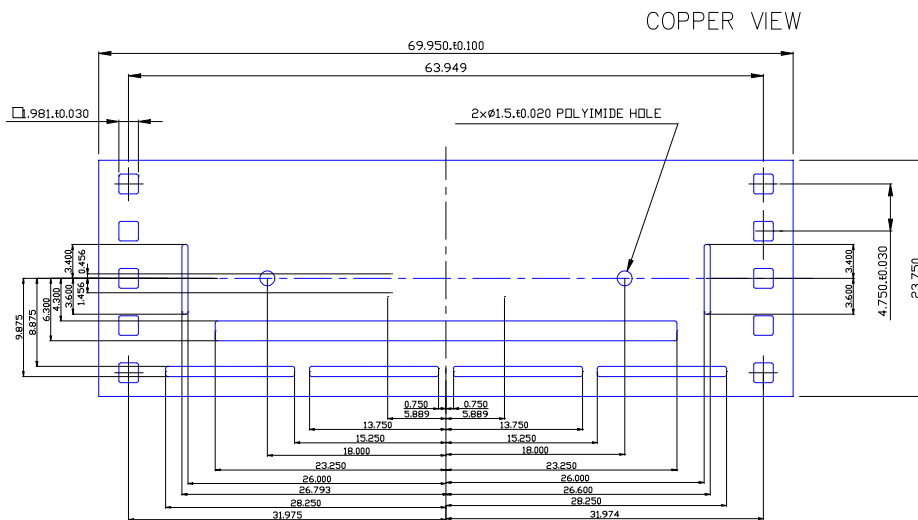
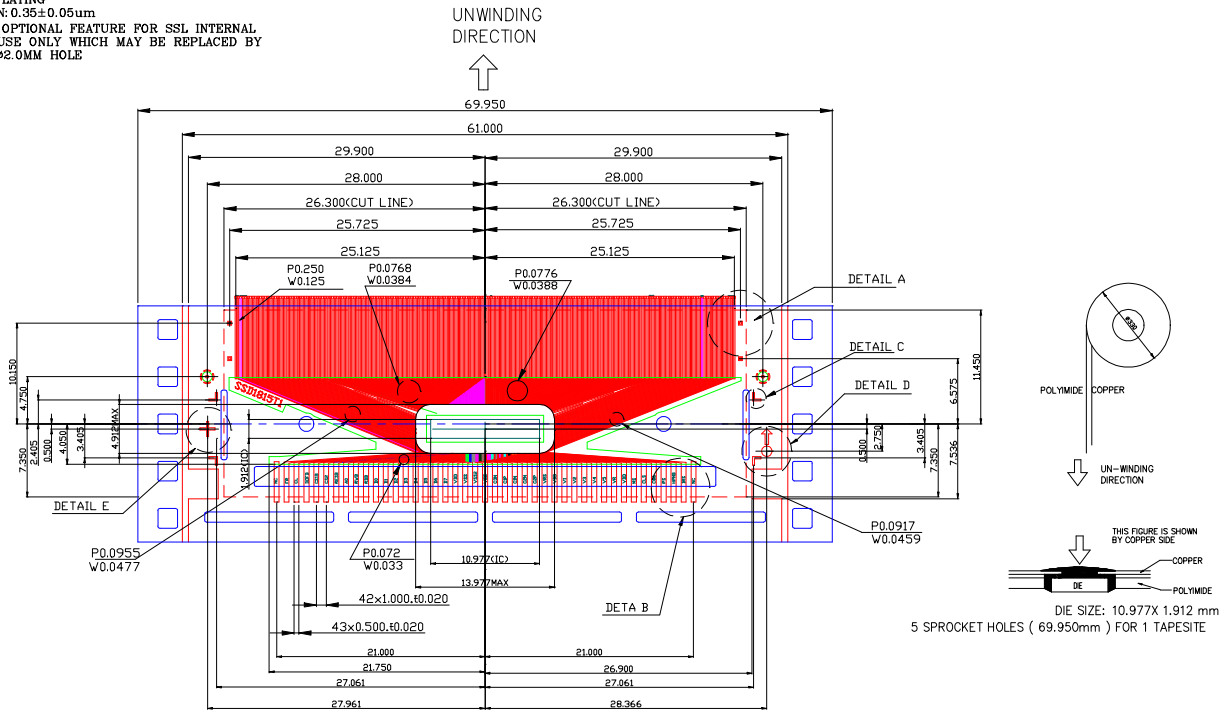
ALL OTHER CHAMFER IS R0.200
GENERAL TOLERANCE ± 0.05

APPENDIX A0-2. SDD1815T TAB Drawing



APPENDIX A1-1. SDD1815T1 TAB Drawing

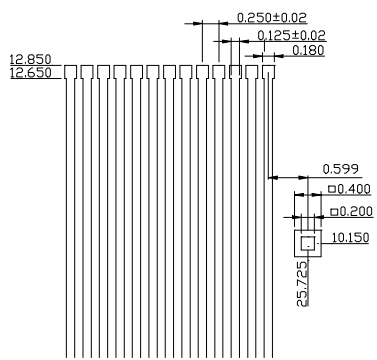
- 1: GENERAL TOLERANCE : $\pm 0.050\text{MM}$
- 2: ALL CHAMFER IS R0.20
- 3: MATERIAL
PI : UPILEX-S 75um ± 6 THICKNESS
CU : ED-SLP 25um
- 4: PLATING
SN: 0.35 ± 0.05 um
- 5: OPTIONAL FEATURE FOR SSL INTERNAL
USE ONLY WHICH MAY BE REPLACED BY
 $\phi 2.0\text{MM}$ HOLE



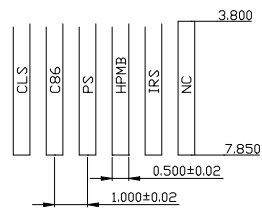
| MATERIAL UPILEX-S PI FILM 75um ± 6 um | | |
|---|----------------|--------|
| HOLE | YES | NO |
| | YES | NO |
| SQUARE | HOLE DIMENSION | NUMBER |
| | 1.981X1.981 | 10 |
| | 11.378X2.312 | 1 |
| | 13.000X1.000 | 4 |
| | 7.000X0.600 | 2 |
| | 46.500X2.500 | 1 |
| CIRCLE | HOLE DIMENSION | NUMBER |
| | Ø1.500 | 2 |
| ELLIPSE | HOLE DIMENSION | NUMBER |
| | | |

ALL OTHER CHAMFER IS R0.200
GENERAL TOLERANCE ± 0.05

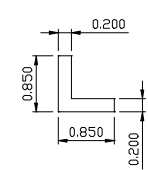
APPENDIX A1-2. SDD1815T1 TAB Drawing



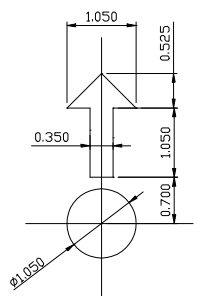
DETAIL A



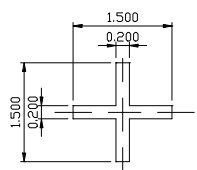
DETAIL B



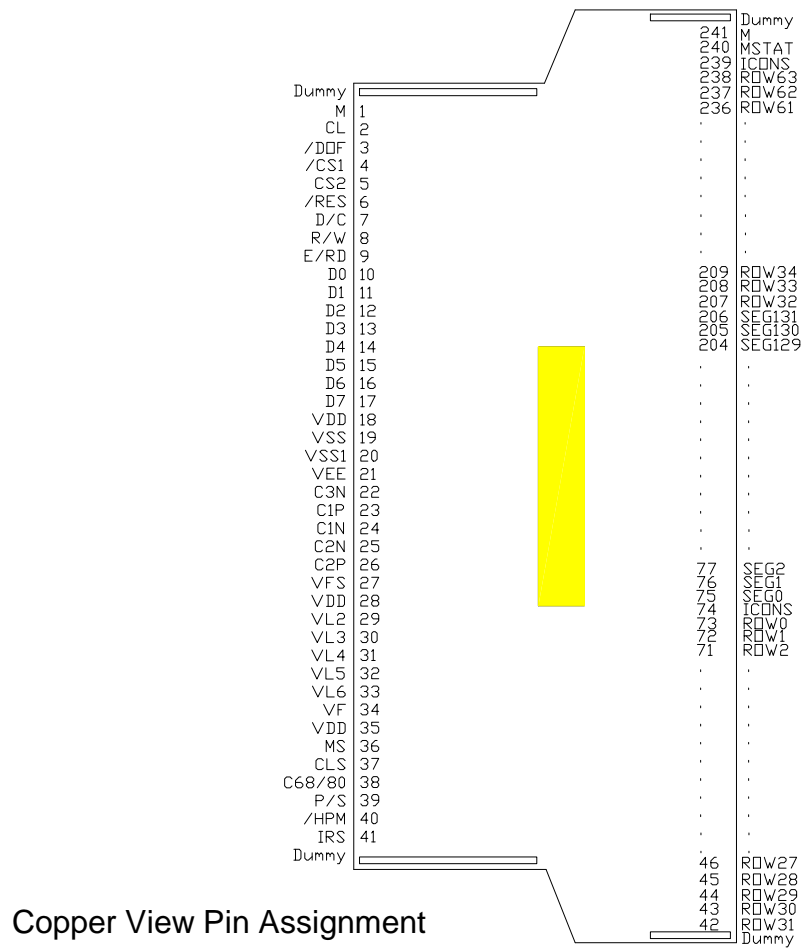
DETAIL C



DETAIL D



DETAIL E



Copper View Pin Assignment

APPENDIX A2-1. SDD1815T2 TAB Drawing

1:GENERAL TOLERANCE :±0.050MM

2:ALL CHAMFER IS R0.20

3:MATERIAL

PI :UPILEXS 75um ±6 THICKNESS

FLEX COATING (PI INK) :FS-100L

ADHESIVE :RAY #7100 12±2um THICKNESS

CU :ED-Su 25um

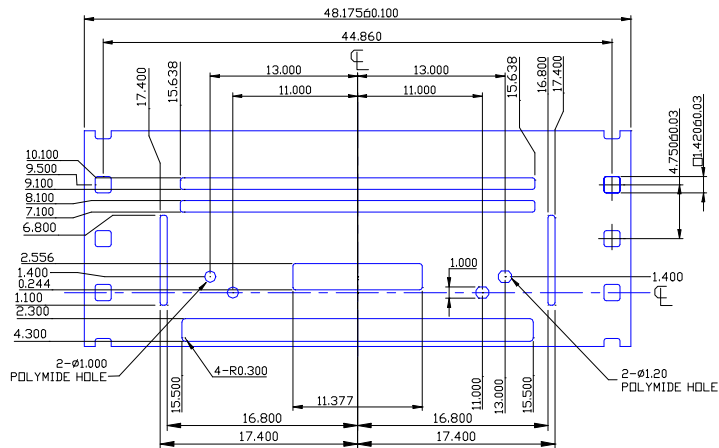
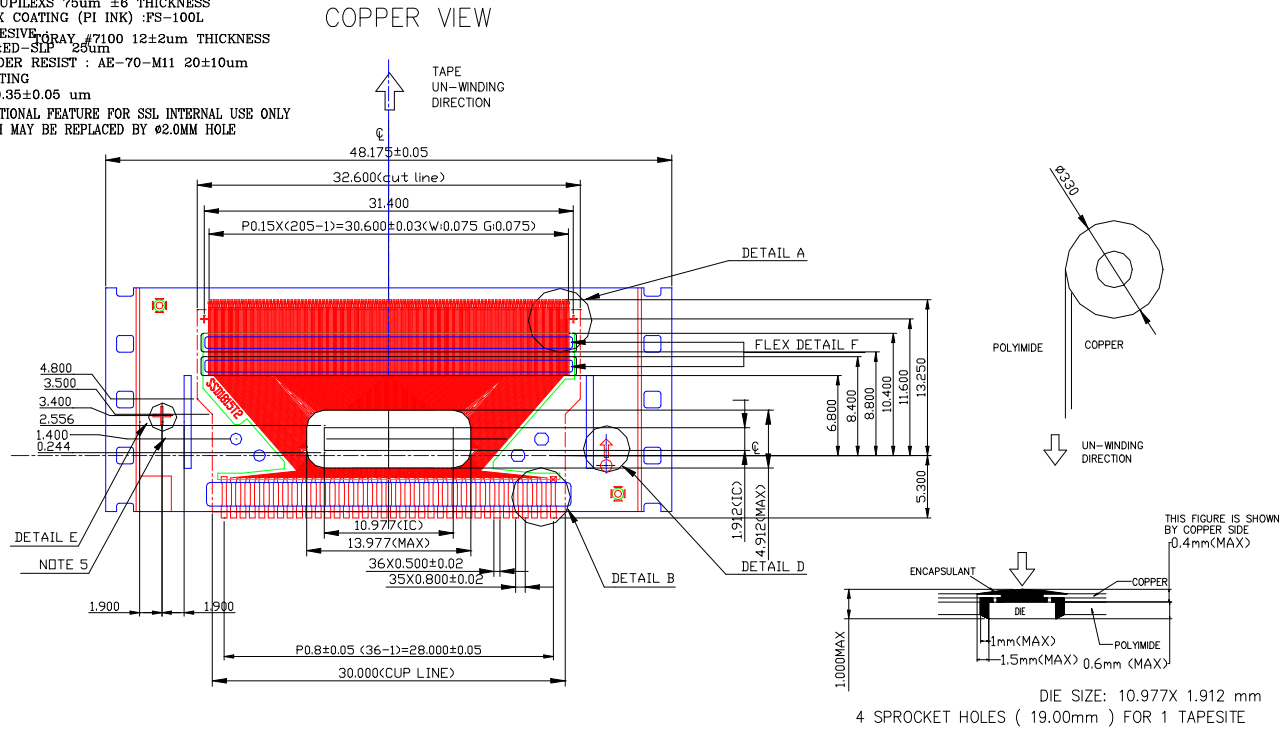
SOLDER RESIST : AE-70-M11 20±10um

4:PLATING

SN:0.35±0.05 um

5: OPTIONAL FEATURE FOR SSL INTERNAL USE ONLY

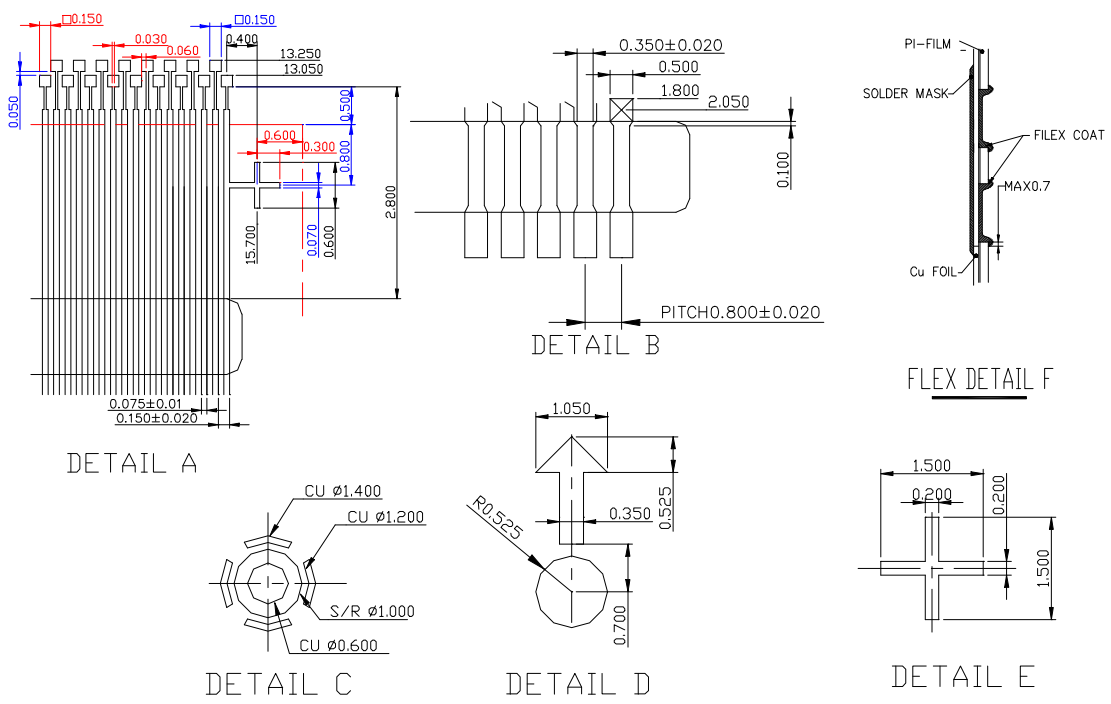
WHICH MAY BE REPLACED BY Ø2.0MM HOLE



| MATERIAL | UPILEX-S | PI FILM | 75um±6um |
|--------------|----------------|--------------|----------------------|
| ADHESIVE | YES | Adhesive | 12um±2um (RAY #7100) |
| PI THICKNESS | NO | PI THICKNESS | 20 um |
| HOLE | HOLE DIMENSION | NUMBER | |
| | 31.275X1.000 | 2 | |
| | 1.420X1.420 | 8 | |
| | 31.000X2.000 | 1 | |
| | 7.900x0.600 | 2 | |
| | 11.377x2.3120 | 1 | |
| SQUARE | | | |
| CIRCLE | Ø1.000 | 2 | |
| | Ø1.200X1.000 | 2 | |
| ELLIPSE | | | |

ALL OTHER CHAMFER IS R0.200
GENERAL TOLERANCE ±0.05

APPENDIX A2-2. SDD1815T2 TAB Drawing

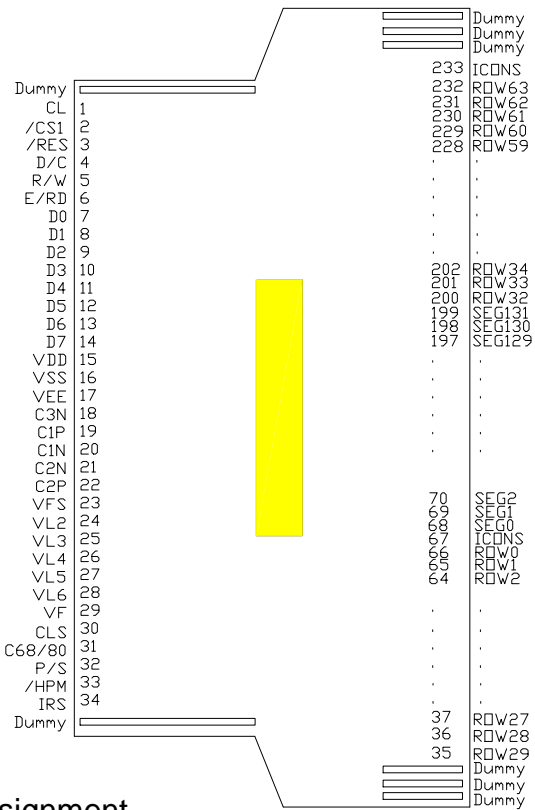


Internal Connections:

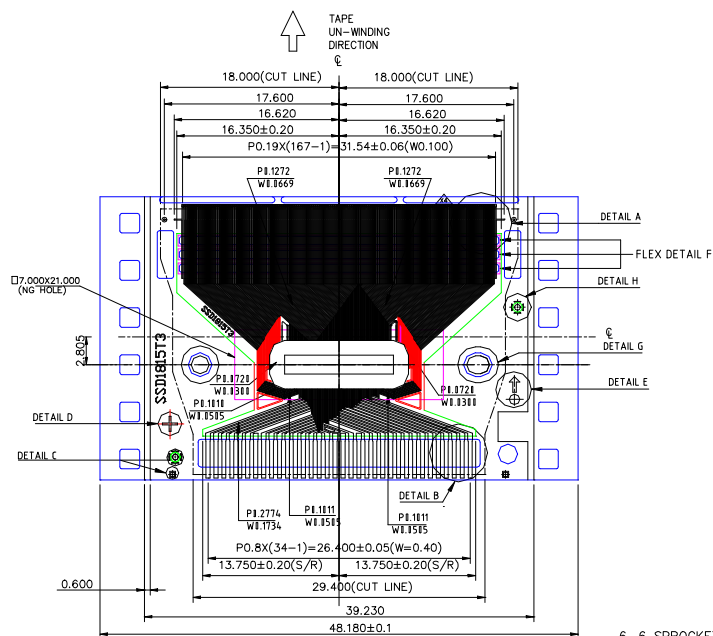
V_{DD} : CS2, $M\bar{S}$

V_{SS} : V_{SS1}

Copper View Pin Assignment



APPENDIX A3-1. SDD1815T3 TAB Drawing



COPPER VIEW

NOTE:

- NOTE:
1:GENERAL TOLERANCE $\pm 0.050\text{MM}$
2:ALL CHAMFER IS R0.20
3:MATERIAL

3:MATERIAL

PI :UPILEX-S 75um ±6 THICKNESS

FLEX COATING (PI INK) :FS-100L

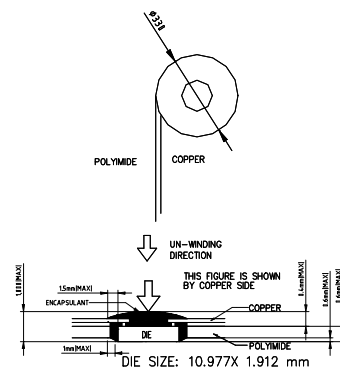
ADHESIVE : TORAY #7100 12±2um THICKNESS

SOLDER RESIST : AN

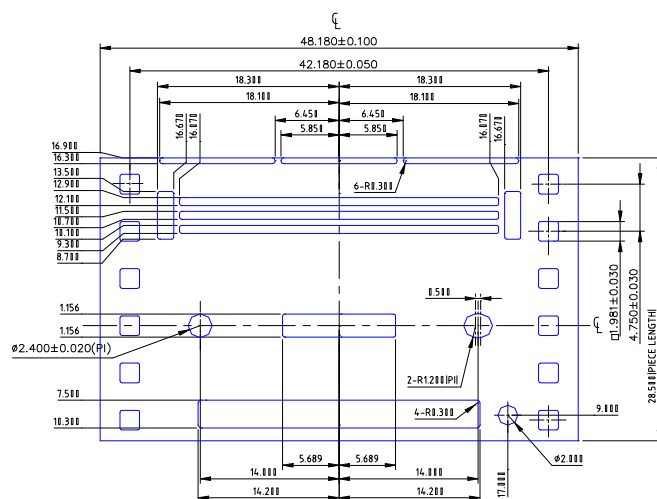
4. PLATING

SN:0.35+

4: PLATING
SN: 0.35±0.05 um
5: OPTIONAL FEATURE FOR SSL INTERNAL USE ONLY
WHICH MAY BE REPLACED BY ø2.0MM HOLE



6. 6 SPROCKET HOLES (28.5mm) FOR 1 TAPESITE, 48mm wide, 72um pitch

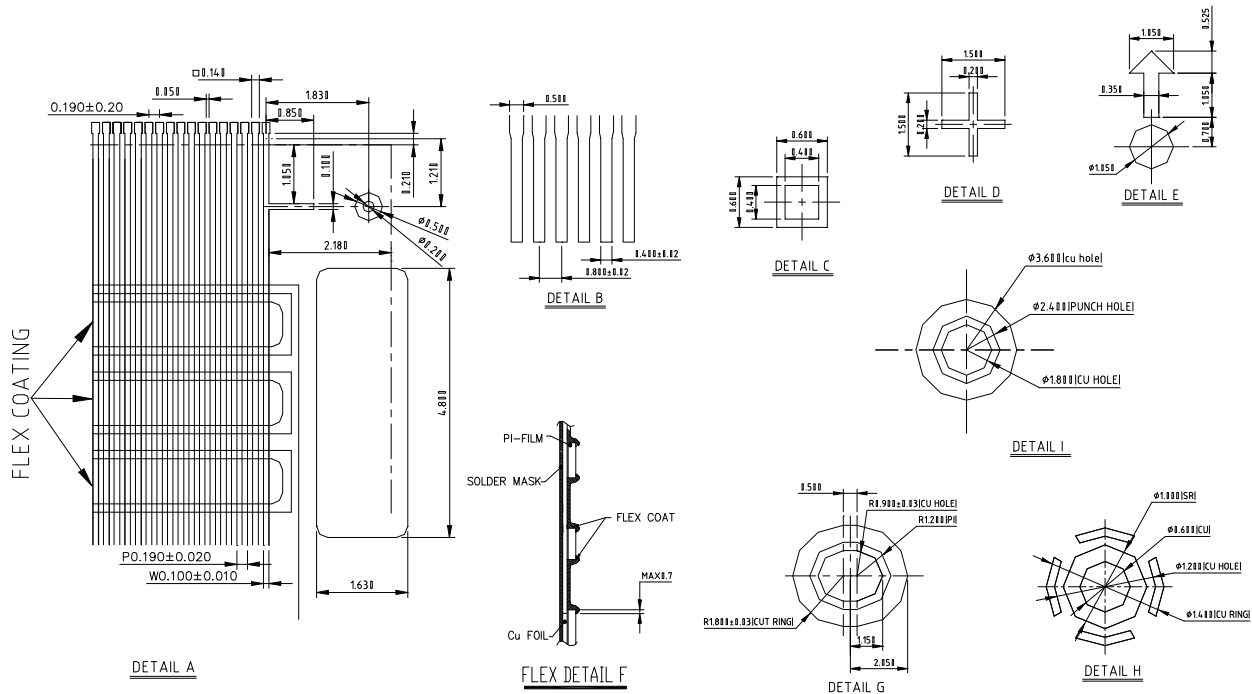


COPPER VIEW

| | | | |
|----------|----------------|---------|------------|
| MATERIAL | ULPlex-3 | PI Film | 75um±6um |
| ADHESION | YES | ✓ | Adhesive |
| | NO | | PROTECTION |
| HOLE | HOLE DIMENSION | | NUMBER |
| | 1.981X1.981 | | 12 |
| SQUARE | 32.140X1.800 | | 3 |
| | 1.630X4.800 | | 2 |
| | 11.650X0.600 | | 2 |
| | 11.780X0.600 | | 1 |
| | 28.400X2.800 | | 1 |
| | 11.378X2.312 | | 1 |
| CIRCLE | ø2.400 | | 1 |
| | ø2.800 | | 1 |
| ELLIPSE | | | 1 |

ALL OTHER CHAMFER IS R0.200
GENERAL TOLERANCE ± 0.05

APPENDIX A3-2. SDD1815T3 TAB Drawing

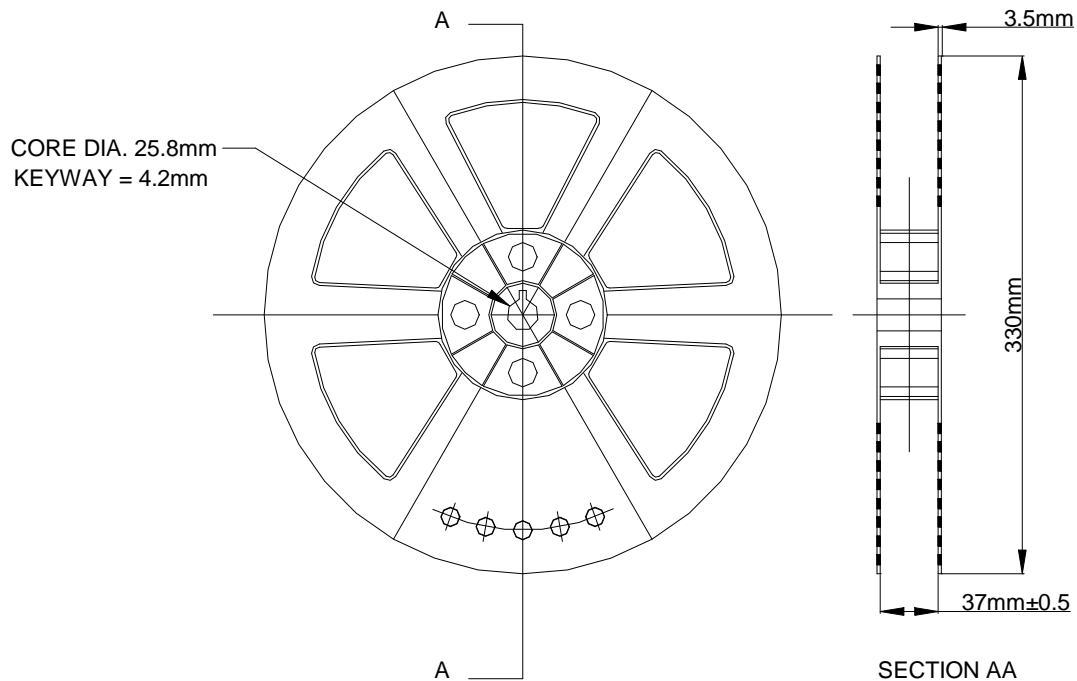


Internal Connections:
 V_{DD} : CS2, M/S, P/S, HPM, IRS
 V_{SS} : C68/80, V_{SS1}
 Floating: V_{FS}

| | | |
|-------|----|-----------|
| CL | 1 | Dummy |
| /CS1 | 2 | 199 ROW63 |
| /RES | 3 | 198 ROW62 |
| D/C | 4 | 197 ROW61 |
| R/W | 5 | 196 ROW60 |
| E/RD | 6 | . |
| DUMMY | 7 | . |
| D0 | 8 | . |
| D1 | 9 | . |
| D2 | 10 | 168 ROW33 |
| D3 | 11 | 167 ROW32 |
| D4 | 12 | 166 SEG99 |
| D5 | 13 | 165 SEG98 |
| D6 | 14 | . |
| D7 | 15 | . |
| VDD | 16 | . |
| DUMMY | 17 | . |
| DUMMY | 18 | . |
| VSS | 19 | . |
| DUMMY | 20 | . |
| VEE | 21 | . |
| C3N | 22 | 69 SEG2 |
| C1P | 23 | 68 SEG1 |
| C1P | 24 | 67 SEG0 |
| C1N | 25 | 66 ROW0 |
| C2N | 26 | 65 ROW1 |
| C2P | 27 | 64 ROW2 |
| VL2 | 28 | . |
| VL3 | 29 | . |
| VL4 | 30 | . |
| VL5 | 31 | . |
| VL6 | 32 | . |
| CLS | 33 | . |
| CLS | 34 | . |
| | 36 | ROW30 |
| | 35 | ROW31 |
| | | Dummy |

Copper View Pin Assignment

APPENDIX B0. R330 TAB Wheel Mechanical Drawing



MATERIAL: HIGH IMPACT POLYSTYRENE (HIPS)
SURFACE RESISTIVITY: 1×10^5 OHM MIN
 1×10^9 OHM MAX
TAPE LENGTH = 20m

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