Sitronix

ST7628

65K Color Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7628 is a driver & controller LSI for 65K color graphic dot-matrix liquid crystal display systems. It generates 294 Segment and 70 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit/16-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

- 294 Segment Outputs / 70 Common Outputs

Applicable Duty Ratios

- Various Partial Display
- Partial Window Moving & Data Scrolling

Gray-Scale Display

- 4FRC & 31 PWM function circuit to display 64 gray-scale display
- Support 8 color mode (Idle mode)

On-chip Display Data RAM

- Capacity: 98 x 70 x 16 =109,760 bits

Color support by Interface

- 256 color mode (via LUT)
- 4K color mode (via LUT)
- 65K color mode
- Truncated 262K color mode
- Truncated 16M color mode

Microprocessor Interface

- 8/16-bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line serial interface
- 3-line (9-bits) serial interface

On-chip Low Power Analog Circuit

- On-chip Oscillator Circuit
- On-chip Voltage Converter (x2, x3, x4, x5, x6, x7, X8) with internal booster capacitors.
- Extremely Few Outsider Components. (Required outsider components: Three Capacitors)
- On-chip Voltage Regulator
- On-chip Electronic Contrast Control Function
- Voltage Follower (LCD bias: 1/5~1/12)

Operating Voltage Range

- Supply Digital Voltage (VDD): 1.65 to 3.0V
- Supply Analog Voltage (VDD2, VDD3, VDD4, VDD5): 2.4 to 3.3V
- LCD Driving Voltage (VOP = V0 - VSS): Max to 18V

LCD Driving Voltage (OTP)

- Contrast Adjustment Value is stored in the Built-In OTP-ROM for better display quality.

LCD Driving setting suggestion

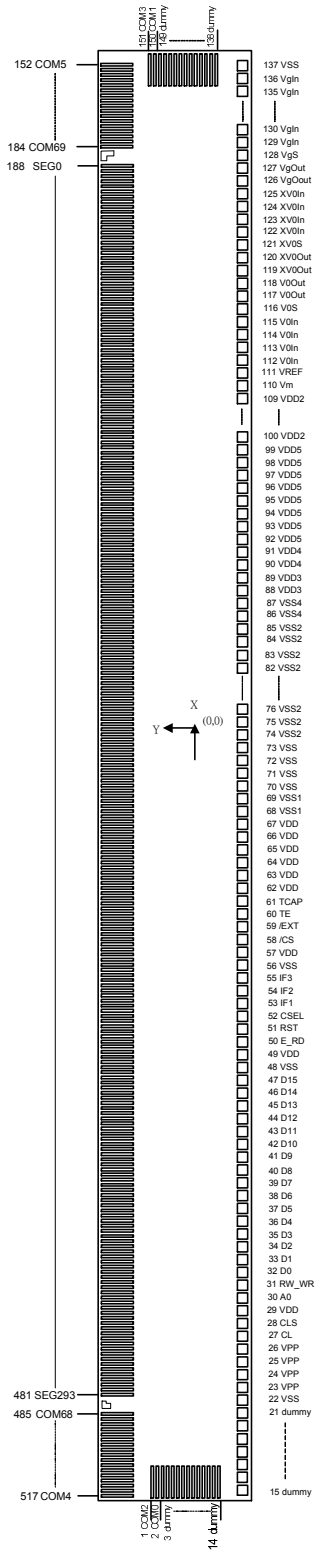
- LCD Driving Voltage (VOP = 11.72V), BIAS=1/8.

Package Type

- Application for COG

ST7628	6800 , 8080 ,4-Line , 3-Line interface	ST

3. ST7628 Pad Arrangement (COG)



Chip Size :

10070 um x 780 um

Bump Pitch :

PAD 1~2, 3~14 pitch=27um(min, com/seg)

PAD 138~149, 150~517 pitch=27um(min, com/seg)

PAD 2~3, 149~150 pitch=28.79um(min, com/seg)

PAD 15 ~ 28, 29~137 pitch=80um (I/O)

PAD 28~29 pitch = 79.72um(I/O)

Bump Size :

PAD 1 ~ 14 , PAD 138 ~ 517

Bump width=14um(min, com/seg)

Bump space=13um(min, com/seg)

Bump length=128um(min, com/seg)

Bump area=1800um^2(com/seg)

PAD 15 ~28, 29~137

Bump width=65um(I/O)

Bump space=15um(I/O)

Bump length=63um(I/O)

Bump area=4095um^2

PAD 28~29

Bump width=65um(I/O)

Bump space=14.72um(I/O)

Bump length=63um(I/O)

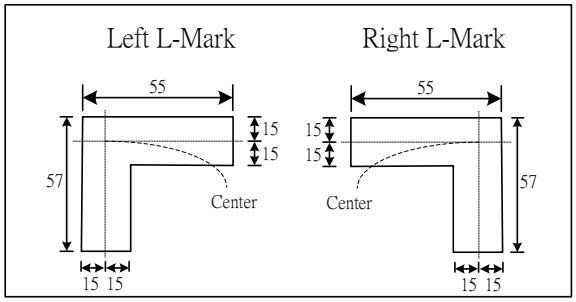
Bump area=4095um^2

Bump Height : 15 um

Chip Thickness : 400 um

Alignment mark

The center of alignment mark: see bellow Table



4. Pad Center Coordinates

PAD	IC-NAME	X	Y
1	COM2	-4917.71	116.94
2	COM0	-4917.71	89.94
3	DUMMY	-4917.71	61.15
4	DUMMY	-4917.71	34.15
5	DUMMY	-4917.71	7.15
6	DUMMY	-4917.71	-19.85
7	DUMMY	-4917.71	-46.85
8	DUMMY	-4917.71	-73.85
9	DUMMY	-4917.71	-100.85
10	DUMMY	-4917.71	-127.85
11	DUMMY	-4917.71	-154.85
12	DUMMY	-4917.71	-181.85
13	DUMMY	-4917.71	-208.85
14	DUMMY	-4917.71	-235.85
15	DUMMY	-4870.80	-299.50
16	DUMMY	-4790.80	-299.50
17	DUMMY	-4710.80	-299.50
18	DUMMY	-4630.80	-299.50
19	DUMMY	-4550.80	-299.50
20	DUMMY	-4470.80	-299.50
21	DUMMY	-4390.80	-299.50
22	VSS	-4310.80	-299.50
23	VPP	-4230.80	-299.50
24	VPP	-4150.80	-299.50
25	VPP	-4070.80	-299.50
26	VPP	-3990.80	-299.50
27	CL	-3910.80	-299.50
28	CLS	-3830.80	-299.50
29	VDD	-3751.08	-299.50
30	A0	-3671.08	-299.50
31	RW_WR	-3591.08	-299.50
32	D0	-3511.08	-299.50
33	D1	-3431.08	-299.50
34	D2	-3351.08	-299.50
35	D3	-3271.08	-299.50
36	D4	-3191.08	-299.50
37	D5	-3111.08	-299.50
38	D6	-3031.08	-299.50
39	D7	-2951.08	-299.50
40	D8	-2871.08	-299.50
41	D9	-2791.08	-299.50
42	D10	-2711.08	-299.50
43	D11	-2631.08	-299.50
44	D12	-2551.08	-299.50
45	D13	-2471.08	-299.50
46	D14	-2391.08	-299.50
47	D15	-2311.08	-299.50
48	VSS	-2231.08	-299.50
49	VDD	-2151.08	-299.50
50	E_RD	-2071.08	-299.50
51	RST	-1991.08	-299.50
52	CSEL	-1911.08	-299.50
53	IF1	-1831.08	-299.50
54	IF2	-1751.08	-299.50
55	IF3	-1671.08	-299.50
56	VSS	-1591.08	-299.50
57	VDD	-1511.08	-299.50
58	/CS	-1431.08	-299.50
59	/EXT	-1351.08	-299.50
60	TE	-1271.08	-299.50
61	TCAP	-1191.08	-299.50
62	VDD	-1111.08	-299.50
63	VDD	-1031.08	-299.50
64	VDD	-951.08	-299.50
65	VDD	-871.08	-299.50
66	VDD	-791.08	-299.50
67	VDD	-711.08	-299.50
68	VSS1	-631.08	-299.50
69	VSS1	-551.08	-299.50
70	VSS	-471.08	-299.50

71	VSS	-391.08	-299.50
72	VSS	-311.08	-299.50
73	VSS	-231.08	-299.50
74	VSS2	-151.08	-299.50
75	VSS2	-71.08	-299.50
76	VSS2	8.92	-299.50
77	VSS2	88.92	-299.50
78	VSS2	168.92	-299.50
79	VSS2	248.92	-299.50
80	VSS2	328.92	-299.50
81	VSS2	408.92	-299.50
82	VSS2	488.92	-299.50
83	VSS2	568.92	-299.50
84	VSS2	648.92	-299.50
85	VSS2	728.92	-299.50
86	VSS4	808.92	-299.50
87	VSS4	888.92	-299.50
88	VDD3	968.92	-299.50
89	VDD3	1048.92	-299.50
90	VDD4	1128.92	-299.50
91	VDD4	1208.92	-299.50
92	VDD5	1288.92	-299.50
93	VDD5	1368.92	-299.50
94	VDD5	1448.92	-299.50
95	VDD5	1528.92	-299.50
96	VDD5	1608.92	-299.50
97	VDD5	1688.92	-299.50
98	VDD5	1768.92	-299.50
99	VDD5	1848.92	-299.50
100	VDD2	1928.92	-299.50
101	VDD2	2008.92	-299.50
102	VDD2	2088.92	-299.50
103	VDD2	2168.92	-299.50
104	VDD2	2248.92	-299.50
105	VDD2	2328.92	-299.50
106	VDD2	2408.92	-299.50
107	VDD2	2488.92	-299.50

108	VDD2	2568.92	-299.50
109	VDD2	2648.92	-299.50
110	Vm	2728.92	-299.50
111	VREF	2808.92	-299.50
112	V0in	2888.92	-299.50
113	V0in	2968.92	-299.50
114	V0in	3048.92	-299.50
115	V0in	3128.92	-299.50
116	V0s	3208.92	-299.50
117	V0out	3288.92	-299.50
118	V0out	3368.92	-299.50
119	XV0out	3448.92	-299.50
120	XV0out	3528.92	-299.50
121	XV0S	3608.92	-299.50
122	XV0in	3688.92	-299.50
123	XV0in	3768.92	-299.50
124	XV0in	3848.92	-299.50
125	XV0in	3928.92	-299.50
126	Vgout	4008.92	-299.50
127	Vgout	4088.92	-299.50
128	Vgs	4168.92	-299.50
129	Vgin	4248.92	-299.50
130	Vgin	4328.92	-299.50
131	Vgin	4408.92	-299.50
132	Vgin	4488.92	-299.50
133	Vgin	4568.92	-299.50
134	Vgin	4648.92	-299.50
135	Vgin	4728.92	-299.50
136	Vgin	4808.92	-299.50
137	VSS	4888.92	-299.50
138	DUMMY	4917.71	-235.85
139	DUMMY	4917.71	-208.85
140	DUMMY	4917.71	-181.85
141	DUMMY	4917.71	-154.85
142	DUMMY	4917.71	-127.85
143	DUMMY	4917.71	-100.85
144	DUMMY	4917.71	-73.85

145	DUMMY	4917.71	-46.85
146	DUMMY	4917.71	-19.85
147	DUMMY	4917.71	7.15
148	DUMMY	4917.71	34.15
149	DUMMY	4917.71	61.15
150	COM1	4917.71	89.94
151	COM3	4917.71	116.94
152	COM5	4938.50	272.71
153	COM7	4911.50	272.71
154	COM9	4884.50	272.71
155	COM11	4857.50	272.71
156	COM13	4830.50	272.71
157	COM15	4803.50	272.71
158	COM17	4776.50	272.71
159	COM19	4749.50	272.71
160	COM21	4722.50	272.71
161	COM23	4695.50	272.71
162	COM25	4668.50	272.71
163	COM27	4641.50	272.71
164	COM29	4614.50	272.71
165	COM31	4587.50	272.71
166	COM33	4560.50	272.71
167	COM35	4533.50	272.71
168	COM37	4506.50	272.71
169	COM39	4479.50	272.71
170	COM41	4452.50	272.71
171	COM43	4425.50	272.71
172	COM45	4398.50	272.71
173	COM47	4371.50	272.71
174	COM49	4344.50	272.71
175	COM51	4317.50	272.71
176	COM53	4290.50	272.71
177	COM55	4263.50	272.71
178	COM57	4236.50	272.71
179	COM59	4209.50	272.71
180	COM61	4182.50	272.71
181	COM63	4155.50	272.71

182	COM65	4128.50	272.71
183	COM67	4101.50	272.71
184	COM69	4074.50	272.71
185	L-Mark	4038.50	325.00
186	L-Mark	4038.50	325.00
187	L-Mark	4038.50	325.00
188	SEG0	3955.50	272.71
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190	SEG2	3901.50	272.71
191	SEG3	3874.50	272.71
192	SEG4	3847.50	272.71
193	SEG5	3820.50	272.71
194	SEG6	3793.50	272.71
195	SEG7	3766.50	272.71
196	SEG8	3739.50	272.71
197	SEG9	3712.50	272.71
198	SEG10	3685.50	272.71
199	SEG11	3658.50	272.71
200	SEG12	3631.50	272.71
201	SEG13	3604.50	272.71
202	SEG14	3577.50	272.71
203	SEG15	3550.50	272.71
204	SEG16	3523.50	272.71
205	SEG17	3496.50	272.71
206	SEG18	3469.50	272.71
207	SEG19	3442.50	272.71
208	SEG20	3415.50	272.71
209	SEG21	3388.50	272.71
210	SEG22	3361.50	272.71
211	SEG23	3334.50	272.71
212	SEG24	3307.50	272.71
213	SEG25	3280.50	272.71
214	SEG26	3253.50	272.71
215	SEG27	3226.50	272.71
216	SEG28	3199.50	272.71
217	SEG29	3172.50	272.71
218	SEG30	3145.50	272.71

219	SEG31	3118.50	272.71
220	SEG32	3091.50	272.71
221	SEG33	3064.50	272.71
222	SEG34	3037.50	272.71
223	SEG35	3010.50	272.71
224	SEG36	2983.50	272.71
225	SEG37	2956.50	272.71
226	SEG38	2929.50	272.71
227	SEG39	2902.50	272.71
228	SEG40	2875.50	272.71
229	SEG41	2848.50	272.71
230	SEG42	2821.50	272.71
231	SEG43	2794.50	272.71
232	SEG44	2767.50	272.71
233	SEG45	2740.50	272.71
234	SEG46	2713.50	272.71
235	SEG47	2686.50	272.71
236	SEG48	2659.50	272.71
237	SEG49	2632.50	272.71
238	SEG50	2605.50	272.71
239	SEG51	2578.50	272.71
240	SEG52	2551.50	272.71
241	SEG53	2524.50	272.71
242	SEG54	2497.50	272.71
243	SEG55	2470.50	272.71
244	SEG56	2443.50	272.71
245	SEG57	2416.50	272.71
246	SEG58	2389.50	272.71
247	SEG59	2362.50	272.71
248	SEG60	2335.50	272.71
249	SEG61	2308.50	272.71
250	SEG62	2281.50	272.71
251	SEG63	2254.50	272.71
252	SEG64	2227.50	272.71
253	SEG65	2200.50	272.71
254	SEG66	2173.50	272.71
255	SEG67	2146.50	272.71

256	SEG68	2119.50	272.71
257	SEG69	2092.50	272.71
258	SEG70	2065.50	272.71
259	SEG71	2038.50	272.71
260	SEG72	2011.50	272.71
261	SEG73	1984.50	272.71
262	SEG74	1957.50	272.71
263	SEG75	1930.50	272.71
264	SEG76	1903.50	272.71
265	SEG77	1876.50	272.71
266	SEG78	1849.50	272.71
267	SEG79	1822.50	272.71
268	SEG80	1795.50	272.71
269	SEG81	1768.50	272.71
270	SEG82	1741.50	272.71
271	SEG83	1714.50	272.71
272	SEG84	1687.50	272.71
273	SEG85	1660.50	272.71
274	SEG86	1633.50	272.71
275	SEG87	1606.50	272.71
276	SEG88	1579.50	272.71
277	SEG89	1552.50	272.71
278	SEG90	1525.50	272.71
279	SEG91	1498.50	272.71
280	SEG92	1471.50	272.71
281	SEG93	1444.50	272.71
282	SEG94	1417.50	272.71
283	SEG95	1390.50	272.71
284	SEG96	1363.50	272.71
285	SEG97	1336.50	272.71
286	SEG98	1309.50	272.71
287	SEG99	1282.50	272.71
288	SEG100	1255.50	272.71
289	SEG101	1228.50	272.71
290	SEG102	1201.50	272.71
291	SEG103	1174.50	272.71
292	SEG104	1147.50	272.71

293	SEG105	1120.50	272.71
294	SEG106	1093.50	272.71
295	SEG107	1066.50	272.71
296	SEG108	1039.50	272.71
297	SEG109	1012.50	272.71
298	SEG110	985.50	272.71
299	SEG111	958.50	272.71
300	SEG112	931.50	272.71
301	SEG113	904.50	272.71
302	SEG114	877.50	272.71
303	SEG115	850.50	272.71
304	SEG116	823.50	272.71
305	SEG117	796.50	272.71
306	SEG118	769.50	272.71
307	SEG119	742.50	272.71
308	SEG120	715.50	272.71
309	SEG121	688.50	272.71
310	SEG122	661.50	272.71
311	SEG123	634.50	272.71
312	SEG124	607.50	272.71
313	SEG125	580.50	272.71
314	SEG126	553.50	272.71
315	SEG127	526.50	272.71
316	SEG128	499.50	272.71
317	SEG129	472.50	272.71
318	SEG130	445.50	272.71
319	SEG131	418.50	272.71
320	SEG132	391.50	272.71
321	SEG133	364.50	272.71
322	SEG134	337.50	272.71
323	SEG135	310.50	272.71
324	SEG136	283.50	272.71
325	SEG137	256.50	272.71
326	SEG138	229.50	272.71
327	SEG139	202.50	272.71
328	SEG140	175.50	272.71
329	SEG141	148.50	272.71

330	SEG142	121.50	272.71
331	SEG143	94.50	272.71
332	SEG144	67.50	272.71
333	SEG145	40.50	272.71
334	SEG146	13.50	272.71
335	SEG147	-13.50	272.71
336	SEG148	-40.50	272.71
337	SEG149	-67.50	272.71
338	SEG150	-94.50	272.71
339	SEG151	-121.50	272.71
340	SEG152	-148.50	272.71
341	SEG153	-175.50	272.71
342	SEG154	-202.50	272.71
343	SEG155	-229.50	272.71
344	SEG156	-256.50	272.71
345	SEG157	-283.50	272.71
346	SEG158	-310.50	272.71
347	SEG159	-337.50	272.71
348	SEG160	-364.50	272.71
349	SEG161	-391.50	272.71
350	SEG162	-418.50	272.71
351	SEG163	-445.50	272.71
352	SEG164	-472.50	272.71
353	SEG165	-499.50	272.71
354	SEG166	-526.50	272.71
355	SEG167	-553.50	272.71
356	SEG168	-580.50	272.71
357	SEG169	-607.50	272.71
358	SEG170	-634.50	272.71
359	SEG171	-661.50	272.71
360	SEG172	-688.50	272.71
361	SEG173	-715.50	272.71
362	SEG174	-742.50	272.71
363	SEG175	-769.50	272.71
364	SEG176	-796.50	272.71
365	SEG177	-823.50	272.71
366	SEG178	-850.50	272.71

367	SEG179	-877.50	272.71
368	SEG180	-904.50	272.71
369	SEG181	-931.50	272.71
370	SEG182	-958.50	272.71
371	SEG183	-985.50	272.71
372	SEG184	-1012.50	272.71
373	SEG185	-1039.50	272.71
374	SEG186	-1066.50	272.71
375	SEG187	-1093.50	272.71
376	SEG188	-1120.50	272.71
377	SEG189	-1147.50	272.71
378	SEG190	-1174.50	272.71
379	SEG191	-1201.50	272.71
380	SEG192	-1228.50	272.71
381	SEG193	-1255.50	272.71
382	SEG194	-1282.50	272.71
383	SEG195	-1309.50	272.71
384	SEG196	-1336.50	272.71
385	SEG197	-1363.50	272.71
386	SEG198	-1390.50	272.71
387	SEG199	-1417.50	272.71
388	SEG200	-1444.50	272.71
389	SEG201	-1471.50	272.71
390	SEG202	-1498.50	272.71
391	SEG203	-1525.50	272.71
392	SEG204	-1552.50	272.71
393	SEG205	-1579.50	272.71
394	SEG206	-1606.50	272.71
395	SEG207	-1633.50	272.71
396	SEG208	-1660.50	272.71
397	SEG209	-1687.50	272.71
398	SEG210	-1714.50	272.71
399	SEG211	-1741.50	272.71
400	SEG212	-1768.50	272.71
401	SEG213	-1795.50	272.71
402	SEG214	-1822.50	272.71
403	SEG215	-1849.50	272.71

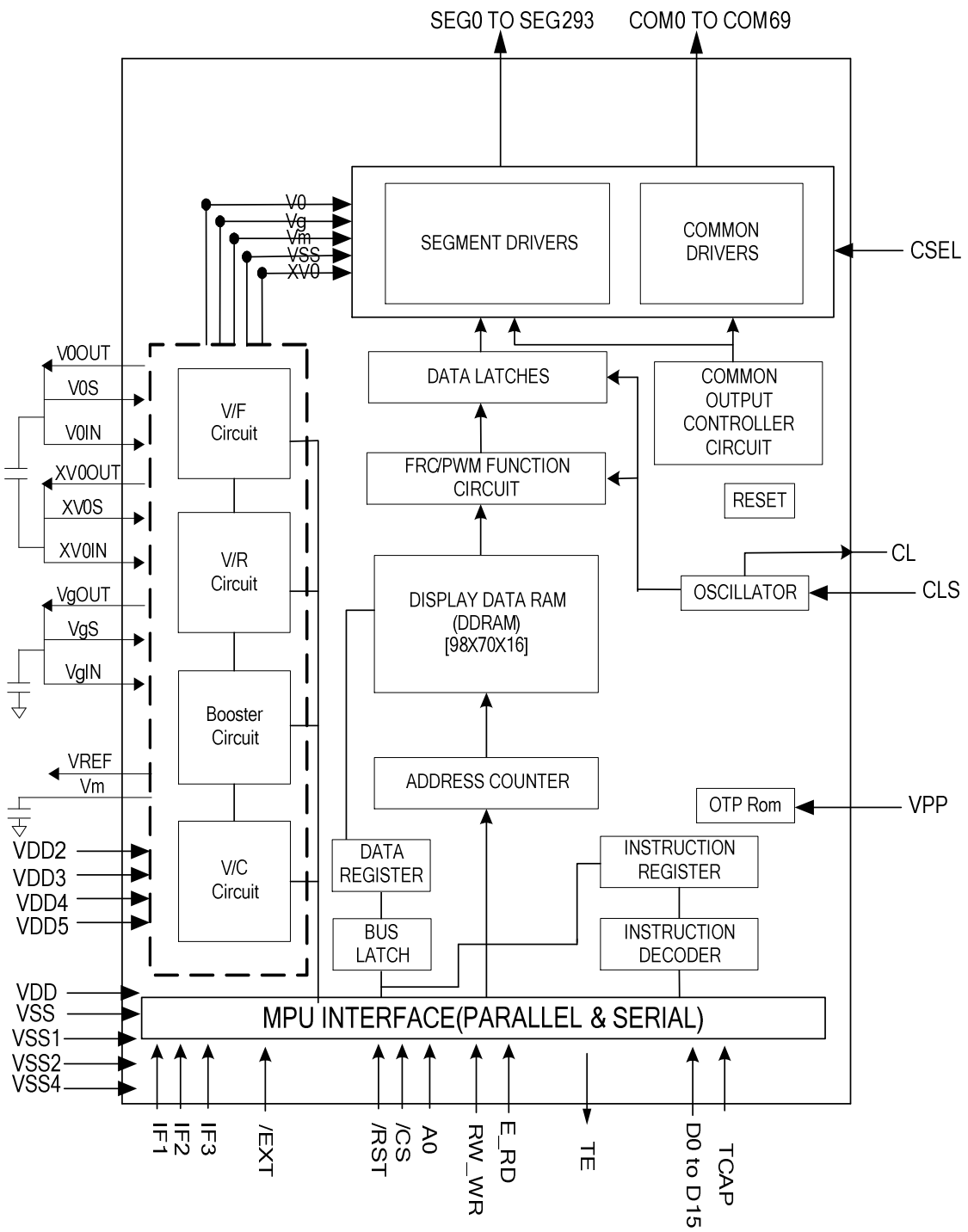
404	SEG216	-1876.50	272.71
405	SEG217	-1903.50	272.71
406	SEG218	-1930.50	272.71
407	SEG219	-1957.50	272.71
408	SEG220	-1984.50	272.71
409	SEG221	-2011.50	272.71
410	SEG222	-2038.50	272.71
411	SEG223	-2065.50	272.71
412	SEG224	-2092.50	272.71
413	SEG225	-2119.50	272.71
414	SEG226	-2146.50	272.71
415	SEG227	-2173.50	272.71
416	SEG228	-2200.50	272.71
417	SEG229	-2227.50	272.71
418	SEG230	-2254.50	272.71
419	SEG231	-2281.50	272.71
420	SEG232	-2308.50	272.71
421	SEG233	-2335.50	272.71
422	SEG234	-2362.50	272.71
423	SEG235	-2389.50	272.71
424	SEG236	-2416.50	272.71
425	SEG237	-2443.50	272.71
426	SEG238	-2470.50	272.71
427	SEG239	-2497.50	272.71
428	SEG240	-2524.50	272.71
429	SEG241	-2551.50	272.71
430	SEG242	-2578.50	272.71
431	SEG243	-2605.50	272.71
432	SEG244	-2632.50	272.71
433	SEG245	-2659.50	272.71
434	SEG246	-2686.50	272.71
435	SEG247	-2713.50	272.71
436	SEG248	-2740.50	272.71
437	SEG249	-2767.50	272.71
438	SEG250	-2794.50	272.71
439	SEG251	-2821.50	272.71
440	SEG252	-2848.50	272.71

441	SEG253	-2875.50	272.71
442	SEG254	-2902.50	272.71
443	SEG255	-2929.50	272.71
444	SEG256	-2956.50	272.71
445	SEG257	-2983.50	272.71
446	SEG258	-3010.50	272.71
447	SEG259	-3037.50	272.71
448	SEG260	-3064.50	272.71
449	SEG261	-3091.50	272.71
450	SEG262	-3118.50	272.71
451	SEG263	-3145.50	272.71
452	SEG264	-3172.50	272.71
453	SEG265	-3199.50	272.71
454	SEG266	-3226.50	272.71
455	SEG267	-3253.50	272.71
456	SEG268	-3280.50	272.71
457	SEG269	-3307.50	272.71
458	SEG270	-3334.50	272.71
459	SEG271	-3361.50	272.71
460	SEG272	-3388.50	272.71
461	SEG273	-3415.50	272.71
462	SEG274	-3442.50	272.71
463	SEG275	-3469.50	272.71
464	SEG276	-3496.50	272.71
465	SEG277	-3523.50	272.71
466	SEG278	-3550.50	272.71
467	SEG279	-3577.50	272.71
468	SEG280	-3604.50	272.71
469	SEG281	-3631.50	272.71
470	SEG282	-3658.50	272.71
471	SEG283	-3685.50	272.71
472	SEG284	-3712.50	272.71
473	SEG285	-3739.50	272.71
474	SEG286	-3766.50	272.71
475	SEG287	-3793.50	272.71
476	SEG288	-3820.50	272.71
477	SEG289	-3847.50	272.71

478	SEG290	-3874.50	272.71
479	SEG291	-3901.50	272.71
480	SEG292	-3928.50	272.71
481	SEG293	-3955.50	272.71
482	L-Mark	-4038.50	325.00
483	L-Mark	-4038.50	325.00
484	L-Mark	-4038.50	325.00
485	COM68	-4074.50	272.71
486	COM66	-4101.50	272.71
487	COM64	-4128.50	272.71
488	COM62	-4155.50	272.71
489	COM60	-4182.50	272.71
490	COM58	-4209.50	272.71
491	COM56	-4236.50	272.71
492	COM54	-4263.50	272.71
493	COM52	-4290.50	272.71
494	COM50	-4317.50	272.71
495	COM48	-4344.50	272.71
496	COM46	-4371.50	272.71
497	COM44	-4398.50	272.71
498	COM42	-4425.50	272.71
499	COM40	-4452.50	272.71
500	COM38	-4479.50	272.71
501	COM36	-4506.50	272.71
502	COM34	-4533.50	272.71
503	COM32	-4560.50	272.71
504	COM30	-4587.50	272.71
505	COM28	-4614.50	272.71
506	COM26	-4641.50	272.71
507	COM24	-4668.50	272.71
508	COM22	-4695.50	272.71
509	COM20	-4722.50	272.71
510	COM18	-4749.50	272.71
511	COM16	-4776.50	272.71
512	COM14	-4803.50	272.71
513	COM12	-4830.50	272.71
514	COM10	-4857.50	272.71

515	COM8	-4884.50	272.71
516	COM6	-4911.50	272.71
517	COM4	-4938.50	272.71

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 POWER SUPPLY

Name	I/O	Description
VDD	Supply	Power supply for logic circuit (Digital VDD 1.65V~3.0V)
VDD2	Supply	Power supply for Booster Circuit (Analog VDD 2.4V~3.3V)
VDD3	Supply	Power supply for LCD. (Analog VDD 2.4V~3.3V)
VDD4	Supply	Power supply for LCD. (Analog VDD 2.4V~3.3V)
VDD5	Supply	Power supply for LCD. (Analog VDD 2.4V~3.3V)
VSS	Supply	Ground for logic circuit. Ground system should be connected together.
VSS1	Supply	Ground for OSC circuit. Ground system should be connected together.
VSS2	Supply	Ground for Booster Circuit. Ground system should be connected together.
VSS4	Supply	Ground for LCD. Ground system should be connected together.

6.2 LCD Power Supply Pins

Name	I/O	Description
$V0_{OUT}$ $V0_{IN}$ $V0_S$	I/O	Positive LCD driver supply voltages. $V0_{OUT}$ is the output voltage of V0 generated by ST7628. $V0_{IN}$ is the input pin of power supply to generate V0 voltage for LCD. $V0_S$ is the input pin of power supply to sense the V0 voltage. $V0_{OUT}$ 、$V0_{IN}$ & $V0_S$ should be connected together.
$XV0_{OUT}$ $XV0_{IN}$ $XV0_S$	I/O	Negative LCD driver supply voltages. $XV0_{OUT}$ is the output voltage of XV0 generated by ST7628. $XV0_{IN}$ is the input pin of power supply to generate XV0 voltage for LCD. $XV0_S$ is the input pin of power supply to sense the XV0 voltage. $XV0_{OUT}$ 、$XV0_{IN}$ & $XV0_S$ should be connected together.
Vg_{OUT} Vg_{IN} Vg_S Vm	I/O	Bias LCD driver supply voltages. Vg_{OUT} is the output voltage of Vg generated by ST7628. Vg_{IN} is the input pin of power supply to generate Vg voltage for LCD. Vg_S is the input pin of power supply to sense the Vg voltage. Vg_{OUT} 、Vg_{IN} & Vg_S should be connected together. Vm is the I/O pin of LCD bias supply voltage Voltages should have the following relationship; $V0 \geqq Vg \geqq Vm \geqq VSS \geqq XV0$ 0.7V< Vm< VDDA-0.7V and 1.8V < Vg < 2xVDDA. When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias. **LCD bias** | **Vg** | **Vm** **1/N bias** | (2/N) x V0 | (1/N) x V0 NOTE: N = 5 to 12

6.3 SYSTEM CONTROL

Name	I/O	Description
CLS	I	When using internal clock oscillator, connect CLS to VDD. When using external clock oscillator, connect CLS to VSS.
CL	I/O	When using internal clock oscillator, it's oscillator output. When using external clock oscillator, it is clock input.
CSEL	I	This PIN should connect to VDD.
TCAP	I/O	Test pin. Left it opens.
VREF	O	Reference voltage output for monitor only. Left it opened.
VPP	I	When writing OTP, it needs external power supply voltage 7.5V~7.75V (>4mA) input to write successfully.

6.4 MICROPROCESSOR INTERFACE

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RST</td><td>I</td><td>Reset input pin, when RST is “L”, initialization is executed.</td></tr>
<tr><td>IF[3:1]</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><th>IF3</th><th>IF2</th><th>IF1</th><th>MPU interface type</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>80 series 16-bit parallel</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>68 series 16-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>68 series 8-bit parallel</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>8-bit serial (4 line)</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>9-bit serial (3 line)</td></tr>
</table>
Note:
1. When fixing IF2=H & IF1=L, IF3 can be defined as P/SX pin (parallel/Serial selection pin).
IF3=H: Parallel interface(80 8-bit); IF3=L:Serial interface(3-line)
2. Refer to Table 7.1.1. for detail interface connections.</td></tr>
<tr><td>/CS</td><td>I</td><td>Chip select input pins
Data / Instruction I/O is enabled only when /CS is "L". When chip select is non-active, D0 to D15 become high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
A0 = "H": D0 to D15 or SI are display data
A0 = "L": D0 to D15 or SI are control command
In 3-line/4-line interface this pad will be used for SCL function</td></tr>
</table>

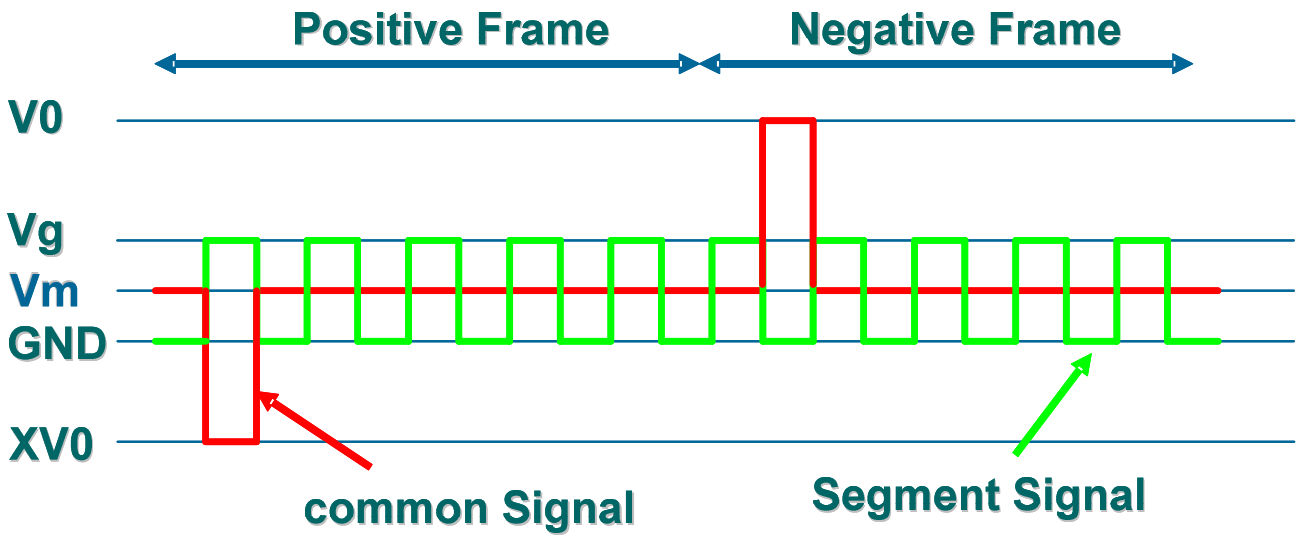
<table>
<tr><td>RW_WR</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>RW</td><td>Read / Write control input pin
RW = “H” : read
RW = “L” : write</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D15 are latched at the rising edge of the /WR signal.</td></tr>
</table>
When in the serial interface, connect it to VSS or VDD.</td></tr>
<tr><td>E_RD</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Enable clock pin:
Write status: The data on D0 to D15 are latched at the falling edge of the E signal.
Read status: The data on D0 to D15 are latched at the rising edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
The data on D0 to D15 are latched at the falling edge of the /WR signal.</td></tr>
</table>
When in the serial interface, connect it to VSS or VDD.</td></tr>
<tr><td>D15 to D0</td><td>I/O</td><td>They connect to the standard 8-bit or 16 bit MPU bus via the 8/16 –bit bi-directional bus.
When the following interface is selected and the /CS pin is high, the following pins become high impedance.
1. In 8-bit parallel: D15-D8 pins are in the state of high impedance should connect to VDD.
2. In 3-line/4-line interface D0 pad will be used for SI function
3. In 4-line interface D1 pad will be used for A0 function
4. In Serial interface: Unused pins are in the state of high impedance should connect to VDD.</td></tr>
<tr><td>SI</td><td>I</td><td>SI is used to input serial data when the serial interface is selected.(3 line and 4 line)
It is used by “D0” pad , See Table 7.1.1</td></tr>
<tr><td>SCL</td><td>I</td><td>SCL is used to input serial clock when the serial interface is selected.
The data is converted in the rising edge. (3 line and 4 line)
It is used by “A0” pad , See Table 7.1.1</td></tr>
<tr><td>TE</td><td>O</td><td>Tearing effect output.</td></tr>
<tr><td>/EXT</td><td>I</td><td>Instruction selection Pin. There is a pull-high resistor between /EXT & VDD in ST7628.
When using normal instruction table, please let it open.
When using extension instruction table, please add an external VSS on /EXT.</td></tr>
</table>

Note: 1. All of the microprocessor interface pin should not be floating on any operations.

2. Unused pins should connect to VDD(supply digital voltage)

6.5 LCD DRIVER OUTPUTS

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG293</td><td>O</td><td>LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">M (Internal)</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>Vg</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>Vg</td></tr>
<tr><td>L</td><td>H</td><td>VSS</td><td>Vg</td></tr>
<tr><td>L</td><td>L</td><td>Vg</td><td>VSS</td></tr>
<tr><td colspan="2">Sleep-In mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM69</td><td>O</td><td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>M (Internal)</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>H</td><td>XV0</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>Vm</td></tr>
<tr><td>L</td><td>L</td><td>Vm</td></tr>
<tr><td colspan="2">Sleep-In mode</td><td>VSS</td></tr>
</table></td></tr>
</table>



ST7628 I/O PIN ITO Resister Limitation

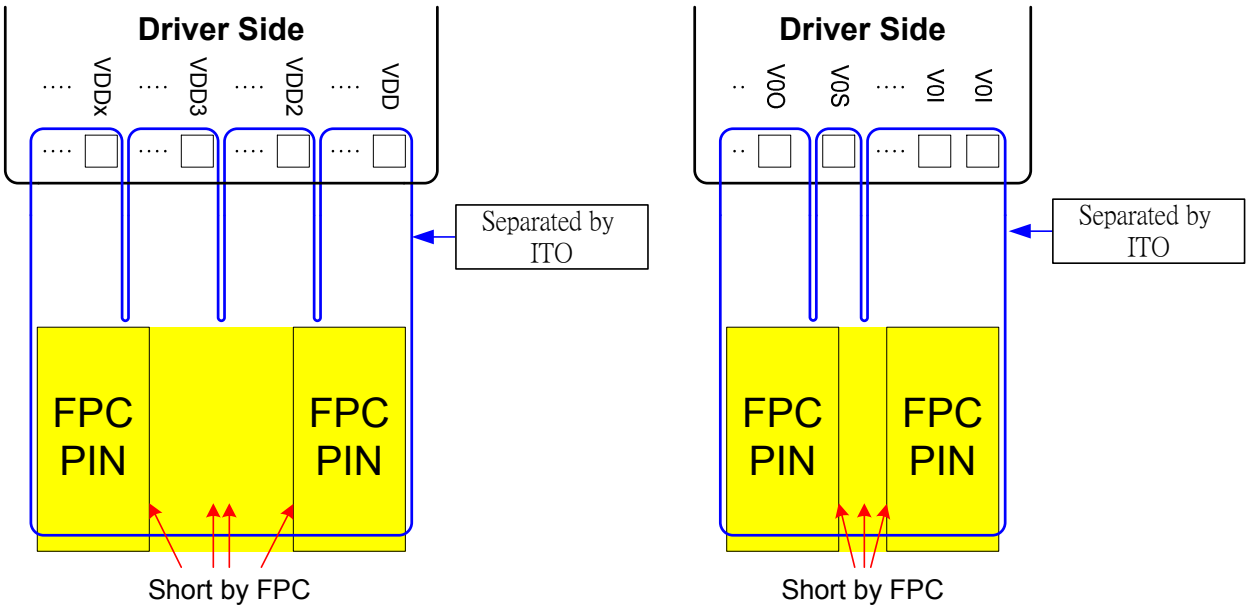
Pin Name	ITO Resister
VDD, VDD2~VDD5, VSS,VSS1,VSS2,VSS4, SI (In serial interface is D0)	<100Ω
$V0_{IN}$, $V0_{OUT}$, $V0_S$,$XV0_{IN}$, $XV0_{OUT}$,$XV0_S$, Vg_{IN}, Vg_{OUT} ,Vg_S ,Vm	<300Ω
VPP	<100Ω
A0, E_RD, RW_WR, /CS, D0(parallel interface), D2…D15, (SCL), TE	<1KΩ
RST	<10KΩ
IF[3:1], CLS, CSEL, /EXT	<1KΩ
TCAP, CL, VREF	Floating

NOTE:

1. Make sure that the ITO resistance of COM0 ~ COM69 is equal, and so is it of SEG0 ~ SEG293. These Limitations include the bottleneck of ITO layout.

2. To avoid the noise in different power system affect other power system, please separate different power source on ITO layout.

3. The V0, XV0 and Vg power circuits have output pins, input pins and a sensor input. To avoid the power noise affects the sensor of the power circuits. The trace should be separated by ITO and should be connected together by FPC.



7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

/CS pin is chip selection. The ST7628 is active when /CS=L. In serial interface mode, the internal shift register and the counter are reset when /CS=H.

7.1.1 Selecting Parallel / Serial Interface

ST7628 has six types of interface with an MPU, which are two serial and four parallel interfaces. This parallel or serial interface is determined by IF pin as shown in Table 7.1.1.

Table 7.1.1Parallel / Serial Interface Mode

I/F Mode			I/F Description	Pin Assignment							
IF3	IF2	IF1		/CS	A0	E_RD	RW_WR	D15 to D8	Used Data Bus	D1	D0
H	H	H	80 serial 16-bit parallel	/CS	A0	/RD	/WR	D15 ~ D8	D7 ~ D2	D1	D0
H	H	L	80 serial 8-bit parallel	/CS	A0	/RD	/WR	--	D7 ~ D2	D1	D0
H	L	H	68 serial 16-bit parallel	/CS	A0	E	R/W	D15 ~ D8	D7 ~ D2	D1	D0
H	L	L	68 serial 8-bit parallel	/CS	A0	E	R/W	--	D7 ~ D2	D1	D0
L	H	H	8-bit SPI mode (4 line)	/CS	SCL	--	--	--	--	A0	SI
L	H	L	9-bit SPI mode (3 line)	/CS	SCL	--	--	--	--	--	SI

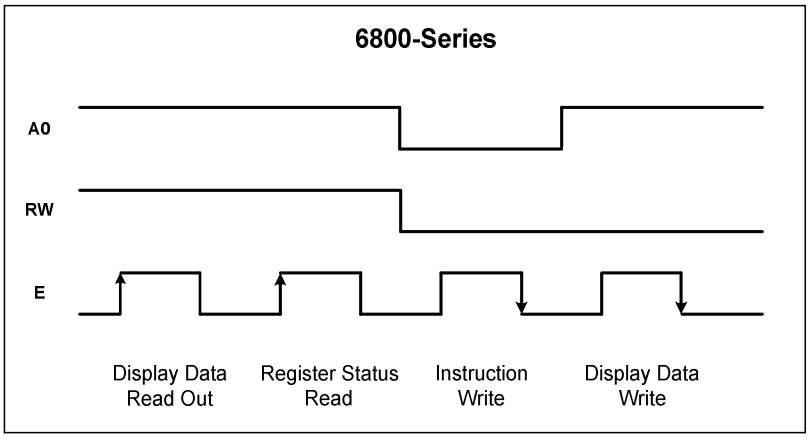
NOTE: When these pins are set to any other combination, A0, E_RD and RW_WR inputs are disabled and D0 to D15 are to be high impedance.

7.1.2 8-bit or 16-bit Parallel Interface

The ST7628 identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (W/R) signals, as shown in Table 7.1.2.

Table 7.1.2Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	R/W	E	/WR	/RD	
H	H	↑	H	↓	Register status read
H	H	↑	H	↓	Display data read out
L	L	↓	↑	H	Instruction write
H	L	↓	↑	H	Display data write



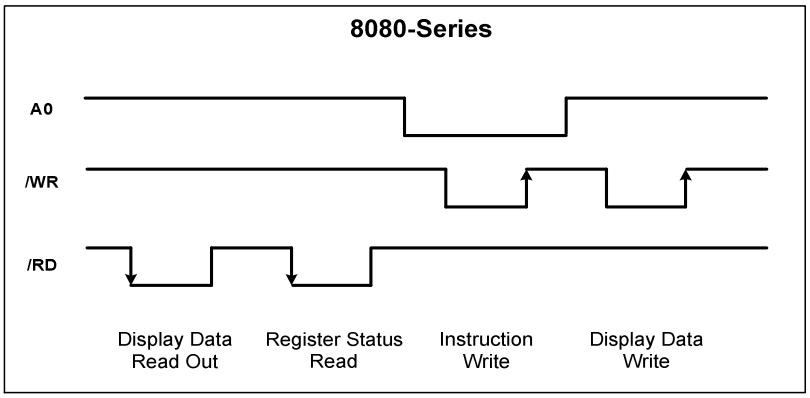


Figure 7.1Parallel Data Transfer Example Chart

Relation between Data Bus and Gradation Data

The interface of ST7628 supports 256 color display, 4096 color display, 65K color display, truncated 262K color display, and truncated 16M color display.

When using 256, 4096, 65K, 262K, and 16M color display; you can specify color for each of R, G, B using the palette function.

Use the command for switching between these modes.

(1) 256 color input mode

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: RRRGGGBB 1st writes

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st -write operation finishes.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: XXXXXXXXRRRGGGBB 1st writes

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes. “X” are ignored dummy bits.

(2) 4096-color display

(1-1) Type A 4096 color display

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: RRRRGGGG 1st writes

D7, D6, D5, D4, D3, D2, D1, D0: BBBBRRRR 2nd writes

D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB 3rd writes

There are 3 write operations for 2 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes, and 2nd pixel data is written in the display data RAM when 3rd–write operation finishes.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRGGGGBBBBXXXX

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes. “X” are ignored dummy bits.

(1-2) Type B 4096 color display

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRR 1st writes

D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB 2nd writes

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes. “X” are ignored dummy bits.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRRGGGGBBBB

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes. “X” are ignored dummy bits.

(3) 65K color input mode

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGG 1st writes

D7, D6, D5, D4, D3, D2, D1, D0: GGGBBBBB 2nd writes

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGGGGGBBBBB 1st writes

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes.

(4) Truncated 262K color input mode

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXX 1st writes

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGXX 2nd writes

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXX 3rd writes

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

"X" is dummy bit, and it is ignored for display.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXXGGGGGGXX 1st writes

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXXXXXXXXXXXX 2nd writes

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

(5) Truncated 16M color input mode

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRR 1st writes

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGGG 2nd writes

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBB 3rd writes

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRRGGGGGGGG 1st writes

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBBXXXXXXXX 2nd writes

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

7.1.3 8- and 9-bit Serial Interface

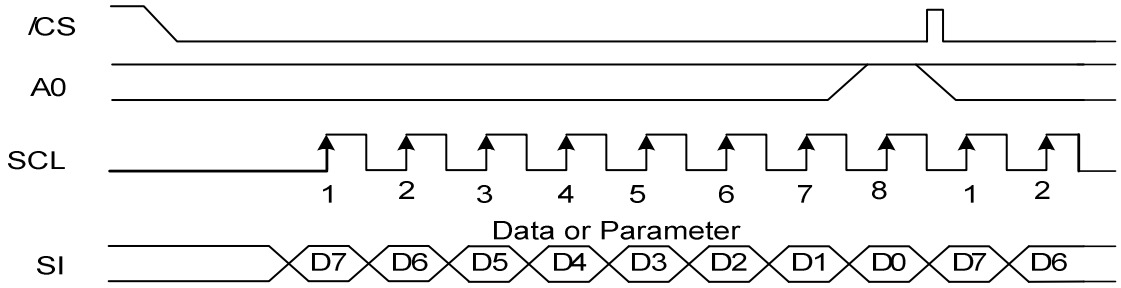
The 8-bit serial interface uses four pins /CS, SI, SCL, and A0 to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins /CS, SI and SCL for the same purpose.

Data read is not available in the serial interface. Data entered must be 8 bits for each time.

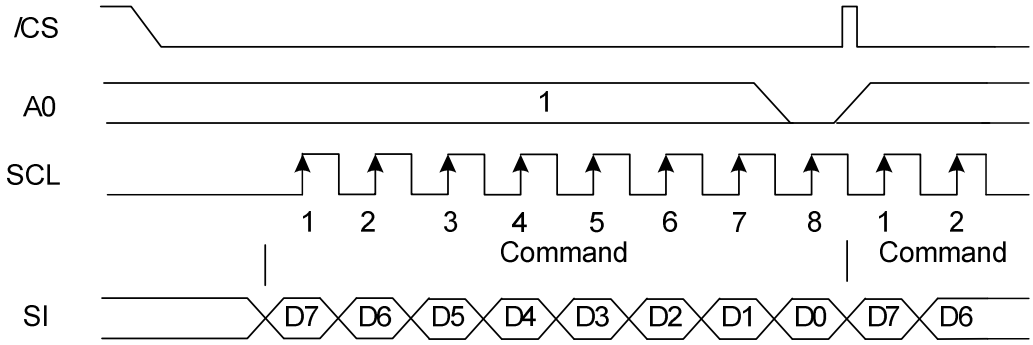
The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4-line)

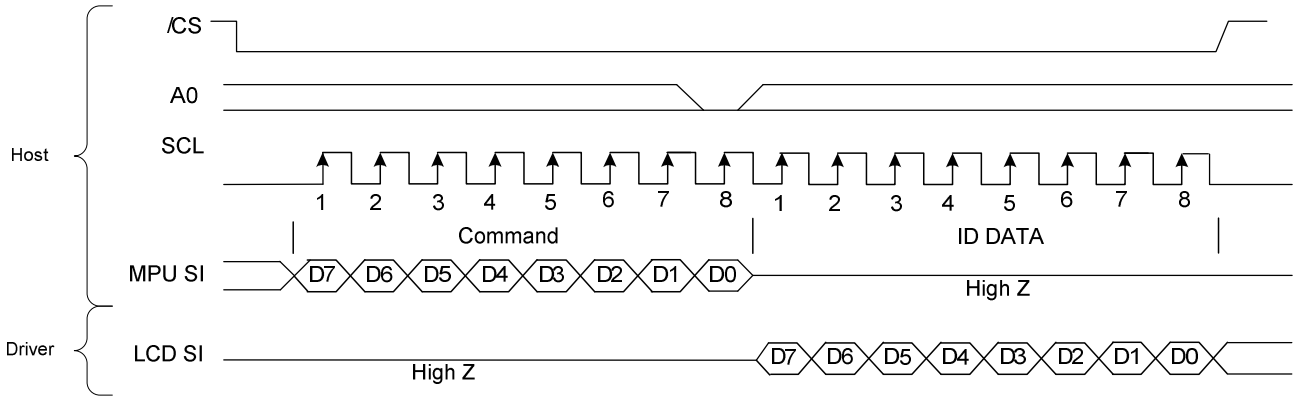
When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.



When entering command: A0= LOW at the rising edge of the 8th SCL

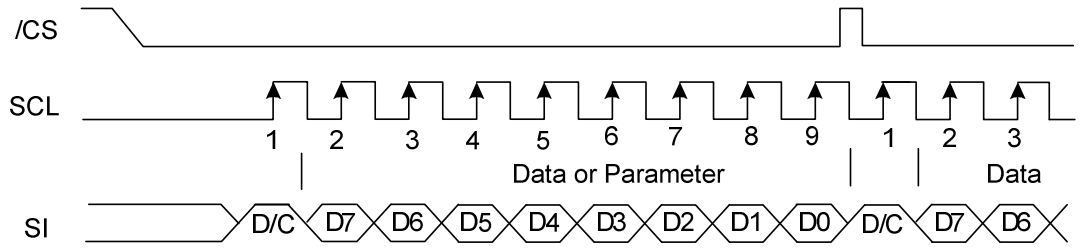


When entering reading command:

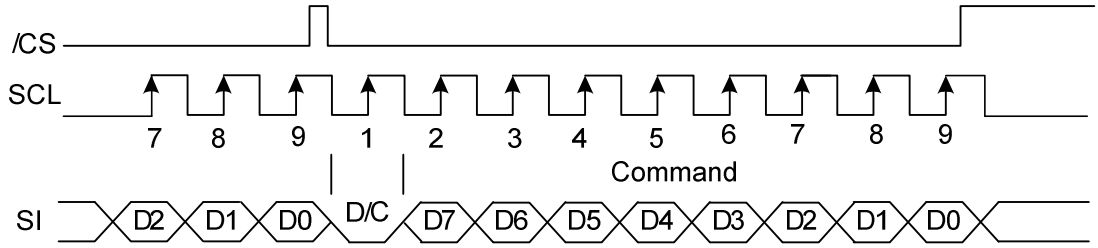


(2) 9-bit serial interface (3-line)

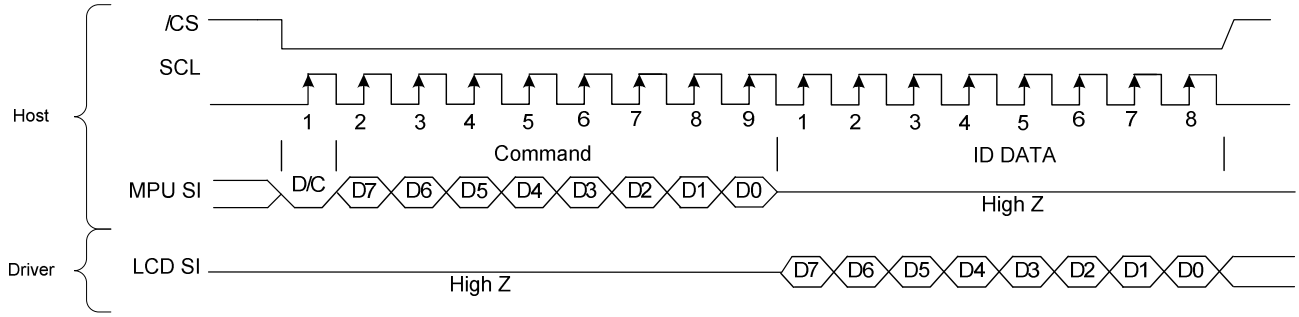
When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.



When entering command: SI= LOW at the rising edge of the 1st SCL.



When entering reading command:



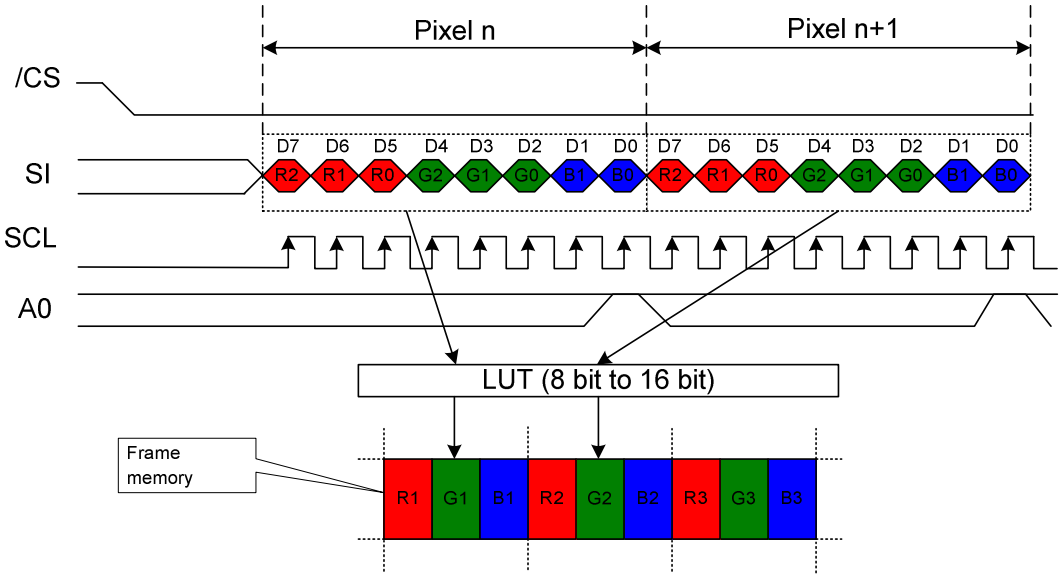
- If /CS is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set /CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register
- When executing the command RAMWR, set /CS to HIGH after writing the last address. The internal shift register and the counter are reset when /CS =H.

7.1.4 8-bit and 9-bit Serial Interface Data Color Coding

8-bit serial interface (4-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

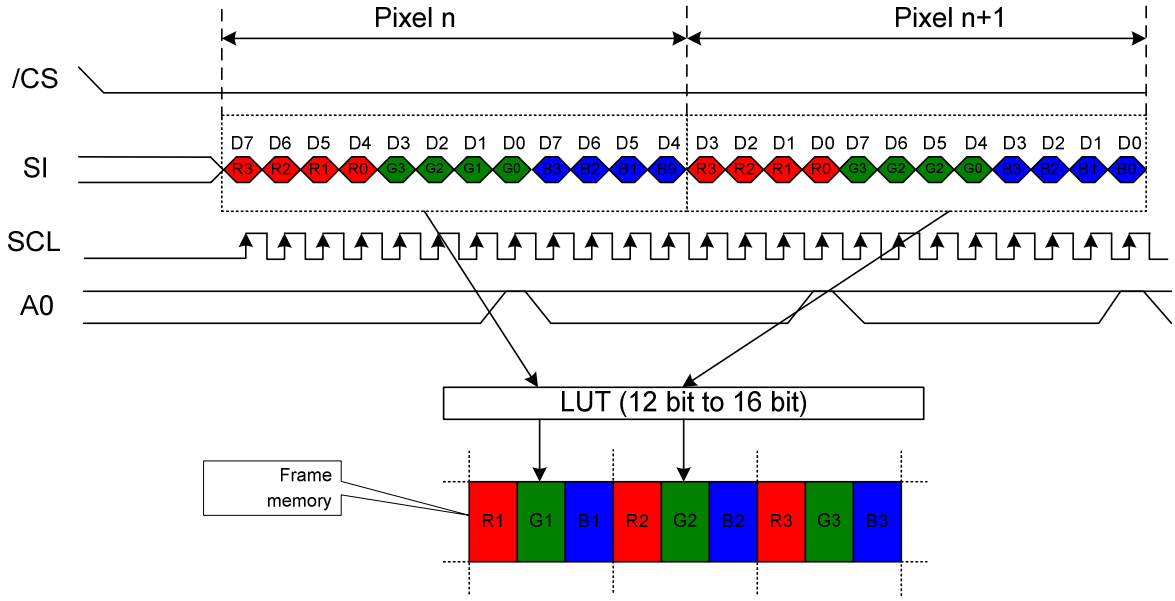
There is 1 pixel (= 3 sub-pixels) per byte.



Note: R2, G2, B1 are the most significant bits and R0, G0, B0 are the least significant bits.

(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type A

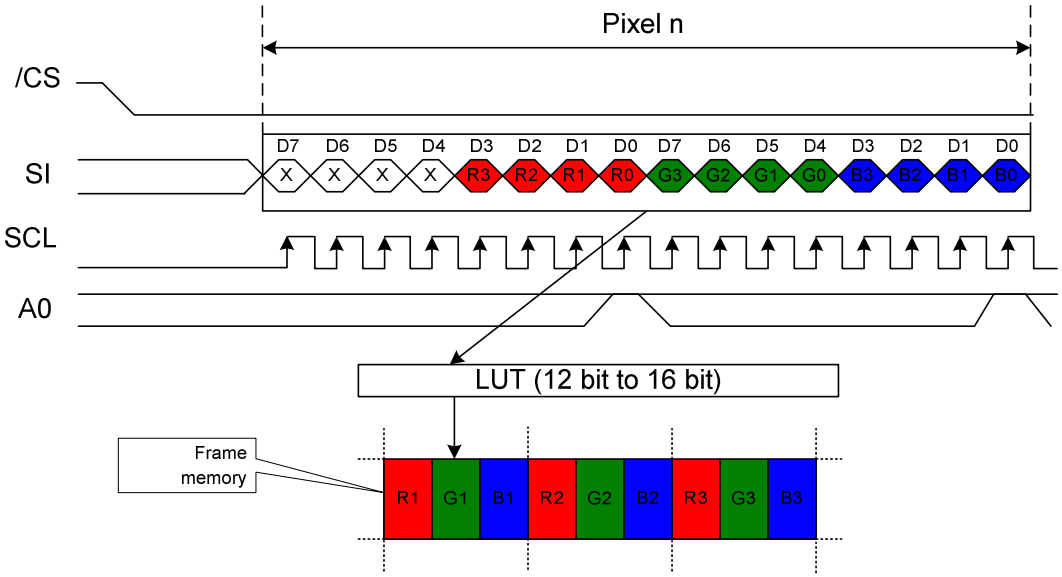
There are 2 pixel (= 3 sub-pixels) per 3 byte.



Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(3) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type B

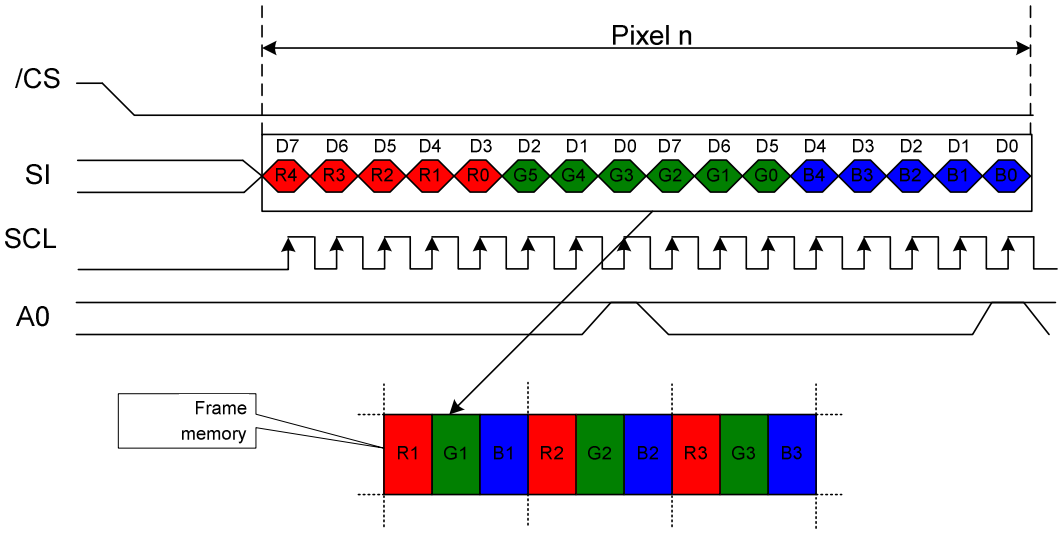
There is 1 pixel (= 3 sub-pixels) per 2 bytes.



Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(4) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

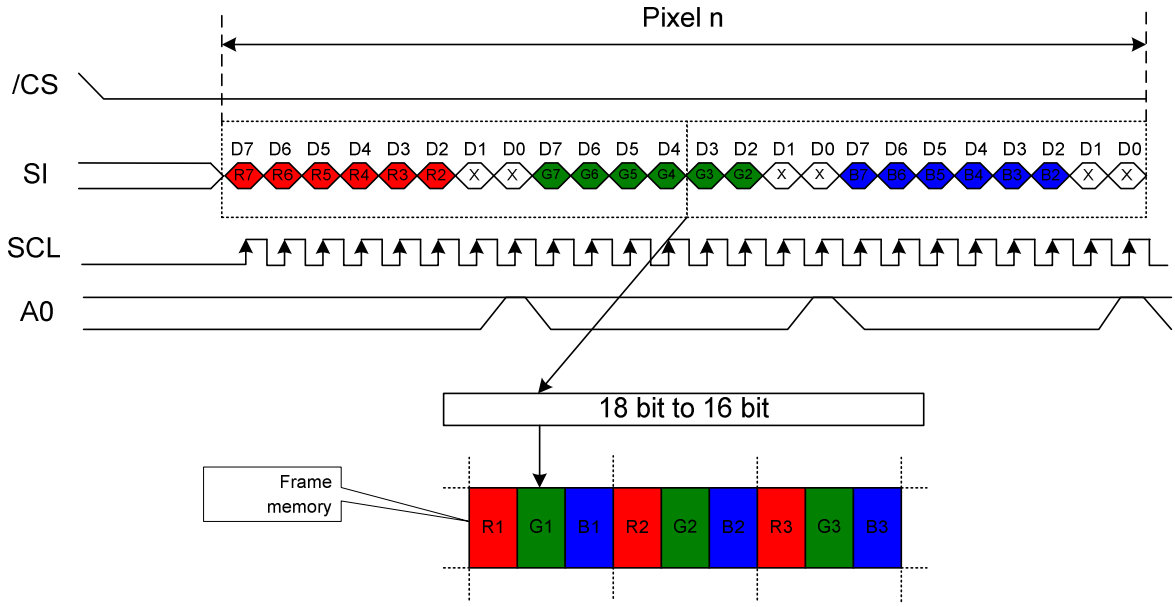
There is 1 pixel (= 3 sub-pixels) per 2 byte.



Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

(5) R 6-bit, G 6-bit, B 6-bit, 262k colors

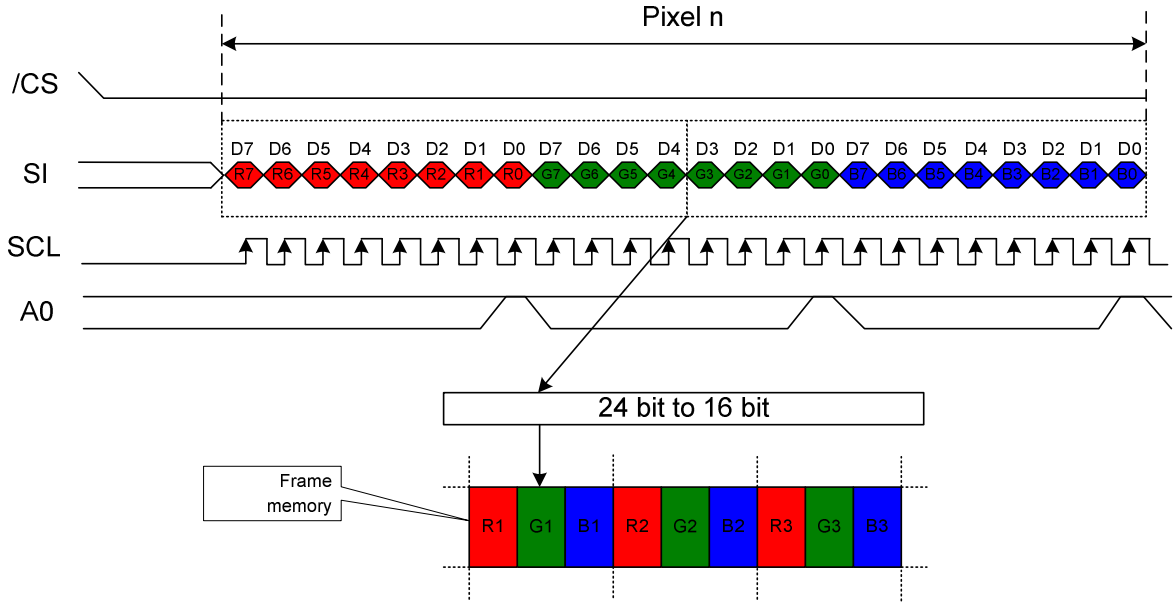
There is 1 pixel (= 3 sub-pixels) per 3 byte.



Note: R7, G7, B7 are the most significant bits and R2, G2, B2 are the least significant bits.

(6) R 8-bit, G 8-bit, B 8-bit, 16M colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.

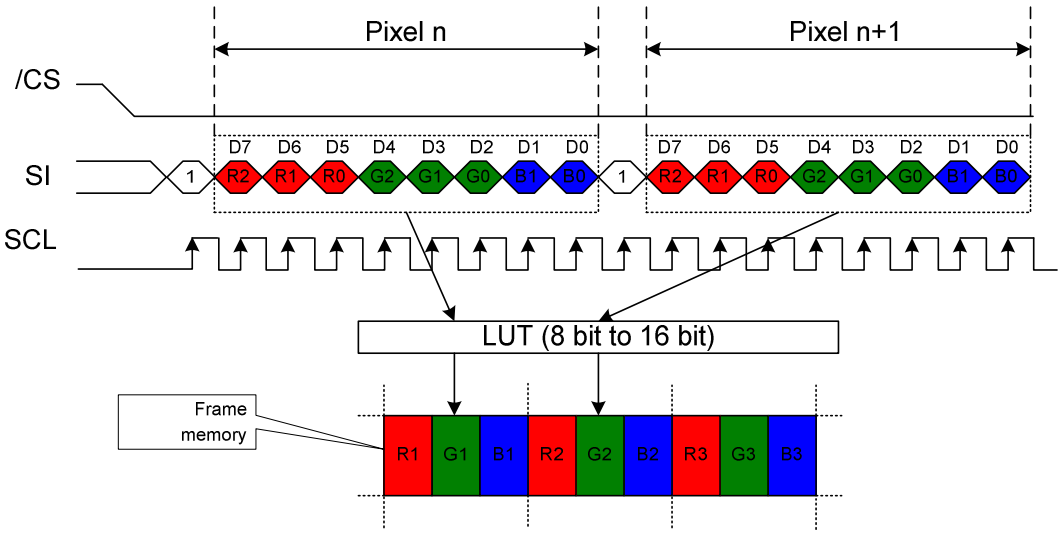


Note: R7, G7, B7 are the most significant bits and R0, G0, B0 are the least significant bits.

9-bit serial interface (3-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

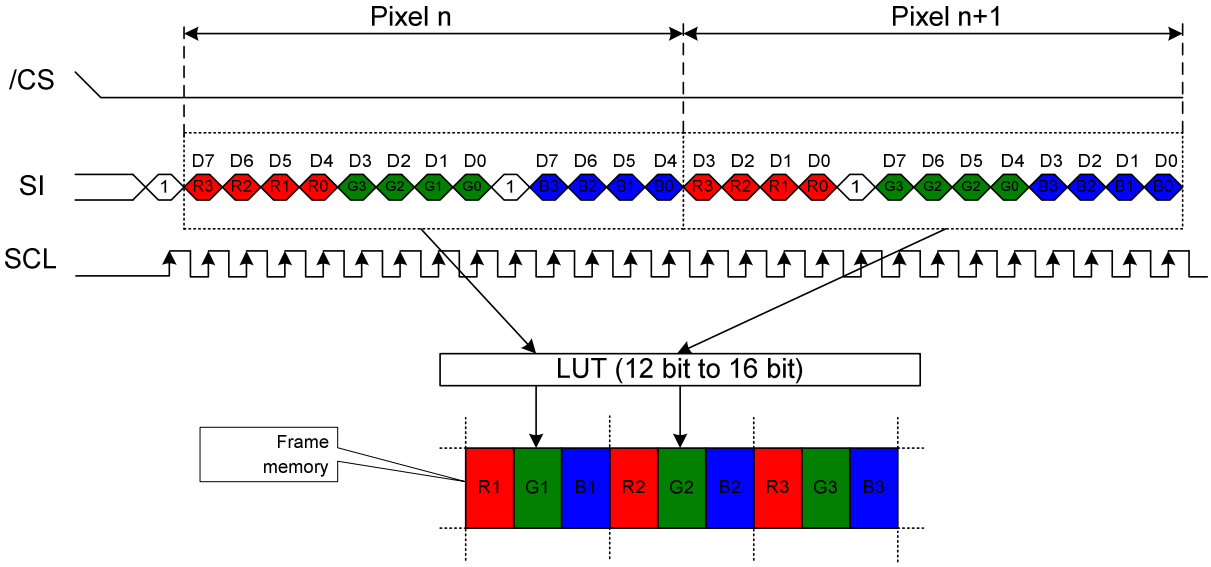
There is 1 pixel (= 3 sub-pixels) per byte.



Note: R2, G2, B1 are the most significant bits and R0, G0, B0 are the least significant bits.

(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type A

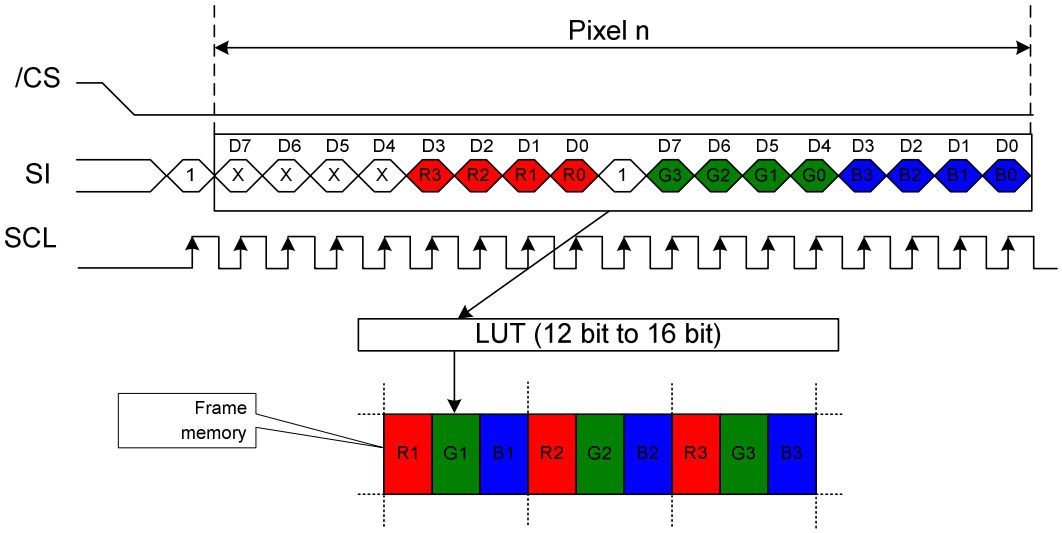
There are 2 pixel (= 3 sub-pixels) per 3 byte.



Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(3) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type B

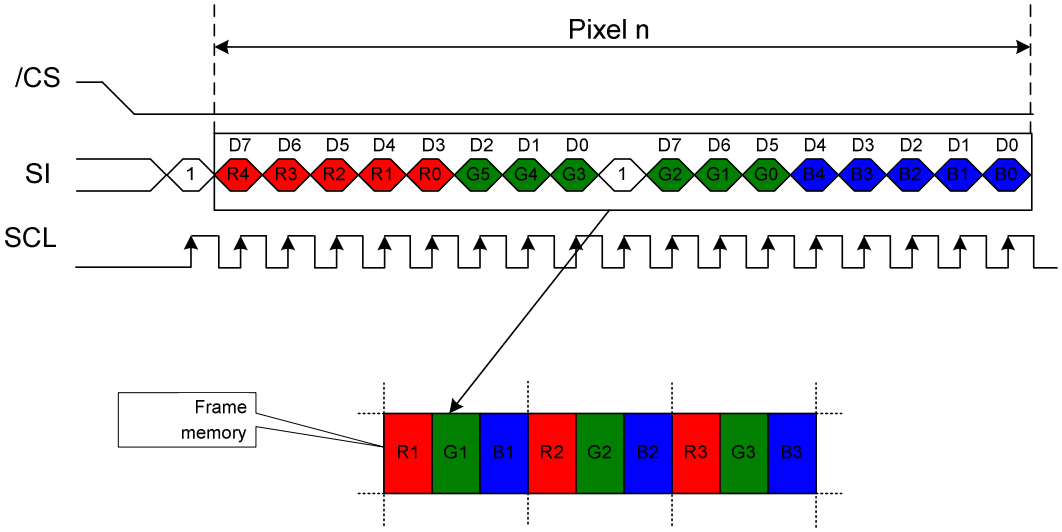
There is 1 pixel (= 3 sub-pixels) per 2 bytes.



Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(4) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

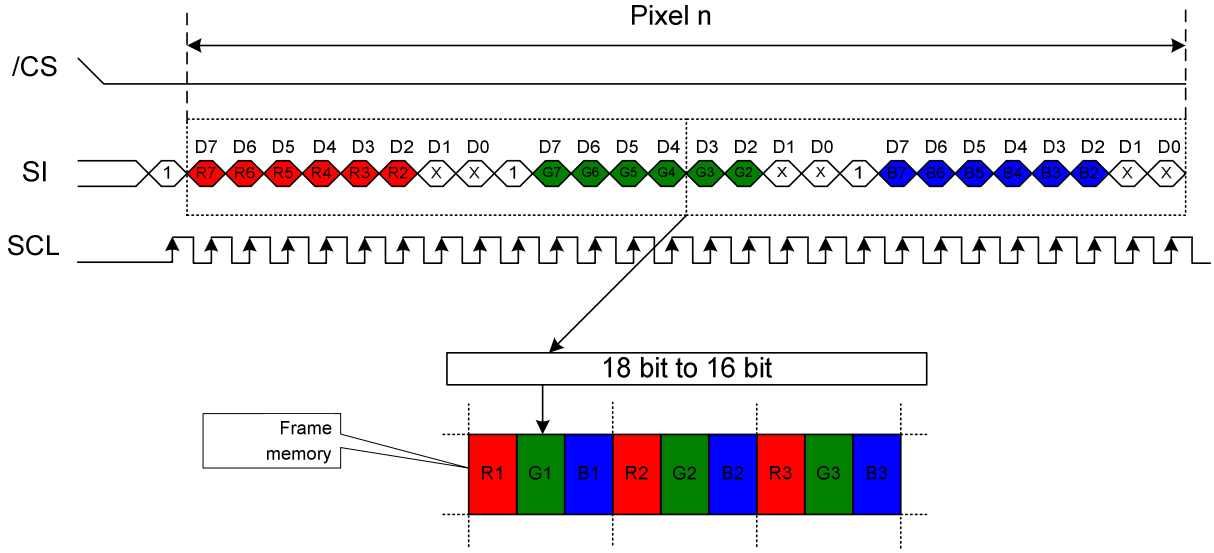
There is 1 pixel (= 3 sub-pixels) per 2 byte.



Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

(5) R 6-bit, G 6-bit, B 6-bit, 262k colors

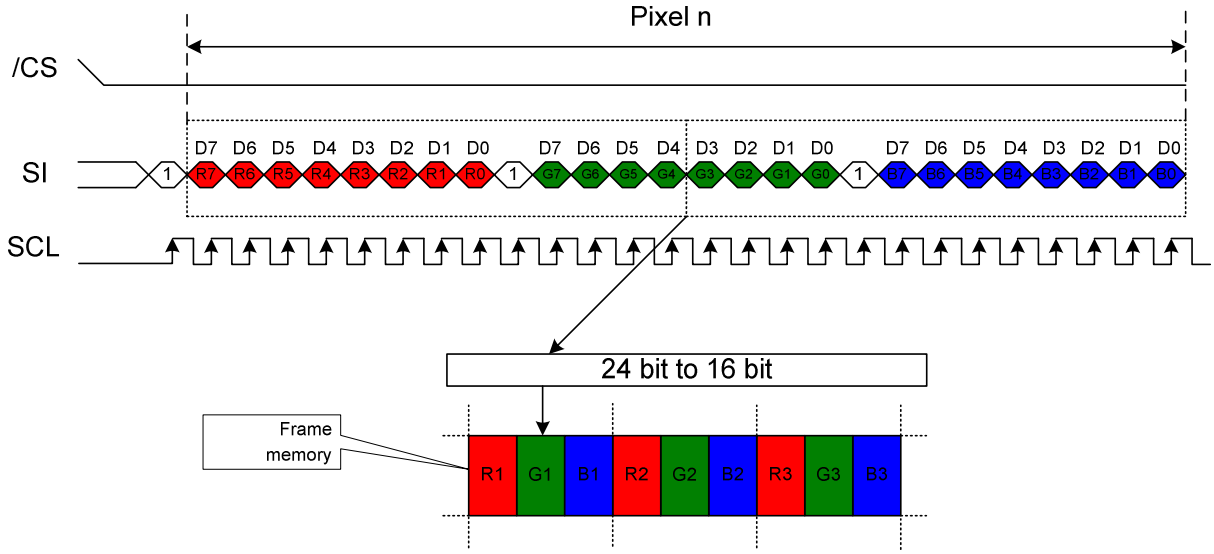
There is 1 pixel (= 3 sub-pixels) per 3 byte.



Note: R7, G7, B7 are the most significant bits and R2, G2, B2 are the least significant bits.

(6) R 8-bit, G 8-bit, B 8-bit, 16M colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.



Note: R7, G7, B7 are the most significant bits and R0, G0, B0 are the least significant bits.

7.2 ACCESS TO DDRAM AND INTERNAL REGISTERS

ST7628 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Figure 7.2 illustrates these relations.

In 80-series interface mode:

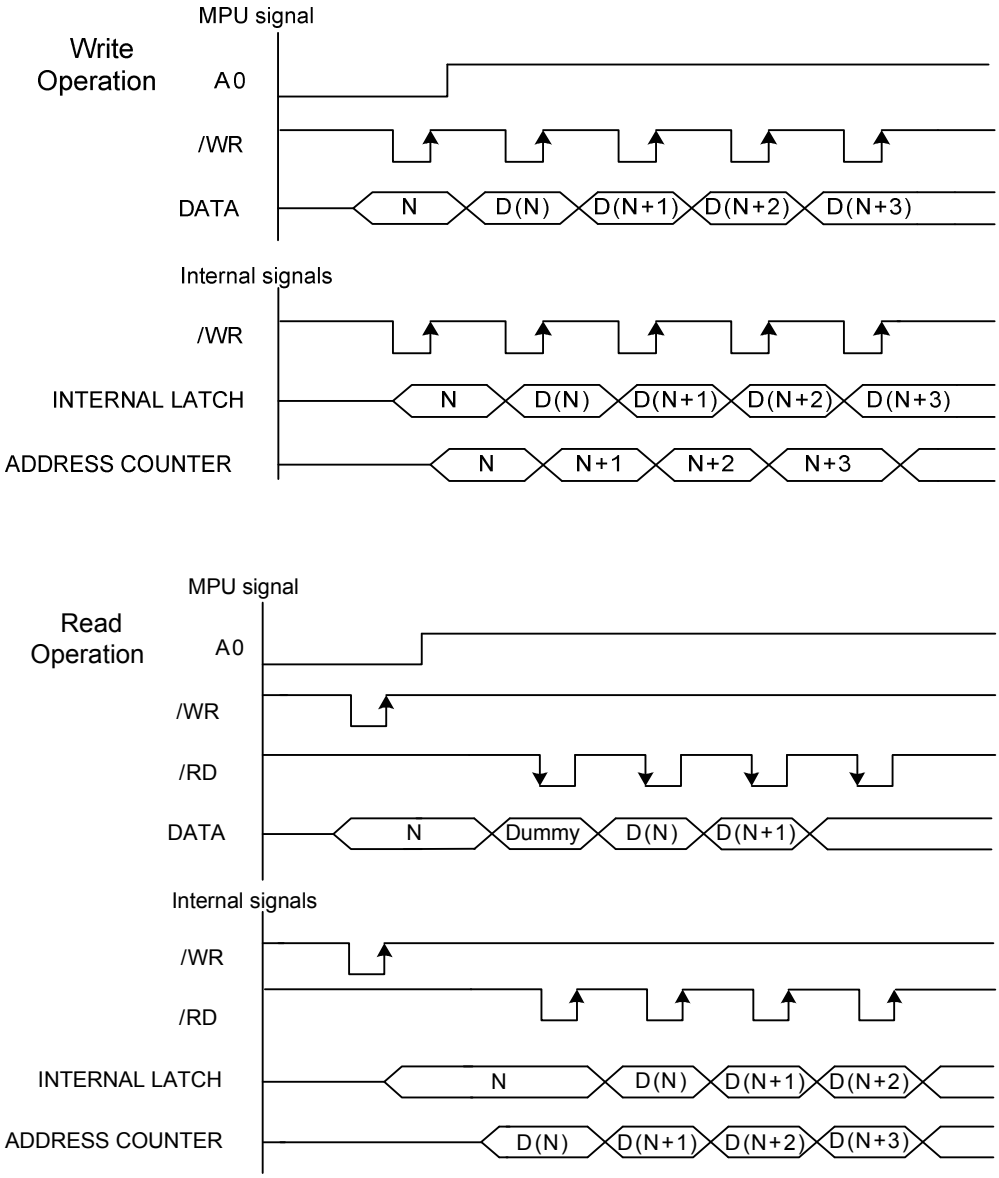


Figure 7.2

7.3 DISPLAY DATA RAM (DDRAM)

7.3.1 DDRAM

It is 98 X 70 X 16 bits capacity RAM prepared for storing dot data. Refer to the following memory map for the RAM configuration.

Memory Map

RGB alignment												
Data control command			Column									
	(MADCTR) MX=0		0			1				97		
	(MADCTR) MX=1		97			96				0		
	Color		R	G	B	R	G	B		R	G	B
	Page \ Data											
	(MADCTR) MY=0	(MADCTR) MY=1										
	0	69										
	1	68										
	2	67										
	3	66										
	4	65										
	5	64										
	6	63										
	7	62										
	:	:										
	62	7										
	63	6										
	64	5										
	65	4										
	66	3										
	67	2										
	68	1										
	69	0										
SEGout			0	1	2	3	4	5		291	292	293

You can change position of R and B with MADCTR command.

7.3.2 Address Counter

The address counter sets the addresses of the display data RAM for writing.

Data is written pixel into the RAM matrix of ST7628. The data for one pixel or two pixels is collected (RGB 5-6-5-bit), according to the data formats. As soon as this pixel-data information is complete, the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=97 (61hex) and Y=0 to Y=69 (45h). Addresses outside these ranges are not allowed.

Before writing to the RAM, a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=97 (61h), YE=69 (45h).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (MV=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS). For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTR” (see section “9.1.31”), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Figure 7.3 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the databus be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

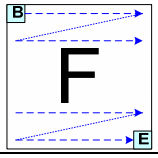
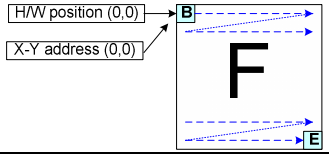
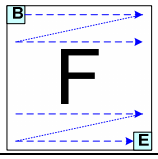
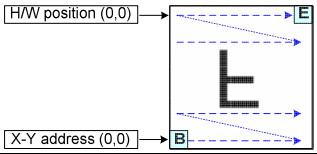
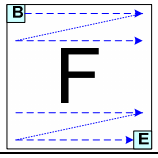
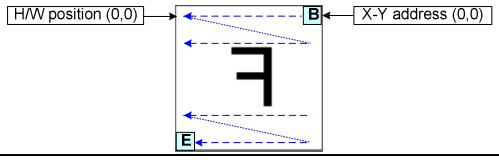
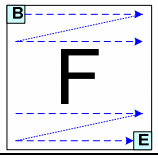
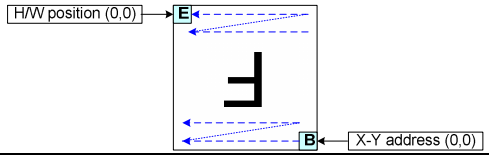
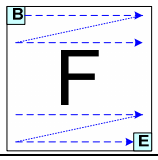
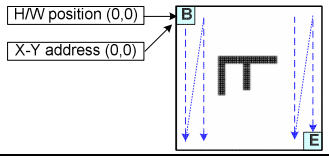
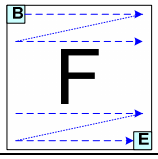
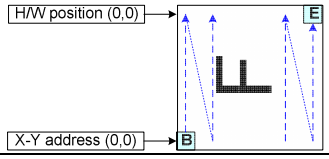
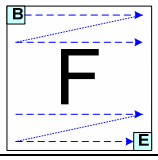
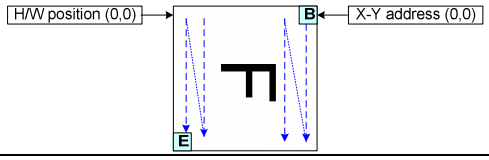
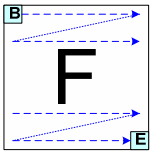
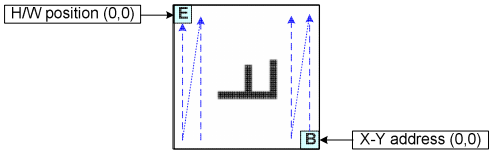
Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 7.3

Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

7.3.3 I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM when the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.4 Scroll Address Circuit

The circuit associates lines on DDRAM with COM output. ST7628 processes signals for the liquid crystal display on 1-line basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in line.

7.3.5 Display data Latch Circuit

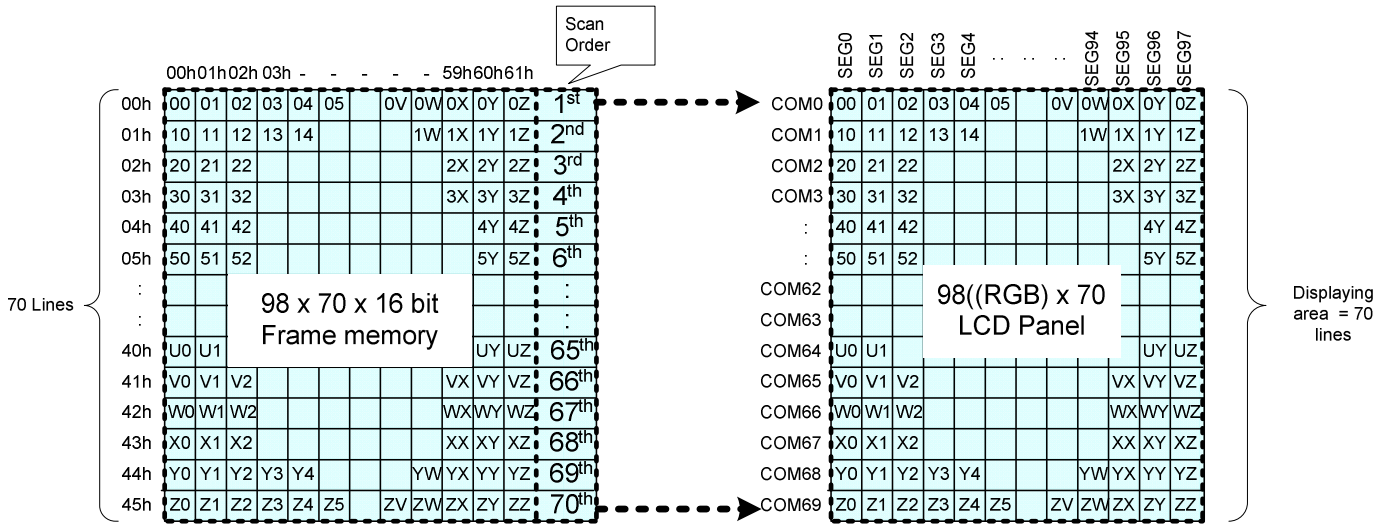
This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.3.6 Normal Display On or Partial Mode On, Vertical Scroll Off

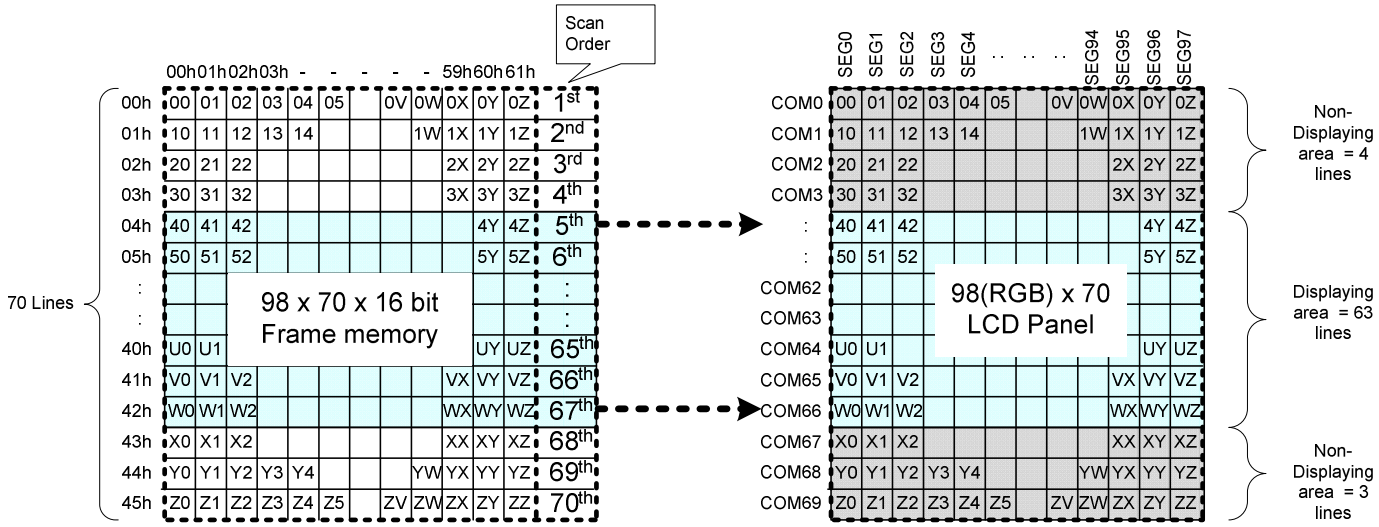
In this mode, contents of the frame memory within an area where column address is 00h to 61h and row address is 00h to 45h is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1) Normal Display On



Example2) Partial Display On: PSL[6:0] = 04h, PEL[6:0] = 42h, MADCTR (ML)=0



7.3.7 Vertical Scroll

Rolling Scroll

There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

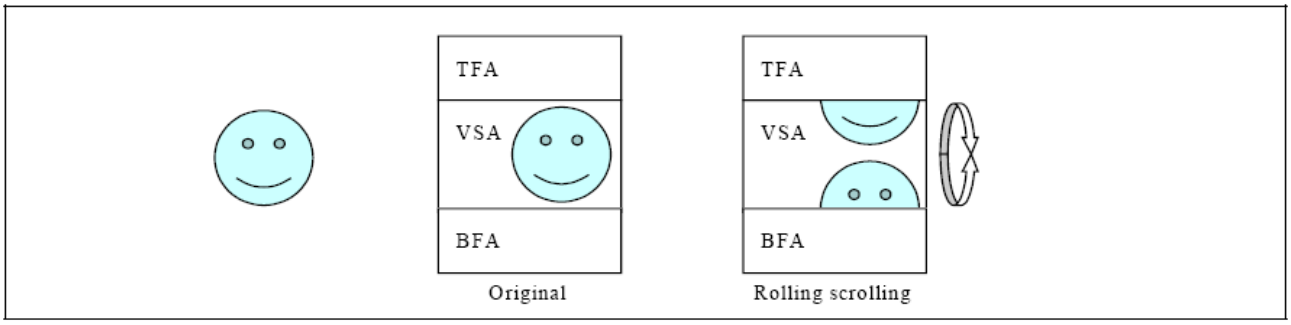
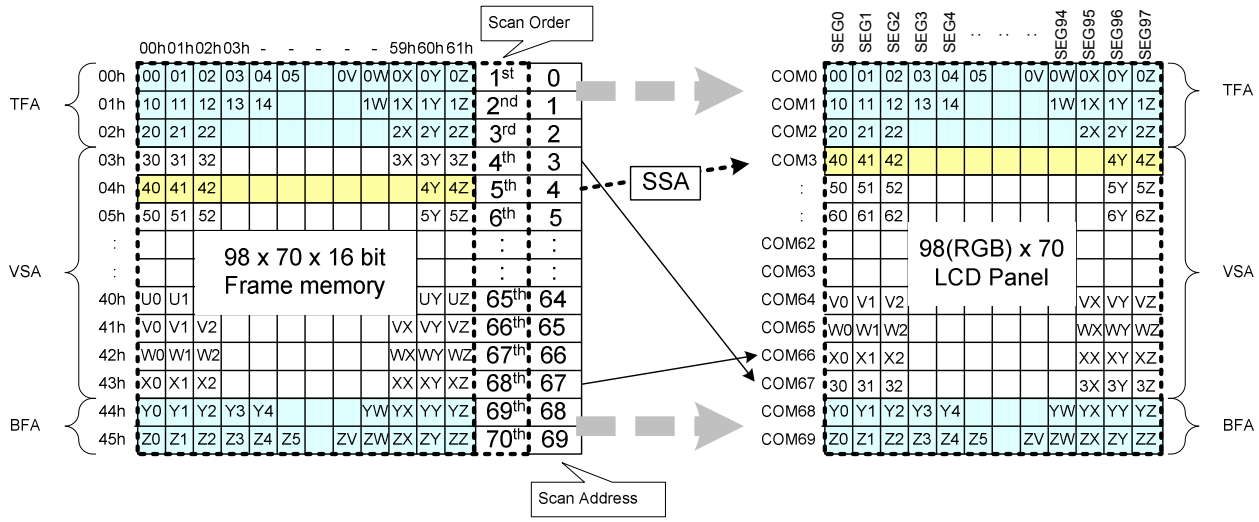


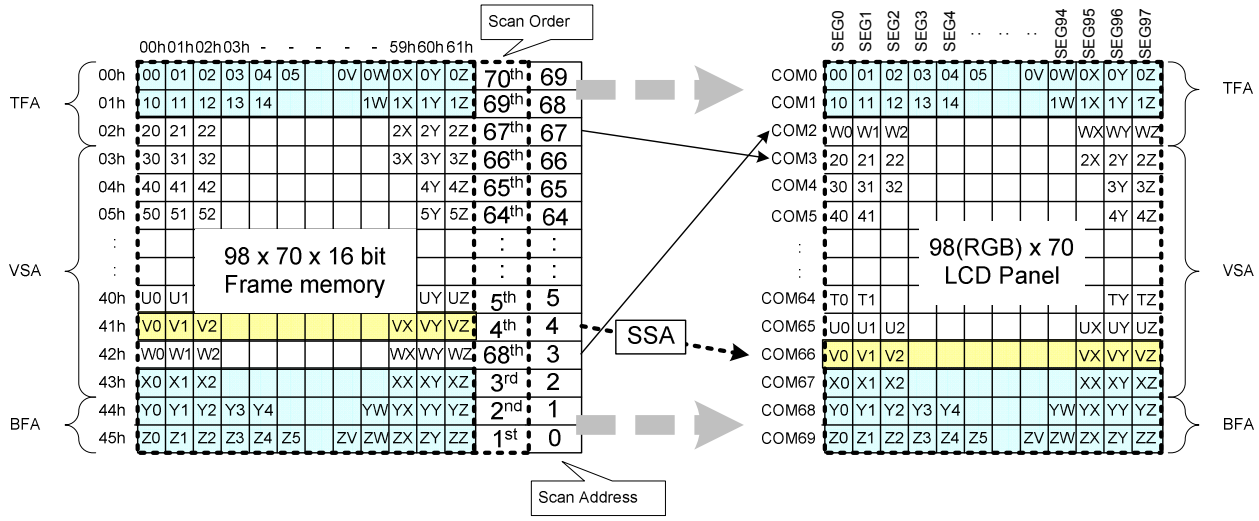
Figure 7.4 Rolling Scroll Definition

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =70. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example1) Panel size=98(RGB) x 70, TFA =3, VSA=65, BFA=2, SSA=4, MADCTR (ML) =0: Rolling Scroll



Example2) Panel size=98(RGB) x 70, TFA =3, VSA=65, BFA=2, SSA=4, MADCTR (ML) =1: Rolling Scroll



Vertical Scroll Example

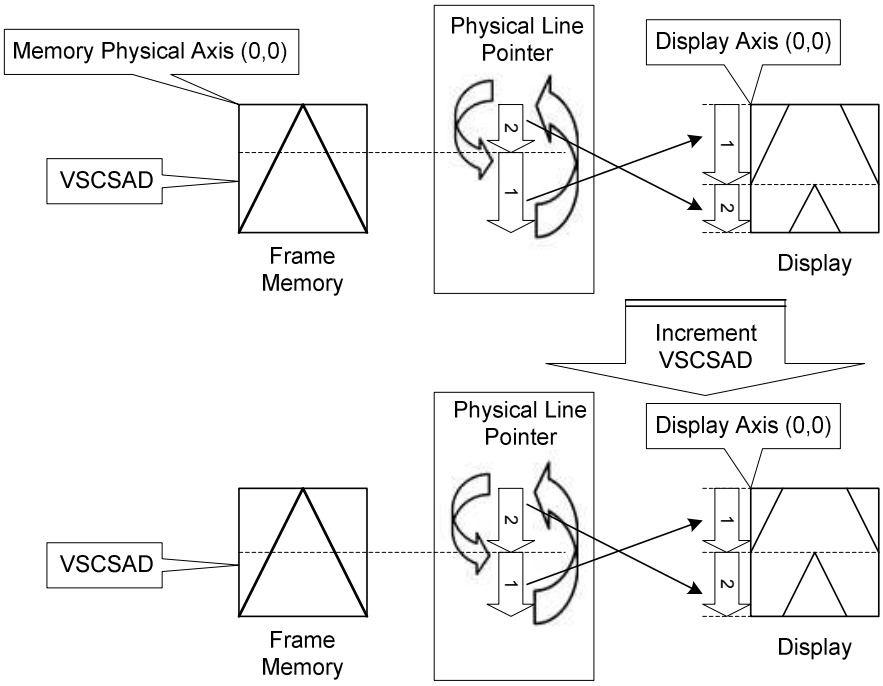
There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA<70

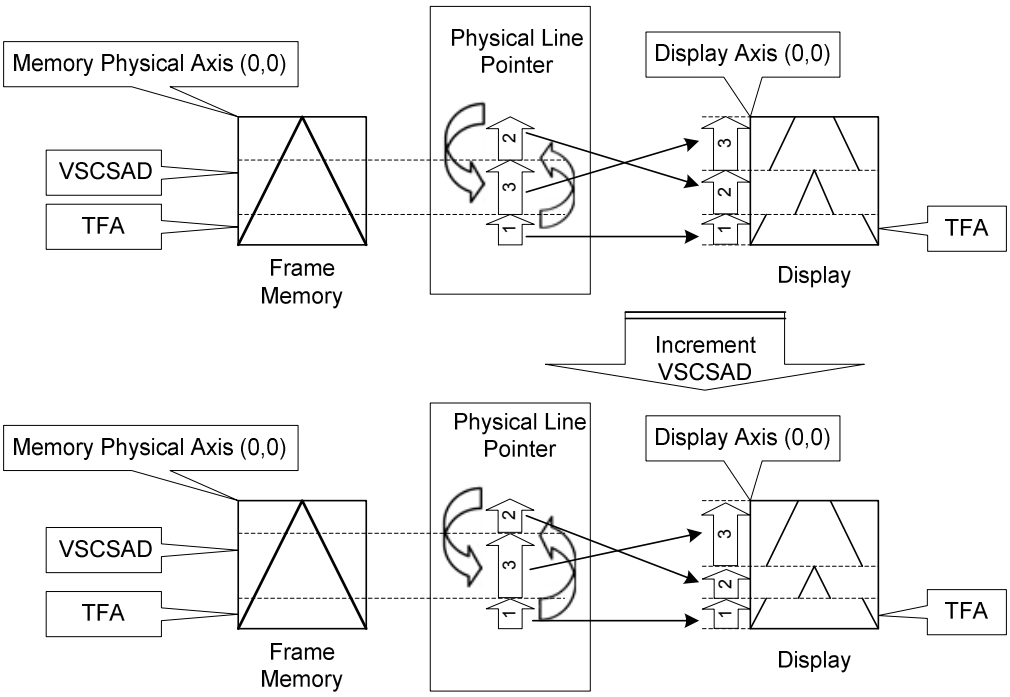
N/A. Do not set TFA + VSA + BFA<70. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=70 (Rolling Scrolling)

Example1) When MADCTR parameter ML="0", TFA=0, VSA=70, BFA=0 and VSCSAD=40.



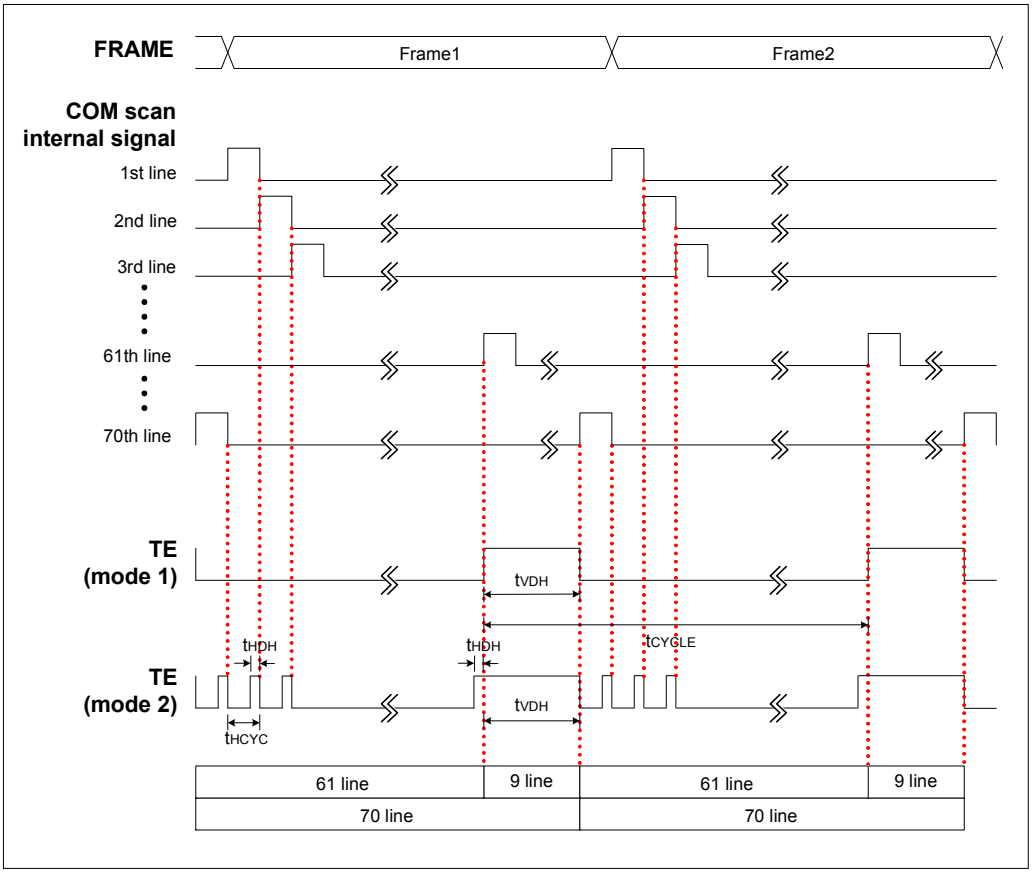
Example2) When MADCTR parameter ML="1", TFA=10, VSA=60, BFA=0 and VSCSAD=30.



7.3.8 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

Tearing Effect Line Modes(Frame rate=77Hz)



Mode 1, the Tearing Effect Output signal consists of V-Sync(tVDH) information. It starts at 61th line signal and ends at the 70th line signal. There is one high pulse during each frame.

Mode 2, the Tearing Effect Output signal consists of both H-Sync(tHDH) and V-Sync(tVDH) information. TE pin output tHDH pulse on each COM scan signal. During 61th ~ 70th line signal, it output a high pulse which equals 1 tHDH + 1 tVDH.

Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

Tearing Effect Line Timing

The Tearing Effect signal is described below:

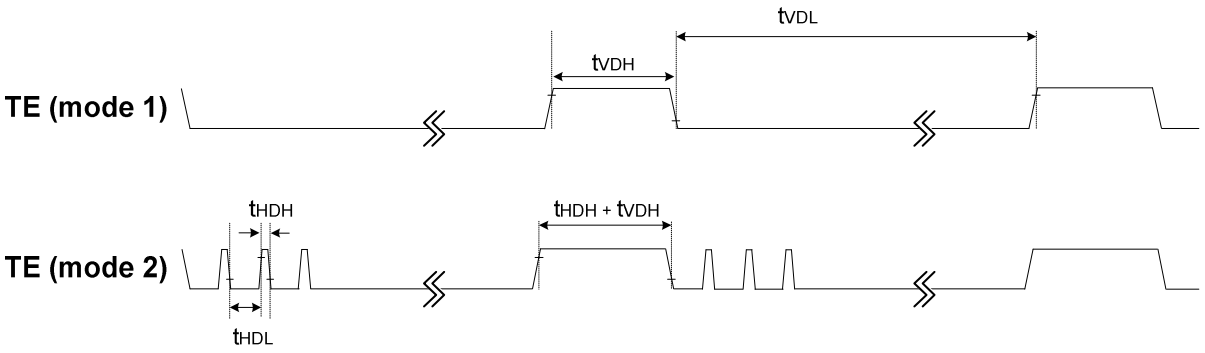
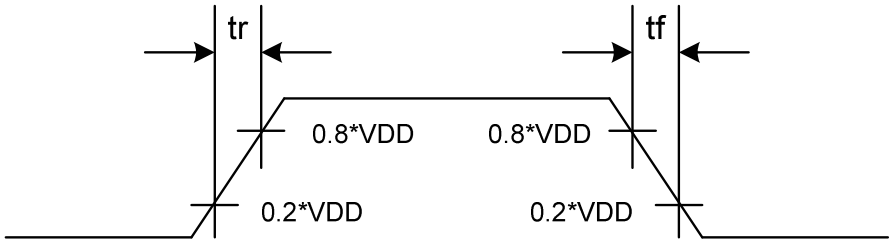


Table 7.3.1 AC characteristics of Tearing Effect Signal

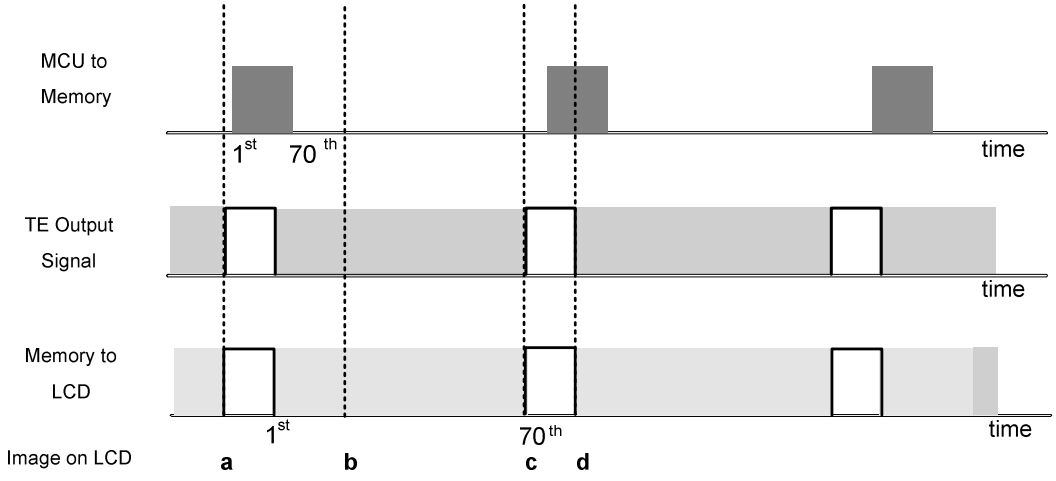
Idle Mode Off (Frame Rate = 77Hz)

Symbol	Parameter	Min	Typ	Max	Unit	description
t_{VDL}	Vertical Timing Low Duration	--	13	--	ms	Mode1
t_{VDH}	Vertical Timing High Duration	1	1.6	--	ms	
t_{HDL}	Horizontal Timing Low Duration	--	185	--	us	Mode2
t_{HDH}	Horizontal Timing High Duration	11	12	--	us	

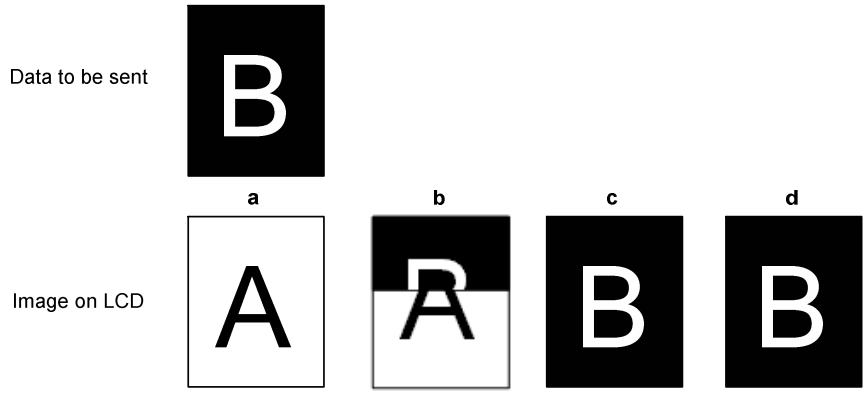
Note: The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



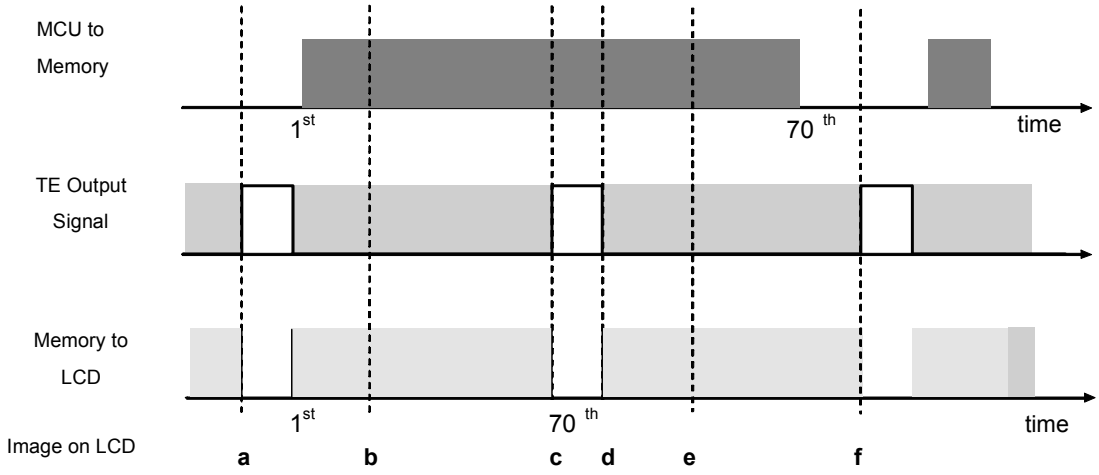
Example 1: MPU Write is Faster than Panel Read.



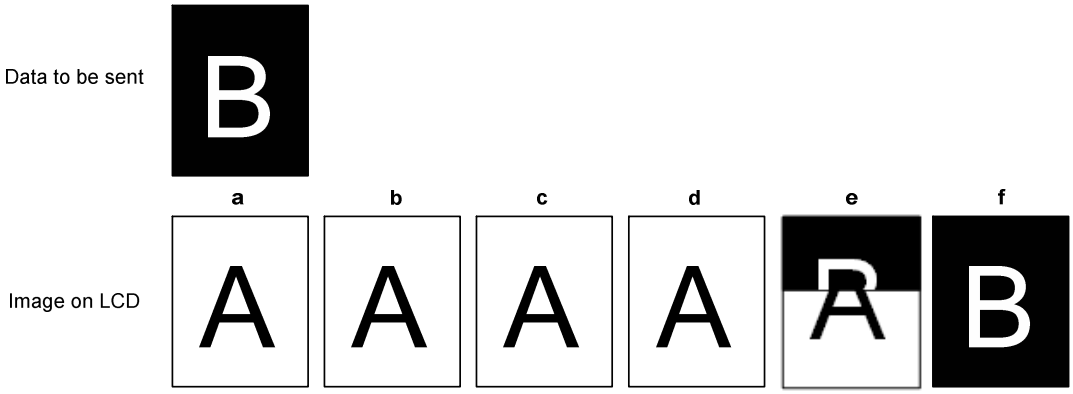
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



Example 2: MPU Write is Slower than Panel Read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



7.4 Gary-Scale Display

ST7628 incorporates a 4FRC & 31 PWM function circuit to display a 64 gray-scale display.

7.5 Oscillation circuit

This is on-chip Oscillator without external resistor. When the internal oscillator is used, CLS must connect to VDD; when the external oscillator is used, CL could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.6 Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock CL (internal), which is generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 96-bits display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.5.

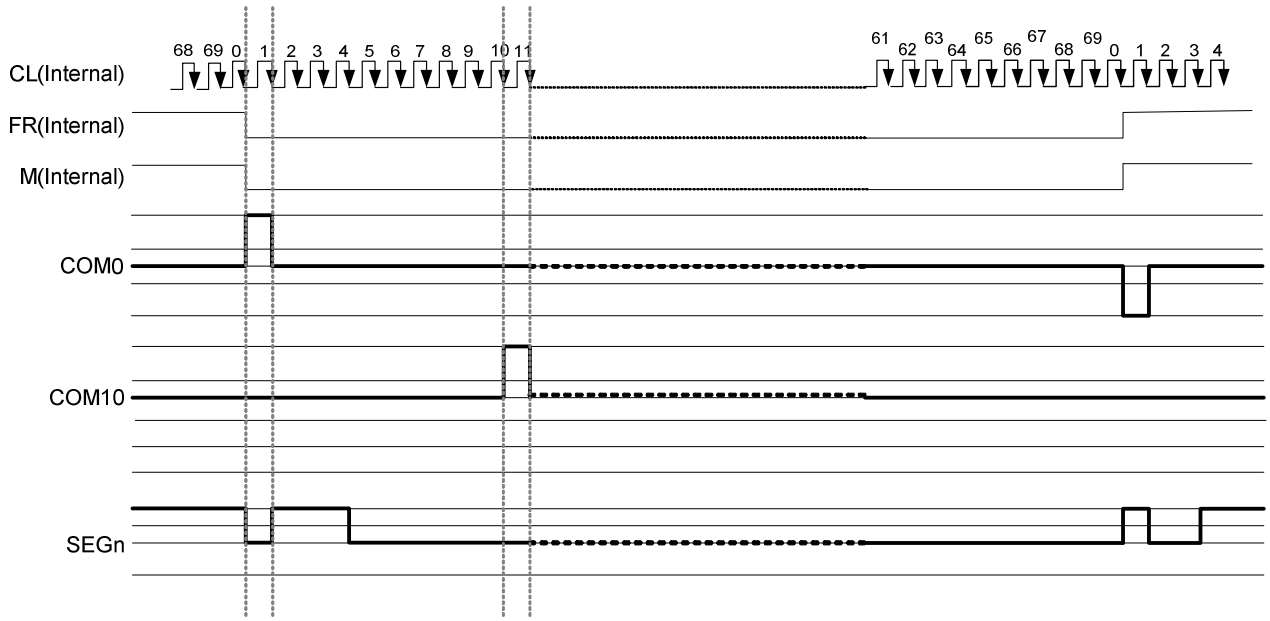


Figure 7.5 2-frame AC Driving Waveform (Duty Ratio: 1/70)

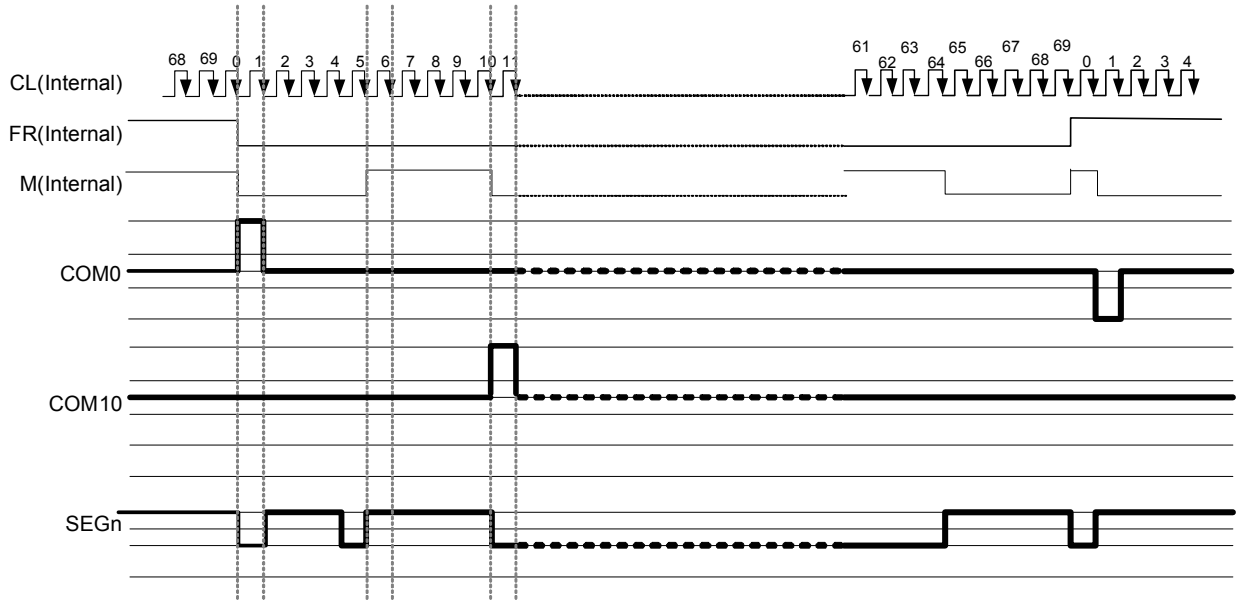


Figure 7.6 N-Line Inversion Driving Waveform (N=5, Duty Ratio=1/70)

7.7 POWER LEVEL DEFINITION

7.7.1 Power ON/OFF SEQUENCE

VDDI and VDDA can be applied in any order. **(VDDI=VDD, VDDA=VDD2, VDD3, VDD4, VDD5)**

VDDI and VDDA can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VDDA and VDDI must be powered down minimum 120msec after /RST has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDDA can be powered down minimum 0msec after /RST has been released.

/CS can be applied at any timing or can be permanently grounded. /RST has priority over /CS.

There will be no damage to the display module if the power sequences are not met.

There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

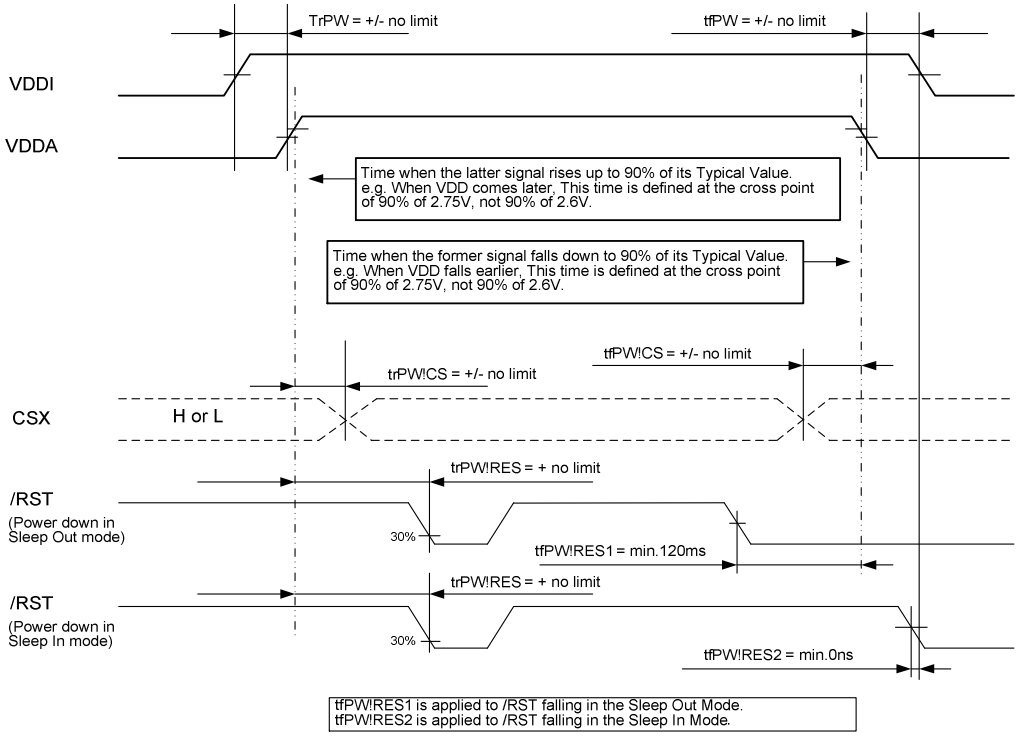
There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

If /RST line is not held stable by host during Power On Sequence as defined in Sections case1 and case2, then it will be necessary to apply a Hardware Reset (/RST) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

Case 1 – /RST line is held High or Unstable by Host at Power On

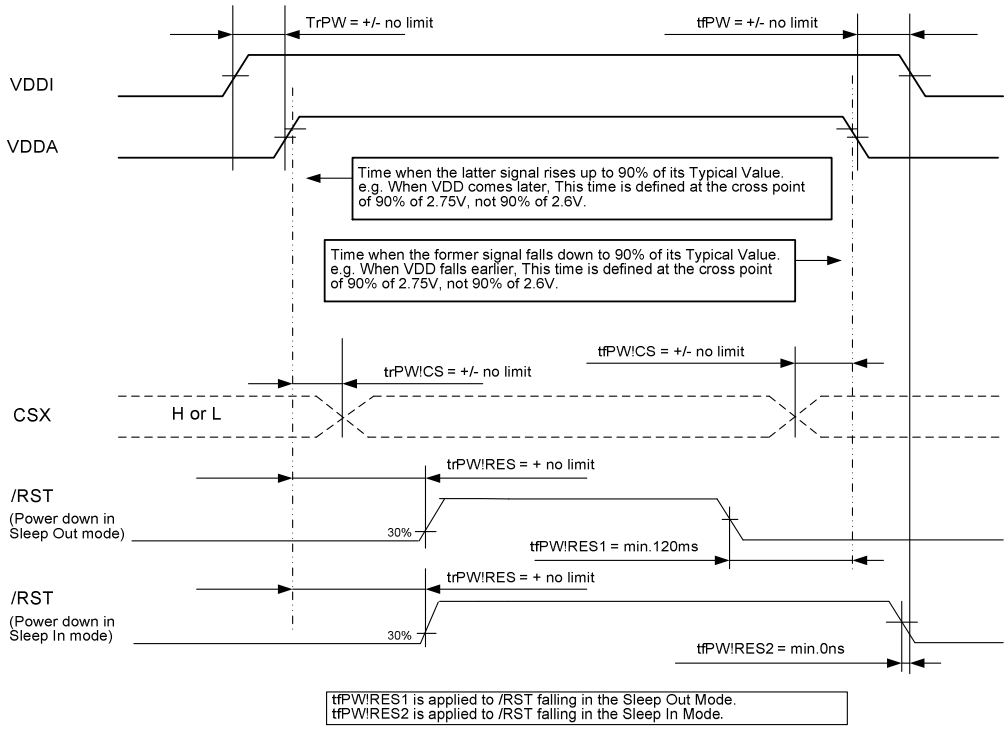
If /RST line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDDA and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Case 2 – /RST line is held Low by host at Power On

If /RST line is held Low (and stable) by the host during Power On, then the /RST must be held low for minimum 10µsec after both VDDA and VDDI have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

UNCONTROLLED POWER OFF

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

7.7.2 Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out:

In this mode, the display is able to show maximum 65K colors.

2. Partial Mode On, Idle Mode Off, Sleep Out:

In this mode part of the display is used with maximum 65K colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out:

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out:

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode:

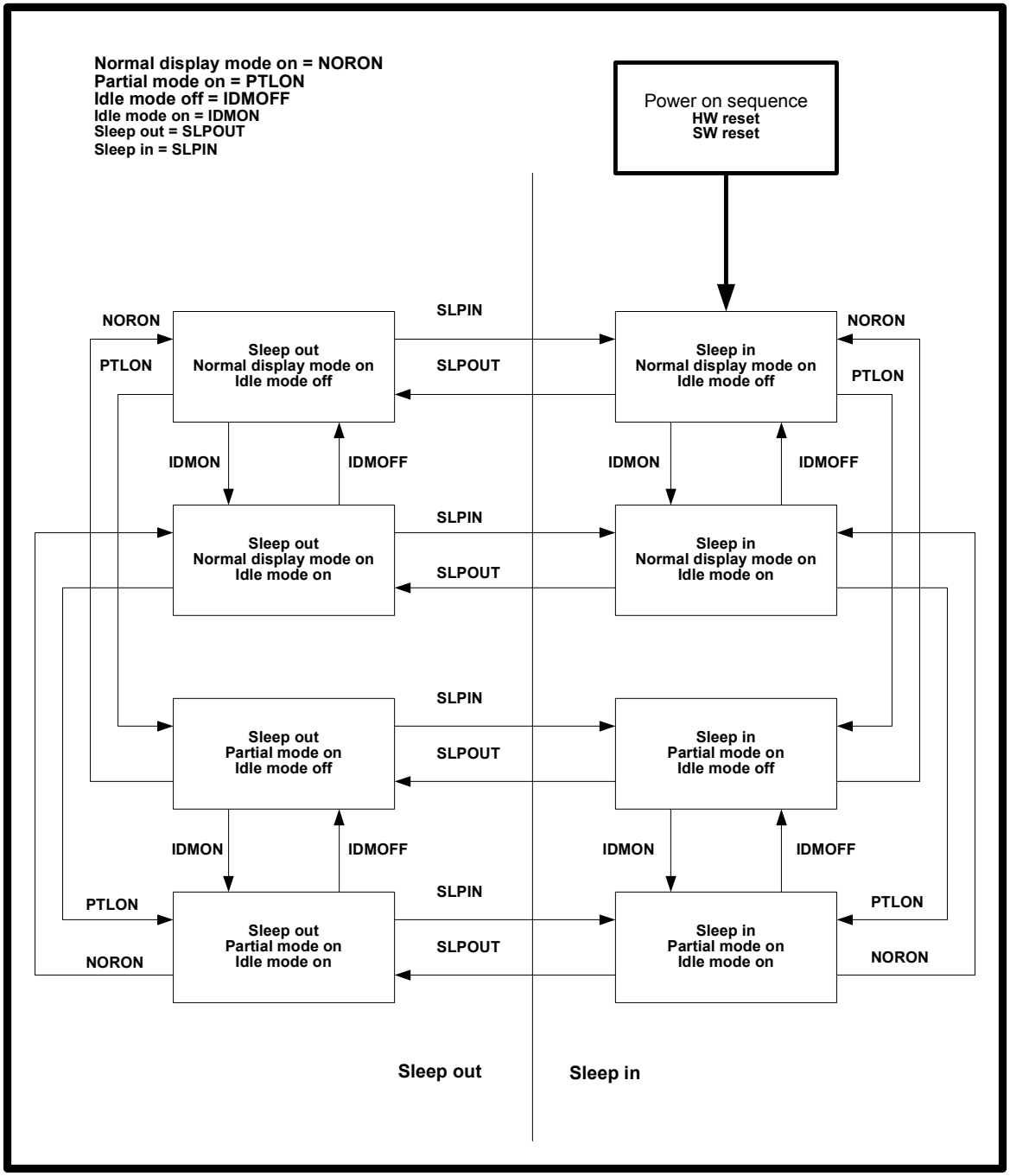
In this mode, the DC:DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with Digital VDD power supply. Contents of the memory are safe.

6. Power Off Mode:

In this mode, both Analog VDD and Digital VDD are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

7.7.3 POWER FLOW CHART FOR DIFFERENT POWER MODES



Note

1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

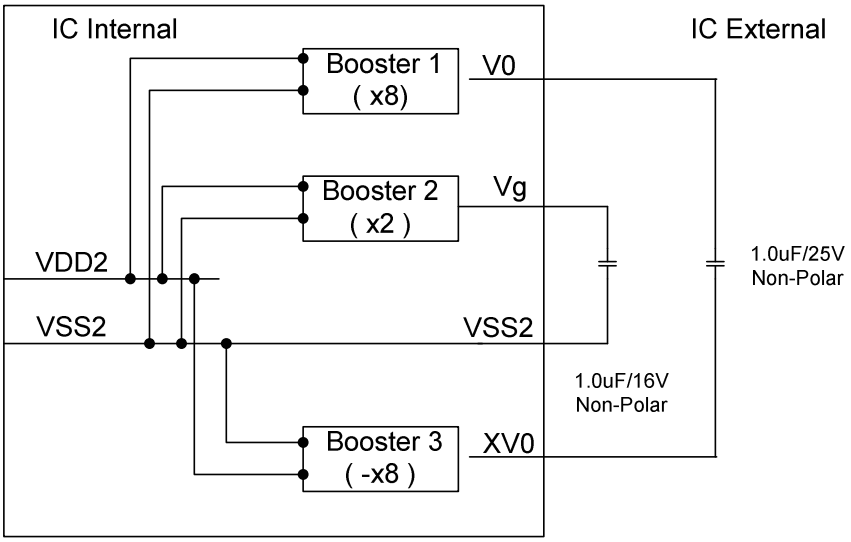
2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

7.8 Color Depth Conversion Look Up Tables

Color	Look Up Table Inputs		Look Up Table Outputs	Default	RGBSET
	256 Color Data	4096 Color Data	Frame Memory Data (5 or 6-bit)	Value	parameter
RED	000	0000	R_{004} R_{003} R_{002} R_{001} R_{000}	00000	**1**
	001	0001	R_{014} R_{013} R_{012} R_{011} R_{010}	00010	**2**
	010	0010	R_{024} R_{023} R_{022} R_{021} R_{020}	00100	**3**
	011	0011	R_{034} R_{033} R_{032} R_{031} R_{030}	00110	**4**
	100	0100	R_{044} R_{043} R_{042} R_{041} R_{040}	01000	**5**
	101	0101	R_{054} R_{053} R_{052} R_{051} R_{050}	01010	**6**
	110	0110	R_{064} R_{063} R_{062} R_{061} R_{060}	01100	**7**
	111	0111	R_{074} R_{073} R_{072} R_{071} R_{070}	01110	**8**
	Dummy input	1000	R_{084} R_{083} R_{082} R_{081} R_{080}	10000	**9**
		1001	R_{094} R_{093} R_{092} R_{091} R_{090}	10010	**10**
		1010	R_{104} R_{103} R_{102} R_{101} R_{100}	10100	**11**
		1011	R_{114} R_{113} R_{112} R_{111} R_{110}	10110	**12**
		1100	R_{124} R_{123} R_{122} R_{121} R_{120}	11000	**13**
		1101	R_{134} R_{133} R_{132} R_{131} R_{130}	11010	**14**
		1110	R_{144} R_{143} R_{142} R_{141} R_{140}	11100	**15**
		1111	R_{154} R_{153} R_{152} R_{151} R_{150}	11111	**16**
GREEN	000	0000	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	000000	**17**
	001	0001	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	000100	**18**
	010	0010	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	001000	**19**
	011	0011	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	001100	**20**
	100	0100	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	010000	**21**
	101	0101	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	010100	**22**
	110	0110	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	011000	**23**
	111	0111	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	011100	**24**
	Dummy input	1000	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	100000	**25**
		1001	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}	100100	**26**
		1010	G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}	101000	**27**
		1011	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}	101100	**28**
		1100	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}	110000	**29**
		1101	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}	110100	**30**
		1110	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}	111000	**31**
		1111	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}	111111	**32**
BLUE	00	0000	B_{004} B_{003} B_{002} B_{001} B_{000}	00000	**33**
	01	0001	B_{014} B_{013} B_{012} B_{011} B_{010}	00010	**34**
	10	0010	B_{024} B_{023} B_{022} B_{021} B_{020}	00100	**35**
	11	0011	B_{034} B_{033} B_{032} B_{031} B_{030}	00110	**36**
	Dummy input	0100	B_{044} B_{043} B_{042} B_{041} B_{040}	01000	**37**
		0101	B_{054} B_{053} B_{052} B_{051} B_{050}	01010	**38**
		0110	B_{064} B_{063} B_{062} B_{061} B_{060}	01100	**39**
		0111	B_{074} B_{073} B_{072} B_{071} B_{070}	01110	**40**
		1000	B_{084} B_{083} B_{082} B_{081} B_{080}	10000	**41**
		1001	B_{094} B_{093} B_{092} B_{091} B_{090}	10010	**42**
		1010	B_{104} B_{103} B_{102} B_{101} B_{100}	10100	**43**
		1011	B_{114} B_{113} B_{112} B_{111} B_{110}	10110	**44**
		1100	B_{124} B_{123} B_{122} B_{121} B_{120}	11000	**45**
		1101	B_{134} B_{133} B_{132} B_{131} B_{130}	11010	**46**
		1110	B_{144} B_{143} B_{142} B_{141} B_{140}	11100	**47**
		1111	B_{154} B_{153} B_{152} B_{151} B_{150}	11111	**48**

7.9 Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.



DC/DC Booster Block Diagram

7.9.1 Voltage Regulator Circuits

SET V0 (Temperature = 24℃)

V0=a+{Vop[8:0] + VopOffset[8:0]+ (EV[6:0]-3Fh)}xb (V)

Example:

Vop[8:0]=011010010

VopOffset[8:0]=000000011

EV[6:0]=0111111

V0=3.6 + (210 + 3 + (63-63)) x 0.04 =12.12 (V)

- a is a fixed constant value (seeTable 7.9.1).
- b is a fixed constant value (seeTable 7.9.1).
- Vop [8:0] is the programmed VOP value. The programming range for Vop[8:0] is 5 to 410 (19Ahex).
- The range of contrast is 128 steps for fine tuning VOP.

Table 7.9.1

SYMBOL	VALUE	UNIT
a	3.6	V
b	0.04	V

The Vop [8:0] value must be in the V0 programming range as given in Figure 7.7. Evaluating V0 equation, values outside the programming range indicated in many result.

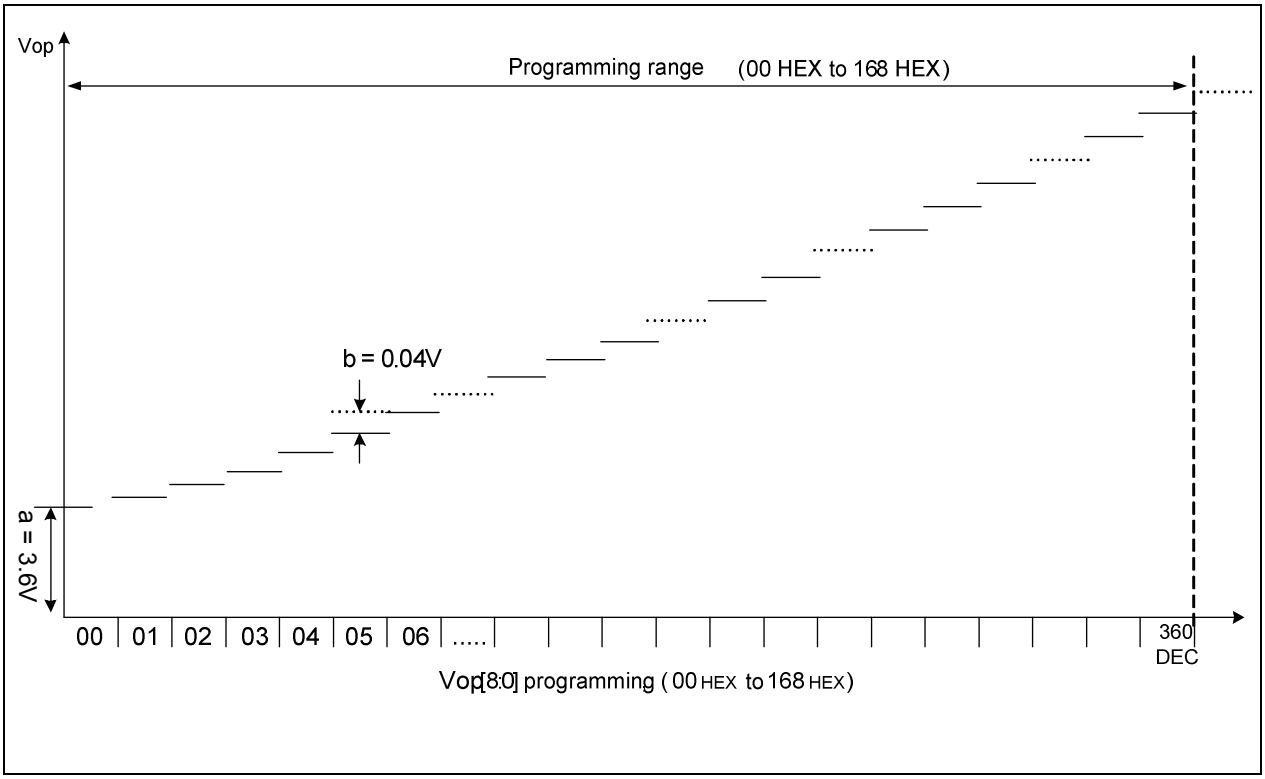


Figure 7.7 V0 programming range

As the programming range for the internally generated V0 voltage is above the limited V0 (18V), users has to ensure while setting the VOP register and selecting the temperature compensation that under all conditions and including all tolerances that the V0 voltage remains below 18V.

SET V0 with temperature compensation (Temperatue ≠ 24℃)

There are 16-line slope in each temperature steps and customer can select one line slope of temperature compensation coefficiency for each temperature step. Each temperature step is 8°C. Please see Figure 7.8 as below.

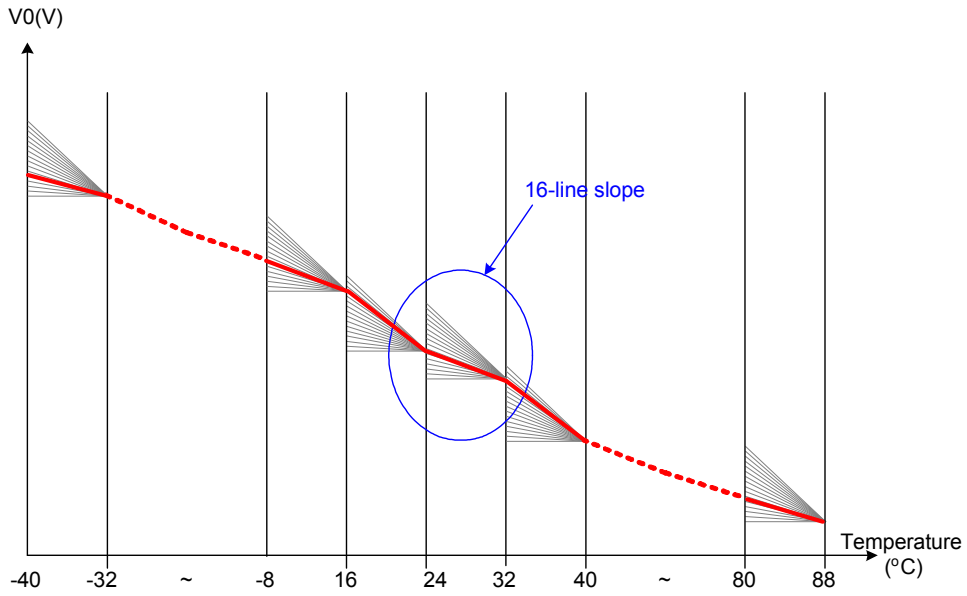
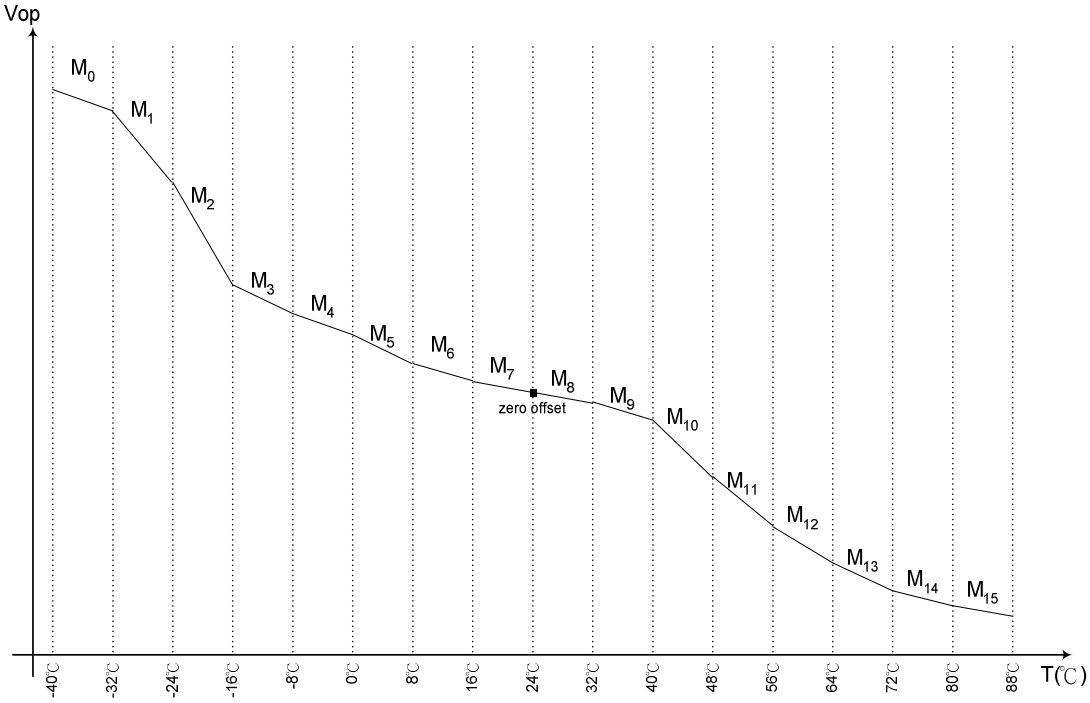


Figure 7.8

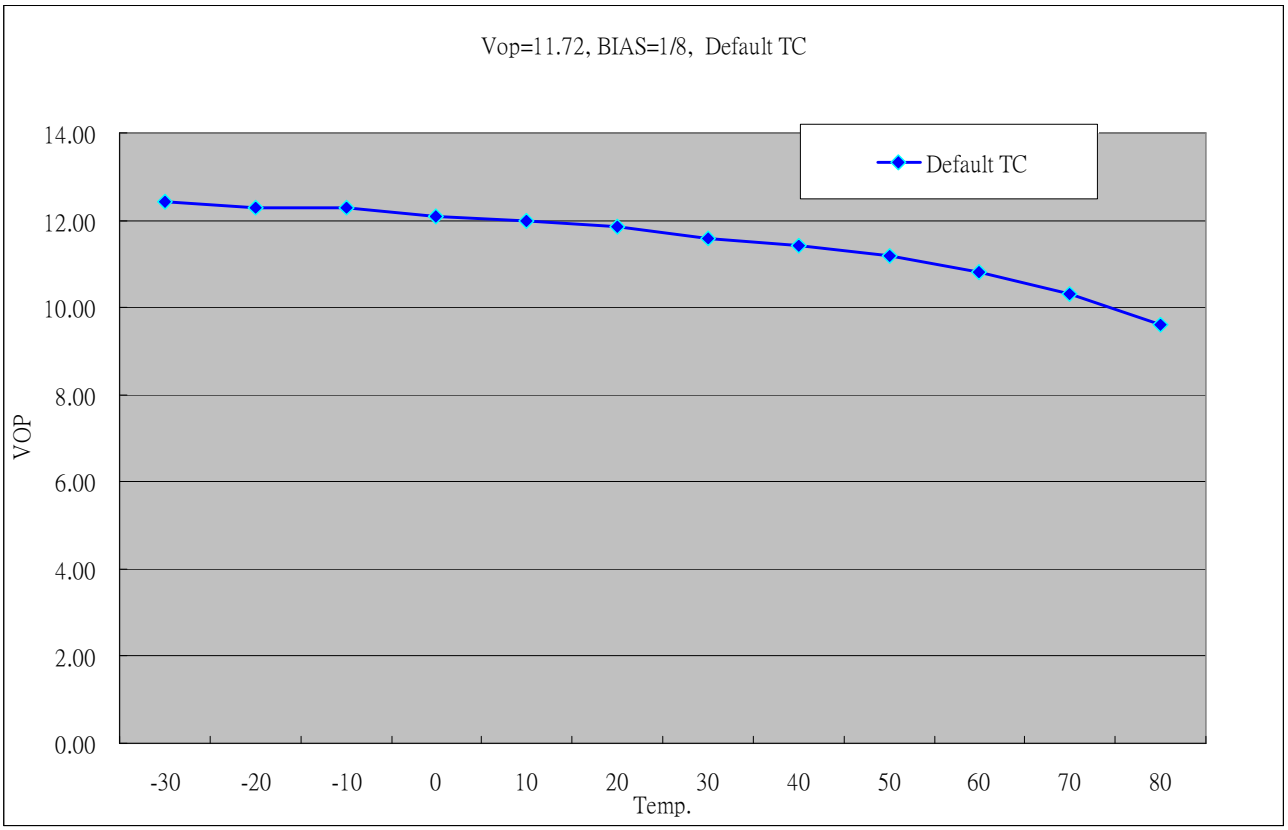
In command TEMPSEL (see section 9.1.72) each MTx, where x=0, 1, 2,…, E, F, has a value between 0 and 15. MTx = 0 results in 0V increment on V0, MTx = 1 results in Mx=5mV increment, …, MTx = 15 results in Mx=15x5mV=75mV increment. Note that each MTx individually corresponds to a temperature interval; The relations between Mx and V0 quantity due to temperature V0(T) are described in the equations shown as follows:

Temperature range	Equation V0(V) at temperature=T℃
-40℃ ≦ T ＜ -32℃	$V0(T) = V0(T_{24}) + (-32-T) \cdot M0 + (M1 + M2 + M3 + M4 + M5 + M6 + M7) \cdot 8$
-32℃ ≦ T ＜ -24℃	$V0(T) = V0(T_{24}) + (-24-T) \cdot M1 + (M2 + M3 + M4 + M5 + M6 + M7) \cdot 8$
-24℃ ≦ T ＜ -16℃	$V0(T) = V0(T_{24}) + (-16-T) \cdot M2 + (M3 + M4 + M5 + M6 + M7) \cdot 8$
-16℃ ≦ T ＜ -8℃	$V0(T) = V0(T_{24}) + (-8-T) \cdot M3 + (M4 + M5 + M6 + M7) \cdot 8$
-8℃ ≦ T ＜ 0℃	$V0(T) = V0(T_{24}) + (0-T) \cdot M4 + (M5 + M6 + M7) \cdot 8$
0℃ ≦ T ＜ 8℃	$V0(T) = V0(T_{24}) + (8-T) \cdot M5 + (M6 + M7) \cdot 8$
8℃ ≦ T ＜ 16℃	$V0(T) = V0(T_{24}) + (16-T) \cdot M6 + M7 \cdot 8$
16℃ ≦ T ＜ 24℃	$V0(T) = V0(T_{24}) + (24-T) \cdot M7$
24℃ ≦ T ＜ 32℃	$V0(T) = V0(T_{24}) - (T-24) \cdot M8$
32℃ ≦ T ＜ 40℃	$V0(T) = V0(T_{24}) - (T-32) \cdot M9 - M8 \cdot 8$
40℃ ≦ T ＜ 48℃	$V0(T) = V0(T_{24}) - (T-40) \cdot M10 - (M9 + M8) \cdot 8$
48℃ ≦ T ＜ 56℃	$V0(T) = V0(T_{24}) - (T-48) \cdot M11 - (M10 + M9 + M8) \cdot 8$
56℃ ≦ T ＜ 64℃	$V0(T) = V0(T_{24}) - (T-56) \cdot M12 - (M11 + M10 + M9 + M8) \cdot 8$
64℃ ≦ T ＜ 72℃	$V0(T) = V0(T_{24}) - (T-64) \cdot M13 - (M12 + M11 + M10 + M9 + M8) \cdot 8$
72℃ ≦ T ＜ 80℃	$V0(T) = V0(T_{24}) - (T-72) \cdot M14 - (M13 + M12 + M11 + M10 + M9 + M8) \cdot 8$
80℃ ≦ T ＜ 88℃	$V0(T) = V0(T_{24}) - (T-80) \cdot M15 - (M14 + M13 + M12 + M11 + M10 + M9 + M8) \cdot 8$


Vop
M0
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
zero offset
-40℃
-32℃
-24℃
-16℃
-8℃
0℃
8℃
16℃
24℃
32℃
40℃
48℃
56℃
64℃
72℃
80℃
88℃
T(℃)

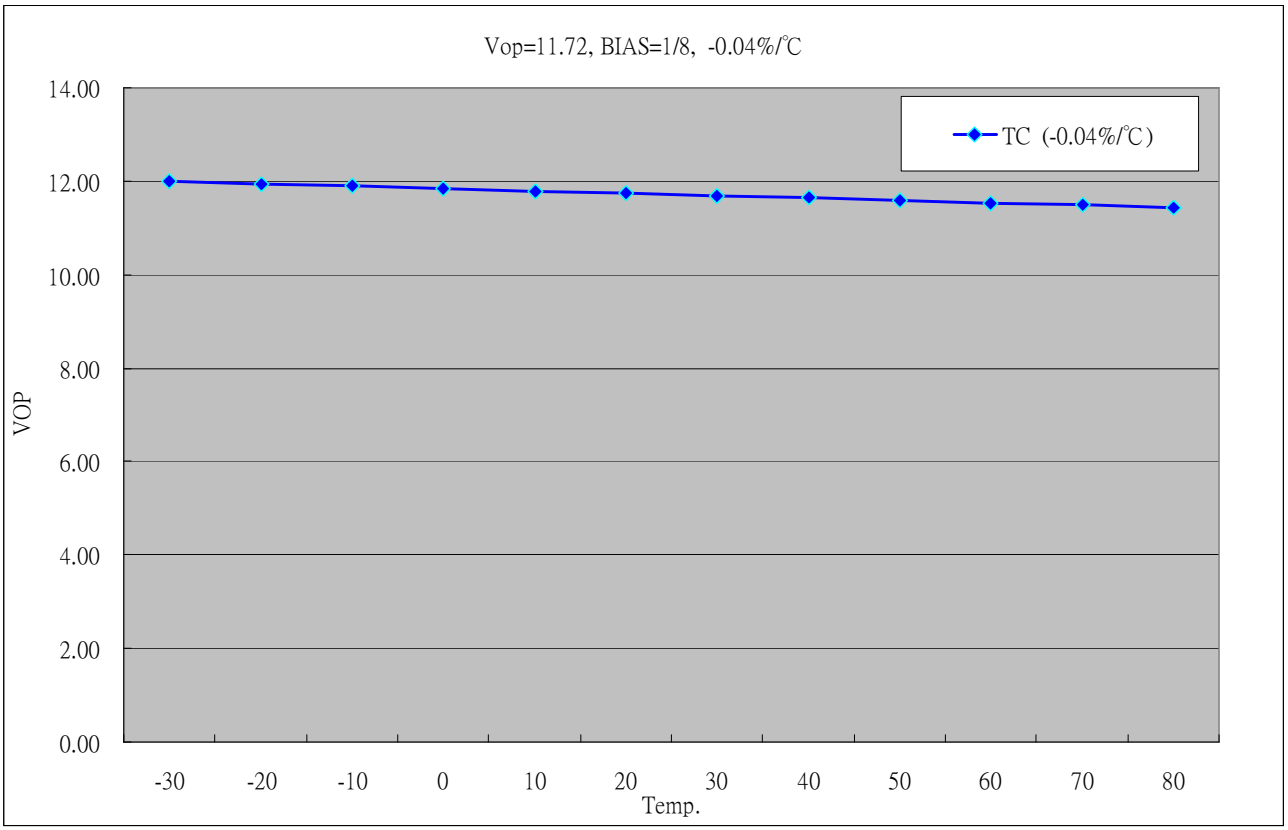
Setting example for default TC curve

COMMAND	
0xF4	
DATA	
1st: 0x50	2nd: 0x00
3rd: 0x25	4th: 0x61
5th: 0x35	6th: 0x64
7th: 0xAA	8th: 0xFF



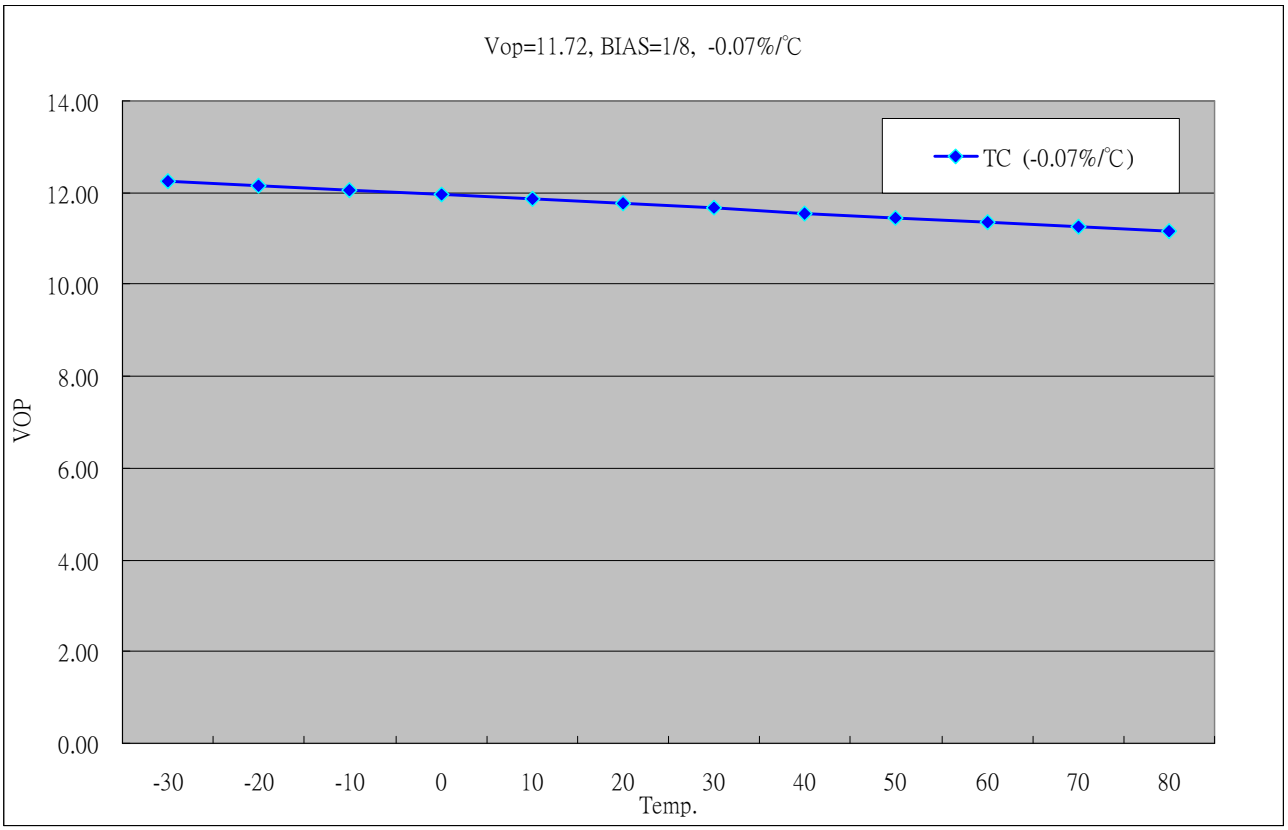
Setting example for -0.04%/℃ TC curve

COMMAND	
0xF4	
DATA	
1st: 0x01	1st: 0x01
3rd: 0x01	3rd: 0x01
5th: 0x01	5th: 0x01
7th: 0x01	7th: 0x01



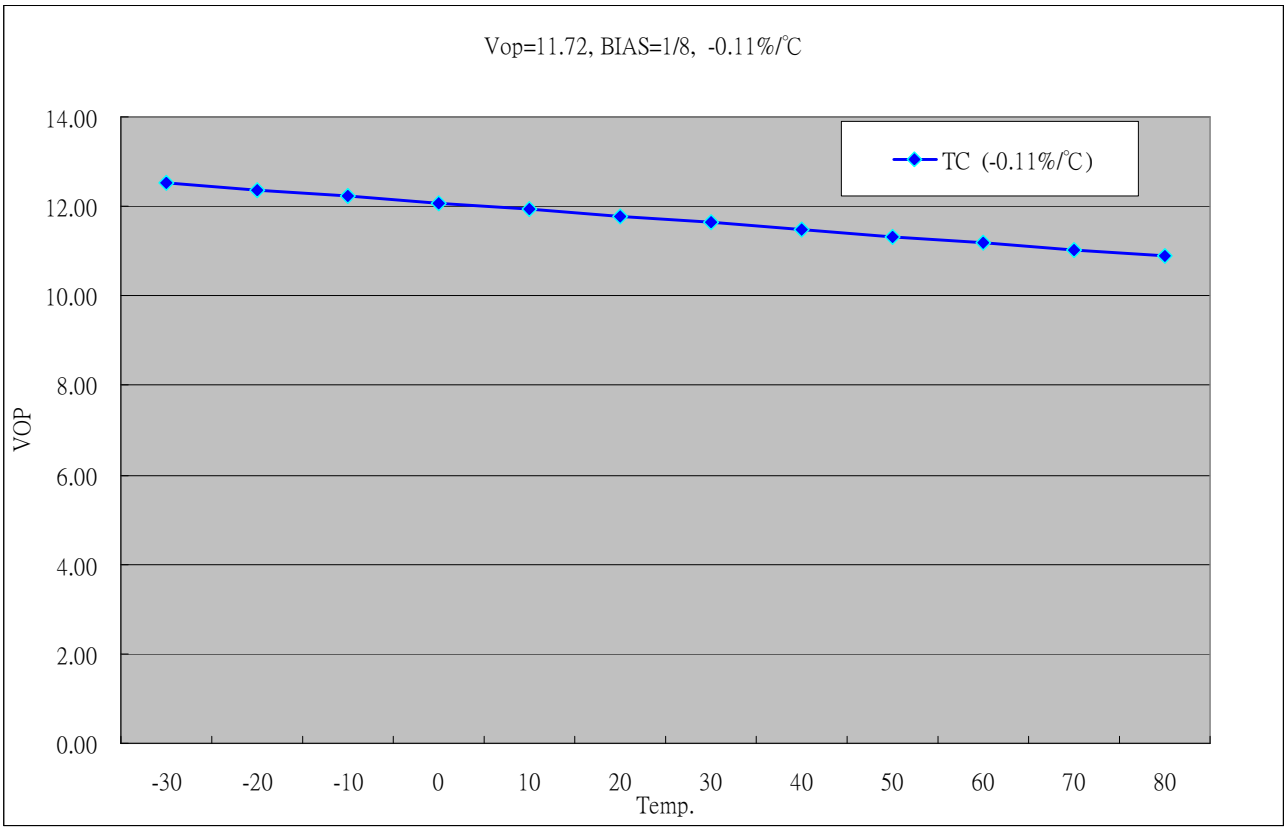
Setting example for -0.07%/℃ TC curve

COMMAND	
0xF4	
DATA	
1st: 0x02	1st: 0x02
3rd: 0x02	3rd: 0x02
5th: 0x02	5th: 0x02
7th: 0x02	7th: 0x02



-0.11%/℃ TC Curve example

COMMAND	
0xF4	
DATA	
1st: 0x03	1st: 0x03
3rd: 0x03	3rd: 0x03
5th: 0x03	5th: 0x03
7th: 0x03	7th: 0x03



V0 fine tuning

ST7628 has 2 commands for fine tuning V0. These commands are VopOfsetInc (see section 9.1.48) and VopOfsetDec (see section 9.1.49). When writing VopOfsetInc into IC for each time, V0 would increase 40mV; when writing VopOfsetDec into IC for each time, V0 would decrease 40mV.

Example:

Vop[8:0]=011010010

Vopoffset[8:0]=000000011

EV[6:0]=0111111

VopOfsetInc x2

→ V0=3.6 +(210 +3+ (63-63) +2 } x 0.04 =12.2 (V)

7.9.2 Voltage Follower Circuits

There is a built-in voltage follower circuits in ST7628 for generating Vg and Vm. These voltages are decided by bias ratio selection circuitry which is set by users with software to control 1/5 to 1/12 bias ratios to match the optimum display performance of LCD panel. Bias driving rule is listed below:

LCD bias	Vg	Vm
1/N bias	(2/N) x V0	(1/N) x V0

N=5 to 12

7.9.3 OTP Setting Flow

OTP Setting Flow

ST7628 provide the Write and Read function to write the Electronic Control value and Built-in resistance ratio into and read them from the built-in OTP. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.

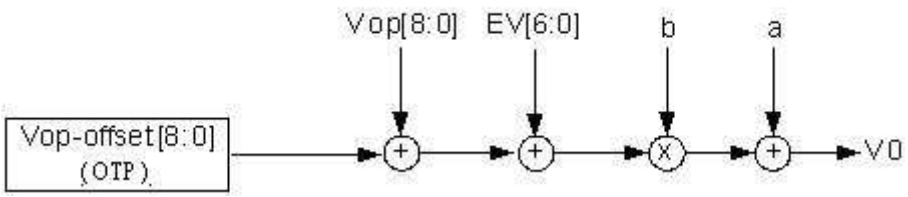


Figure 7.9 V0 value control for different modules by loading OTP offset

Note1: This setting flow is used for LCM assembler.

Note2: OTP shouldn't be written without preceding loading correctly from OTP to avoid some errors during IC operation.

Note3: When writing value to OTP, the voltage of VPP must be more than 7.5V(7.5V~7.75V); the current of Ivpp must be more than 4 mA.

Note4: If the OTP is exposed to a high temperature for hours, data in the memory cell may probably be lost before the data retention guarantee period. To retain data in the memory cell, keep the memory cell below 90℃. The data retention guarantee period is specified including the retention period.

7.9.4 Frquency Temperature Gradient Compensation Coefficient

ST7628 will auto-switch frame rate on different temperature such as Figure 11.1. TA, TB and TC are frame rate switching temperatures which can be defined by customer with command TMPRNG(see section 9.1.70). FA, FB, FC and FD are switched frame rate which also can be defined by customer with command FRMSEL (see section 9.1.68). The frame rate range is from 37.5Hz to 170Hz.

When the temperature is in increasing state, frame rate changes to the higher step at TA/TB/TC+TH(℃). When the temperature is in decreasing state, frame rate changes to the lower step at TA/TB/TC. For example: TC=10℃ and TH=5℃, FC switches to FD at 15℃ but FD switches to FC at 10℃. Please take Figure 11.1for reference.

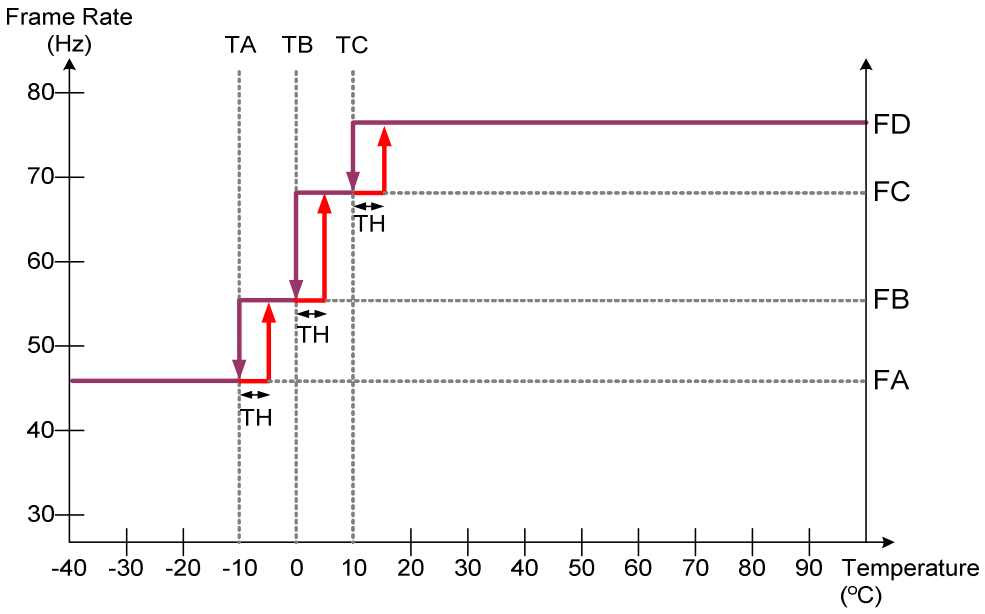


Figure 7.10

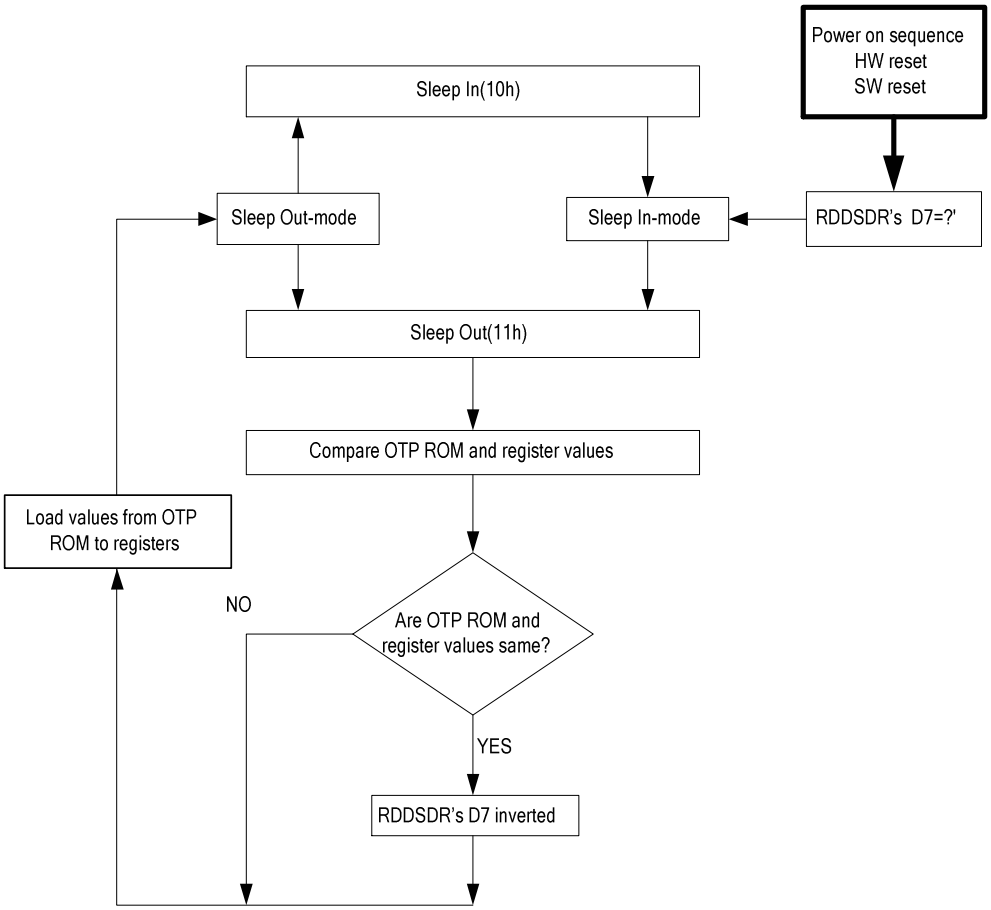
7.10 Sleep Out –Command and Self-Diagnostic Functions of the Display Module

7.10.1 Register loading Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP ROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the OTP ROM and register values of the display controller by the display controller (1st step: compares register and OTP ROM values, 2nd step: loads OTP ROM values to registers). If those both values (OTP ROM and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

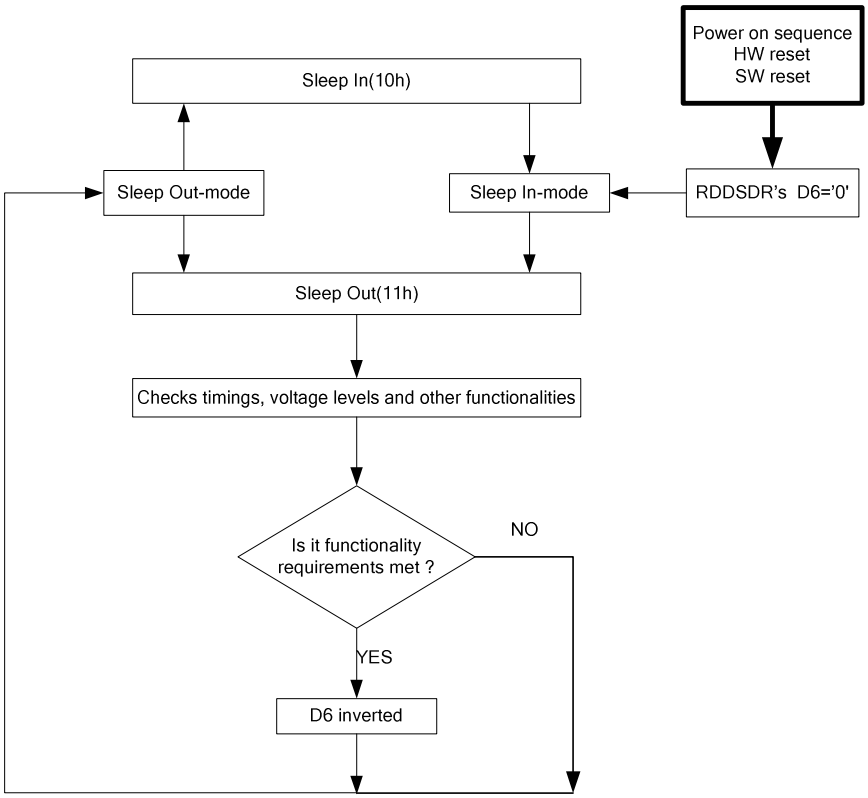


7.10.2 Functionality Detection

Sleep Out-command is a trigger for an internal function of the display module.

The internal function (= the display controller) is comparing if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1).

The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.

8. RESET value

Item	After Power On	After Software Reset	After Hardware Reset
Frame memory (RAM data)	Random	No Change	No Change
RDDID	45h,D2h,0Eh	45h,D2h,0Eh	45h,D2h,0Eh
RDDPM	08h	08h	08h
RDDMADCTR	00h	No Change	00h
RDDCOLMOD	05h (16-Bit/Pixel)	No Change	05h (16-Bit/Pixel)
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
Sleep In/Out	In	In	In
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
All Pixel Off mode	Disable	Disable	Disable
All Pixel On mode	Disable	Disable	Disable
Contrast (EV)	3Fh	3Fh	3Fh
Display On/Off	Display Off	Display Off	Display Off
Column: Start Address (XS)	00h	00h	00h
Column: End Address (XE)	45h	45h (when MV=0) 61h (when MV=1)	45h
Row: Start Address (YS)	00h	00h	00h
Row: End Address (YE)	45h	61h (when MV=0) 45h (when MV=1)	45h
Color set	Refer to Section 7.8	Contents of the look-up table protected	Refer to Section 7.8
Partial: Start Address (PS)	00h	00h	00h
Partial: End Address (PE)	61h	61h	61h
Scroll: Top Fixed Area (TFA)	00h	00h	00h
Scroll: Scroll Area (VSA)	46h	46h	46h
Scroll: Bottom Fixed Area (BFA)	00h	00h	00h
TE On/Off	Off	Off	Off
TE Mode	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control MY/MX/MV/ML/RGB)	0/0/0/0/0	No Change	No Change
Scroll Start Address (SSA)	00h	00h	00h
Idle Mode On/Off	Off	Off	Off
Interface Color Pixel Format (P)	05h (16Bit/Pixel)	No change	05h (16Bit/Pixel)
ID1[7:0]	45h	45h	45h
ID2[6:0]	D2h	D2h	D2h
ID3[7:0]	0Eh	0Eh	0Eh
Drive Duty	45h	45h	45h
First Common	00h	00h	00h
FOSC Divider	No division	No division	No division
Vop	0D2h	0D2h	0D2h
Vop Offset	0000h	0000h	0000h
Bias	1/10 Bias	1/10 Bias	1/10 Bias

Booster setting	8x	8x	8x
Booster Efficiency	01	01	01
Vg source	From VDD2x2	From VDD2x2	From VDD2x2
EPCTIN	0	0	0
OTP selection	Disable	Disable	Disable
Frame Frequency in Normal Color (FA/FB/FC/FD)	46Hz/61.5Hz/77Hz/82Hz	46Hz/61.5Hz/77Hz/82Hz	46Hz/61.5Hz/77Hz/82Hz
Frame Frequency in 8-Color (Idle) (F8A/F8B/F8C/F8D)	46Hz/61.5Hz/77Hz/82Hz	46Hz/61.5Hz/77Hz/82Hz	46Hz/61.5Hz/77Hz/82Hz
Temperature Range (TA/TB/TC)	-16℃/0℃/48℃	-16℃/0℃/48℃	-16℃/0℃/48℃
Temperature Hysteresis (TH)	5℃	5℃	5℃
TEMPSEL	Refer to 9.1.72	Refer to 9.1.72	Refer to 9.1.72

Note. Some of above default values can be modified by customer after OTP writing.

Please refer to OTPB related register list for the content of OTP.

9. INSTRUCTIONS

9.1 INSTRUCTION table

Command Table-1 , /EXT= H , L, or floating														
Hex	**Command**	**A0**	**/RD**	**/WR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Function**	**Ref**
(00h)	NOP	0	1	0	0	0	0	0	0	0	0	0	No Operation	9.1.1
(01h)	SWRESET	0	1	0	0	0	0	0	0	0	0	1	Software reset	9.1.2
(04h)	RDDID	0	1	0	0	0	0	0	0	1	0	0	Read Display ID	9.1.3
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	ID1 read (D23-D16)	
-		1	0	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	ID2 read (D15-D8)	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	ID3 read (D7-D0)	
(09h)	RDDST	0	1	0	0	0	0	0	1	0	0	1	Read Display Status	9.1.4
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	(D31-D24)	
-		1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	(D23-D16)	
-		1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	(D15-D8)	
-		1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	(D7-D0)	
(0Ah)	RDDPM	0	1	0	0	0	0	0	1	0	1	0	Read Display Power Mode	9.1.5
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	D2	0	0	-	
(0Bh)	RDDMADCTR	0	1	0	0	0	0	0	1	0	1	1	Read Display MADCTR	9.1.6
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	0	0	0	-	
(0Ch)	RDDCOLMOD	0	1	0	0	0	0	0	1	1	0	0	Read Display Pixel Format	9.1.7
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	0	0	0	0	0	D2	D1	D0	-	
(0Dh)	RDDIM	0	1	0	0	0	0	0	1	1	0	1	Read Display Image Mode	9.1.8
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	0	D5	D4	D3	0	0	0	-	
(0Eh)	RDDSM	0	1	0	0	0	0	0	1	1	1	0	Read Display Signal Mode	9.1.9
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	0	0	0	0	0	0	-	
(0Fh)	RDDSDR	0	1	0	0	0	0	0	1	1	1	1	Read Display Self-diagnostic result	9.1.10
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	D7	D6	D5	D4	0	0	0	0	-	

(10h)	SLPIN	0	1	0	0	0	0	1	0	0	0	0	Sleep in & booster off	9.1.11
(11h)	SLPOUT	0	1	0	0	0	0	1	0	0	0	1	Sleep out & booster on	9.1.12
(12h)	PTLON	0	1	0	0	0	0	1	0	0	1	0	Partial mode on	9.1.13
(13h)	NORON	0	1	0	0	0	0	1	0	0	1	1	Partial off (Normal)	9.1.14
(20h)	INVOFF	0	1	0	0	0	1	0	0	0	0	0	Display inversion off (normal)	9.1.15
(21h)	INVON	0	1	0	0	0	1	0	0	0	0	1	Display inversion on	9.1.16
(22h)	APOFF	0	1	0	0	0	1	0	0	0	1	0	All pixel off (Only for test purpose)	9.1.17
(23h)	APON	0	1	0	0	0	1	0	0	0	1	1	All pixel on (Only for test purpose)	9.1.18
(25h)	WRCNTR	0	1	0	0	0	1	0	0	1	0	1	Write contrast	9.1.19
-		1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	EV = 0 to 127	
(28h)	DISPOFF	0	1	0	0	0	1	0	1	0	0	0	Display off	9.1.20
(29h)	DISPON	0	1	0	0	0	1	0	1	0	0	1	Display on	9.1.21
(2Ah)	CASET	0	1	0	0	0	1	0	1	0	1	0	Column address set	9.1.22
		1	1	0	0	XS6	XS5	XS4	XS3	XS2	XS1	XS0	X_ADR start: 0≦XS≦61h	
		1	1	0	0	XE6	XE5	XE4	XE3	XE2	XE1	XE0	X_ADR end: XS≦XE ≦61h	
(2Bh)	RASET	0	1	0	0	0	1	0	1	0	1	1	Row address set	9.1.23
		1	1	0	0	YS6	YS5	YS4	YS3	YS2	YS1	YS0	Y_ADR start: 0≦YS≦45h	
		1	1	0	0	YE6	YE5	YE4	YE3	YE2	YE1	YE0	Y_ADR end: YS≦YE≦45h	
(2Ch)	RAMWR	0	1	0	0	0	1	0	1	1	0	0	Memory write	9.1.24
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data	
(2Dh)	RGBSET	0	1	0	0	0	1	0	1	1	0	1	Color set for 256 or 4k color display	9.1.25
-		1	1	0	-	-	R5	R4	R3	R2	R1	R0	Red tone (00000)	
-		1	1	0	:	:	:	:	:	:	:	:	: -	
-		1	1	0	-	-	R5	R4	R3	R2	R1	R0	Red tone (11111)	
-		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (000000)	
		1	1	0	:	:	:	:	:	:	:	:	: -	
		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (111111)	
		1	1	0	-	-	B5	B4	B3	B2	B1	B0	Blue tone (00000)	
		1	1	0	:	:	:	:	:	:	:	:	: -	
		1	1	0	-	-	B5	B4	B3	B2	B1	B0	Blue tone (11111)	
(2Eh)	RAMRD	0	1	0	0	0	1	0	1	1	1	0	Memory Read	9.1.26
		1	1	0	-	-	-	-	-	-	-	-	Dummy read	
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0		
(30h)	PTLAR	0	1	0	0	0	1	1	0	0	0	0	Partial start/end address set	9.1.27

-		1	1	0	0	PS6	PS5	PS4	PS3	PS2	PS1	PS0	Start address (0~69)	
-		1	1	0	0	PE6	PE5	PE4	PE3	PE2	PE1	PE0	End address (0~69)	
(33h)	SCRLAR	0	1	0	0	0	1	1	0	0	1	1	Scroll Area	9.1.28
-		1	1	0	0	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	TFA= 0~70	
-		1	1	0	0	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	VSA= 0~70	
-		1	1	0	0	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	BFA= 0~70	
(34h)	TEOFF	0	1	0	0	0	1	1	0	1	0	0	Tearing effect line off	9.1.29
(35h)	TEON	0	1	0	0	0	1	1	0	1	0	1	Tearing effect mode set & on	9.1.30
-		1	1	0	-	-	-	-	-	-	-	M	“0”: mode1, “1”: mode2	
(36h)	MADCTR	0	1	0	0	0	1	1	0	1	1	0	Memory data access control	9.1.31
-		1	1	0	MY	MX	MV	ML	RGB	-	-	-	-	
(37h)	VSCSAD	0	1	0	0	0	1	1	0	1	1	1	Scroll start address of RAM	9.1.32
		1	1	0	0	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	SSA = 0~69	
(38h)	IDMOFF	0	1	0	0	0	1	1	1	0	0	0	Idle mode off	9.1.33
(39h)	IDMON	0	1	0	0	0	1	1	1	0	0	1	Idle mode on	9.1.34
(3Ah)	COLMOD	0	1	0	0	0	1	1	1	0	1	0	Interface pixel format	9.1.35
-		1	1	0	-	-	-	-	-	P2	P1	P0	Interface format	
(DAh)	RDID1	0	1	0	1	1	0	1	1	0	1	0	Read ID1	9.1.36
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	(D7-D0)	
(DBh)	RDID2	0	1	0	1	1	0	1	1	0	1	1	Read ID2	9.1.37
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	(D7-D0)	
(DCh)	RDID3	0	1	0	1	1	0	1	1	1	0	0	Read ID3	9.1.38
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	(D7-D0)	

Note 1: When /EXT connects to H or floating, commands which are not defined in “Command Table-1” are treated as NOP (00H) command.

Note 2: Commands 10H, 12H, 13H, 20H, 21H, 25H, 28H, 29H, 30H, 36H (Bit ML only), 38H and 39H are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects.

During Sleep In mode, these commands are updated immediately.

Read status (09H), Read Display Power Mode (0AH), Read Display MADCTR (0BH), Read Display Pixel Format (0CH), Read Display Image Mode (0DH), Read Display Signal Mode (0EH) and Read Display Self Diagnostic Result (0FH) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

Command Table-2 , /EXT= L

Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(B0h)	DutySet	0	1	0	1	0	1	1	0	0	0	0	Display Duty setting	9.1.39
		1	1	0	0	Du6	Du5	Du4	Du3	Du2	Du1	Du0		
(B1h)	FirstCom	0	1	0	1	0	1	1	0	0	0	1	First Com. Page address	9.1.40
		1	1	0	-	F6	F5	F4	F3	F2	F1	F0		
(B3h)	OscDiv	0	1	0	1	0	1	1	0	0	1	1	FOSC divider	9.1.41
		1	1	0	-	-	-	-	-	-	CLD1	CLD0		
(B4h)	PTLMOD	0	1	0	1	0	1	1	0	1	0	0	Partial Saving Power Mode Selection	9.1.42
		1	1	0	PTLM	0	0	1	1	0	0	0		
(B5h)	NLInvSet	0	1	0	1	0	1	1	0	1	0	1	N-line control	9.1.43
		1	1	0	M	N6	N5	N4	N3	N2	N1	N0		
(B7h)	ComScanDir	0	1	0	1	0	1	1	0	1	1	1	Com/Seg Scan Direction for Glass layout	9.1.44
		1	1	0	SMY	SMX	SINV	SML	SBGR	-	-	-		
(B8h)	RmwIn	0	1	0	1	0	1	1	1	0	0	0	read modify write control IN	9.1.45
(B9h)	RmwOut	0	1	0	1	0	1	1	1	0	0	1	read modify write control Out	9.1.46
(C0h)	VopSet	0	1	0	1	1	0	0	0	0	0	0	Vop setting	9.1.47
		1	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0		
		1	1	0	-	-	-	-	-	-	-	Vop8		
(C1h)	VopOfsetInc	0	1	0	1	1	0	0	0	0	0	1	+40mv/setp	9.1.48
(C2h)	VopOfsetDec	0	1	0	1	1	0	0	0	0	1	0	-40mv/setp	9.1.49
(C3h)	BiasSel	0	1	0	1	1	0	0	0	0	1	1	Bias selection	9.1.50
		1	1	0	-	-	-	-	-	Bias2	Bias1	Bias0		
(C4h)	BstBmpXSel	0	1	0	1	1	0	0	0	1	0	0	Booster setting	9.1.51
		1	1	0	-	-	-	-	-	BST2	BST 1	BST0		
(C5h)	BstEffSel	0	1	0	1	1	0	0	0	1	0	1	Booster efficiency selection	9.1.52
		1	1	0	-	-	1	0	-	-	BTF1	BTF0		
(C7h)	VopOffset	0	1	0	1	1	0	0	0	1	1	1	Vop offset fuse bit adjust	9.1.53
		1	1	0	VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0		
		1	1	0	-	-	-	-	-	-	-	VOS8		
(CBh)	VgSorcSel	0	1	0	1	1	0	0	1	0	1	1	FV3 with Booster x2 control	9.1.54

		1	1	0	-	-	-	-	-	-	-	2BT0		
(CCh)	ID1Set	0	1	0	1	1	0	0	1	1	0	0	ID1 setting	9.1.55
		1	1	0	ID1_7	ID1_6	ID1_5	ID1_4	ID1_3	ID1_2	ID1_1	ID1_0		
(CDh)	ID2Set	0	1	0	1	1	0	0	1	1	0	1	ID2 setting	9.1.56
		1	1	0	1	ID2_6	ID2_5	ID2_4	ID2_3	ID2_2	ID2_1	ID2_0		
(CEh)	ID3Set	0	1	0	1	1	0	0	1	1	1	0	ID3 setting	9.1.57
		1	1	0	ID3_7	ID3_6	ID3_5	ID3_4	ID3_3	ID3_2	ID3_1	ID3_0		
(D0h)	ANASET	0	1	0	1	1	0	0	0	0	0	0	Analog circuit setting	9.1.58
		1	1	0	0	0	0	1	1	1	0	1		
(D7h)	AutoLoadSet	0	1	0	1	1	0	1	0	1	1	1	mask rom data auto re-load control	9.1.59
		1	1	0	EXTE	OTPBE	0	ARD	1	1	1	1		
(DEh)	RDTstStatus	0	1	0	1	1	0	1	1	1	1	0	read IC status	9.1.60
		1	0	1	-	-	-	-	-	-	-	-	Dummy Read	
		1	0	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	OTP / RDA / PWR_VOP read control	
(E0h)	EPCTIN	0	1	0	1	1	1	0	0	0	0	0	Control OTP WR/RD	9.1.61
		1	1	0	0	0	WR /XRD	0	0	0	0	0		
(E1h)	EPCTOUT	0	1	0	1	1	1	0	0	0	0	1	OTP control cancel	9.1.62
(E2h)	EPMWR	0	1	0	1	1	1	0	0	0	1	0	Write to OTP	9.1.63
(E3h)	EPMRD	0	1	0	1	1	1	0	0	0	1	1	Read from OTP	9.1.64
(E4h)	OTPSEL	0	1	0	1	1	1	0	0	1	0	0	Select OTP	9.1.65
		1	1	0	MS1	MS0	0	1	1	0	0	0		
(E5h)	ROMSET	0	1	0	0	1	1	1	0	1	0	1	Programmable rom setting	9.1.66
		1	1	0	0	0	0	0	1	0	0	1		
(E6h)	StusRDSEL	0	1	0	1	1	1	0	0	1	1	0	Fuse data readout control	9.1.66
		1	1	0	-	-	-	-	STU3	STU2	STU1	STU0		
(F0h)	FRMSEL	0	1	0	1	1	1	1	0	0	0	0	Frame Freq. in Temp range A,B,C and D	9.1.68
		1	1	0	-	-	-	FA4	FA3	FA2	FA1	FA0		
		1	1	0	-	-	-	FB4	FB3	FB2	FB1	FB0		
		1	1	0	-	-	-	FC4	FC3	FC2	FC1	FC0		
		1	1	0	-	-	-	FD4	FD3	FD2	FD1	FD0		
(F1h)	FRM8SEL	0	1	0	1	1	1	1	0	0	0	1	Frame Freq. in Temp range A,B,C and D (idle)	9.1.69

		1	1	0	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0		
		1	1	0	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0		
		1	1	0	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0		
		1	1	0	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0		
(F2h)	TMPRNG	0	1	0	1	1	1	1	0	0	1	0	Temp range A,B and C	9.1.70
		1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0		
		1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0		
		1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0		
(F3h)	TMPHYS	0	1	0	1	1	1	1	0	0	1	1	Hysteresis value set	9.1.71
		1	1	0	-	-	-	-	TH3	TH2	TH1	TH0		
(F4h)	TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	TEMPSEL	9.1.72
		1	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00		
		1	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20		
		1	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40		
		1	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60		
		1	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80		
		1	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0		
		1	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0		
		1	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0		
(F7h)	THYS	0	1	0	1	1	1	1	0	1	1	1	Temperature detection threshold	9.1.73
		1	1	0	THYS7	THYS6	THYS5	THYS4	THYS3	THYS2	THYS1	THYS0		
(F9h)	Frame Set	0	1	0	1	1	1	1	1	0	0	1	Set Frame RGB PWM value	9.1.74
		1	1	0	-	-	-	P14	P13	P12	P11	P10		
		1	1	0	-	-	-	P24	P23	P22	P21	P20		
		:	:	:	:	:	:	:	:	:	:	:		
		1	1	0	-	-	-	P154	P153	P152	P151	P150		
		1	1	0	-	-	-	P164	P163	P162	P161	P160		

OTPB related register list

function	Register	function	Register	function	Register
Bias[2:0]	0xC3[2:0]	BstPumpX[2:0]	0xC4[2:0]	BstFreq[1:0]	0xC5[1:0]
Bst2_XEVD	0xCB[0]	ID1[7:0]	0xCC[7:0]	ID3[7:0]	0xCE[7:0]
SMY	0xB7[7]	SMX	0xB7[6]	SBGR	0xB7[3]

OTP related register list

function	Register	function	Register	function	Register
PTLMOD	0xB4[7]	NLMod[7], N_line[6:0]	0xB5[7:0]	VopOfst1[8:0]	0xC7[8:0]
ID2[6:0]	0xCD[6:0]	ExtCmdEn	0xD7[7]	OTPBEn	0xD7[6]

9.1.1 NOP(00h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
NOP	0	1	0	0	0	0	0	0	0	0	0	**(00h)**
Parameter	No Parameter											

Description	This command is empty command. It does not have effect on the display module. However it can be used to terminate RAM data write as described in RAMWR (Memory Write) and parameter write commands.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	-

9.1.2 SWRESET: Software Reset(01h)

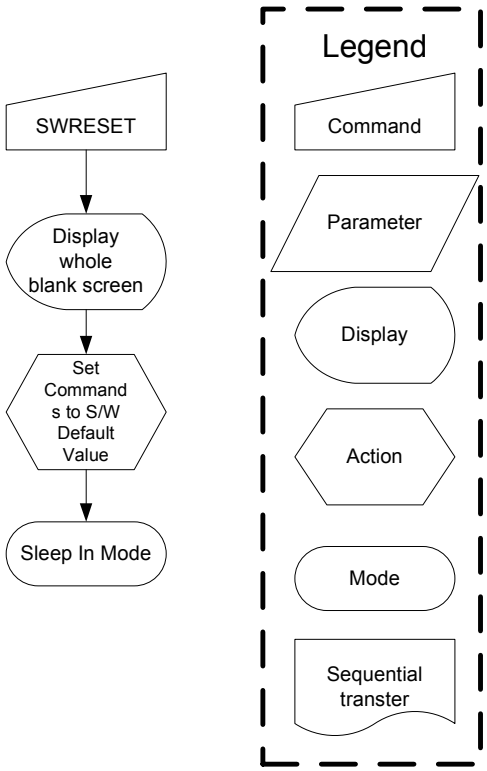
Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
SWRESET	0	1	0	0	0	0	0	0	0	0	1	**(01h)**
Parameter	No Parameter											

Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all segment & common outputs are set to Vm (display off: blank display). (See default tables in each command description) *Note: The Frame Memory contents are not affected by this command.*
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. Software Reset command cannot be sent during Sleep Out sequence.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	

SWRESET
Display whole blank screen
Set Command s to S/W Default Value
Sleep In Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.3 RDDID: Read Display ID (04h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDDID	0	1	0	0	0	0	0	0	1	0	0	**(04h)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
3rd parameter	1	0	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
4th parameter	1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-" Don't care

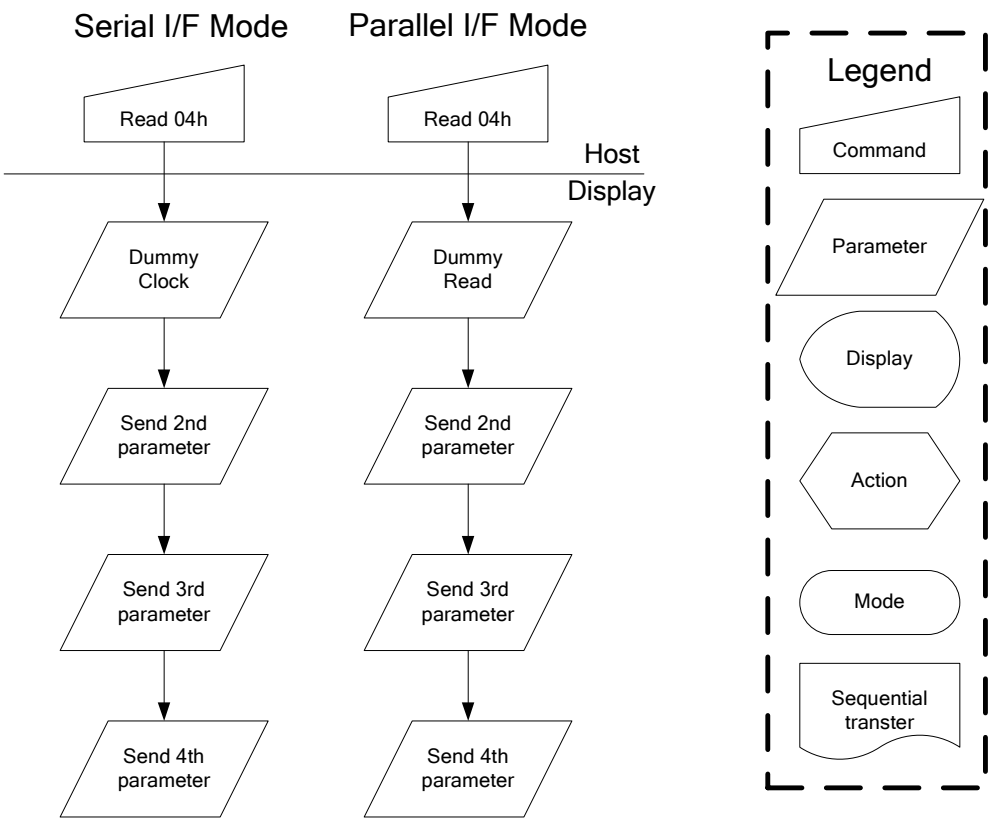
Description	This read byte returns 24-bit display identification information. The 1st parameter is dummy data The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID. The 3rd parameter (ID26 to ID20): LCD module/driver version ID The 4th parameter (ID37 to ID30): LCD module/driver ID. *NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.*
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	45h	D2h	0Eh
S/W Reset	45h	D2h	0Eh
H/W Reset	45h	D2h	0Eh

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read 04h
Read 04h
Host
Display
Dummy Clock
Dummy Read
Send 2nd parameter
Send 2nd parameter
Send 3rd parameter
Send 3rd parameter
Send 4th parameter
Send 4th parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.4 RDDST: Read Display Status (09h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDDST	0	1	0	0	0	0	0	1	0	0	1	**(09h)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-
3rd parameter	1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-
4th parameter	1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-
5th parameter	1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
ST31	Booster Voltage Status	"1"=Booster on, "0"=off
ST30	Row Address Order (MY)	"1"=Decrement, "0"=Increment
ST29	Column Address Order (MX)	"1"=Decrement, "0"=Increment
ST28	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
ST27	Scan Address Order (ML)	"1"=Decrement, "0"=Increment
ST26	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB
ST25	Not Used	"0"
ST24	Not Used	"0"
ST23	Not Used	"0"
ST22 ST21 ST20	Interface Color Pixel Format Definition	"010" = 8-bit / pixel, "011" = 12-bit / pixel type A "100" = 12-bit / pixel type B "101" = 16-bit / pixel, "110" = 18-bit / pixel, "111" = 24-bit / pixel,
ST19	Idle Mode On/Off	"1" = On, "0" = Off
ST18	Partial Mode On/Off	"1" = On, "0" = Off
ST17	Sleep In/Out	"1" = Out, "0" = In
ST16	Display Normal Mode On/Off	"1" = Normal Display, "0" = Partial Display
ST15	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
ST14	Not Used	"0"
ST13	Inversion Status	"1" = On, "0" = Off
ST12	All Pixels On	"1" = mode On, "0" = mode Off
ST11	All Pixels Off	"1" = mode On, "0" = mode Off
ST10	Display On/Off	"1" = On, "0" = Off
ST9	Tearing effect line on/off	"1" = On, "0" = Off
ST8	Not Used	"0"
ST7	Not Used	"0"
ST6	Not Used	"0"
ST5	Tearing effect line mode	"0" = mode1, "1" = mode2
ST4	Not Used	"0"
ST3	Not Used	"0"
ST2	Not Used	"0"
ST1	Not Used	"0"

	ST0	Not Used	“0”

Restriction

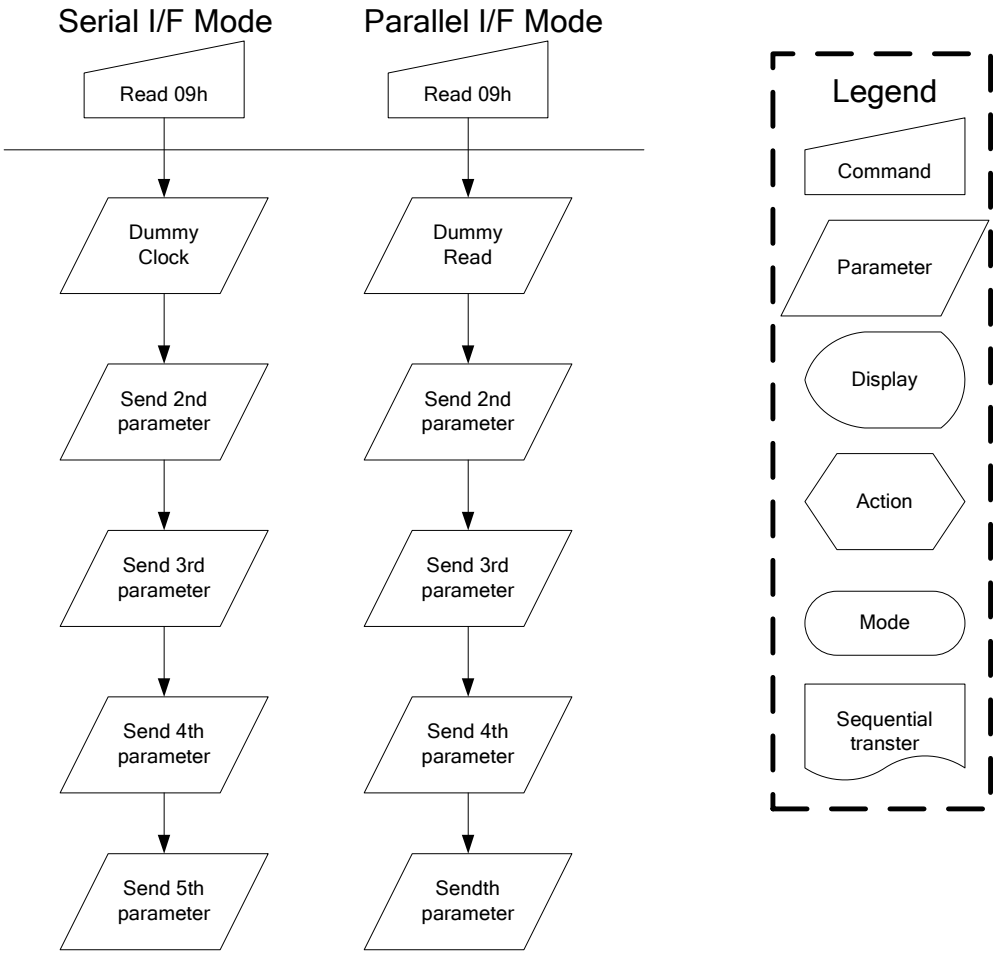
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (ST31 to ST0)
Power On Sequence	0000 0000_0101 0001_0000 0000_0000 0000
S/W Reset	0xxx xx00_0xxx 0001_0000 0000_0000 0000
H/W Reset	0000 0000_0101 0001_0000 0000_0000 0000

Flow Chart



9.1.5 RDDPM: Read Display Power Mode (0Ah)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDDPM	0	1	0	0	0	0	0	1	0	1	0	**(0Ah)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	D5	D4	D3	D2	0	0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	"1"=Booster on, "0"=Booster off
D6	Idle Mode On/Off	"1" = Idle Mode On, "0" = Idle Mode Off
D5	Partial Mode On/Off	"1" = Partial Mode On, "0" = Partial Mode
D4	Sleep In/Out	"1" = Sleep Out, "0" = Sleep In
D3	Display Normal Mode On/Off	"1" = Normal Display, "0" = Partial Display
D2	Display On/Off	"1" = Display On, "0" = Display Off
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

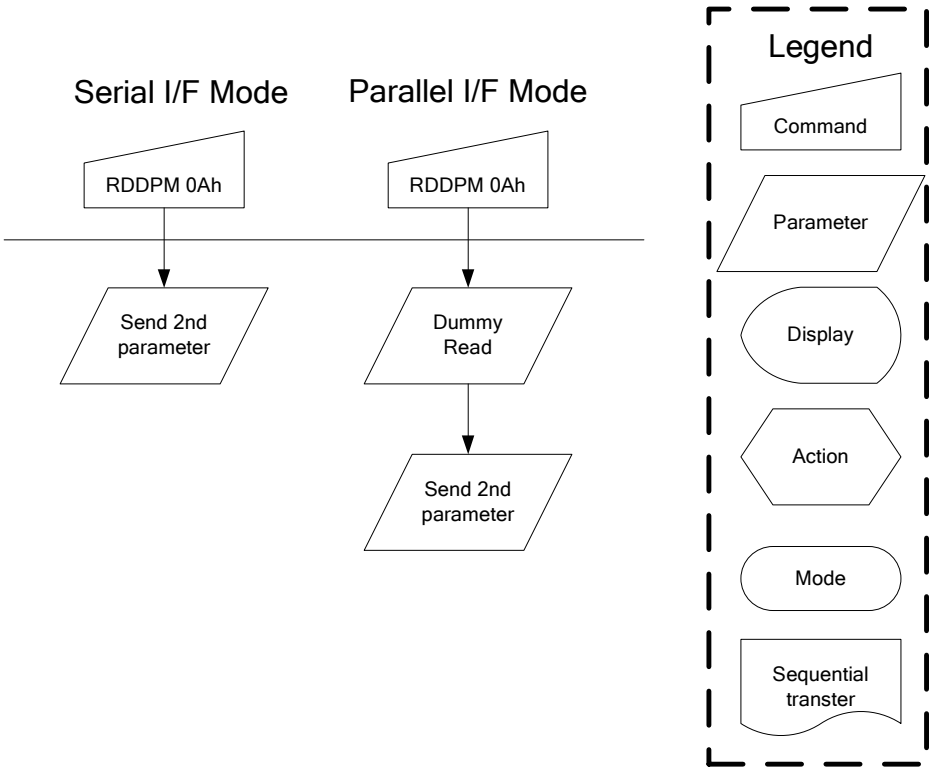
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D[7:0])
Power On Sequence	0000_1000 (08h)
S/W Reset	0000_1000 (08h)
H/W Reset	0000_1000 (08h)

Flow Chart


Serial I/F Mode
Parallel I/F Mode
RDDPM 0Ah
RDDPM 0Ah
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.6 RDDMADCTR: Read Display MADCTR (0Bh)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDDMADCTR	0	1	0	0	0	0	0	1	0	1	1	**(0Bh)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	D5	D4	D3	0	0	0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Row Address Order (MY)	"1"=Decrement, "0"=Increment
D6	Column Address Order (MX)	"1"=Decrement, "0"=Increment
D5	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
D4	Scan Address Order (ML)	"1"=Decrement, "0"=Increment
D3	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

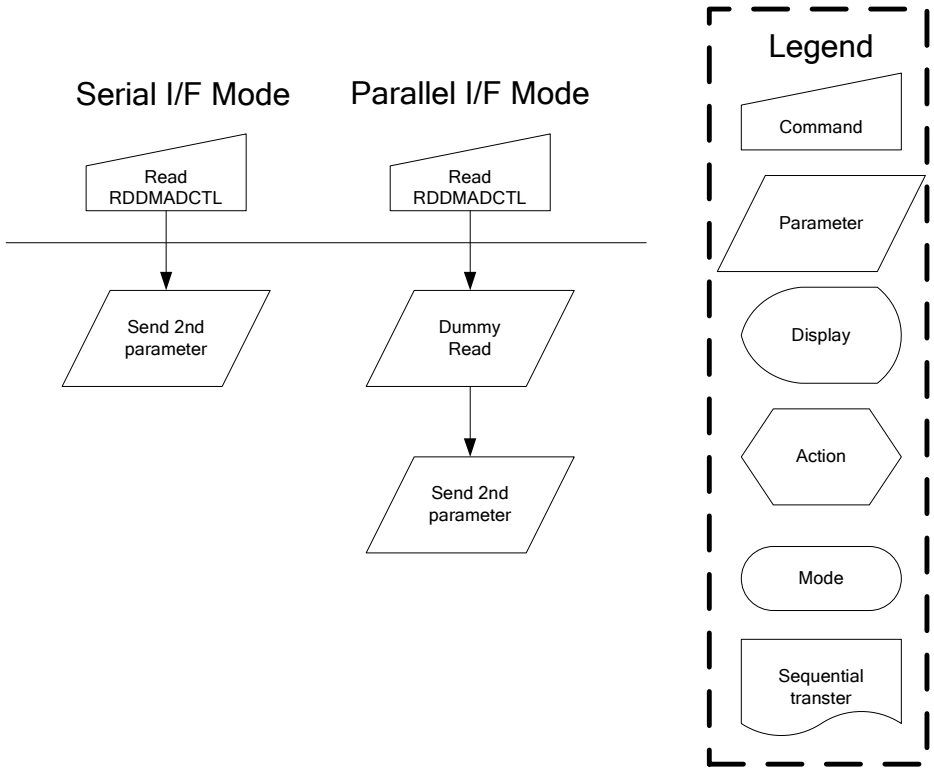
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D[7:0])
Power On Sequence	0000_1011 (0Bh)
S/W Reset	No change
H/W Reset	0000_1011 (0Bh)

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read RDDMADCTL
Read RDDMADCTL
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.7 RDDCOLMOD: Read Display Pixel Format (0Ch)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDDCOLMOD	0	1	0	0	0	0	0	1	1	0	0	**(0Ch)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	0	0	0	0	0	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	RGB Interface Color Format	"0" (Not Used)
D6		"0" (Not Used)
D5		"0" (Not Used)
D4		"0" (Not Used)
D3	Control Interface Color Format	"0"
D2		"010"=8 bit/pixel "011"=12 bit/pixel (type A) "100"=12 bit/pixel (type B) "101"=16 bit/pixel "110"=18 bit/pixel "111"=24 bit/pixel
D1		
D0		

Restriction

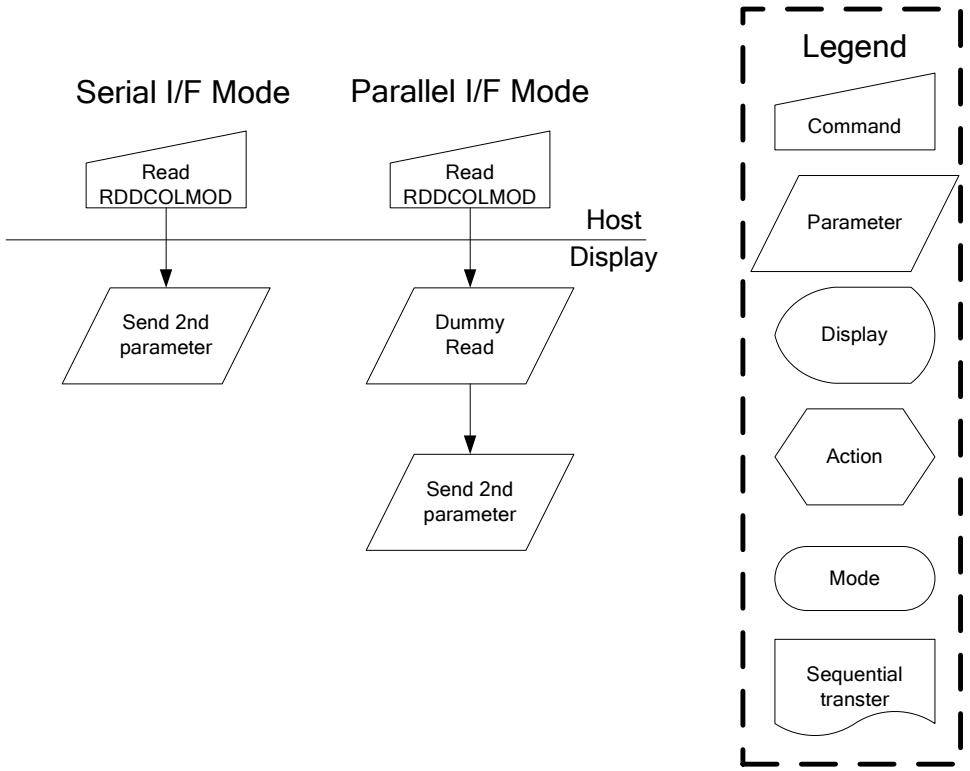
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D[7:0])
Power On Sequence	0000_0101 (05h)
S/W Reset	No change
H/W Reset	0000_0101 (05h)

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read RDDCOLMOD
Read RDDCOLMOD
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.8 RDDIM: Read Display Image Mode (0Dh)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDDIM	0	1	0	0	0	0	0	1	1	0	1	**(0Dh)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	0	D5	D4	D3	0	0	0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Vertical Scrolling On/Off	"1" = Vertical scrolling is On, "0" = Vertical scrolling is Off
D6	Horizontal Scrolling On/Off	"0" (Not used)
D5	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	All Pixels On	"1" = All Pixels On, "0" = Normal Mode
D3	All Pixels Off	"1" = All Pixels Off, "0" = Normal Mode
D2	Undefine	Undefine
D1		
D0		

Restriction

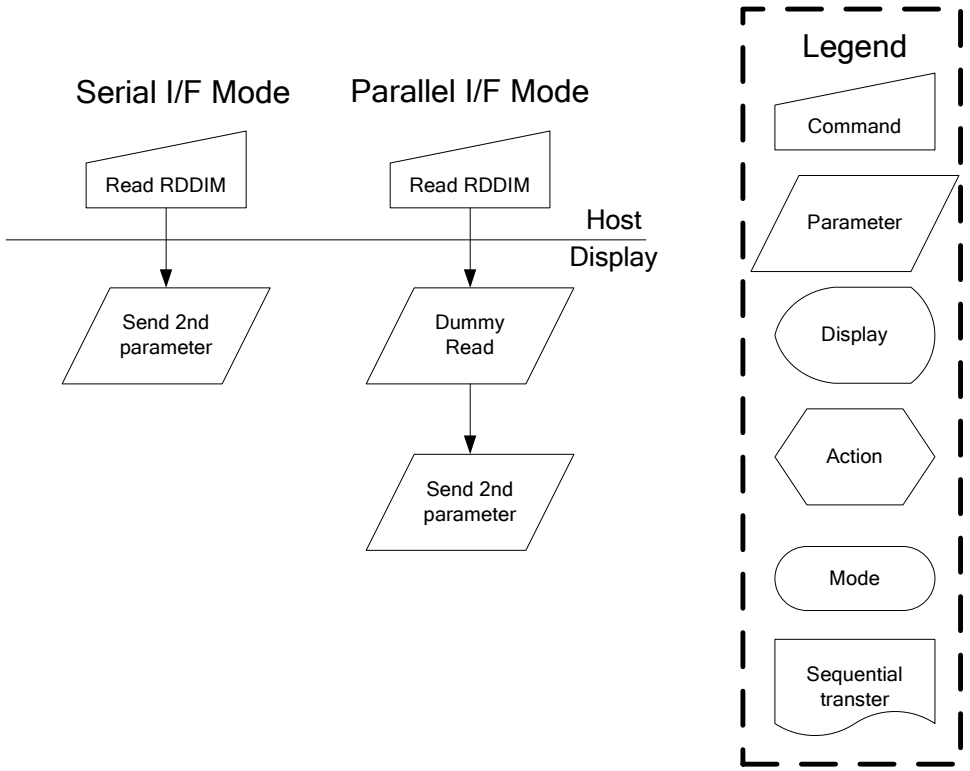
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D[7:0])
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read RDDIM
Read RDDIM
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.9 RDDSM: Read Display Signal Mode (0Eh)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDDSM	0	1	0	0	0	0	0	1	1	1	0	**(0Eh)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	0	0	0	0	0	0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	"1" = On, "0" = Off
D6	Tearing effect line mode	"0" = mode1, "1" = mode2
D5	Horizontal Sync. (RGB I/F) On/Off	"0" (Not Used)
D4	Vertical Sync. (RGB I/F) On/Off	"0" (Not Used)
D3	Pixel Clock (DCK, RGB I/F) On/Off	"0" (Not Used)
D2	Data Enable (ENABLE, RGB I/F)	"0" (Not Used)
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

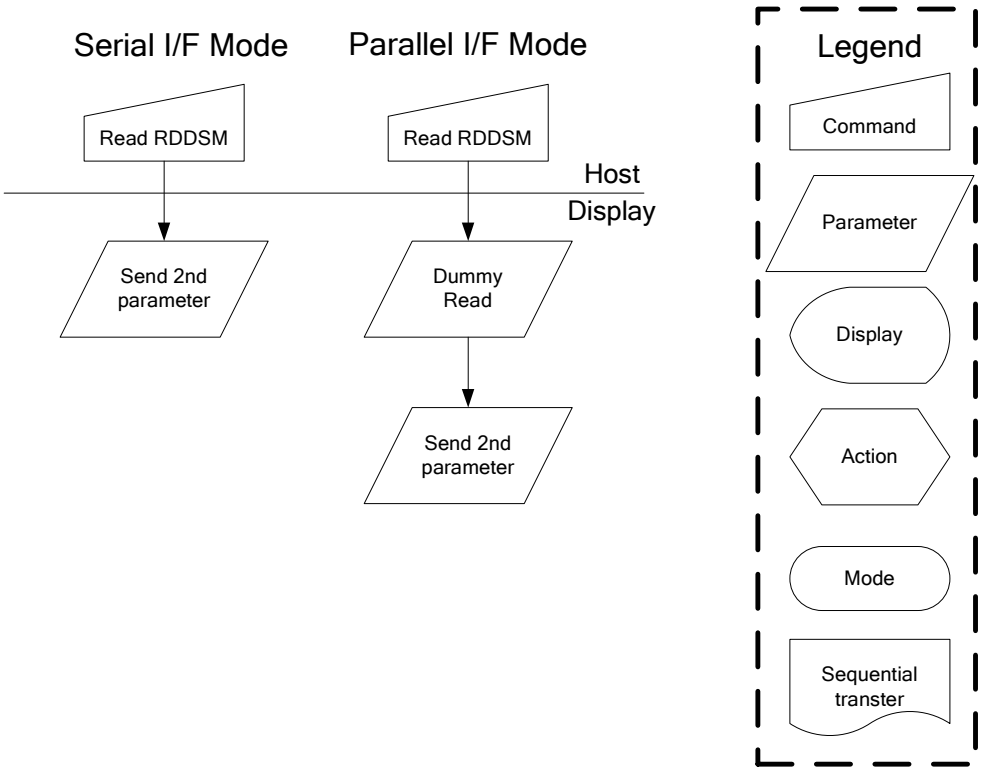
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D[7:0])
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read RDDSM
Read RDDSM
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.10 RDDSDR: Read Display Self-Diagnostic Result (0Fh)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDDSDR	0	1	0	0	0	0	0	1	1	1	1	**(0Fh)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	D5	D4	0	0	0	0	

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Register Loading Detection	See section 7.10
D6	Functionality Detection	
D5	Chip Attachment Detection	
D4	Display Glass Break Detection	
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

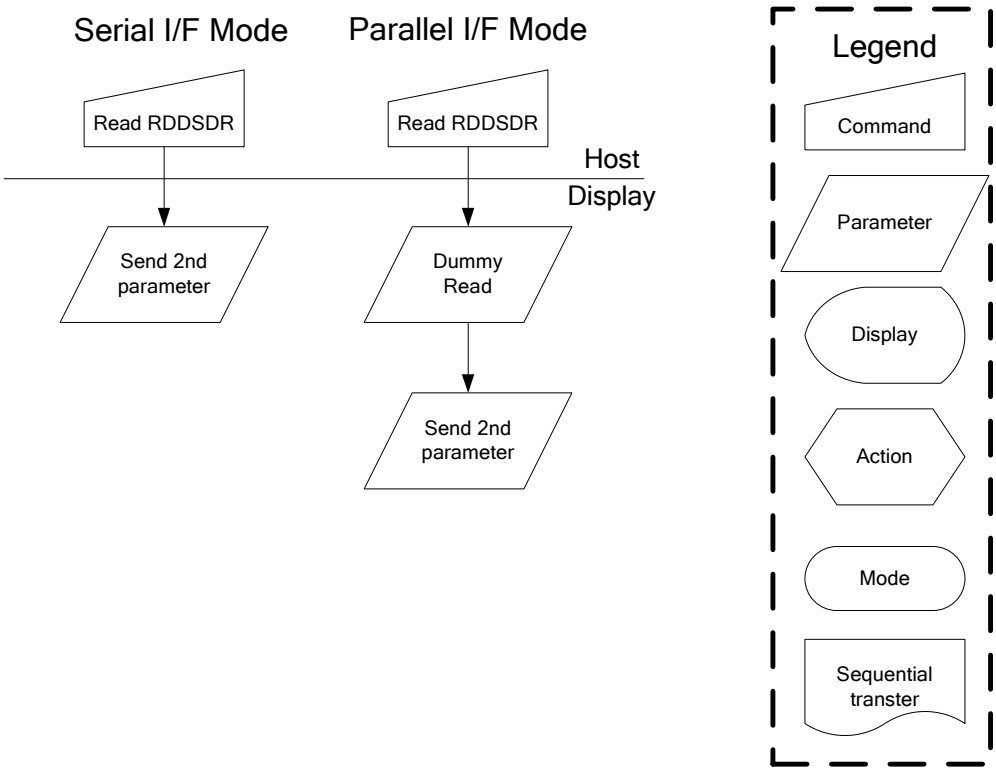
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D[7:0])
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read RDDSDR
Read RDDSDR
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

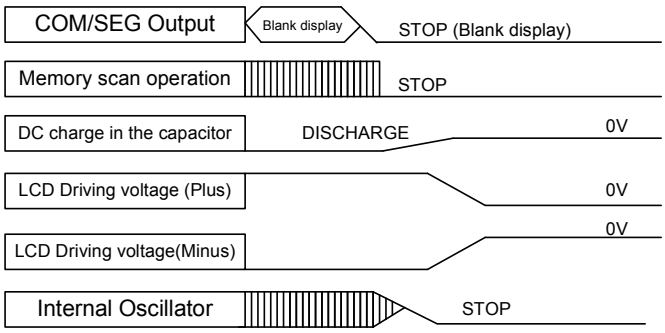
9.1.11 SLPIN: Sleep In (10h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
SLPIN	0	1	0	0	0	0	1	0	0	0	0	**(10h)**
Parameter	No Parameter											

Description

This command causes the LCD module to enter the minimum power consumption mode.

In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



MCU interface and memory are still working and the memory keeps its contents

Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).

It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

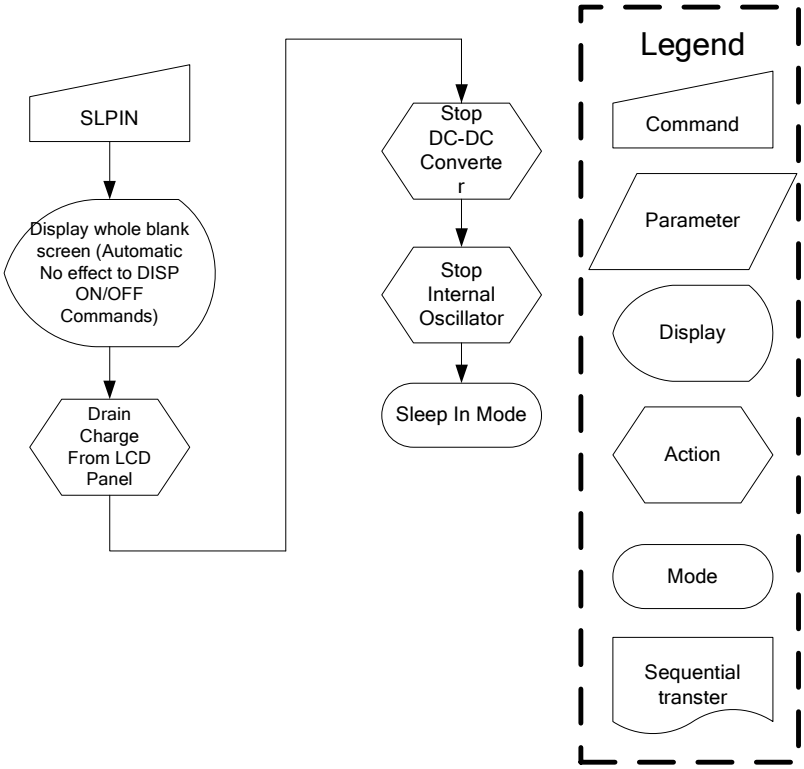
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

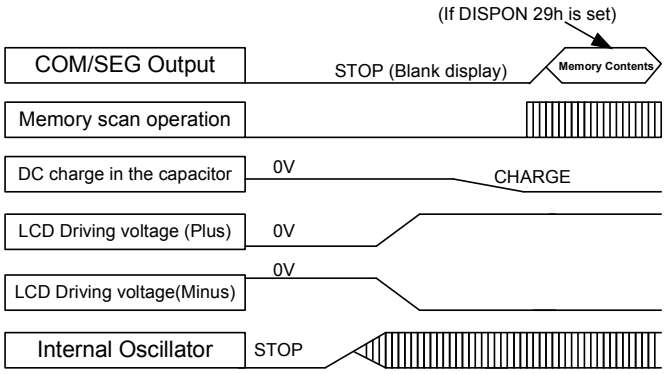
Flow Chart	It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (09h) command Bit31. 

9.1.12 SLPOUT: Sleep Out (11h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
SLPOUT	0	1	0	0	0	0	1	0	0	0	1	**(11h)**
Parameter	No Parameter											

Description

This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



Restriction

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).

It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.

The display module is doing self-diagnostic functions during this 5msec. See also section 7.10.

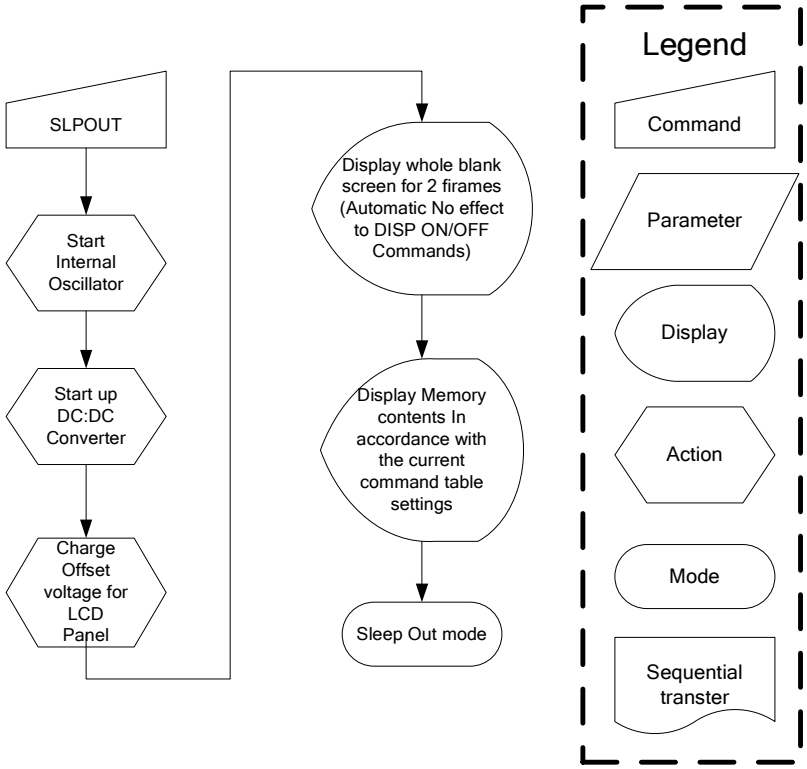
It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. The results of booster on can be check by RDDST (09h) command Bit31. 

9.1.13 PTLON: Partial Display Mode On (12h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
PTLON	0	1	0	0	0	0	1	0	0	1	0	**(12h)**
Parameter	No Parameter											

Description	This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H) Exit from PTLON by Normal Display Mode On command (13H) There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Partial mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Partial mode off
S/W Reset	Partial mode off
H/W Reset	Partial mode off

Flow Chart	See Partial Area (30h)

9.1.14 NORON: Normal Display Mode On (13h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
NORON	0	1	0	0	0	0	1	0	0	1	1	**(13h)**
Parameter	No Parameter											

Description	This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off. Exit from NORON by the Partial mode On command (12h) There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command

9.1.15 INVOFF: Display Inversion Off (20h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
INVOFF	0	1	0	0	0	1	0	0	0	0	0	**(20h)**
Parameter	No Parameter											

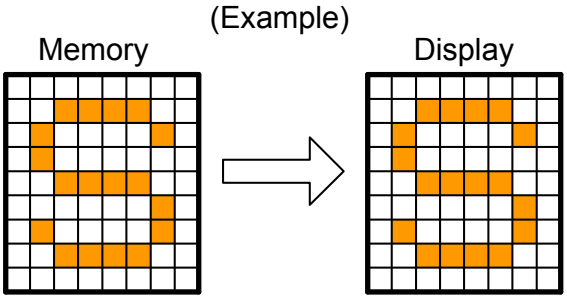
Description

This command is used to recover from display inversion mode.

This command makes no change of contents of frame memory.

This command does not change any other status.

(Example)



Restriction

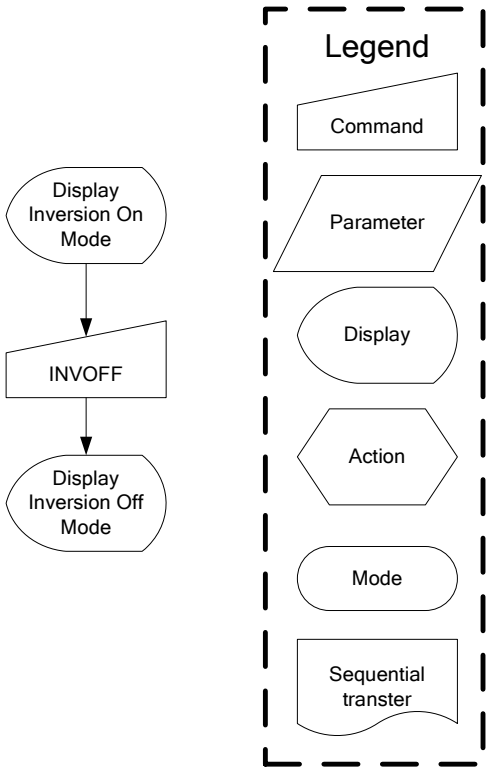
This command has no effect when module is already inversion off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart	 Display Inversion On Mode INVOFF Display Inversion Off Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.16 INVON: Display Inversion On (21h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
INVON	0	1	0	0	0	1	0	0	0	0	1	**(21h)**
Parameter	No Parameter											

Description

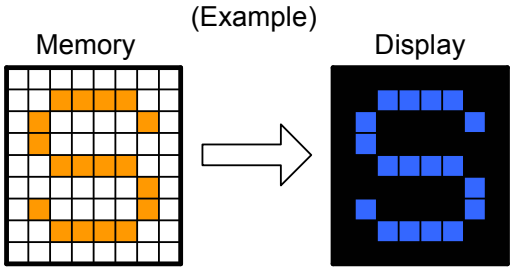
This command is used to enter into display inversion mode

This command makes no change of contents of frame memory.

This command does not change any other status.

To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

(Example)



Restriction

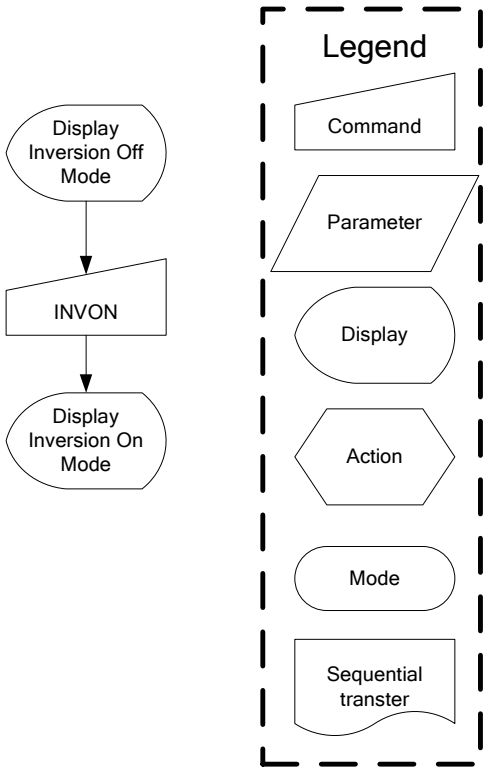
This command has no effect when module is already Inversion On mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart	 Display Inversion Off Mode INVON Display Inversion On Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.17 APOFF: All Pixels Off (22h) (Only for Test Purposes)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
APOFF	0	1	0	0	0	1	0	0	0	1	0	**(22h)**
Parameter	No Parameter											

Description

This command is only used for test purpose e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software.

All driver outputs become “Low” data state and display becomes black.

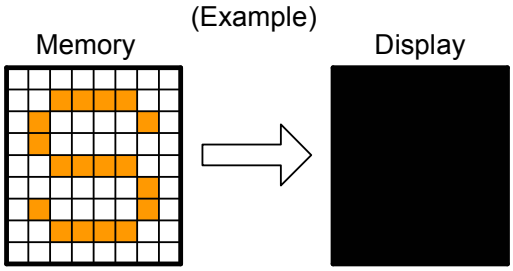
This command makes no change of contents of display memory.

This command does not change any other status.

Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”.

The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands.

(Example)



Restriction

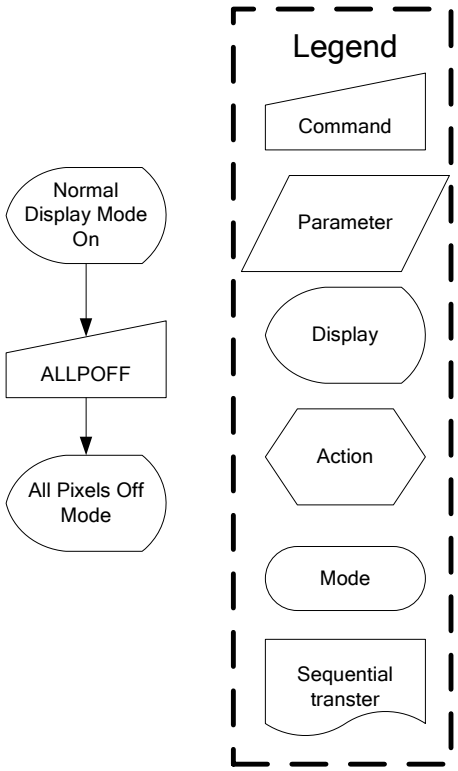
This command has no effect when module is already All Pixel Off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All pixel off mode disable
S/W Reset	All pixel off mode disable
H/W Reset	All pixel off mode disable

Flow Chart	 Normal Display Mode On ALLPOFF All Pixels Off Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.18 APON: All Pixels On (23h) (Only for Test Purposes)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
APON	0	1	0	0	0	1	0	0	0	1	1	**(23h)**
Parameter	No Parameter											

Description

This command is only used for test purpose e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software.

All driver outputs become “High” data state and display becomes white.

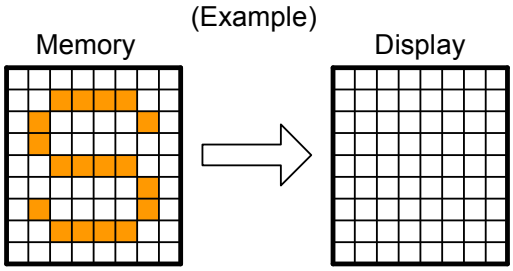
This command makes no change of contents of display memory.

This command does not change any other status.

Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”.

The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands.

(Example)



Restriction

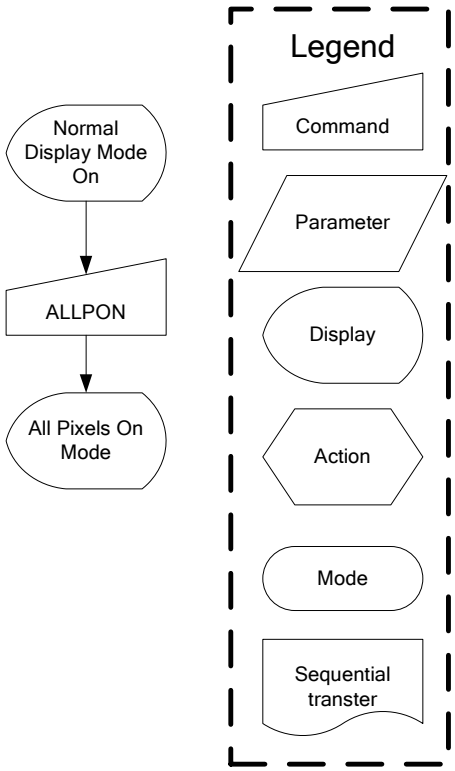
This command has no effect when module is already All Pixel On mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All pixel on mode disable
S/W Reset	All pixel on mode disable
H/W Reset	All pixel on mode disable

Flow Chart	 Normal Display Mode On ALLPON All Pixels On Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.19 WRCNTR: Write Contrast (25h)

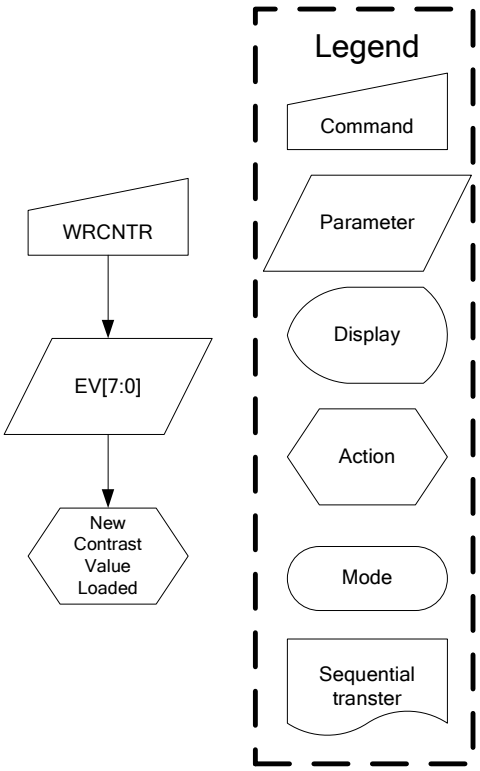
Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
WRCNTR	0	1	0	0	0	1	0	0	1	0	1	**(25h)**
1st Parameter	1	1	0	-	EV6	EV5	EV4	EV3	EV2	EV1	EV0	

Description	This command is used to fine tuning the contrast of the current display. This contrast values can affect segment and common outputs. Parameter range: 0-127dec. MSB is EV6 and LSB is EV0. Default value: 63dec (3Fh)
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3Fh
S/W Reset	3Fh
H/W Reset	3Fh

Flow Chart	

Legend
Command
Parameter
Display
Action
Mode
Sequential transter
WRCNTR
EV[7:0]
New Contrast Value Loaded

9.1.20 DISPOFF: Display Off (28h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
DISPOFF	0	1	0	0	0	1	0	1	0	0	0	**(28h)**
Parameter	No Parameter											

Description

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and blank page inserted.

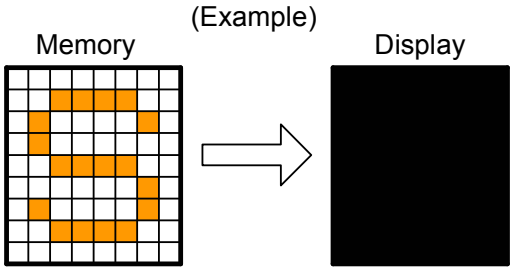
This command makes no change of contents of frame memory.

This command does not change any other status.

There will be no abnormal visible effect on the display.

Exit from this command by Display On (29h)

(Example)



Restriction

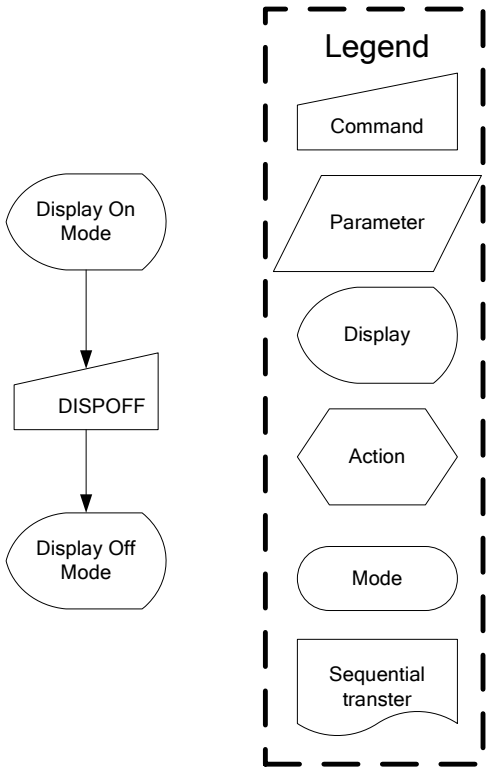
This command has no effect when module is already in Display Off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart	 Display On Mode DISPOFF Display Off Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.21 DISPON: Display On (29h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
DISPON	0	1	0	0	0	1	0	1	0	0	1	**(29h)**
Parameter	No Parameter											

Description

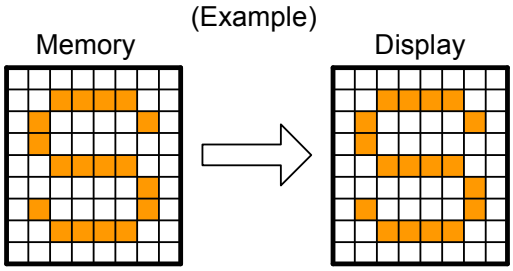
Turn on the display screen according to the current display data RAM content and the display timing and setting.

This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.

This command makes no change of contents of frame memory.

This command does not change any other status.

(Example)



Restriction

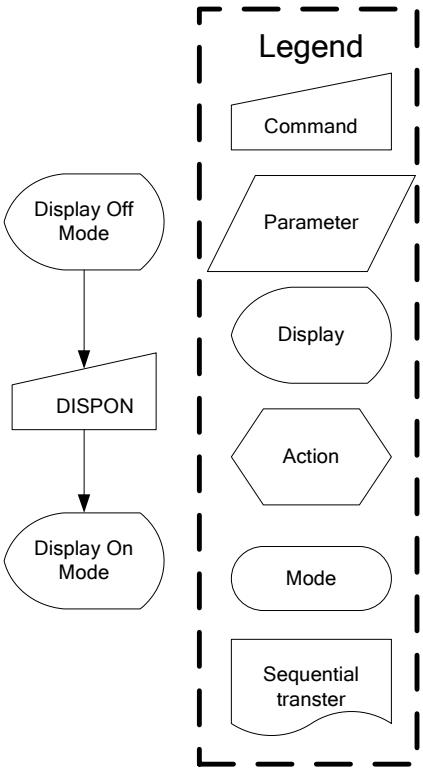
This command has no effect when module is already in Display On mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart	 Legend Command Parameter Display Action Mode Sequential transter Display Off Mode DISPON Display On Mode

9.1.22 CASET: Column Address Set (2Ah)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
CASET	0	1	0	0	0	1	0	1	0	1	0	**(2Ah)**
1st Parameter	1	1	0	-	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
2nd Parameter	1	1	0	-	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

NOTE: "-" Don't care

Description

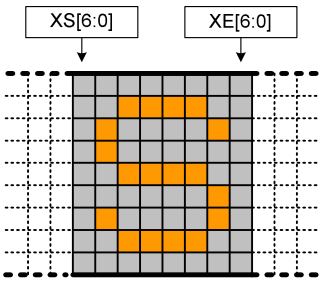
This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The value of XS [6:0] and XE [6:0] are referred when RAMWR command comes.

Each value represents one column line in the Frame Memory.

(Example)



Restriction

XS [6:0] always must be equal to or less than XE [6:0]

When XS [6:0] or XE [6:0] is greater than 61h (when MV=0) or 45h (when MV=1), data of out of range will be ignored.

(Parameter range: 0 ≦ XS [7:0] ≦ XE [7:0] ≦ 97(61h)) : MV="0"

(Parameter range: 0 ≦ XS [7:0] ≦ XE [7:0] ≦ 69(45h)) : MV="1"

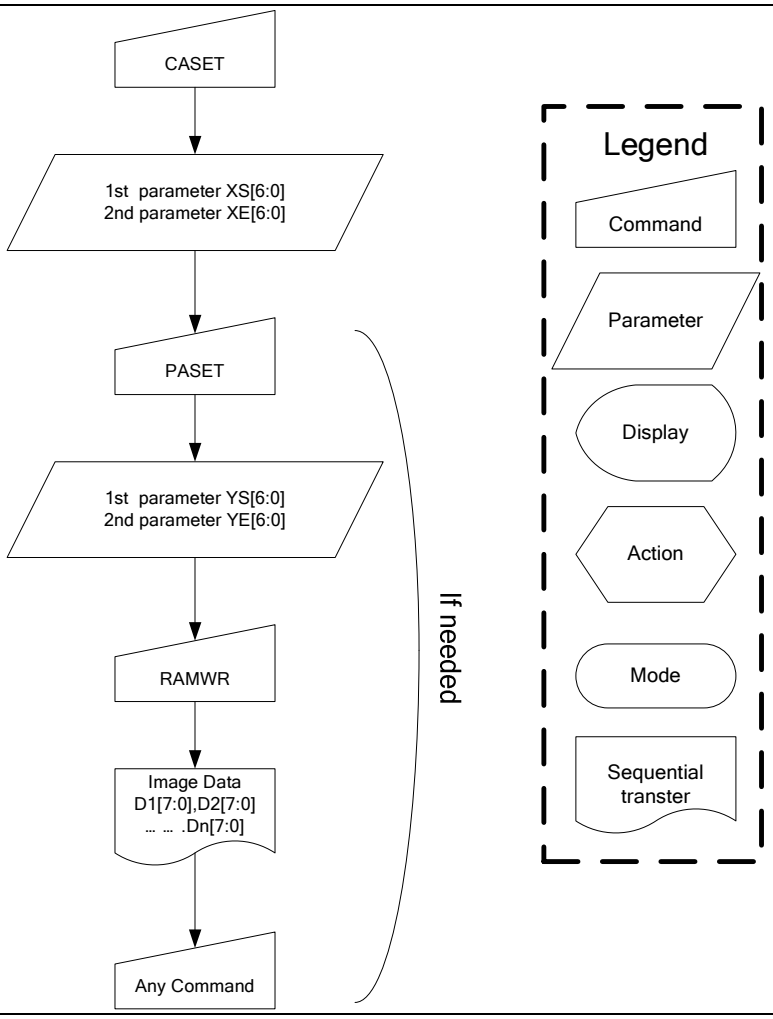
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	XS [6:0]	XE [6:0] (MV=0)	XE [6:0] (MV=1)
Power On Sequence	00h (00d)	61h (97d)	
S/W Reset	00h (00d)	61h (97d)	45h (69d)
H/W Reset	00h (00d)	61h (97d)	

Flow Chart


CASET
1st parameter XS[6:0]
2nd parameter XE[6:0]
PASET
1st parameter YS[6:0]
2nd parameter YE[6:0]
RAMWR
Image Data
D1[7:0],D2[7:0]
... ... .Dn[7:0]
Any Command
If needed
Legend
Command
Parameter
Display
Action
Mode
Sequential
transter

9.1.23 RASET: Row Address Set (2Bh)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RASET	0	1	0	0	0	1	0	1	0	1	1	**(2Bh)**
1st Parameter	1	1	0	-	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
2nd Parameter	1	1	0	-	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

NOTE: "-" Don't care

Description

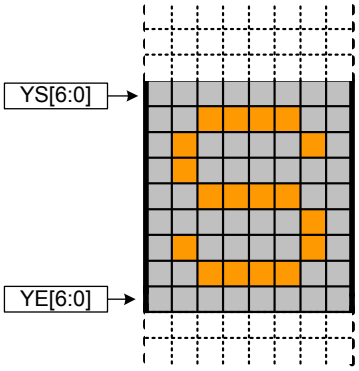
This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The value of YS [6:0] and YE [6:0] are referred when RAMWR command comes.

Each value represents one column line in the Frame Memory.

(Example)



Restriction

YS [6:0] always must be equal to or less than YE [6:0]

When YS [6:0] or YE [6:0] is greater than 45h (when MV=0) or 61h (when MV=1), data of out of range will be ignored.

(Parameter range: 0≤YS [6:0] ≤YE [6:0] ≤69 (45h)) : MV = "0"

(Parameter range: 0≤YS [6:0] ≤YE [6:0] ≤97 (61h)) : MV = "1"

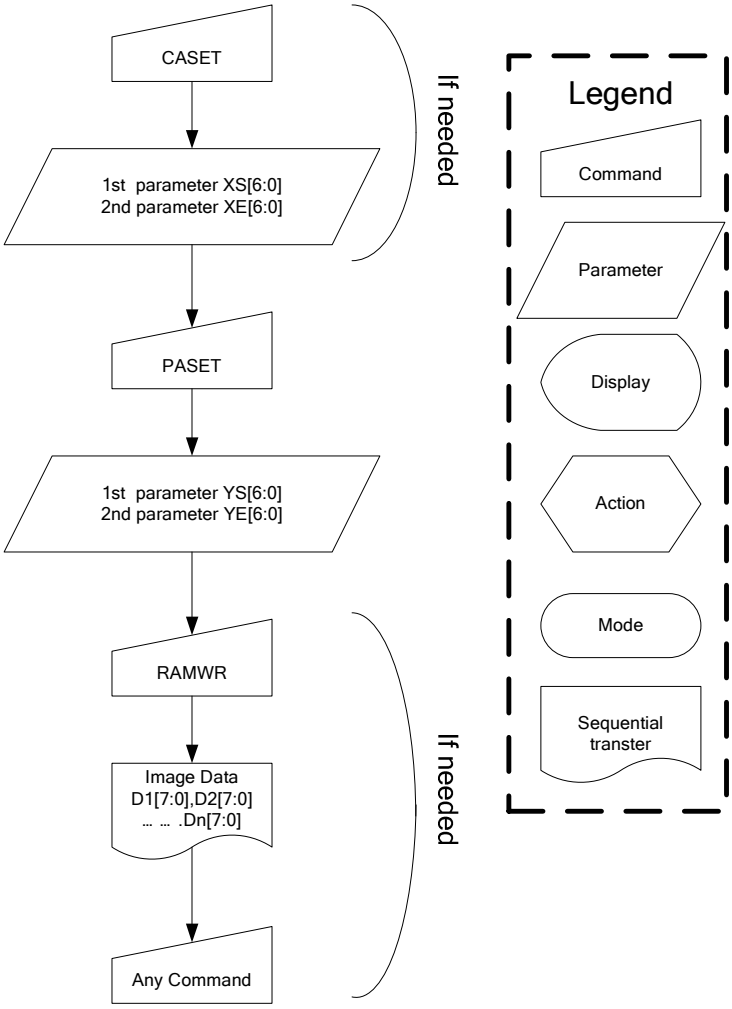
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	YS [6:0]	YE [6:0] (MV=0)	YE [6:0] (MV=1)
Power On Sequence	00h (00d)	45h (69d)	
S/W Reset	00h (00d)	45h (69d)	61h (97d)
H/W Reset	00h (00d)	45h (69d)	

Flow Chart


CASET
1st parameter XS[6:0]
2nd parameter XE[6:0]
PASET
1st parameter YS[6:0]
2nd parameter YE[6:0]
RAMWR
Image Data
D1[7:0],D2[7:0]
… … .Dn[7:0]
Any Command
If needed
If needed
Legend
Command
Parameter
Display
Action
Mode
Sequential
transter

9.1.24 RAMWR: Memory Write (2Ch)

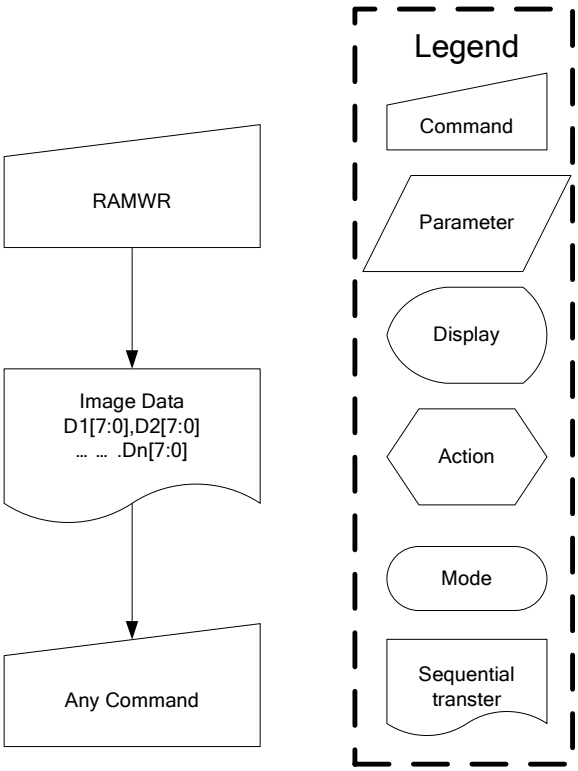
Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RAMWR	0	1	0	0	0	1	0	1	1	0	0	**(2Ch)**
Write Data 1 D1[7:0]	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	-
:	1	1	0	:	:	:	:	:	:	:	:	-
Write Data n Dn[7:0]	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	-

Description	This command is used to transfer data MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. The Start Column/Start Row positions are different in accordance with MADCTR setting. Then D [7:0] is stored in frame memory and the column register and the row register incremented as in Figure 7.3. Frame Write can be canceled by sending any other command.
Restriction	In all color modes, there is no restriction on length of parameters.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is remained
H/W Reset	Contents of memory is remained

Flow Chart	

RAMWR
Image Data
D1[7:0],D2[7:0]
... ... .Dn[7:0]
Any Command
Legend
Command
Parameter
Display
Action
Mode
Sequential
transter

9.1.25 RGBSET: Color Set for 256-Color Display (2Dh)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RGBSET	0	1	0	0	0	1	0	1	1	0	1	**(2Dh)**
1st parameter	1	1	0	-	-	-	R004	R003	R002	R001	R000	-
:	1	1	0	:	:	:	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	-
16th parameter	1	1	0	-	-	-	R154	R153	R152	R151	R150	-
17th parameter	1	1	0	-	-	G005	G004	G003	G002	G001	G000	-
:	1	1	0	:	:	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	
32nd parameter	1	1	0	-	-	G155	G154	G153	G152	G151	G150	
33rd parameter	1	1	0	-	-	-	B004	B003	B002	B001	B000	
:	1	1	0	:	:	:	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	
48th parameter	1	1	0	-	-	-	B154	B153	B152	B151	B150	

NOTE: "-" Don't care

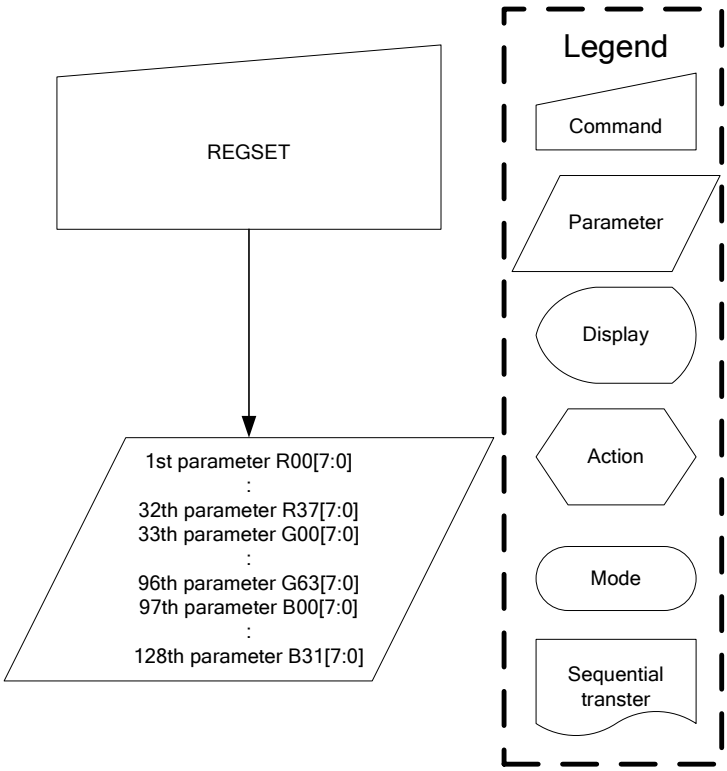
Description	This command is used to define the LUT for 8bit-to-16bit or 12bit-to-16bit color depth conversations. (See also Section 7.8) 48 Bytes must be written to the LUT regardless of the color mode. Only the values in Section 7.8 are referred. This command has no effect on other commands/parameters and Contents of frame memory. Visible change takes effect next time the Frame Memory is written to.
Restriction	Do not send any command before the last data is sent or LUT is not defined correctly.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to Section 7.8
S/W Reset	Contents of the look-up table protected
H/W Reset	Refer to Section 7.8

Flow Chart


REGSET
1st parameter R00[7:0]
:
32th parameter R37[7:0]
33th parameter G00[7:0]
:
96th parameter G63[7:0]
97th parameter B00[7:0]
:
128th parameter B31[7:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.26 RAMRD : Memeory Read (2EH)

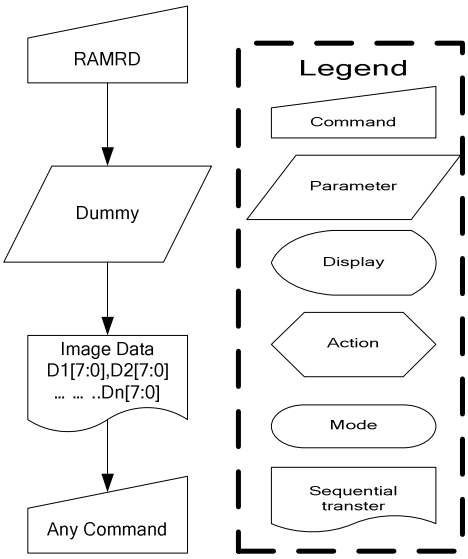
Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RAMRD	0	1	0	0	0	1	0	1	1	0	0	**(2Eh)**
Dummy Read	1	0	1	x	x	x	x	x	x	x	x	**x**
Read Data 1 D1[7:0]	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0	**00H ~ FFH**
…												
Read Data n Dn[7:0]	1	0	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	**00H ~ FFH**

Description	This command is used to transfer data from frame memory to MCU. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTR setting. Then D[7:0] is read back from the frame memory and the column register and the page register incremented. Frame Read can be stopped by sending any other command.
Restriction	Memory Read is only possible via the Parallel Interface.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	 RAMRD Dummy Image Data D1[7:0],D2[7:0] … … ..Dn[7:0] Any Command Legend Command Parameter Display Action Mode Sequential transter

9.1.27 PTLAR: Partial Area (30h)

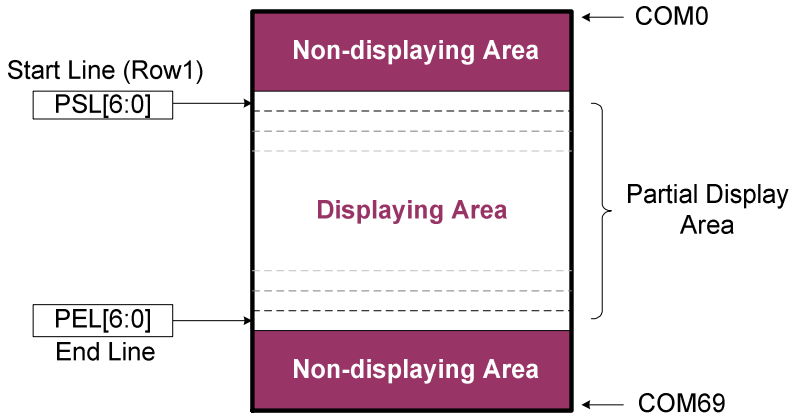
Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
PTLAR	0	1	0	0	0	1	1	0	0	0	0	**(30h)**
1st Parameter	1	1	0	-	PS6	PS5	PS4	PS3	PS2	PS1	PS0	-
2nd Parameter	1	1	0	-	PE6	PE5	PE4	PE3	PE2	PE1	PE0	-

NOTE: "-" Don't care

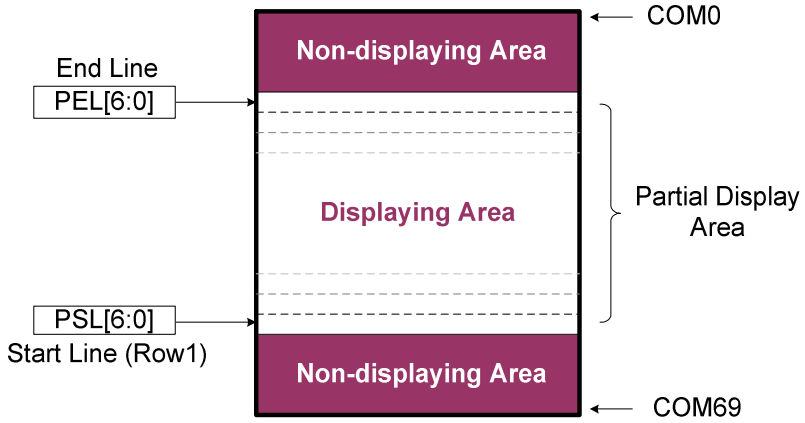
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Line (PSL) and the second the End Line (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory Line counter.

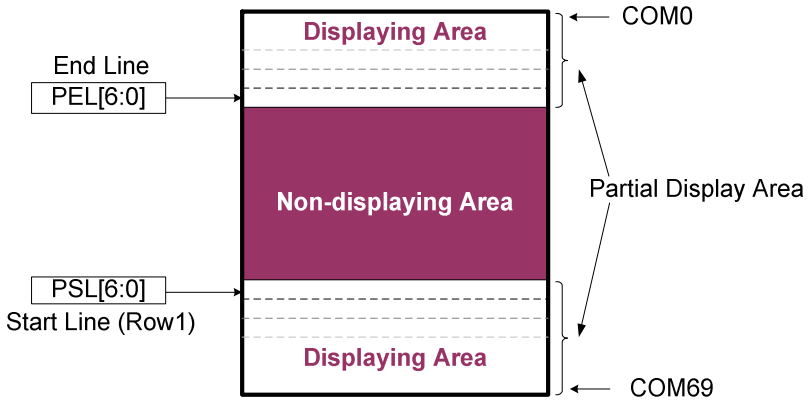
If End Line > Start Line when MADCTR ML=0:



If End Line > Start Line when MADCTR ML=1:



If End Line < Start Line when MADCTR ML=0:



* Row1: Frame memory row address 1.

If End Line = Start Line then the Partial Area will be one line deep.

Restriction

PSL[6:0] and PEL[6:0] is based on line unit.

PSL[6:0]=00h, 01h, 02h, 03h, … , 45h

PEL[6:0]= 00h, 01h, 02h, 03h, … , 45h

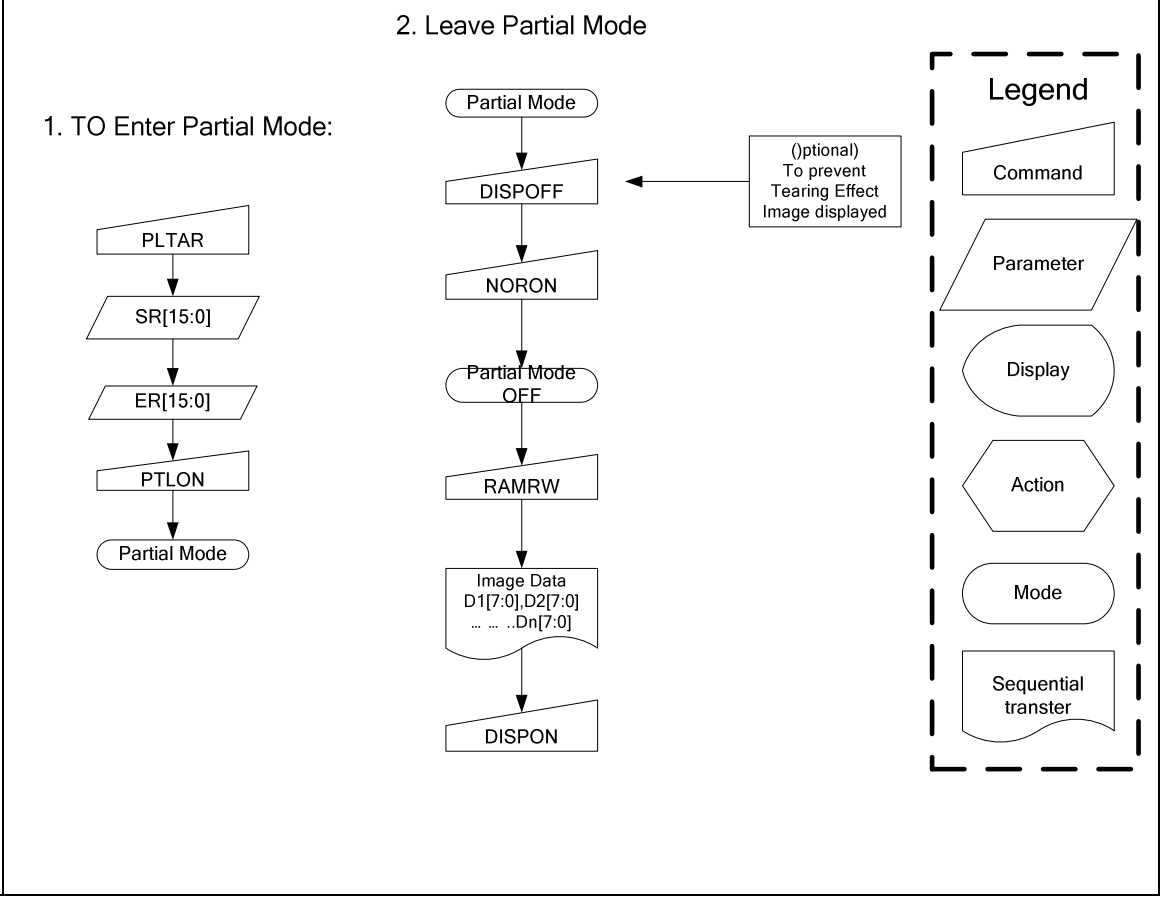
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	PSL [6:0]	PEL [6:0]
Power On Sequence	00h (00d)	45h (69d)
S/W Reset	00h (00d)	45h (69d)
H/W Reset	00h (00d)	45h (69d)

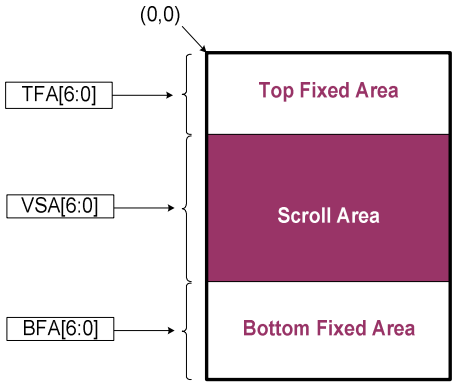
Flow Chart


2. Leave Partial Mode
1. TO Enter Partial Mode:
PLTAR
SR[15:0]
ER[15:0]
PTLON
Partial Mode
Partial Mode
DISPOFF
NORON
Partial Mode OFF
RAMRW
Image Data
D1[7:0],D2[7:0]
... .Dn[7:0]
DISPON
()ptional)
To prevent
Tearing Effect
Image displayed
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.28 SCRLAR: Scroll Area (33h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
SCRLAR	0	1	0	0	0	1	1	0	0	1	1	**(33h)**
1st parameter	1	1	0	-	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-
2nd parameter	1	1	0	-	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-
3rd parameter	1	1	0	-	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-

NOTE: "-" Don't care

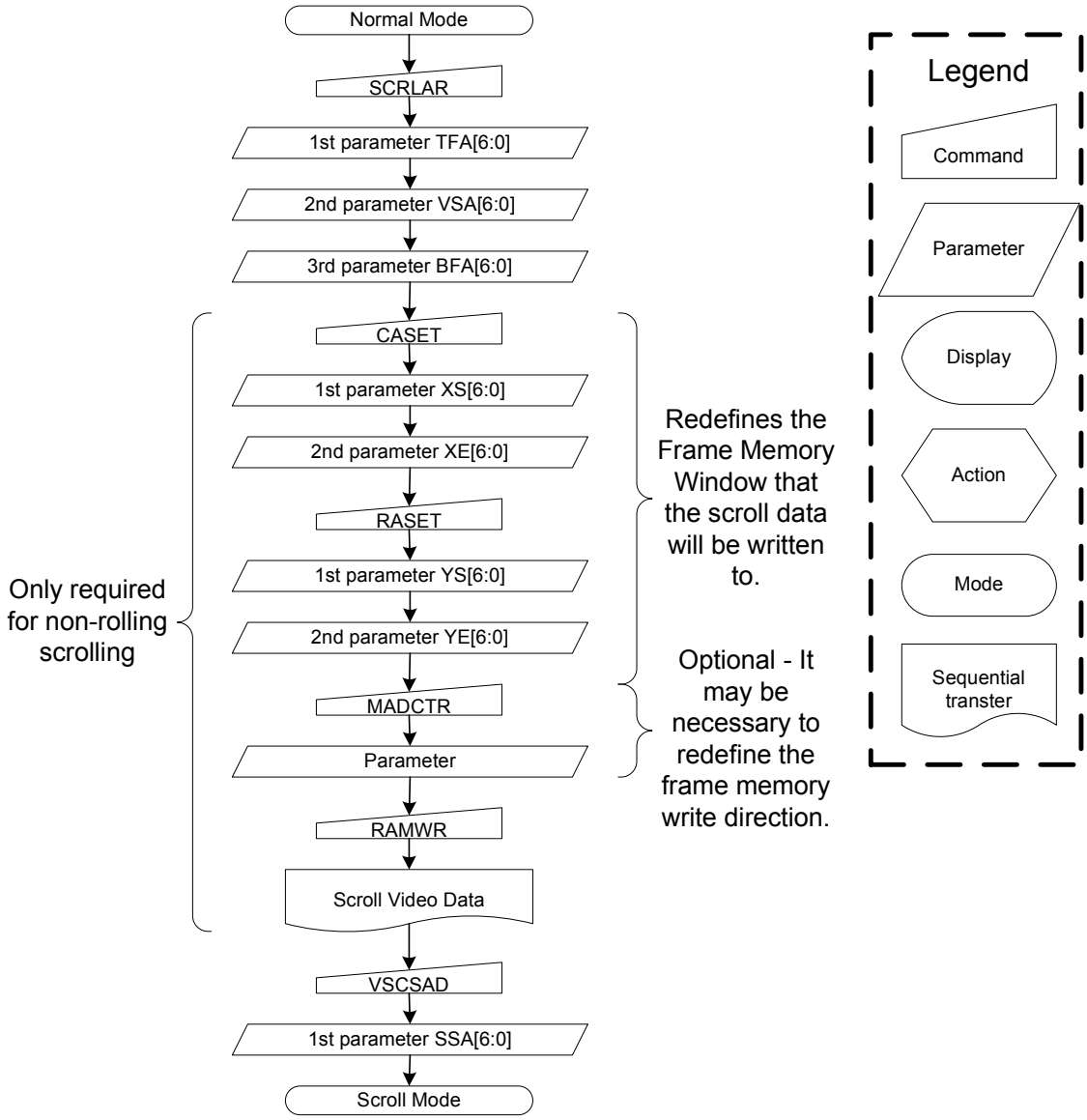
Description	This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll. When MADCTR BL=0 The 1st parameter TFA [6:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 2nd parameter VSA [6:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area. The 3rd parameter BFA [6:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer. 
Restriction	The condition is (TFA+VSA+BFA) = 70, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTR parameter MV should be set to '0'-this only affects the Frame Memory Write. TFA[6:0], VSA[6:0] and BFA[6:0] is based on line unit. TFA[6:0]= 00h, 01h, 02h, 03h, … , 46h VSA[6:0]= 00h, 01h, 02h, 03h, … , 46h BFA[6:0]= 00h, 01h, 02h, 03h, … , 46h

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value		
		TFA [6:0]	VSA [6:0]	BFA [6:0]
	Power On Sequence	00h	46h (70d)	00h
	S/W Reset	00h	46h (70d)	00h
	H/W Reset	00h	46h (70d)	00h

Flow Chart

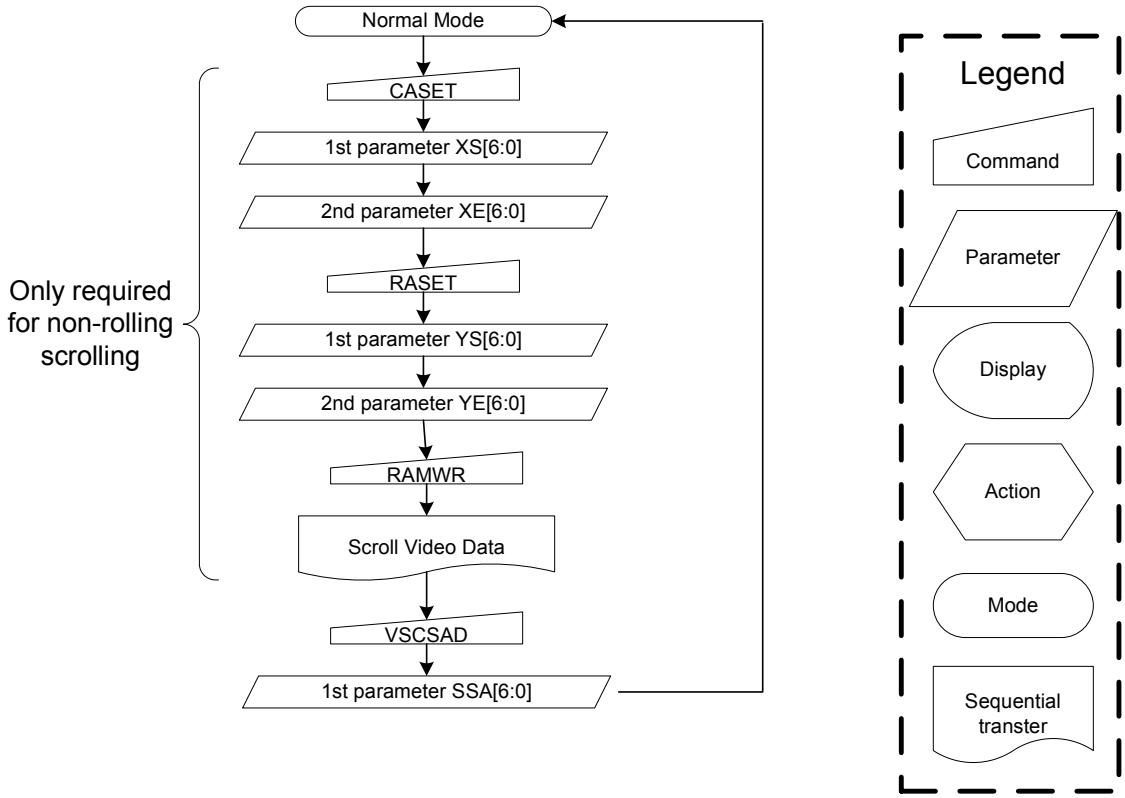
1. TO Enter Vertical Scroll Mode:



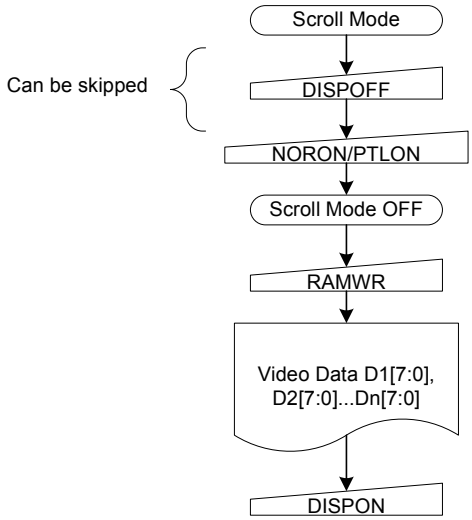
NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

Flow Chart

2. Continuous Scroll:



3. To Exit Vertical Scroll Mode:



NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On (12h) commands.

9.1.29 TEOFF: Tearing Effect Line OFF (34h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
TEOFF	0	1	0	0	0	1	1	0	1	0	0	**(34h)**
Parameter	No Parameter											

Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	This command has no effect when Tearing Effect output is already OFF.

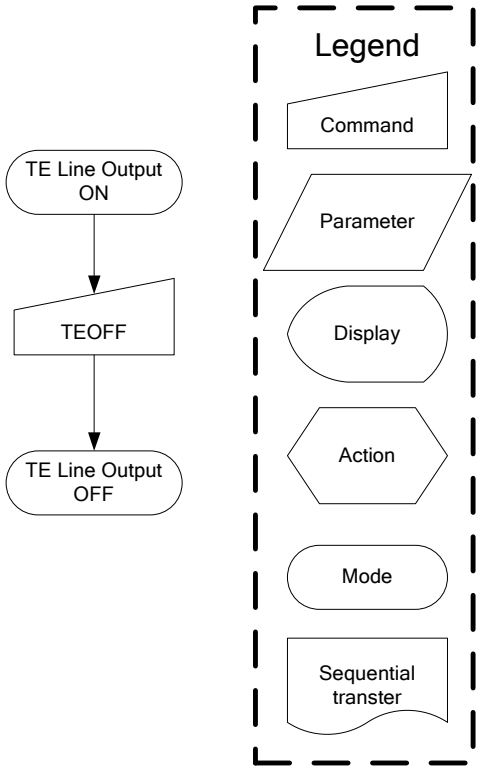
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off
S/W Reset	Tearing effect off
H/W Reset	Tearing effect off

Flow Chart



9.1.30 TEON: Tearing Effect Line ON (35h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
TEON	0	1	0	0	0	1	1	0	1	0	1	**(35h)**
Parameter	1	1	0	-	-	-	-	-	-	-	M	

NOTE: "-" Don't care

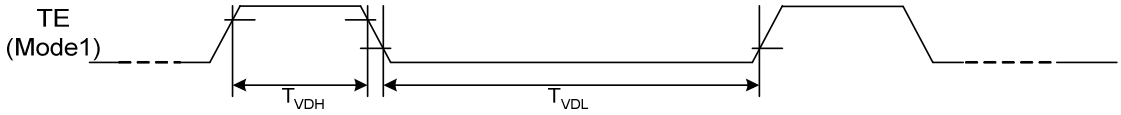
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTR bit ML.

The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).

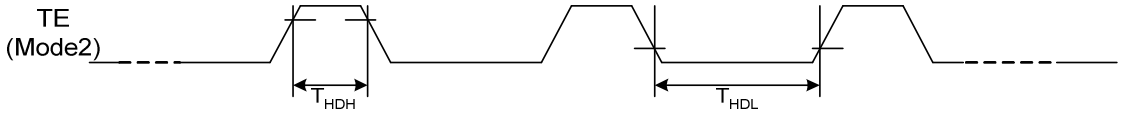
When M=0:

The Tearing Effect Output Line consists of V-Blanking information only:



When M=1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



See section 7.3.8 for more information.

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

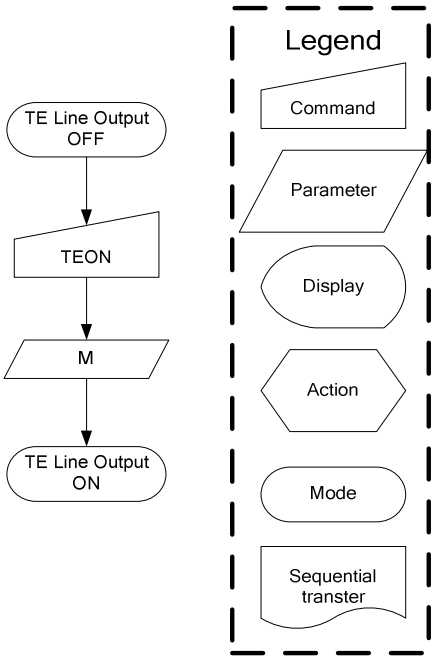
This command has no effect when Tearing Effect output is already OFF.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off & M=0
S/W Reset	Tearing effect off & M=0
H/W Reset	Tearing effect off & M=0

Flow Chart	 TE Line Output OFF TEON M TE Line Output ON Legend Command Parameter Display Action Mode Sequential transter

9.1.31 MADCTR: Memory Data Access Control (36h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
MADCTR	0	1	0	0	0	1	1	0	1	1	0	**(36h)**
Parameter	1	1	0	MY	MX	MV	ML	RGB	-	-	-	-

NOTE: "-" Don't care

Description

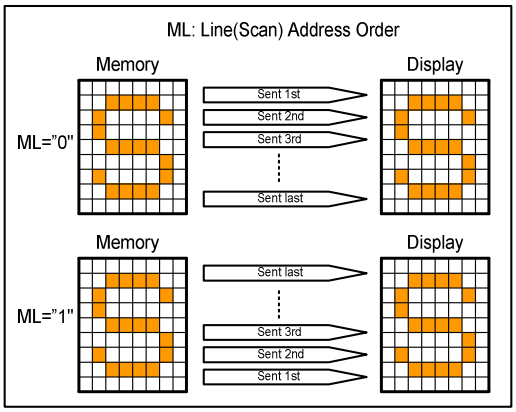
This command defines read/write scanning direction of frame memory.

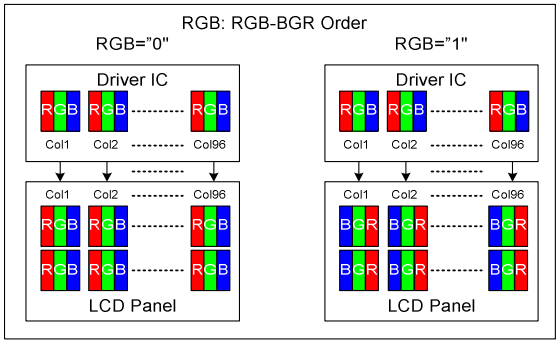
This command makes no change on the other driver status.

Note: ML affects to Partial Area (30h), Vertical Scrolling Definition (33h), Vertical Scrolling Start address (37h), Partial On (12h) commands

Bit Assignment

Bit	NAME	DESCRIPTION
MY	ROW ADDRESS ORDER	These 3bits controls MCU to memory write/read direction. (See Section 7.3.2 "MCU to memory write/read direction")
MX	COLUMN ADDRESS ORDER	
MV	ROW/COLUMN ORDER	
ML	LINE ADDRESS ORDER	LCD refresh direction control
RGB	RGB-BGR ORDER	Color selector switch control 0=RGB color filter panel, 1=BGR color filter panel) The contents of the frame memory are not changed.





Restriction

D2, D1 and D0 of the 1st parameter are set to '000'internally.

Register Availability

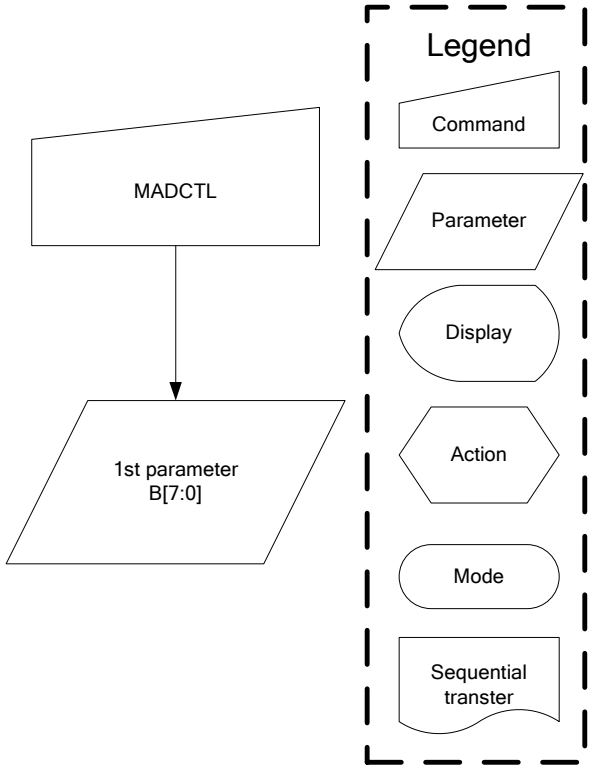
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes

Normal Mode On, Idle Mode On, Sleep Out	Yes	
Partial Mode On, Idle Mode Off, Sleep Out	Yes	
Partial Mode On, Idle Mode On, Sleep Out	Yes	
Sleep In	Yes	

Default

Status	Default Value
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0
S/W Reset	Not changed
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0

Flow Chart



9.1.32 VSCSAD: Vertical Scroll Start Address of RAM (37h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
VSCSAD	0	1	0	0	0	1	1	0	1	1	1	**(37h)**
Parameter	1	1	0	-	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	

NOTE: "-" Don't care

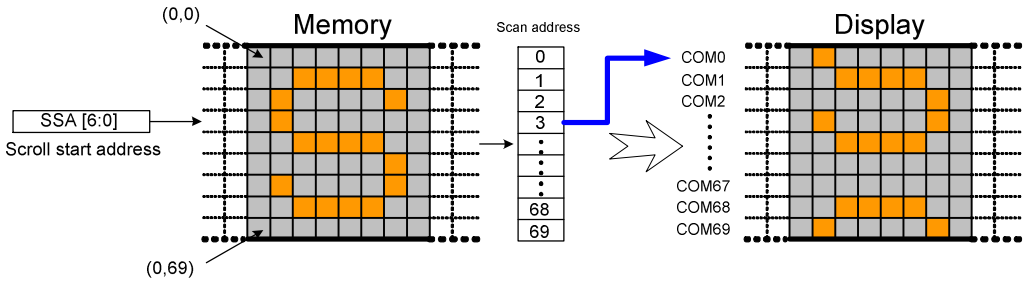
Description

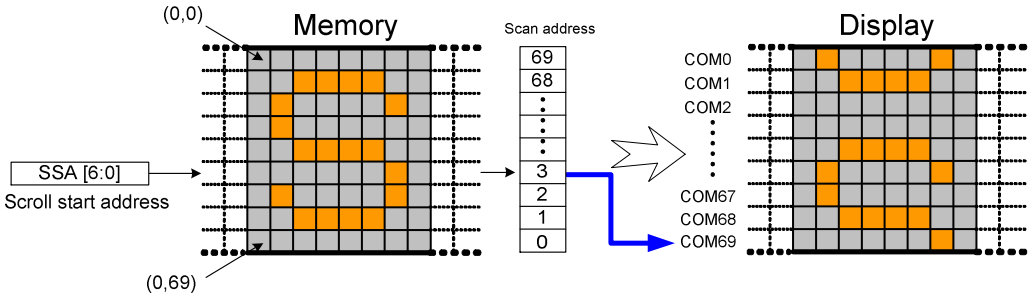
This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.

The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

This command Start the scrolling.

Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).





NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

SSA refers to the Frame Memory line Pointer

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.

SSA [6:0] is based on line unit.

SSA [6:0] = 00h, 01h, 02h, 03h, … , 45h

<table>
<tr><td>Register Availability</td><td><table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td><table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>00</td></tr>
<tr><td>S/W Reset</td><td>00</td></tr>
<tr><td>H/W Reset</td><td>00</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

9.1.33 IDMOFF: Idle Mode Off (38h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
IDMOFF	0	1	0	0	0	1	1	1	0	0	0	**(38h)**
Parameter	No Parameter											

Description

This command is used to recover from Idle mode on.

There will be no abnormal visible effect on the display mode change transition.

In the idle off mode,

1. LCD can display maximum 65536 colors.
2. Normal frame frequency is applied.

Restriction

This command has no effect when module is already in idle off mode.

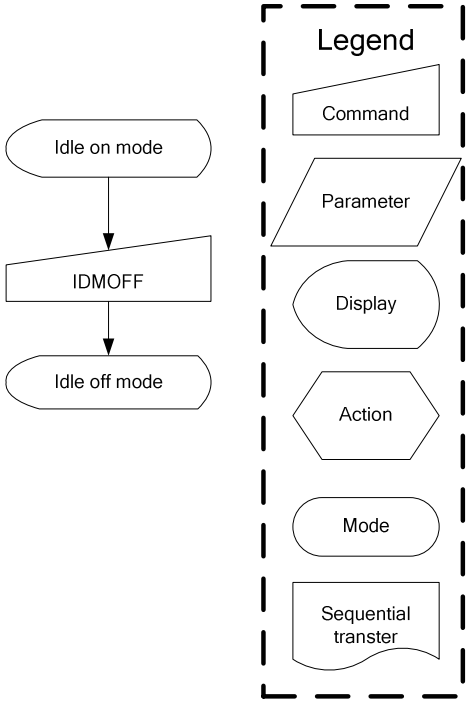
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode off
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Flow Chart



9.1.34 IDMON: Idle Mode On (39h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
IDMON	0	1	0	0	0	1	1	1	0	0	1	**(39h)**
Parameter	No Parameter											

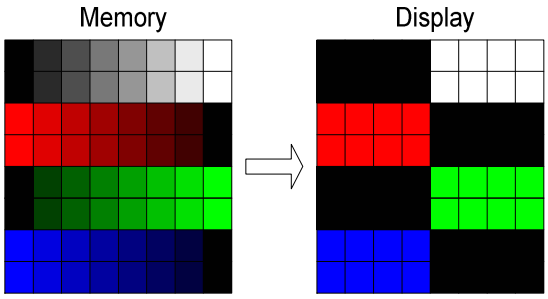
Description

This command is used to enter into Idle mode on.

There will be no abnormal visible effect on the display mode change transition. In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)



"X": don't care

Color	R_4 R_3 R_2 R_1 R_0	G_5 G_4 G_3 G_2 G_1 G_0	B_4 B_3 B_2 B_1 B_0
Black	0XXXX	0XXXXX	0XXXX
Blue	0XXXX	0XXXXX	1XXXX
Red	1XXXX	0XXXXX	0XXXX
Magenta	1XXXX	0XXXXX	1XXXX
Green	0XXXX	1XXXXX	0XXXX
Cyan	0XXXX	1XXXXX	1XXXX
Yellow	1XXXX	1XXXXX	0XXXX
White	1XXXX	1XXXXX	1XXXX

Restriction

This command has no effect when module is already in idle on mode.

Register Availability

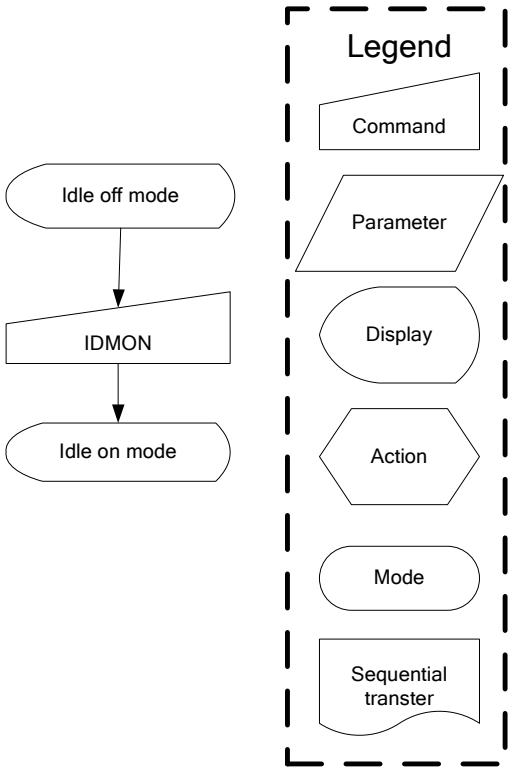
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value

Power On Sequence	Idle mode off	
S/W Reset	Idle mode off	
H/W Reset	Idle mode off	

Flow Chart



9.1.35 COLMOD: Interface Pixel Format (3Ah)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
COLMOD	0	1	0	0	0	1	1	1	0	1	0	**(3Ah)**
Parameter	1	1	0	-	-	-	-	-	P2	P1	P0	-

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU Interface. The formats are shown in the table:

Interface Format	P2	P1	P0
Not Defined	0	0	0
Not Defined	0	0	1
8Bit/Pixel	0	1	0
12Bit/Pixel (Type A)	0	1	1
12Bit/Pixel (Type B)	1	0	0
16Bit/Pixel	1	0	1
18Bit/Pixel	1	1	0
24Bit/Pixel	1	1	1

Note: In 8 bit/pixel or 12 bit/pixel mode, the LUT is applied to transfer data into the Frame Memory.

Restriction

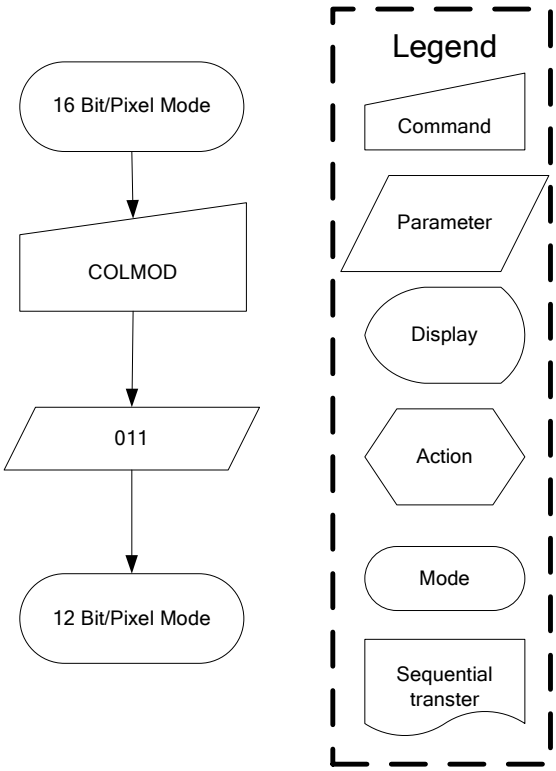
There is no visible effect until the Frame Memory is written to.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	05h (16Bit/Pixel)
S/W Reset	No Change
H/W Reset	05h (16Bit/Pixel)

Flow Chart	

16 Bit/Pixel Mode
COLMOD
011
12 Bit/Pixel Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.36 RDID1: Read ID1 Value (DAh)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDID1	0	1	0	1	1	0	1	1	0	1	0	**(DAh)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-

NOTE: "-" Don't care

Description

This read byte returns 8-bit LCD module's manufacturer ID

D7-D0 (ID17 to ID10): LCD module's manufacturer ID.

NOTE: See command RDDID (04h), 2nd parameter.

Restriction

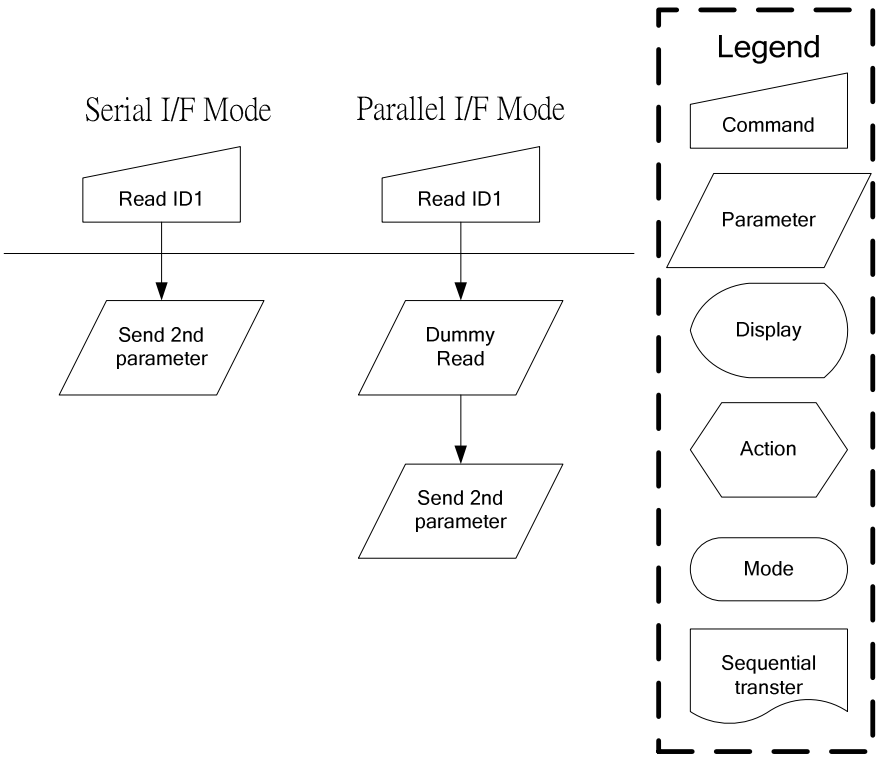
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	45h
S/W Reset	45h
H/W Reset	45h

Flow Chart



9.1.37 RDID2: Read ID2 Value (DBh)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDID2	0	1	0	1	1	0	1	1	0	1	1	**(DBh)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: "-" Don't care

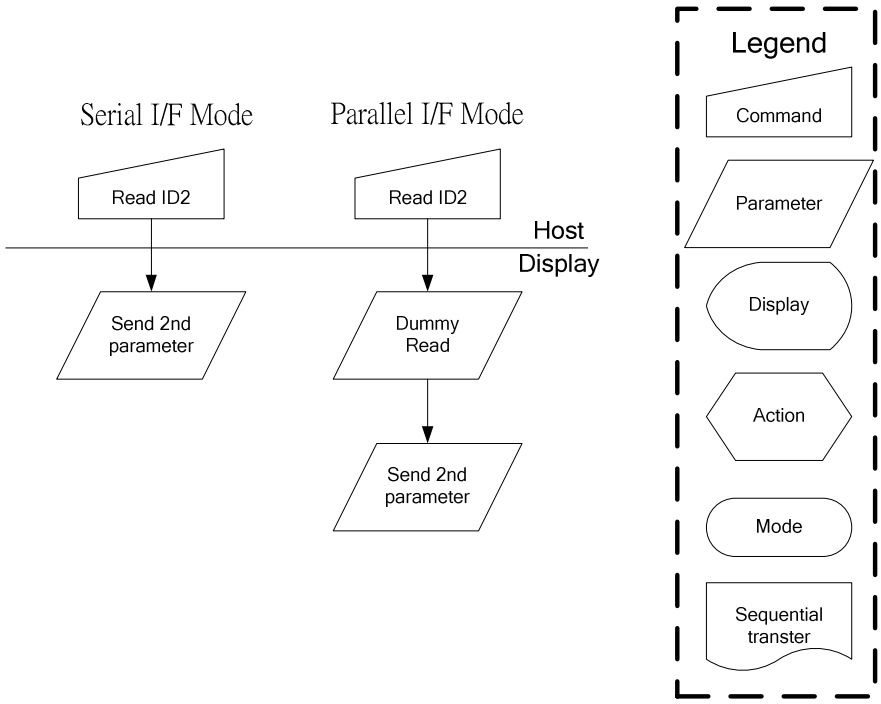
Description	This read byte returns 8-bit LCD module/driver version ID D7-D0 (ID27 to ID20): LCD module/driver version ID Parameter Range: ID=80h to FFh *NOTE: See command RDDID (04h), 3rd parameter.*
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value[6:0]
Power On Sequence	D2h
S/W Reset	D2h
H/W Reset	D2h

Flow Chart



9.1.38 RDID3: Read ID3 Value (DCh)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDID3	0	1	0	1	1	0	1	1	1	0	0	**(DCh)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-" Don't care

Description

This read byte returns 8-bit LCD module/driver ID.

D7-D0 (ID37 to ID30): LCD module/driver ID.

NOTE: See command RDDID (04h), 4th parameter.

Restriction

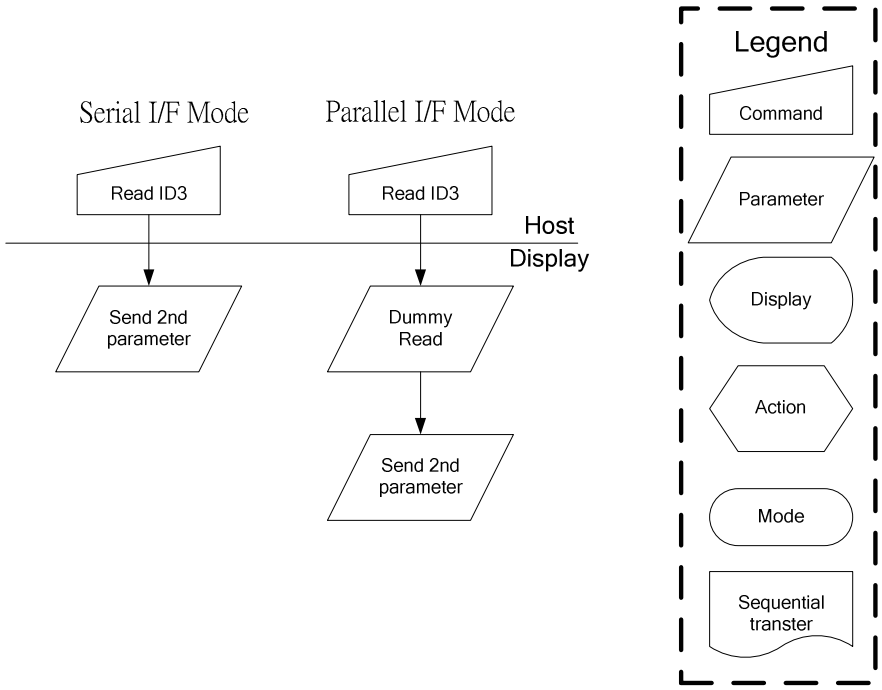
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Eh
S/W Reset	0Eh
H/W Reset	0Eh

Flow Chart



9.1.39 DutySet: Display Duty setting (B0H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
DutySet	0	1	0	1	0	1	1	0	0	0	0	**(B0h)**
Parameter	1	1	0	0	Du6	Du5	Du4	Du3	Du2	Du1	Du0	-

NOTE: "-" Don't care

Description

This command is used to set display duty. Command set = display duty numbers - 1.

Example:

Duty	Du6	Du5	Du4	Du3	Du2	Du1	Du0	Command set= Display duty numbers-1
Example: 1/70 duty	1	0	0	0	1	0	1	70-1=69

Restriction

Display duty must > 4 (1/4 duty)

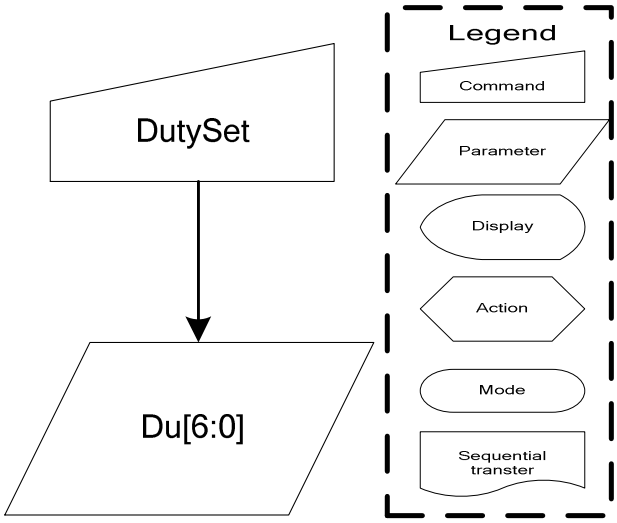
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Du[6:0])
Power On Sequence	01000101b (45h)
S/W Reset	01000101b (45h)
H/W Reset	01000101b (45h)

Flow Chart



9.1.40 FirstCom: First Com. Page address (B1H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
FirstCom	0	1	0	1	0	1	1	0	0	0	1	**(B1h)**
Parameter	1	1	0	--	F6	F5	F4	F3	F2	F1	F0	-

NOTE: "-" Don't care

Description

This command defines the first output COM number that mapping to the RAM page address 0. For detail setting value, please see the table as below.

F6	F5	F4	F3	F2	F1	F0	Line address
0	0	0	0			0	0
0	0	0	0			1	1
0	0	0	1			0	2
0	0	0	1			1	3
:	:	:	:			:	:
1	0	0	0	1	0	1	69

Example:

If FirstCom=8, common 8 would output the data of RAM page address 0.

Restriction

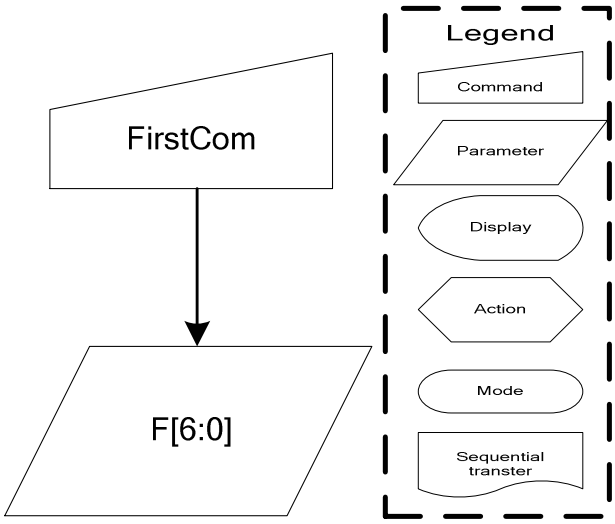
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (F[6:0])
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



9.1.41 OscDiv: FOSC Divider (B3H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
OscDiv	0	1	0	1	0	1	1	0	0	1	1	**(B3h)**
Parameter	1	1	0	-	-	-	-	-	-	CLD1	CLD0	-

NOTE: "-" Don't care

Description

This command is used to specify the CL dividing ratio.

CLD1, CLD0: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.

CLD1	CLD0	CL dividing ratio
0	0	Not divide
0	1	2 divisions
1	0	4 divisions
1	1	8 divisions

Restriction

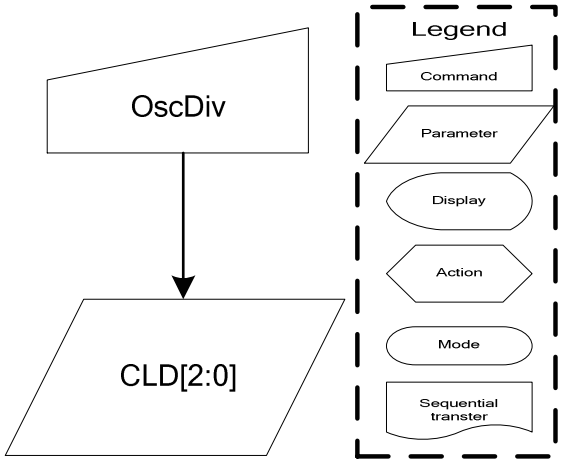
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (CLD[0:1])
Power On Sequence	00b
S/W Reset	00b
H/W Reset	00b

Flow Chart



9.1.42 PTLMOD: Partial Saving Power Mode Selection (B4H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
OscDiv	0	1	0	1	0	1	1	0	1	0	0	**(B4h)**
Parameter	1	1	0	PTLM	0	0	1	1	0	0	0	-

NOTE: "-" Don't care

Description

Two type partial modes are built in ST7628. One is NORMAL MODE(PTLM=0) and another is POWER SAVING MODE(PTML=1). When entering power saving mode, IC would change bias, V0, booster pumping times in 4 special partial lines in order to save power consumptions, please see the following table:

Duty	Bias	Bst pump	V0(V)
24	1/6	5x	9+(Vopoffset/2)
32	1/6	5x	9.68+(Vopoffset/2)
40	1/6	5x	10.12+(Vopoffset/2)
48	1/6	5x	10.52+(Vopoffset/2)

Restriction

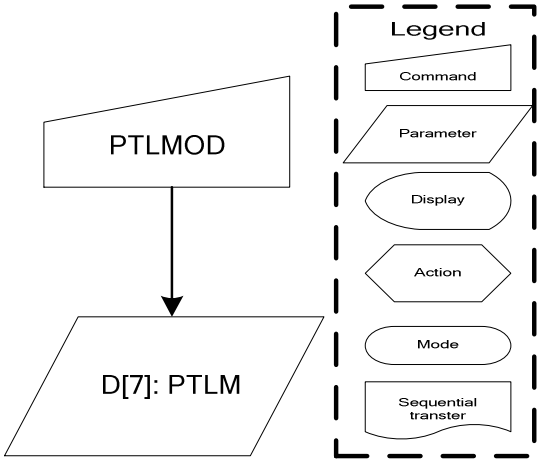
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18h
S/W Reset	18h
H/W Reset	18h

Flow Chart



9.1.43 NLInvSet: N-Line control (B5H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
NLInvSet	0	1	0	1	0	1	1	0	1	0	1	**(B5h)**
Parameter	1	1	0	M	N6	N5	N4	N3	N2	N1	N0	-

NOTE: "-" Don't care

Description

This command is used to set the inverted line number with range of 2 to (duty-1) to improve display quality. When M=0, inversion occurs in every frame; when M=1, inversion is independent from frames. If N[6:0]=0, N-line inversion function is disable.

Line inversion numbers=N[6:0] +1.

Example:

If N[6:0]=7, inversion occurs per 8 line.

Restriction

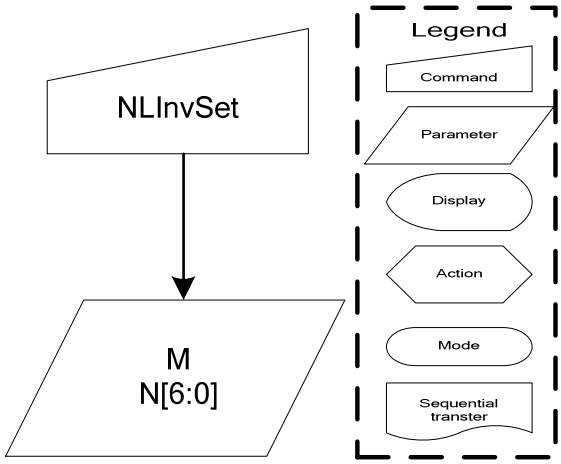
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	M	N[6:0]
Power On Sequence	0b	0000000b
S/W Reset	0b	0000000b
H/W Reset	0b	0000000b

Flow Chart



9.1.44 ComScanDir: Com/Seg Scan Direction for glass layout(B7H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
ComScanDir	0	1	0	1	0	1	1	0	1	1	1	**(B7h)**
Parameter	1	1	0	SMY	SMX	SINV	SML	SBGR	-	-	-	-

NOTE: "-" Don't care

Description

	Function	0	1
SMY	Inverse the MY setting	Keep MY	Inverse MY
SMX	Inverse the MX setting	Keep MX	Inverse MX
SINV	Inverse the INVON setting	Keep INVON	Inverse INVON
SML	Inverse the ML setting	Keep ML	Inverse ML
SBGR	Inverse the BGR setting	Keep BGR	Inverse BGR

Restriction

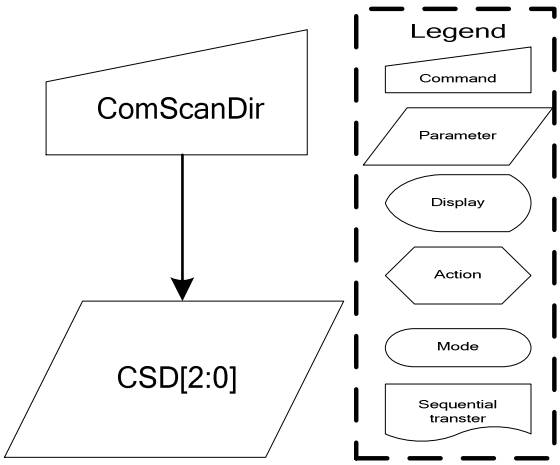
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	49h
S/W Reset	49h
H/W Reset	49h

Flow Chart



9.1.45 RMWIN: Read Modify Write control in(B8H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RMWIN	0	1	0	1	0	1	1	1	0	0	0	**(B8h)**
Parameter	No Parameter											

NOTE: "-" Don't care

Description	Read modify write control IN
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

9.1.46 RMWOUT: Read Modify Write control out(B9H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RMWOUT	0	1	0	1	0	1	1	1	0	0	1	**(B9h)**
Parameter	No Parameter											

NOTE: "-" Don't care

Description	Read modify write control OUT
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

9.1.47 VopSet: Vop set (C0H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
VopSet	0	1	0	1	1	0	0	0	0	0	0	**(C0h)**
1st parameter	1	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	-
2nd parameter	1	1	0	-	-	-	-	-	-	-	Vop8	

NOTE: "-" Don't care

Description	The command is used to program the optimum LCD supply voltage V0.
Restriction	

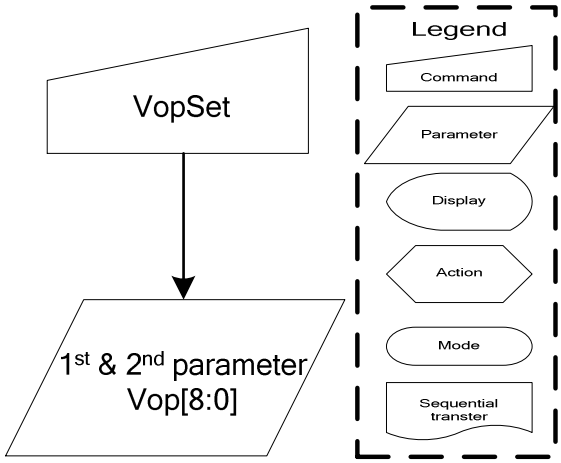
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Vop=12V)	
	Vop8	Vop[7:0]
Power On Sequence	0	11010010b (D2h)
S/W Reset	0	11010010b (D2h)
H/W Reset	0	11010010b (D2h)

Flow Chart



9.1.48 VopOfsetInc: Vop Increase 1 (C1H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
VopOfsetInc	0	1	0	1	1	0	0	0	0	0	1	**(C1h)**

NOTE: "-" Don't care

Description

With the VopOfsetInc and VopOfsetDec command the V0 voltage and therewith the contrast of the LCD can be adjusted. This command increases the value of Vop offset register by 1.

If you set the electronic control value to 1111111, the control value is set to 0000000 after this command has been executed.

Restriction

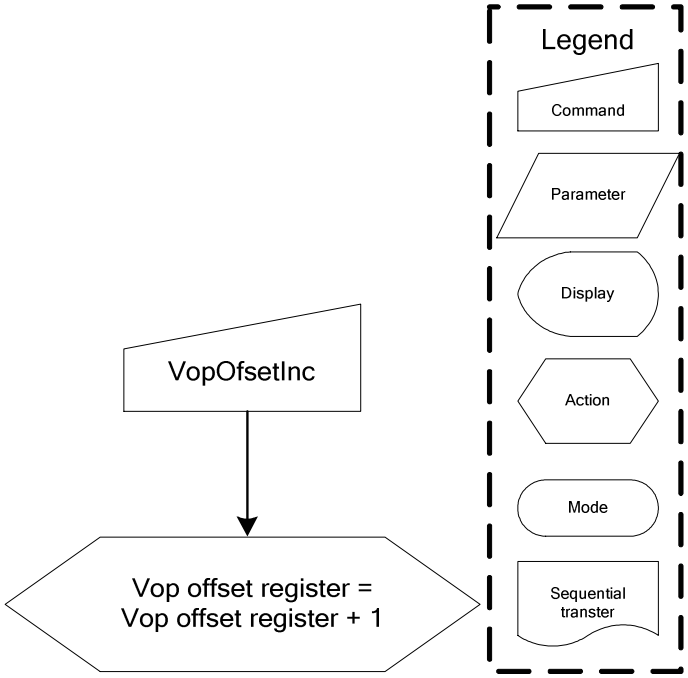
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



9.1.49 VopOfsetDec: Vop Decrease 1 (C2H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
VopOfsetDec	0	1	0	1	1	0	0	0	0	1	0	**(C2h)**

NOTE: "-" Don't care

Description

With the VopOfsetInc and VopOfsetDec command the V0 voltage and therewith the contrast of the LCD can be adjusted. This command decreases the value of Vop offset register by 1.

If you set the electronic control value to 0000000, the control value is set to 1111111 after this command has been executed.

Electronic Control Value	Decimal Equivalent	V0 Offset
0111111	63	+2520 mV
0111110	62	+2480 mV
0111101	61	+2440 mV
…	…	…
0000010	2	+80 mV
0000001	1	+40 mV
0000000	0	0 mV
1111111	-1	-40 mV
1111110	-2	-80 mV
…	…	…
1000010	-62	-2480 mV
1000001	-63	-2520 mV
1000000	-64	-2560mV

Table 9.1.1 Possible Vop[6:0] values

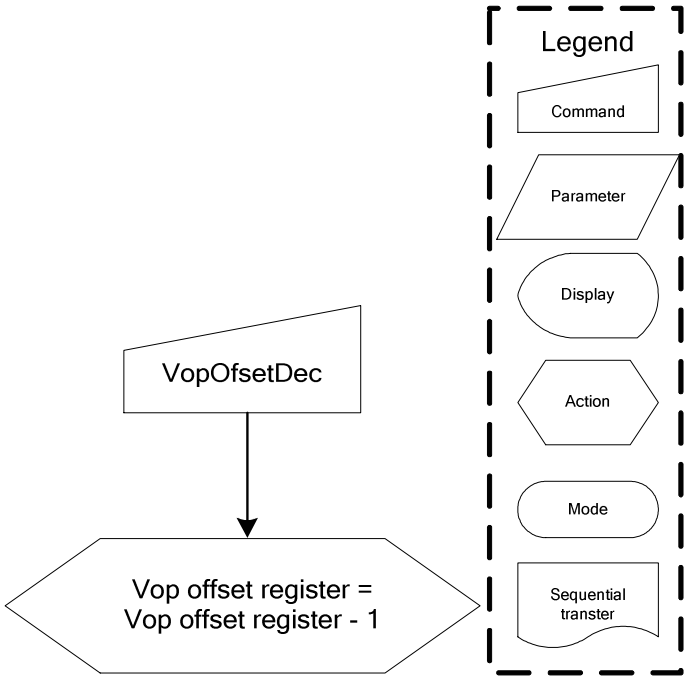
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart	 VopOfsetDec Vop offset register = Vop offset register - 1 Legend Command Parameter Display Action Mode Sequential transter

9.1.50 BiasSel: Bias Selection(C3H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
BiasSel	0	1	0	1	1	0	0	0	0	1	1	**(C3h)**
Parameter	1	1	0	-	-	-	-	-	Bias2	Bias1	Bias0	-

NOTE: "-" Don't care

Description

Select LCD bias ratio of the voltage required for driving the LCD.

Bais2	Bais1	Bais0	LCD bias
0	0	0	1/12
0	0	1	1/11
0	1	0	1/10
0	1	1	1/9
1	0	0	1/8
1	0	1	1/7
1	1	0	1/6
1	1	1	1/5

Restriction

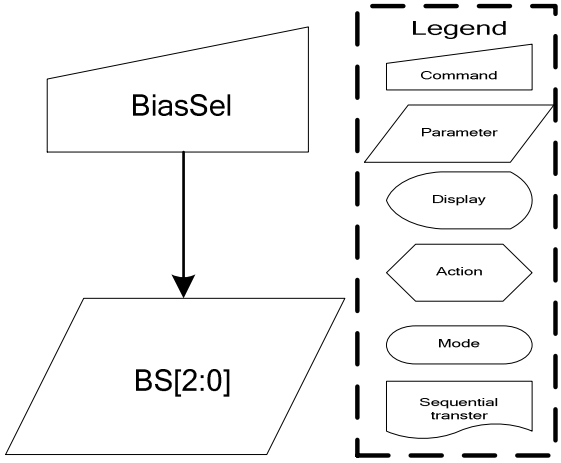
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Bias[2:0])
Power On Sequence	010b
S/W Reset	010b
H/W Reset	010b

Flow Chart



9.1.51 BstPmpXSel: Booster Set(C4H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
BstPmpXSel	0	1	0	1	1	0	0	0	1	0	0	**(C4h)**
Parameter	1	1	0	-	-	-	-	-	BST2	BST 1	BST0	-

NOTE: "-" Don't care

Description

Booster setting

BST2	BST1	BST0	
0	0	0	x1 boosting circuit (Booster off)
0	0	1	x2 boosting circuit
0	1	0	x3 boosting circuit
0	1	1	x4 boosting circuit
1	0	0	x5 boosting circuit
1	0	1	x6 boosting circuit
1	1	0	x7 boosting circuit
1	1	1	x8 boosting circuit

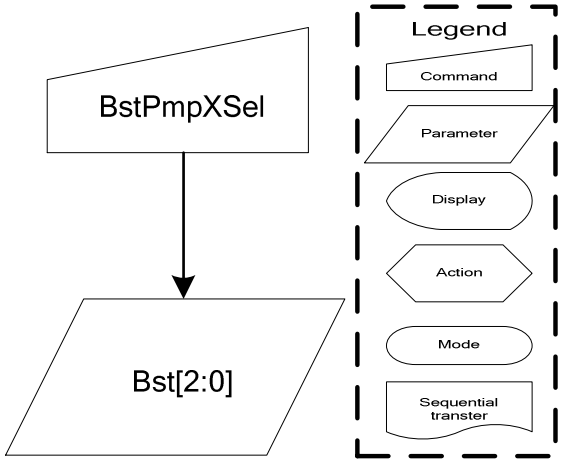
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (BST[2:0])
Power On Sequence	111b
S/W Reset	111b
H/W Reset	111b

Flow Chart	 BstPmpXSel Bst[2:0] Legend Command Parameter Display Action Mode Sequential transter

9.1.52 BstEffSel: Booster Efficiency selection(C5H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
BstEffSel	0	1	0	1	1	0	0	0	1	0	1	**(C5h)**
Parameter	1	1	0	-	-	1	0	-	-	BTF1	BTF0	-

NOTE: "-" Don't care

Description

Booster Efficiency set

BTF1	BTF0	Frequency
0	0	Level 1
0	1	Level 2 (default)
1	0	Level 3

By Booster Stages (2X, 3X, 4X, 5X, 6X, 7X, 8X) and Booster Efficiency (Level1~3) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level3 is higher than level1). The Boost Efficiency is better than lower level, and it just need few more power consumption current.

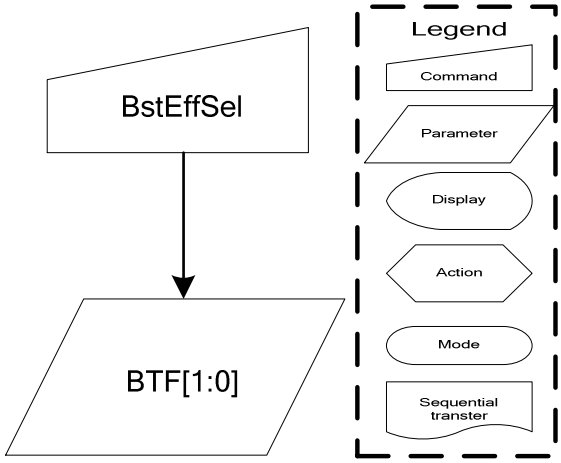
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (BTF[1:0])
Power On Sequence	00100001b (21h)
S/W Reset	00100001b (21h)
H/W Reset	00100001b (21h)

Flow Chart	 BstEffSel BTF[1:0] Legend Command Parameter Display Action Mode Sequential transter

9.1.53 VopOffset: Vop offset fuse bit adjust(C7H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
VopOffset	0	1	0	1	1	0	0	0	1	1	1	**(C7h)**
Parameter1	1	1	0	VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0	**-**
Parameter2	1	1	0	-	-	-	-	-	-	-	VOS8	**-**

NOTE: "-" Don't care

Description

The command is used to the Vop offset for V0.

Vop offset Control Value	**Decimal Equivalent**	**V0 Offset**
…	…	…
000000010	2	+80mV
000000001	1	+40mV
000000000	0	0
111111111	-1	-40mV
111111110	2	-80mV
…	…	…

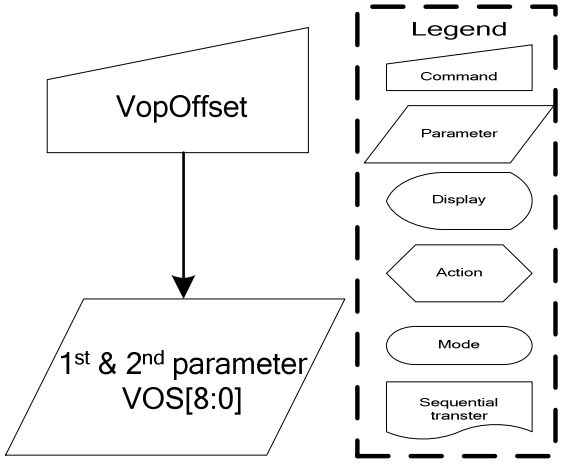
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VOS8	VOS[7:0]
Power On Sequence	0h	00h
S/W Reset	0h	00h
H/W Reset	0h	00h

Flow Chart	 VopOffset 1st & 2nd parameter VOS[8:0] Legend Command Parameter Display Action Mode Sequential transter

9.1.54 V3SorcSel: FV3 with Bst2x control(CBH)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
V3SorcSel	0	1	0	1	1	0	0	1	0	1	1	**(CBh)**
Parameter	1	1	0	-	-	-	-	-	-	-	2BT0	-

NOTE: "-" Don't care

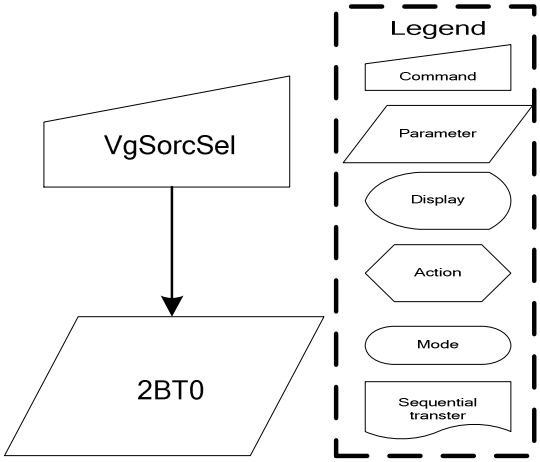
Description	2BT0=0: Vg source comes from VDD2 ; 2BT0=1: Vg source comes from 2-times charge pump.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (2BT0)
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



9.1.55 ID1Set : ID1 setting(CCH)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
ID1Set	0	1	0	1	1	0	0	1	1	0	0	**(CCh)**
Parameter	1	1	0	ID1_7	ID1_6	ID1_5	ID1_4	ID1_3	ID1_2	ID1_1	ID1_0	**-**

NOTE: "-" Don't care

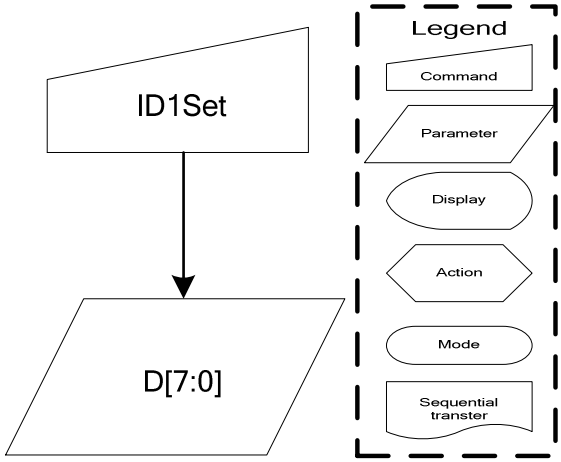
Description	ID1 setting for OPT program data input
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	45h
S/W Reset	45h
H/W Reset	45h

Flow Chart



9.1.56 ID2Set : ID2 setting(CDH)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
ID2Set	0	1	0	1	1	0	0	1	1	0	1	**(CDh)**
Parameter	1	1	0	1	ID2_6	ID2_5	ID2_4	ID2_3	ID2_2	ID2_1	ID2_0	**-**

NOTE: "-" Don't care

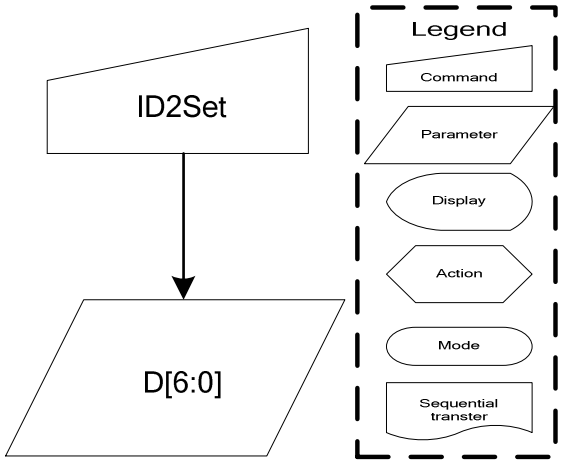
Description	ID2 setting for OPT program data input
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	D2h
S/W Reset	D2h
H/W Reset	D2h

Flow Chart



9.1.57 ID3Set : ID3 setting(CEH)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
ID3Set	0	1	0	1	1	0	0	1	1	1	0	**(CEh)**
Parameter	1	1	0	ID3_7	ID3_6	ID3_5	ID3_4	ID3_3	ID3_2	ID3_1	ID3_0	**-**

NOTE: "-" Don't care

Description	ID3 setting for OPT program data input
Restriction	

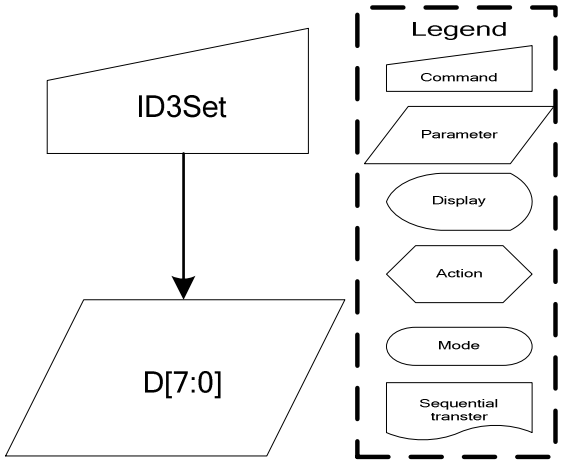
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Eh
S/W Reset	0Eh
H/W Reset	0Eh

Flow Chart



9.1.58 ANASET: Analog circuit setting(D0H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
AutoLoadSet	0	1	0	1	1	0	1	0	0	0	0	**(D0h)**
Parameter	1	1	0	0	0	0	1	1	1	0	1	**-**

NOTE: "-" Don't care

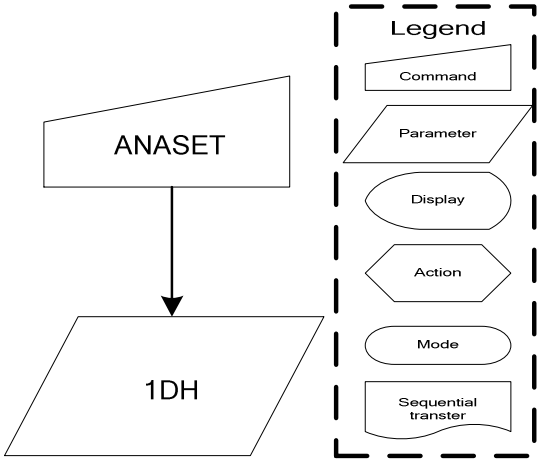
Description	Analog circuit setting. Such as follower selection, level shifter power mode selection.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value D[7:0]
Power On Sequence	1Dh
S/W Reset	1Dh
H/W Reset	1Dh

Flow Chart



9.1.59 AutoLoadSet : mask rom data auto re-load control(D7H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
AutoLoadSet	0	1	0	1	1	0	1	0	1	1	1	**(D7h)**
Parameter	1	1	0	EXTE	OTPBE	0	ARD	1	1	1	1	**-**

NOTE: "-" Don't care

Description

Mask rom data auto re-load control

EXTE : External command enable (OTP bit), 1: enable, 0: disable.

OTPBE: OTPB auto-read enable (OTP bit) , 1: enable, 0: disable.

ARD : OTP auto-read enable control, 1: Disable OTP auto-read,
0: Enable OTP auto-read

Restriction

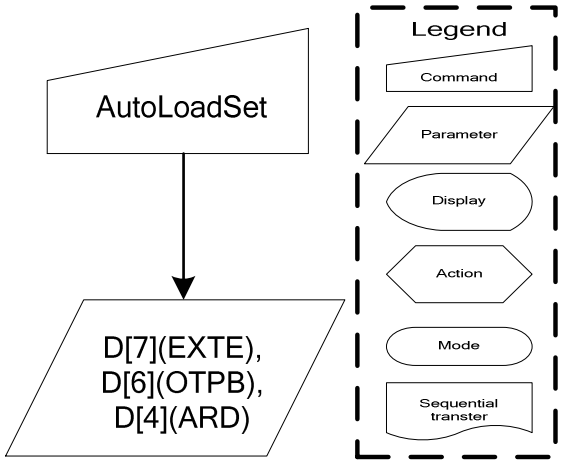
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default ValueD[7:0]
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



9.1.60 RDTstStatus : Read IC status(DEH)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDTstStatus	0	1	0	1	1	0	1	1	1	1	0	**(DEh)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	
Parameter	1	0	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	**-**

NOTE: "-" Don't care

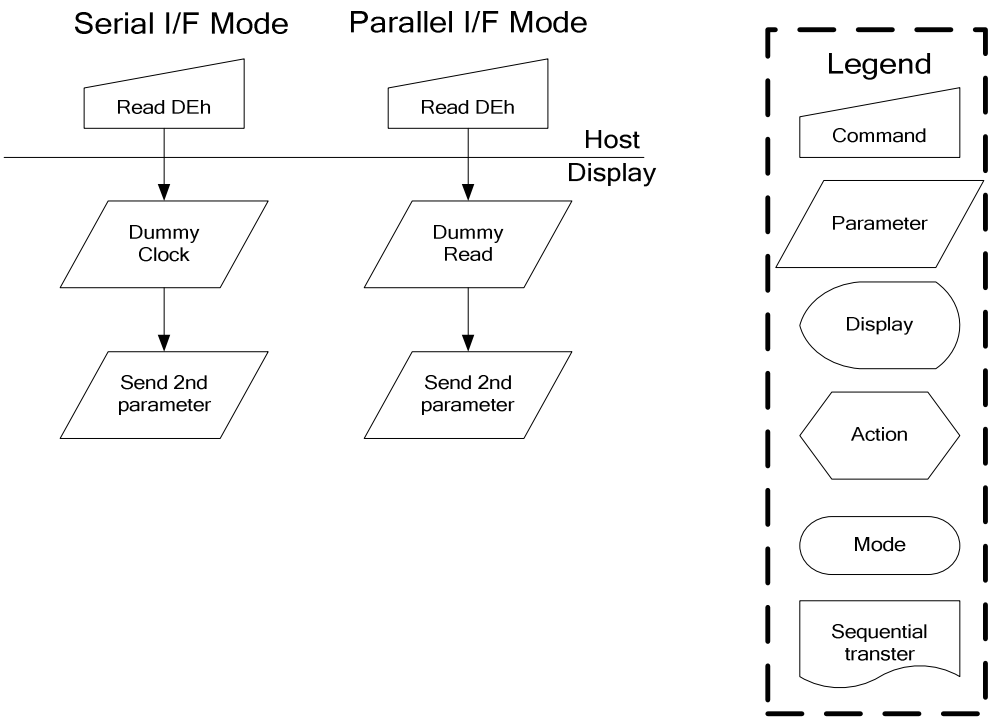
Description	Read IC status. Contect of OTP / RDA / PWR_VOP read control (selection Byte by StusRDSEL[3:0] control)
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	-
S/W Reset	-
H/W Reset	-

Flow Chart



9.1.61 EPCTIN: Control OTP WR/RD(E0H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
EPCTIN	0	1	0	1	1	1	0	0	0	0	0	**(E0h)**
Parameter	1	1	0	0	0	WR /XRD	0	0	0	0	0	-

NOTE: "-" Don't care

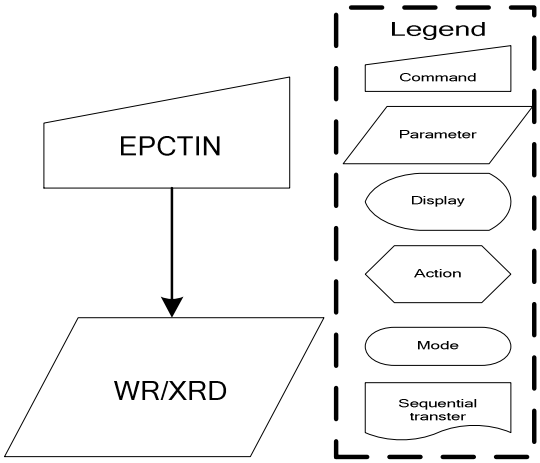
Description	WR/XRD: when setting "1" ➔ The Write Enable of OTP will be opened. WR/XRD: when setting "0" ➔ The Read Enable of OTP will be opened.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (WR/XRD)
Power On Sequence	0
S/W Reset	0
H/W Reset	0

Flow Chart



9.1.62 EPCOUT: OTP control cancel(E1H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
EPCOUT	0	1	0	1	1	1	0	0	0	0	1	**(E1h)**

NOTE: "-" Don't care

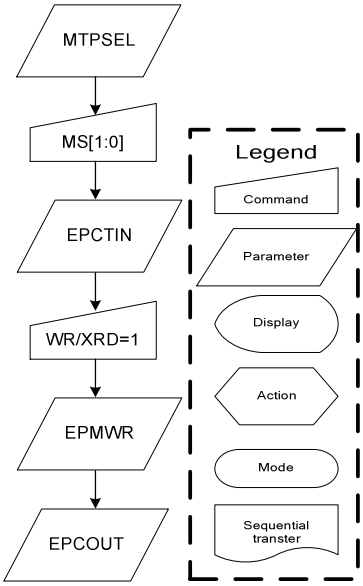
Description	IC exits the OTP control circuit when executing this command.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



9.1.63 EPMWR: Write to OTP(E2H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
EPCOUT	0	1	0	1	1	1	0	0	0	1	0	**(E2h)**

NOTE: "-" Don't care

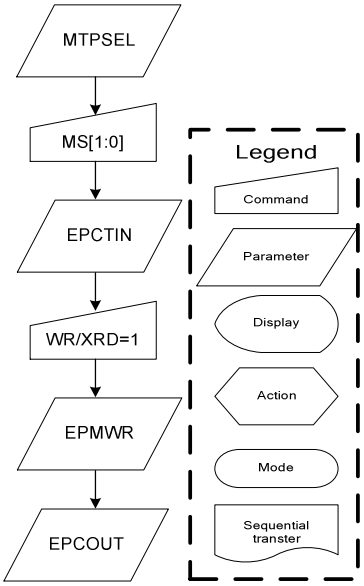
Description	IC actives trigger to start OTP programming when executing this command.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



9.1.64 EPMRD: Read from OTP(E3H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
EPMRD	0	1	0	1	1	1	0	0	0	1	1	**(E3h)**

NOTE: "-" Don't care

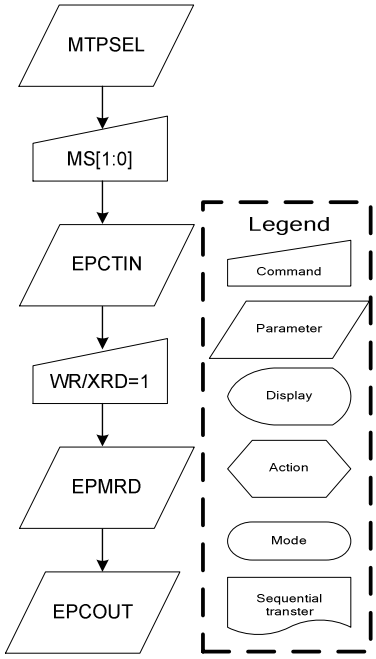
Description	IC actives trigger to start OTP data download to circuit when executing this command.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart



9.1.65 OTPSEL: SEL OTP(E4H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
OTPSEL	0	1	0	1	1	1	0	0	1	0	0	**(E4h)**
Parameter	1	1	0	MS1	MS0	0	1	1	0	0	0	-

NOTE: "-" Don't care

Description

This command defines OTP/ OTPB selection for EEPROM control. Please see the table as below:

MS1	MS0	Mode
0	0	Disable
0	1	OTP
1	1	OTPB

Restriction

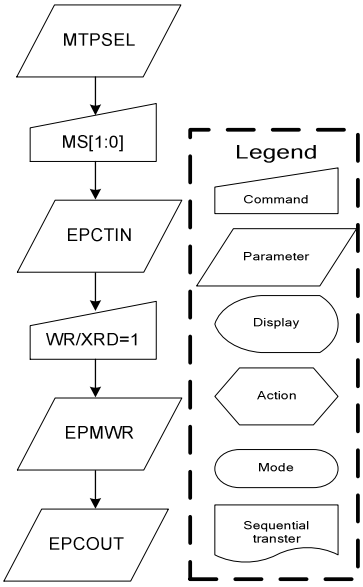
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (MS[1:0])
Power On Sequence	00
S/W Reset	00
H/W Reset	00

Flow Chart



9.1.66 ROMSET: Programmable rom setting(E5H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
AutoLoadSet	0	1	0	0	1	1	1	0	1	0	1	**(E5h)**
Parameter	1	1	0	0	0	0	0	1	0	0	1	**-**

NOTE: "-" Don't care

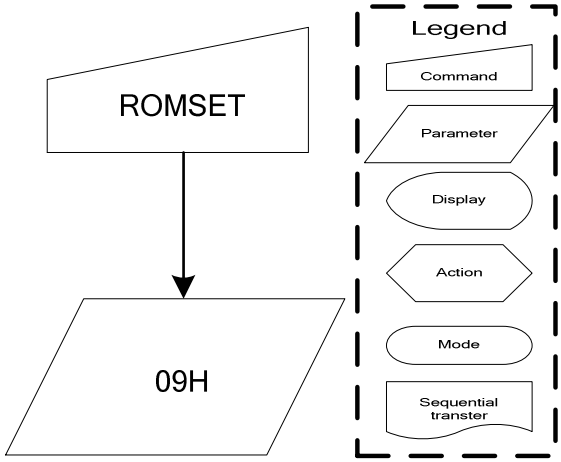
Description	Set the OTP writing timing. Value 0x09 is the best value for ST7628.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value D[7:0]
Power On Sequence	0Fh
S/W Reset	0Fh
H/W Reset	0Fh

Flow Chart



9.1.67 StusRDSel : Fuse data readout control(E6H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
StusRDSel	0	1	0	1	1	1	0	0	1	1	0	**(E6h)**
Parameter	1	1	0	-	-	-	-	STU3	STU2	STU1	STU0	**-**

NOTE: "-" Don't care

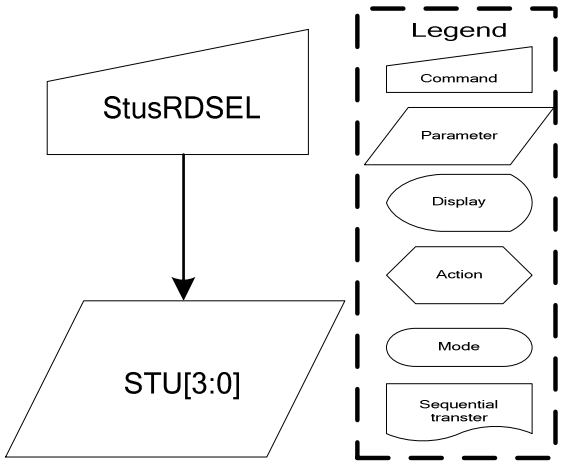
Description	Status read out byte selection STU[3:0] = 0h-3h: OTP.D[7:0], D[15:8], D[23:16], D[31:24], 4h-7h: Dummy data 8h-Bh: OTPB.D[7:0], D[15:8], D[23:16], D[31:24],
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0
S/W Reset	0
H/W Reset	0

Flow Chart



9.1.68 FRMSEL: Frame Freq. in Temp. range (F0H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	0	0	F0H
1st parameter	1	1	0	-	-	-	FA4	FA3	FA2	FA1	FA0	Range A
2nd parameter	1	1	0	-	-	-	FB4	FB3	FB2	FB1	FB0	Range B
3rd parameter	1	1	0	-	-	-	FC4	FC3	FC2	FC1	FC0	Range C
4th parameter	1	1	0	-	-	-	FD4	FD3	FD2	FD1	FD0	Range D

Description

Select Frame Freq. in normal display mode.

1st parameter : Frame freq. value set in temperature range 30(-30℃) to TA

2nd parameter : Frame freq. value set in temperature P range TA to TB

3rd parameter : Frame freq. value set in temperature range TB to TC

4th parameter : Frame freq. value set in temperature range TC to 145(90℃)

For command setting to frame rate value look-up-table, please see the following table:

Reg(dec)	Reg(hex)	Frame Rate (Hz)
0	00	37.5
1	01	38
2	02	38.5
3	03	40
4	04	42
5	05	44
6	06	46
7	07	48.5
8	08	51
9	09	54
10	0A	57.5
11	0B	61.5
12	0C	66.5
13	0D	72
14	0E	77.5
15	0F	85
16	10	75
17	11	76
18	12	77
19	13	80
20	14	84

21	15	88		
22	16	92		
23	17	97		
24	18	102		
25	19	108		
26	1A	115		
27	1B	123		
28	1C	133		
29	1D	144		
30	1E	155		
31	1F	170		

Restriction

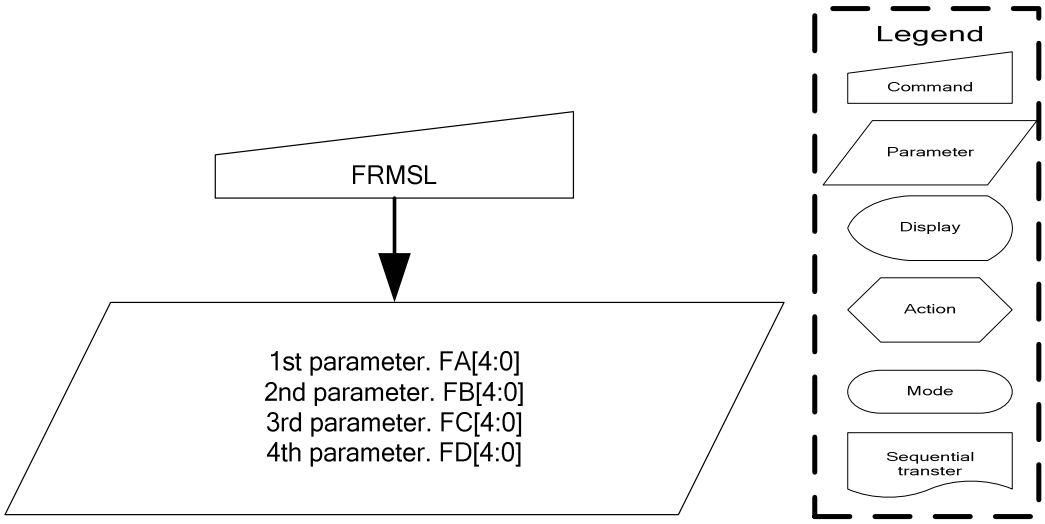
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	FA[4:0]	FB[4:0]	FC[4:0]	FD[4:0]
Power On Sequence	06h	0Bh	12h	14h
S/W Reset	06h	0Bh	12h	14h
H/W Reset	06h	0Bh	12h	14h

Flow Chart


FRMSL
1st parameter. FA[4:0]
2nd parameter. FB[4:0]
3rd parameter. FC[4:0]
4th parameter. FD[4:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.69 FRM8SEL: Frame Freq. in Temp. range (idel-8 color) (F1H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	0	1	F1H
1st parameter	1	1	0	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0	Range A
2nd parameter	1	1	0	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0	Range B
3rd parameter	1	1	0	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0	Range C
4th parameter	1	1	0	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0	Range D

Description

Select Frame Freq. in normal display mode.(idle;8 color mode)

1st parameter : Frame freq. value set in TEMP range 30(-30℃) to TA

2nd parameter : Frame freq. value set in TEMP range TA to TB

3rd parameter : Frame freq. value set in TEMP range TB to TC

4th parameter : Frame freq. value set in TEMP range TC to 145(90℃)

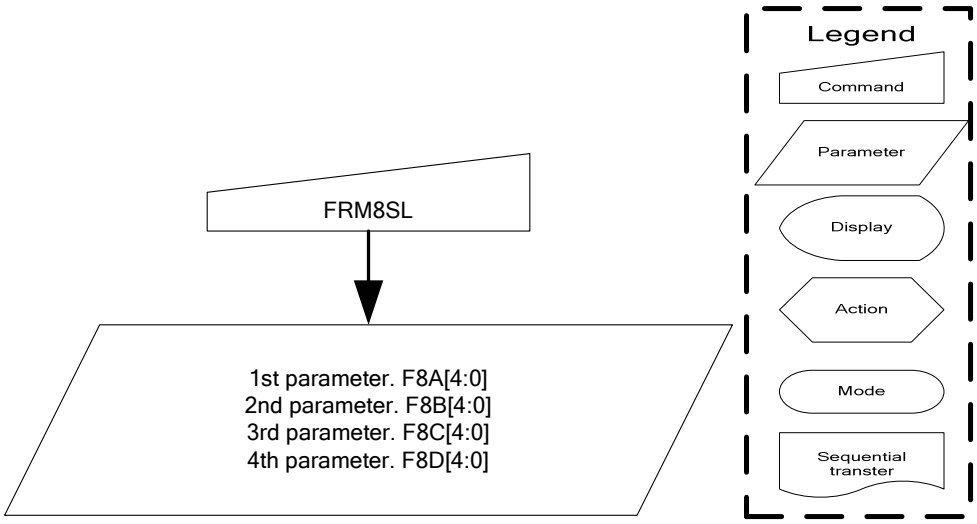
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	FA[4:0]	FB[4:0]	FC[4:0]	FD[4:0]
Power On Sequence	06h	0Bh	12h	14h
S/W Reset	06h	0Bh	12h	14h
H/W Reset	06h	0Bh	12h	14h

Flow Chart	

FRM8SL
1st parameter. F8A[4:0]
2nd parameter. F8B[4:0]
3rd parameter. F8C[4:0]
4th parameter. F8D[4:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.70 TMPRNG: Temp. range set for Frame Freq. Adj. (F2H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	1	0	F2H
1st parameter	1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	Range A
2nd parameter	1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	Range B
3rd parameter	1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	Range C

Description

Temp. range set for automatic frame freq. adj. operation according the current temp. value.

1st parameter: Temp. range A value set

2nd parameter: Temp. range B value set

3rd parameter: Temp. range C value set

TA/TB/TC Temperature(℃) + 40 = TA/TB/TC[6:0]

Example:

If TA wants to be set at 24℃, TA[6:0]=24+40=64(40h),

Restriction

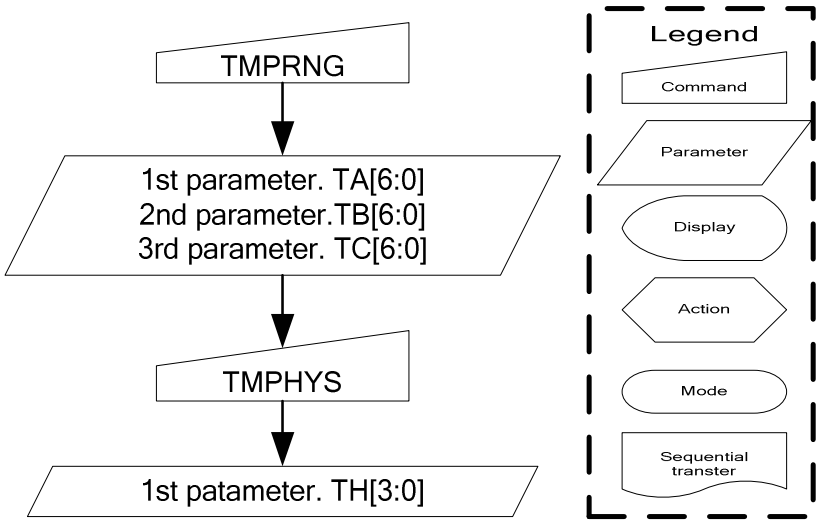
-40℃≦TA≦TA+TH≦TB≦TB+TH≦TC≦87℃

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	TA[6:0]	TB[6:0]	TC[6:0]
Power On Sequence	18h	28h	58h
S/W Reset	18h	28h	58h
H/W Reset	18h	28h	58h

Flow Chart	

TMPRNG
1st parameter. TA[6:0]
2nd parameter.TB[6:0]
3rd parameter. TC[6:0]
TMPHYS
1st patameter. TH[3:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.71 TMPHYS: Temp.Hysteresis Set for Frame Freq. Adj.(F3H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	1	1	F3H
1st parameter	1	1	0	-	-	-	-	TH3	TH2	TH1	TH0	

Description

Temp. hysteresis range set for frame freq. adj.

Parameter TH[3:0] is used to set Temp. hysteresis range.

The relationship between temp. state and temp. range value is shown below.

TEMP Range Value	TEMP Rising State	TEMP Falling State
Freq. changing point A	TA[6:0]+TH[3:0]	TA[6:0]
Freq. changing point B	TB[6:0]+TH[3:0]	TB[6:0]
Freq. changing point C	TC[6:0]+TH[3:0]	TC[6:0]

TH Temperature(℃) - 1 = TH[3:0]

Example:

If TH wants to set 5℃, TH[3:0]=5-1=4.

Restriction

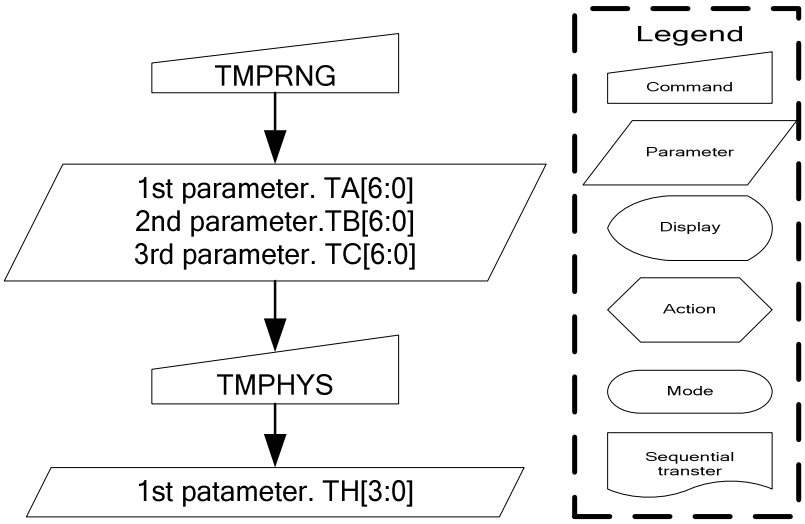
Temp. hysteresis value should be smaller than the gap of temp. range.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value(TH[3:0])
Power On Sequence	04h
S/W Reset	04h
H/W Reset	04h

Flow Chart	

TMPRNG
1st parameter. TA[6:0]
2nd parameter.TB[6:0]
3rd parameter. TC[6:0]
TMPHYS
1st patameter. TH[3:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.72 TEMPSEL: Temp. Set(F4H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	**(F4h)**
1st parameter	1	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00	(-24 °C to -32 °C) (-32 °C to -40 °C)
2nd parameter	1	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	(-8 °C to -16 °C) (-16 °C to -24 °C)
3rd parameter	1	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	(8 °C to 0 °C) (0 °C to -8 °C)
4th parameter	1	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	(24 °C to16 °C) (16 °C to 8 °C)
5th parameter	1	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	(40 °C to 32 °C) (32 °C to 24 °C)
6th parameter	1	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	(56 °C to 48 °C) (48 °C to 40 °C)
7th parameter	1	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	(72 °C to 64 °C) (64 °C to 56 °C)
8th parameter	1	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	(87 °C to 80 °C) (80 °C to 72 °C)

NOTE: "-" Don't care

Description

This command defines temperature gradient compensation coefficient. For this command detail description and opearation, please see Section 1.1.1.

Parameter n	**MT n 3**	**MT n 2**	**MT n 1**	**MT n 0**	**Voltage / °C (+/- 3mv tolerance)**
0	**0**	**0**	**0**	**0**	**0 mv / °C**
1	**0**	**0**	**0**	**1**	**-5 mv / °C**
2	**0**	**0**	**1**	**0**	**-10 mv / °C**
3	**0**	**0**	**1**	**1**	**-15 mv / °C**
: **:** **:**	**:** **:** **:**	**:** **:** **:**	**:** **:** **:**	**:** **:** **:**	**:** **:** **:**
12	**1**	**1**	**0**	**0**	**-60 mv / °C**
13	**1**	**1**	**0**	**1**	**-65 mv / °C**
14	**1**	**1**	**1**	**0**	**-70 mv / °C**
15	**1**	**1**	**1**	**1**	**-75 mv / °C**

Restriction

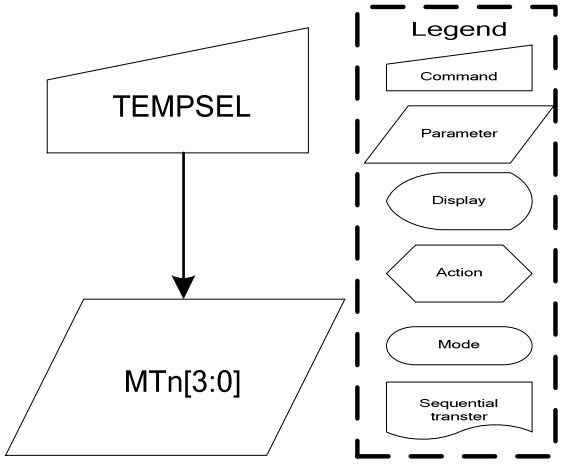
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (MTn[3:0])
Power On Sequence	1st parameter 0x50
S/W Reset	2nd parameter 0x00
H/W Reset	3rd parameter 0x25
	4th parameter 0x61
	5th parameter 0x35
	6th parameter 0x64
	7th parameter 0xAA
	8th parameter 0xFF

Flow Chart



9.1.73 THYS : Temperature detection threshold(F7H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
THYS	0	1	0	1	1	1	1	0	1	1	1	**(F7h)**
Parameter	1	1	0	THYS7	THYS6	THYS5	THYS4	THYS3	THYS2	THYS1	THYS0	**-**

NOTE: "-" Don't care

Description	Temperature detection threshold setting.
Restriction	

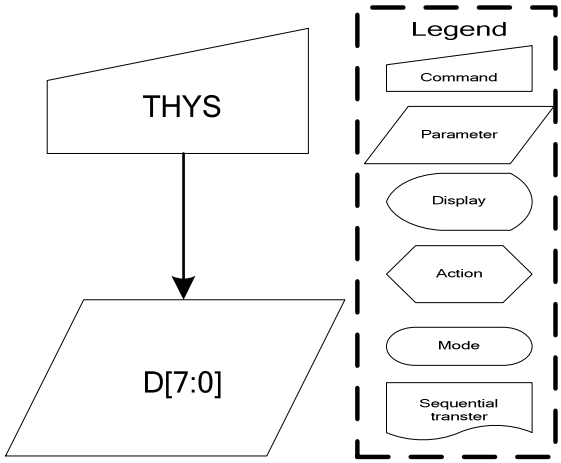
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value D[7:0]
Power On Sequence	06h
S/W Reset	06h
H/W Reset	06h

Flow Chart



9.1.74 Frame Set: Frame PWM Set (F9H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
Frame1 Set	0	1	0	1	1	1	1	1	0	0	1	**(F9h)**
1st parameter	1	1	0	-	-	-	P14	P13	P12	P11	P10	-
2nd parameter	1	1	0	-	-	-	P24	P23	P22	P21	P20	-
:	:	:	:	:	:	:	:	:	:	:	:	-
15th parameter	1	1	0	-	-	-	P154	P153	P152	P151	P150	-
16th parameter	1	1	0	-	-	-	P164	P163	P162	P161	P160	-

NOTE: "-" Don't care

Description	This command is used to set frame1 PWM.
Restriction	

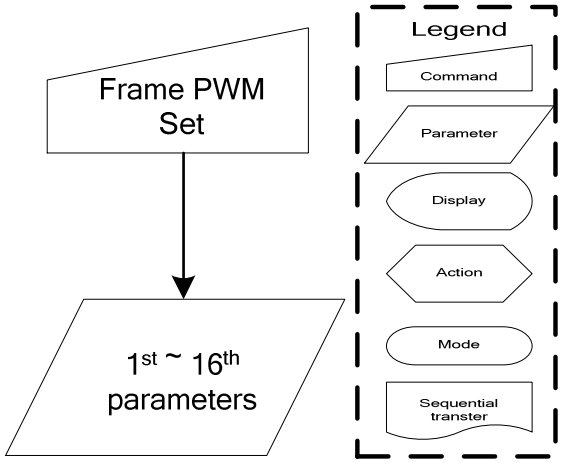
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to below table.
S/W Reset	Refer to below table.
H/W Reset	Refer to below table.

Flow Chart



NOTE:

The default value of RGB level set

RGB level0	00
RGB level1	08
RGB level2	0A
RGB level3	0D
RGB level4	0F
RGB level5	10
RGB level6	12
RGB level7	14
RGB level8	15
RGB level9	16
RGB level10	17
RGB level11	18
RGB level12	19
RGB level13	1A
RGB level14	1B
RGB level15	1D

All the modulation range of each level for each frame is from 00’H to 1F’H.

10. SPECIFICATIONS

10.1 ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Item	Symbol	Value	Unit
Supply voltage (1)	V_{DD}	- 0.3 ~ + 3.0	V
Supply voltage (1)	V_{DD2}, V_{DD3}, V_{DD4}, V_{DD5}	- 0.3 ~ + 4.2	V
Supply voltage (2)	V_{LCD} (V0-VSS)	- 0.3 ~ + 18.0	V
Supply voltage (3)	V_{MAX} (V0- XV0)	- 0.3 ~ + 18.0	V
Input voltage range	V_{IN}	- 0.3 ~ V_{DD} + 0.5	V
Output voltage range	V_O	- 0.3 ~ V_{DD} + 0.5	V
Operating temperature range	T_{OPR}	- 30 ~ + 85	℃
Storage temperature range	T_{STG}	- 40 ~ + 125	℃

NOTE: Voltages are all based on VSS = 0V.

10.2DC CHARACTERISTICS

10.2.1 Basic Characteristics

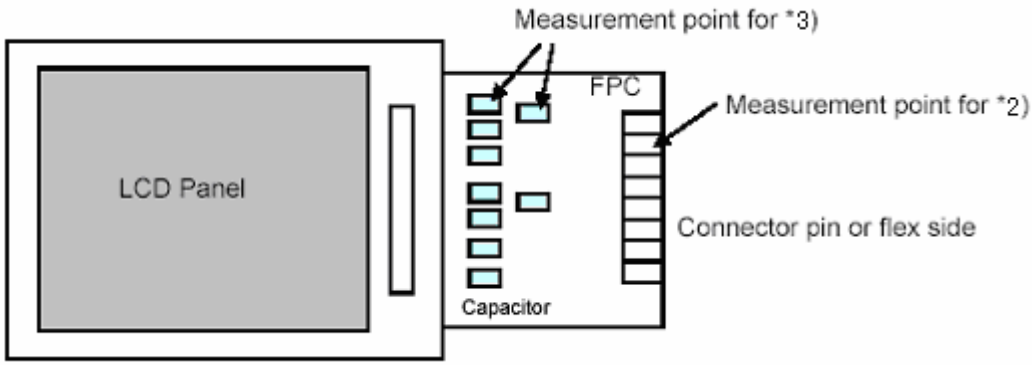
(V_{SS}=0V, Ta = -30 to 70℃)

Parameter	Symbol	Conditions	Related Pins	MIN	TYP	MAX	Unit
Logic Operating voltage	V_{DDI}	-	*2) VDD	1.65	1.8	3.0	V
Analog Operating voltage	V_{DDA}	-	*2) VDD2,3,4,5	2.4	2.75	3.3	
Driving voltage input	V_{LCD}	V0 - VSS	*3) V0, VSS	-	-	18.0	
	XV_{LCD}	VSS – XV0	*3) VSS, XV0	-	-	18.0	
High level input voltage	V_{IH}		*1) *2)	0.7V_{DD}	-	V_{DD}	
Low level input voltage	V_{IL}	-	*1) *2)	V_{SS}	-	0.3V_{DD}	
High level output voltage	V_{OH}	I_{OH} = -1.0mA	*2) SI, TE	0.8V_{DD}	-	V_{DD}	
Low level output voltage	V_{OL}	I_{OL} = +1.0mA		V_{SS}	-	0.2V_{DD}	
Input leakage current	I_{IL}	V_{IN} = V_{DD} or V_{SS}	*1), *2)	-1.0	-	+1.0	μA
Driver on resistance (SEG)	R_{ONSEG}	Vg = 5.0V	S0 to S293	-	0.35	1.0	KΩ
Driver on resistance (COM)	R_{ONCOM}	V0 = 10.0V	C0 to C69	-	0.4	1.0	
External oscillator frequency	f_{OSC}	fFR=77Hz	CL	-	334.18	-	kHz
Frame Rate	Fr			70	77	84	Hz
Booster1 output voltage range	V0		VDD2,3,4,5	1.8*bias/2	-	18	V
Reference voltage	V_{REF}	No load	-	1.75	1.8	1.85	V
Voltage follower output voltage	Vm	Ta = 25℃	-	0.7	Vg/2	V_{DDA} -0.7	V
Booster2 output voltage range	Vg		VDD2,3,4,5	1.8	-	V_{DDA} X2	V
Booster3 output voltage range	XV0		VDD2,3,4,5	Vg-18	-	-	V

NOTE:

**1) Applies to IF1, IF2, IF3, /CS, /RST, /WR, /RD, A0(SCL) and D15-D2, D1 (A0) ,D0(SI) pins*

**2) *3) When the measurement are performed with LCD module, Measurement Points are like below.*



10.2.2 Current Consumption(Bare die)

VDDI=1.8V, VDDA=2.8V, Vop=13V, Booster=8X, BIAS=1/10, Booster efficiency=01.

Host I/F	Mode of operation	Frame Frequency	Image	Memory Data Access Control (MY:MX:MV)	Current consumption			
					Typical		Worst case	
					V_{DDA} (mA)	V_{DDI} (mA)	V_{DDA} (mA)	V_{DDI} (mA)
Host interface NOT active	- **Normal** Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	77Hz±10 %	Note 1	X;X;X	0.12	0.03	0.16	0.04
			Note 2	X;X;X	0.12	0.03	0.16	0.04
			Note 3	X;X;X	0.12	0.03	0.16	0.04
			Note 4	X;X;X	0.12	0.03	0.16	0.04
			Note 5	X;X;X	0.12	0.03	0.16	0.04
			Note 7	X;X;X	0.13	0.03	0.16	0.04
	- Normal Mode On - Partial Mode Off - **Idle** Mode On - Sleep Out Mode	77Hz±10 %	Note 5	X;X;X	0.12	0.03	0.16	0.04
	- Normal Mode Off - **Partial** Mode On (32 lines) - Idle Mode Off - Sleep Out Mode	77Hz±10 %	Grey Levels	X;X;X	0.1	0.03	0.16	0.04
	- Normal Mode Off - **Partial** Mode On (32 lines) - **Idle** Mode On - Sleep Out Mode	77Hz±10 %	Grey Levels	X;X;X	0.1	0.03	0.16	0.04
			Note 6	X;X;X	0.12	0.03	0.16	0.04
	- Sleep In Mode	N/A	N/A	X;X;X	0.002	0.003	0.003	0.005
Host interface active	- **Normal** Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	77Hz±10 %	65536 Colors Note 8 CPU Access @ 10fps	0;0;0	0.12	0.03	0.16	0.04
				0;0;1	0.12	0.03	0.16	0.04
				0;1;0	0.12	0.03	0.16	0.04
				0;1;1	0.12	0.03	0.16	0.04
				1;0;0	0.12	0.03	0.16	0.04
				1;0;1	0.12	0.03	0.16	0.04
				1;1;0	0.12	0.03	0.16	0.04
				1;1;1	0.12	0.03	0.16	0.04

NOTE:

X Do not care

1. All pixels black

2. Checker board one by one

3. Checker board 4 by 4

4. Grey-scale from top to bottom

5. 20% Black, 80%White

6. Black & White Checker board 8 by 8.

7. Absolute Worst Case Patterns: Defined by Display Supplier

8. Absolute Worst Case Patterns and Sequences: Defined by Display Supplier

Typical Case:

TA = 25ºC

VDDI = 1.8V

VDDA = 2.8V

Worst Case:

TA = 25ºC

VDDI= 1.65V to 3.0V

VDDA = 2.4V to 3.3V

9. Absolute worst case VDDA current is less than 1.0mA in the case of Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.

10. Absolute worst case VDDI current is less than 0.2mA in the case of Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.

11. TIMING CHARACTERISTICS

11.1Parallel Interface Characteristics bus (8080-series MCU)

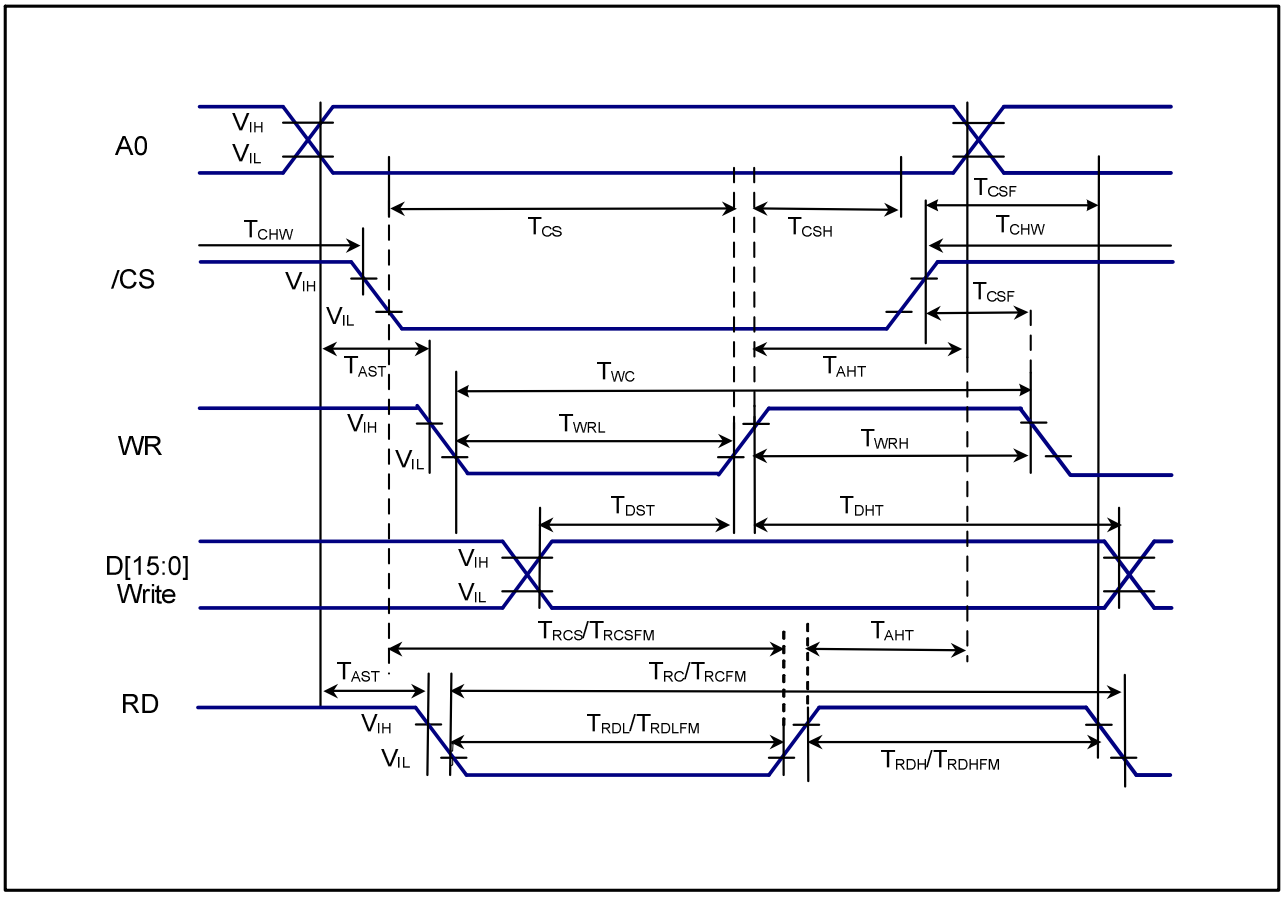


Figure 11.1 Parallel Interface Characteristics bus(8080-series MCU)

(V_{SS}=0V, V_{DDI}=1.65V to 3.0V, V_{DDA}=2.4V to 3.3V,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
A0	T_{AST}	Address setup time	10	-	ns	-
	T_{AHT}	Address hold time (Write/Read)	10	-	ns	
/CS	T_{CHW}	Chip select "H" pulse width	0	-	ns	
	T_{CS}	Chip select setup time (Write)	35	-	ns	
	T_{RCS}	Chip select setup time (Read ID)	100	-	ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355	-	ns	
	T_{CSF}	Chip select wait time (Write/Read)	10	-	ns	
WR	T_{WC}	Write cycle	250	-	ns	
	T_{WRH}	Control pulse "H" duration	150	-	ns	
	T_{WRL}	Control pulse "L" duration	60	-	ns	
RD (ID)	T_{RC}	Read cycle (ID)	160	-	ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	45	-	ns	
	T_{RDL}	Control pulse "L" duration (ID)	100	-	ns	
RD (FM)	T_{RCFM}	Read cycle (FM)	450	-	ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	355	-	ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	90	-	ns	
D[15:0]	T_{DST}	Data setup time	30	-	ns	
	T_{DHT}	Data hold time	10	-	ns	

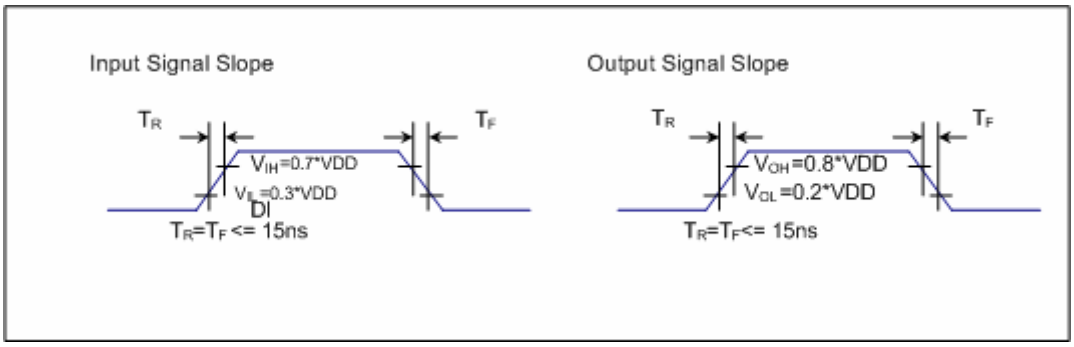


Figure 11.2 Rising and Falling timing for Input and Output signal

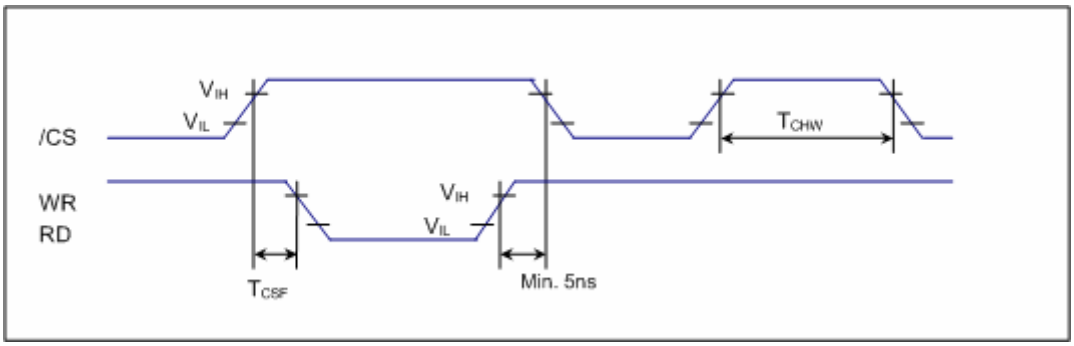


Figure 11.3 Chip selection (CSX) timing

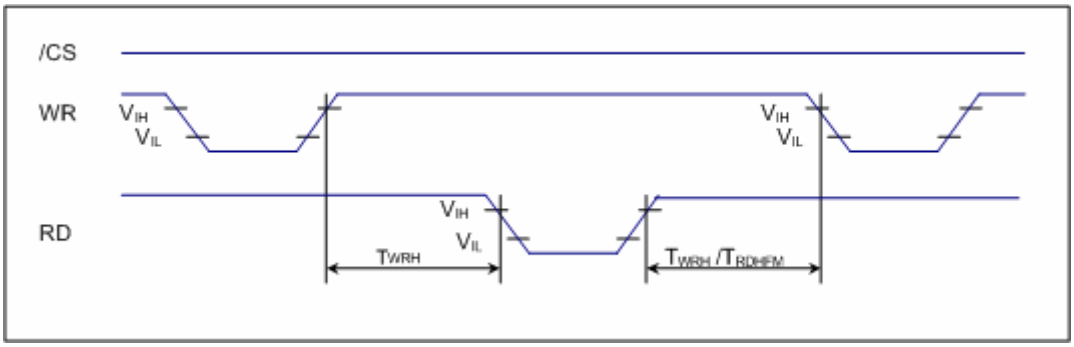


Figure 11.4 Write to read and Read to write timing

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDD for Input signals.

11.2Parallel Interface Characteristics bus (6800-series MCU)

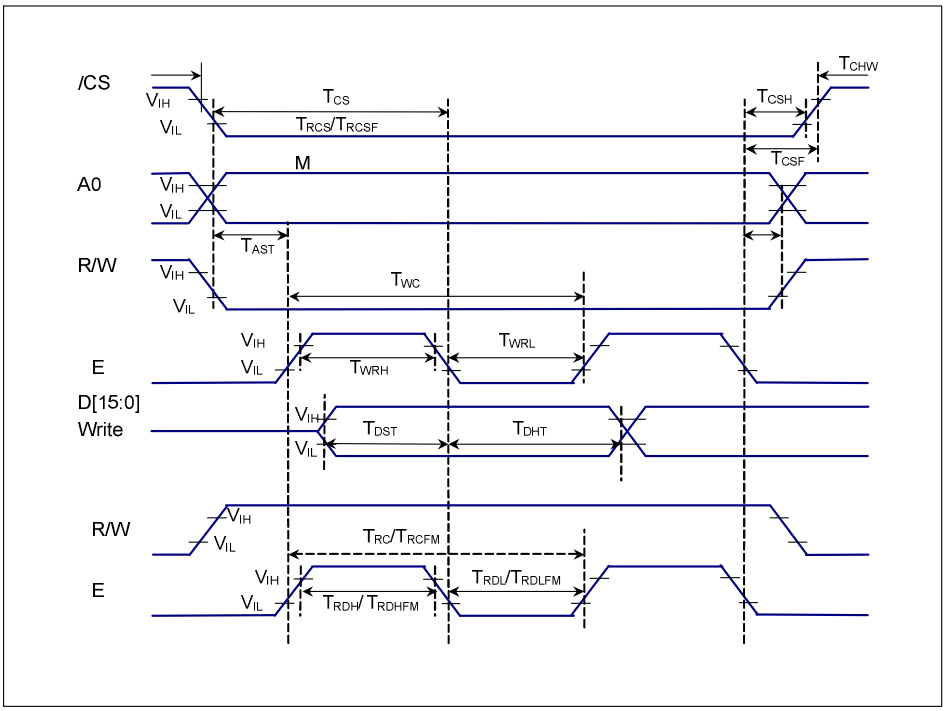


Figure 11.5 Parallel Interface characteristics (6800-Series MCU)

(V_{SS}=0V, V_{DDI}=1.65V to 3.0V, V_{DDA}=2.4V to 3.3V,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
A0	T_{AST}	Address setup time	10	-	ns	-
	T_{AHT}	Address hold time (Write/Read)	10	-	ns	
/CS	T_{CHW}	Chip select "H" pulse width	0	-	ns	
	T_{CS}	Chip select setup time (Write)	35	-	ns	
	T_{RCS}	Chip select setup time (Read ID)	70	-	ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355	-	ns	
	T_{CSF}	Chip select wait time (Write/Read)	10	-	ns	
	T_{CSH}	Chip select hold time	10	-	ns	
R/W	T_{WC}	Write cycle	250	-	ns	
	T_{WRH}	Control pulse "H" duration	50	-	ns	
	T_{WRL}	Control pulse "L" duration	130	-	ns	
E (ID)	T_{RC}	Read cycle (ID)	140	-	ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	50	-	ns	
	T_{RDL}	Control pulse "L" duration (ID)	20	-	ns	
E (FM)	T_{RCFM}	Read cycle (FM)	400	-	ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	80	-	ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	200	-	ns	
D[15:0]	T_{DST}	Data setup time	50	-	ns	
	T_{DHT}	Data hold time	10	-	ns	

11.3Serial Interface Characteristics (3-pin Serial)

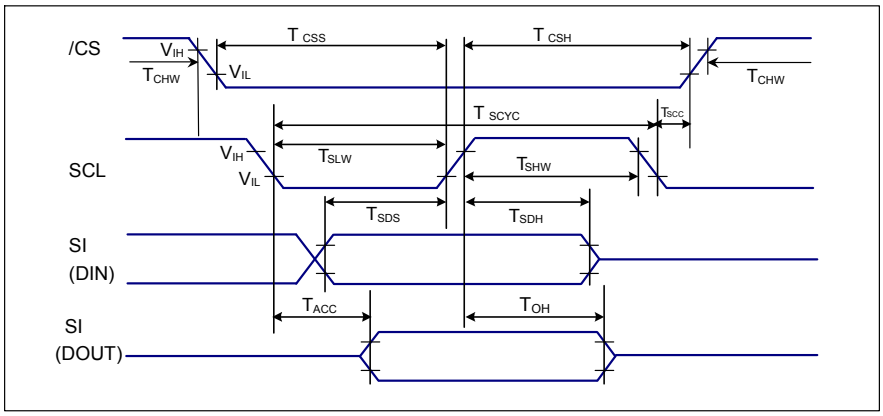


Figure 11.6 3-pin Serial Interface Characteristics

(V_{SS}=0V, V_{DDI}=1.65V to 3.0V, V_{DDA}=2.4V to 3.3V,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
/CS	T_{CHW}	/CS "H" pulse width	45		ns	
	T_{CSS}	/CS-SCL setup time(Write)	60		ns	
	T_{CSH}	/CS-SCL hold time(Write)	65		ns	
	T_{SCC}	Chip select setup time	20		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	100		ns	
	T_{SHW}	SCL "H" pulse width (Write)	35		ns	
	T_{SLW}	SCL "L" pulse width (Write)	35		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SI (DIN) (DOUT)	T_{SDS}	Data setup time	60		ns	
	T_{SDH}	Data hold time	60		ns	
	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	T_{OH}	Output disable time	15	50	ns	

11.4 Serial Interface Characteristics (4-pin Serial)

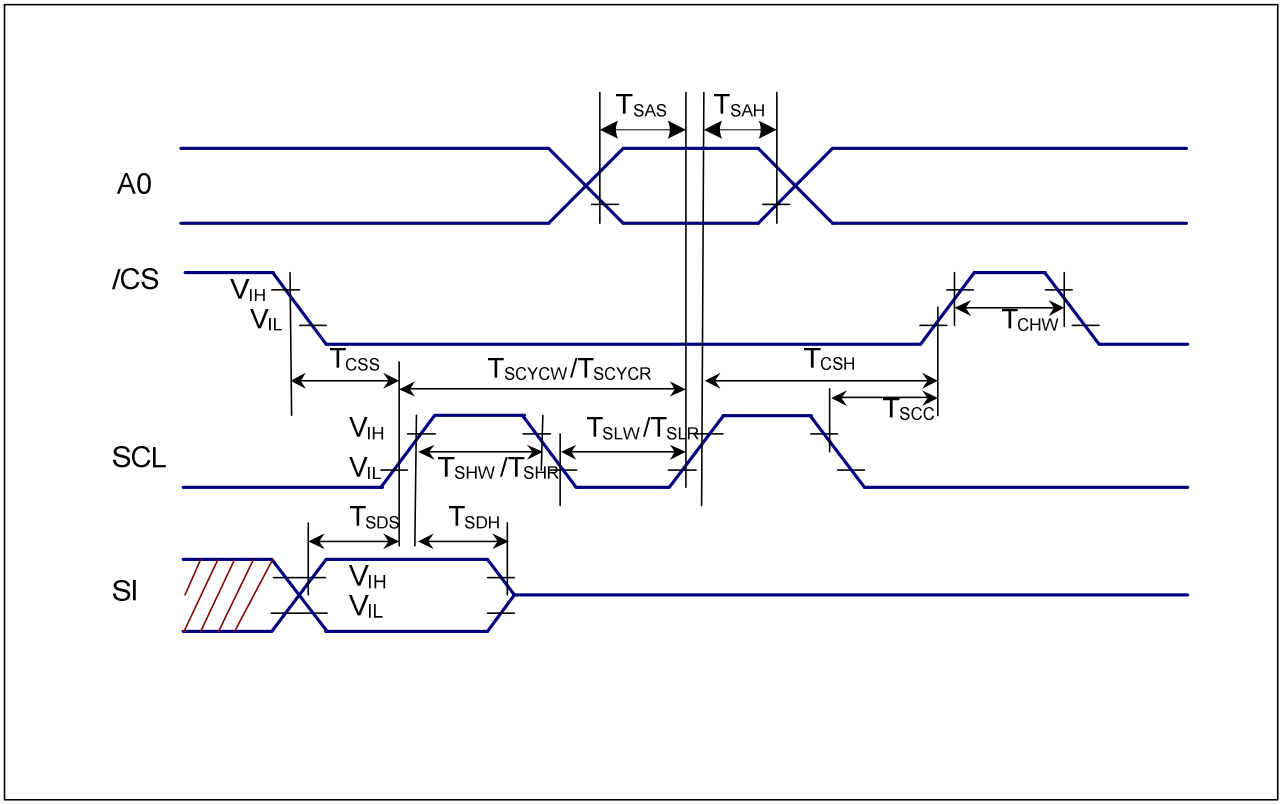
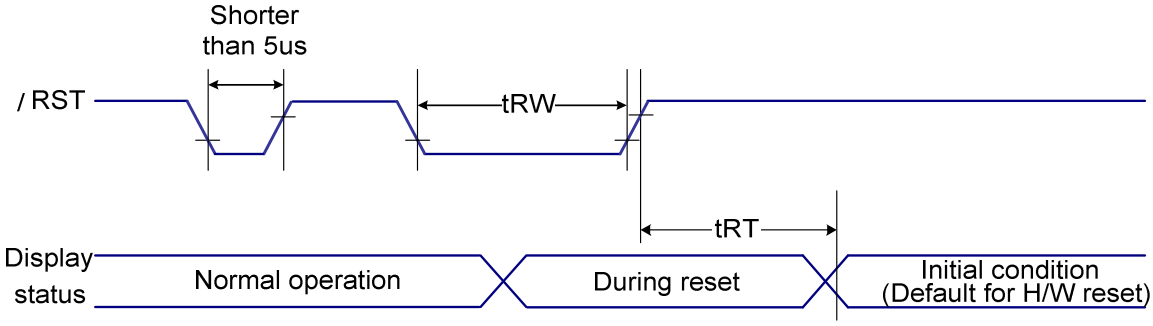


Figure 11.7 4-pin Serial Interface Characteristics

(V_{SS}=0V, V_{DDI}=1.65V to 3.0V, V_{DDA}=2.4V to 3.3V,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
/CS	T_{CSS}	Chip select setup time	60		ns	
	T_{CSH}	Chip select hold time	65		ns	
	T_{SCC}	Chip select setup time	20		ns	
	T_{CHW}	Chip select setup time	45		ns	
A0	T_{SAS}	Address setup time	30		ns	
	T_{SAH}	Address hold time	30		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	100		ns	
	T_{SHW}	SCL “H” pulse width (Write)	35		ns	
	T_{SLW}	SCL “L” pulse width (Write)	35		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SI	T_{SDS}	Data setup time	60		ns	
	T_{SDH}	Data hold time	60		ns	

12. RESET TIMING



(VSS=0V, VDDI=1.65V to 3.0V, VDDA=2.4V to 3.3V,Ta = -30 to 70° C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Reset "L" pulse width	/RST	tRW		10	—	us
Reset time		tRT		—	5 (*note 5)	ms
				—	120 (*note 6,7)	ms

Notes:

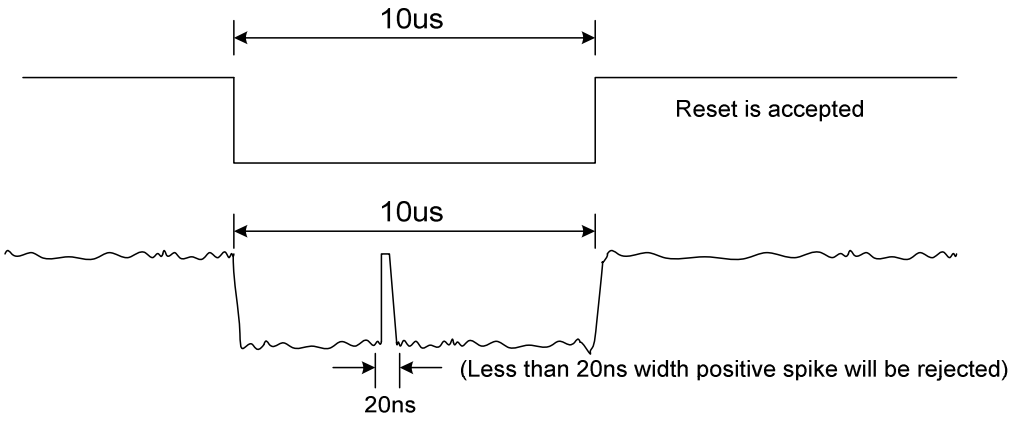
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RST

2. Spike due to an electrostatic discharge on RST line does not cause irregular system reset according to the table below:

RST Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 9µs	Reset
Between 5µs and 9µs	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

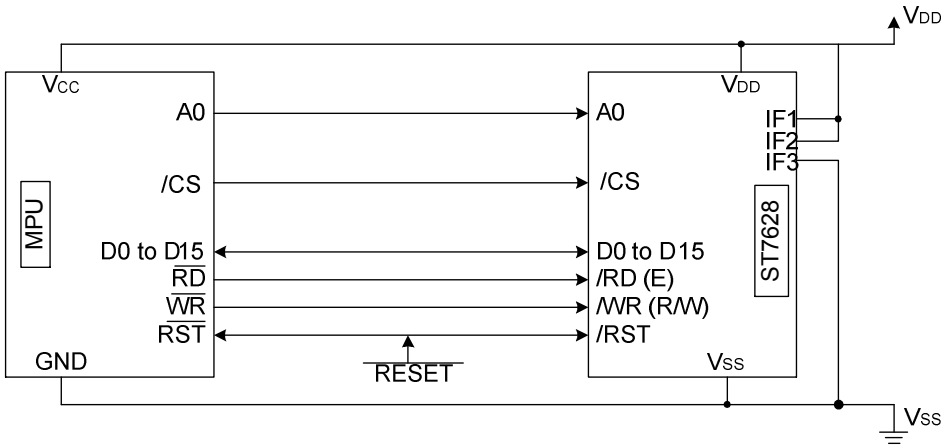
7. It is necessary to wait 5msec after releasing RST before sending commands. Also Sleep Out command cannot be sent for 120msec.

13. THE MPU INTERFACE (REFERENCE EXAMPLES)

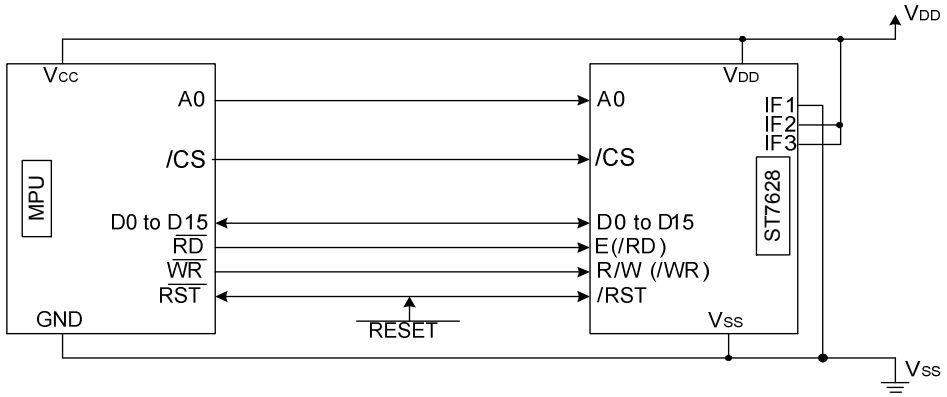
The ST7628 Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7628 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7628 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

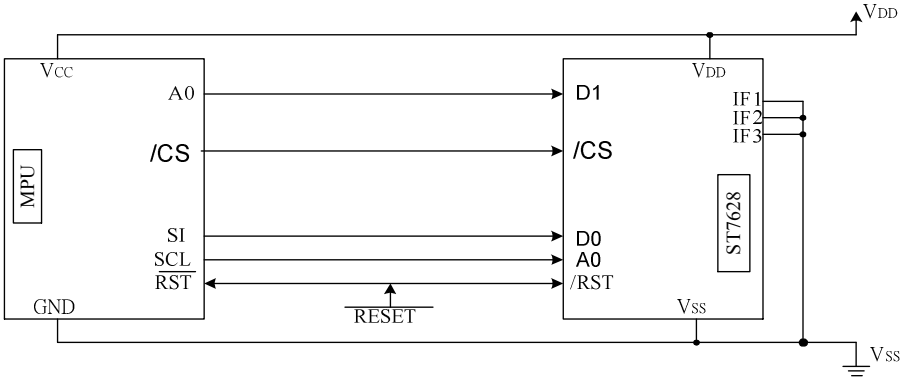
(1) 8080 Series MPUs



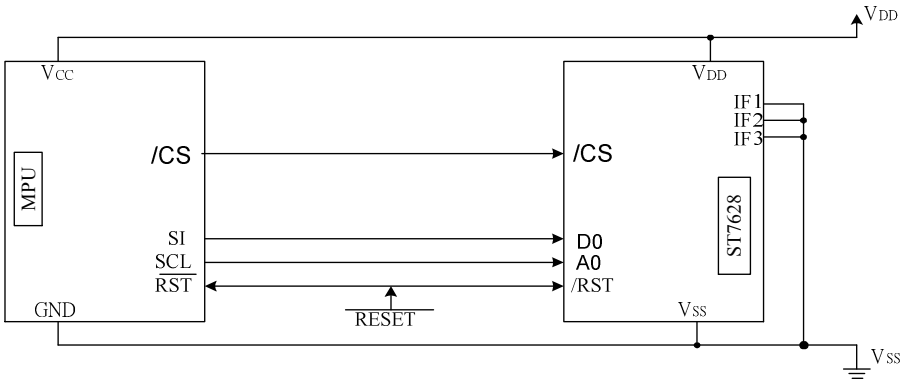
(2) 6800 Series MPUs



(3) Using the Serial Interface (4-line interface)

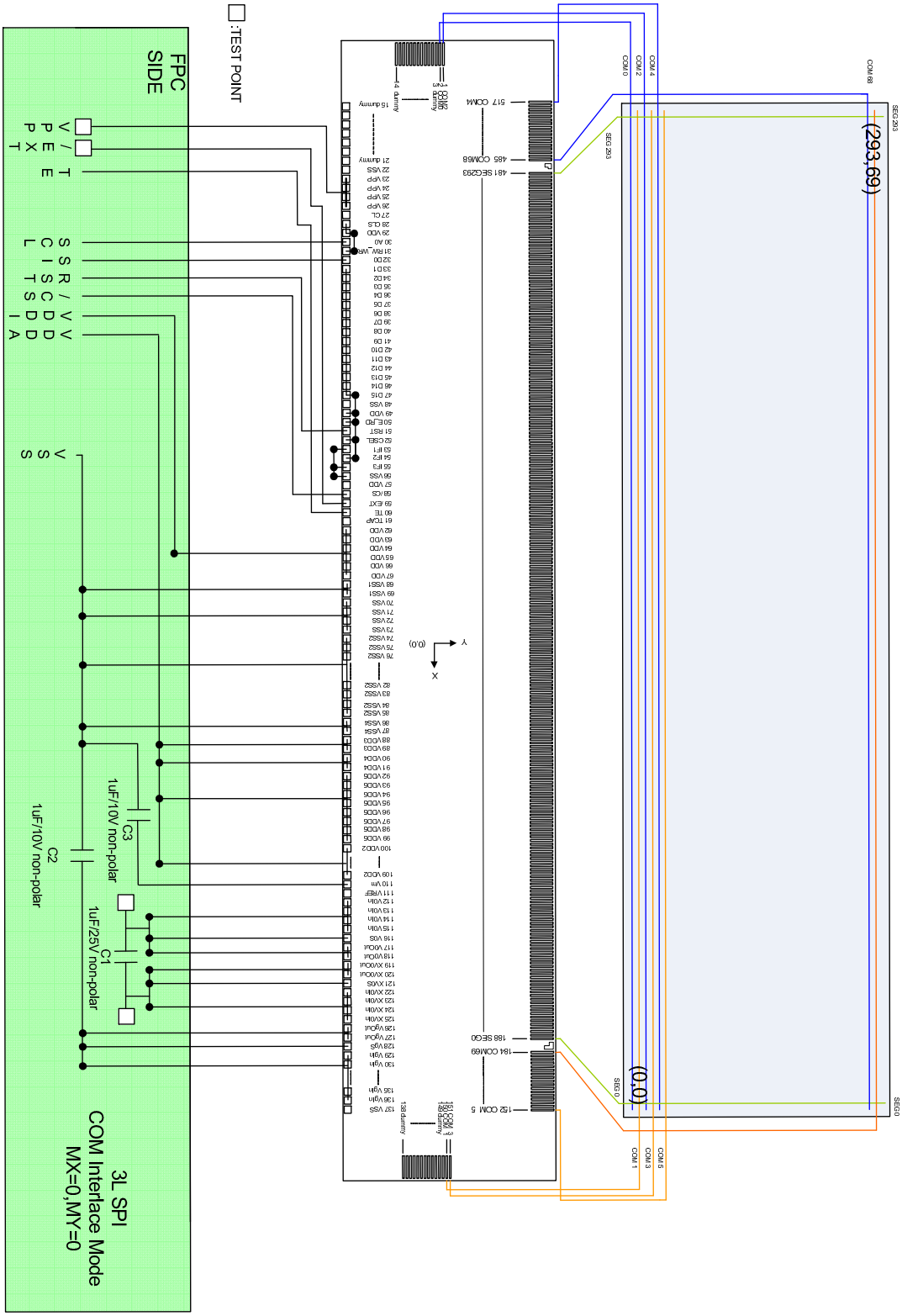


(4) Using the Serial Interface (3-line interface)



A - Application Note

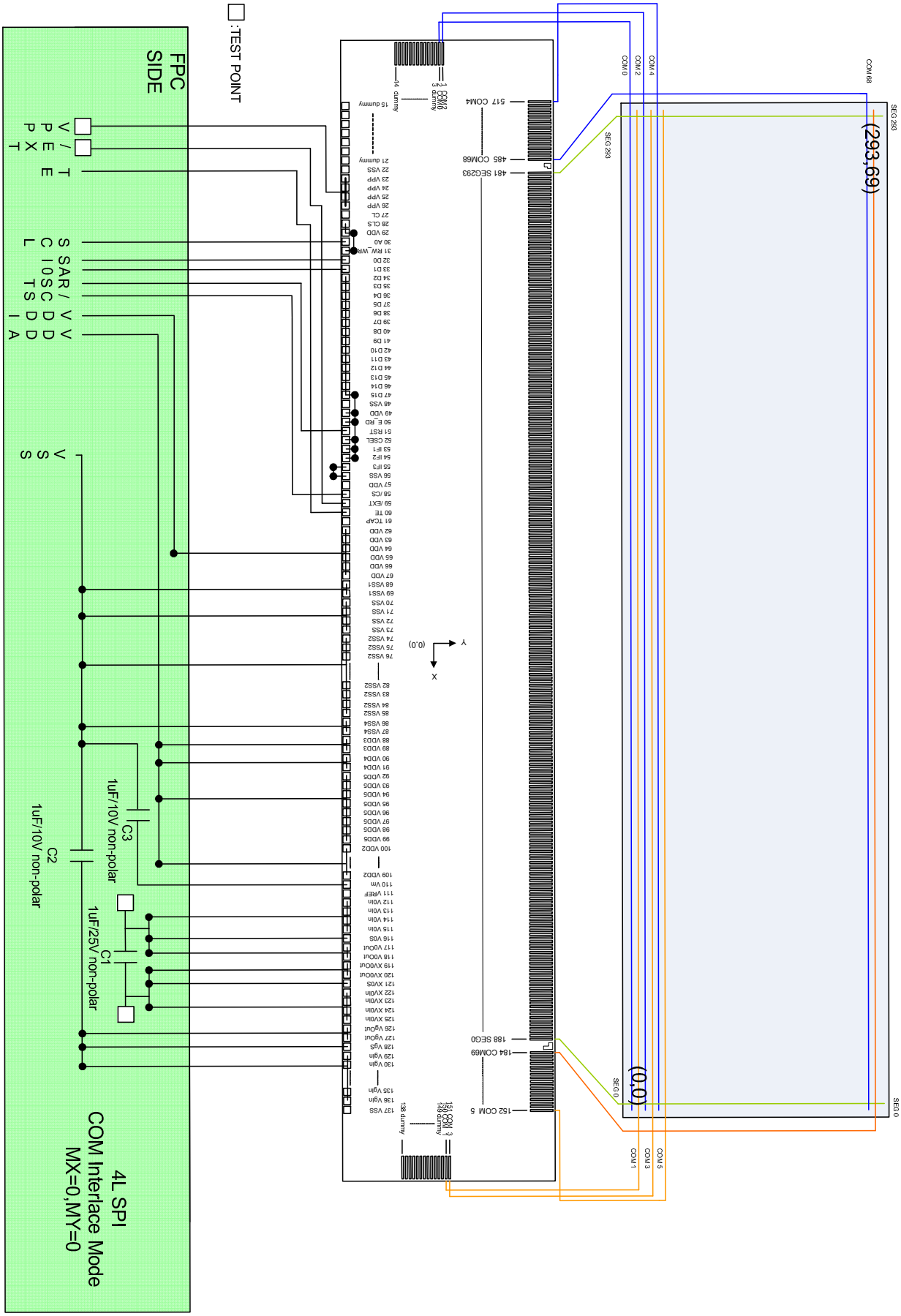
◆ A1 – Reference Circuit (3L SPI / COM interlace Mode)



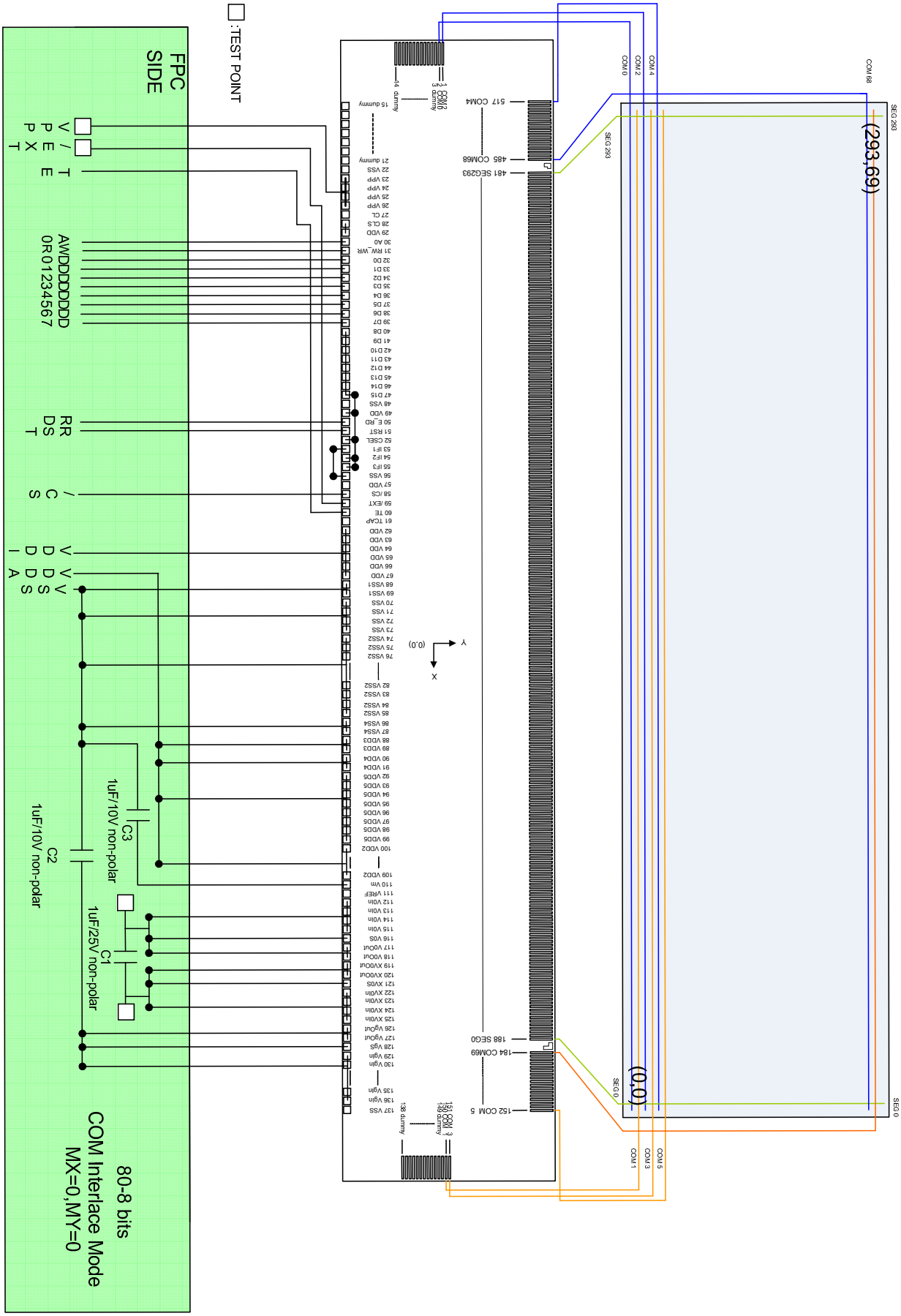
Note1: If VDDI and VDDA need capacitosr toVSS for ripple avoidance, the suggestion type should be 1uf/5V non-polar.

Note2: All of the microprocessor interface pin should not be floating on any operations.

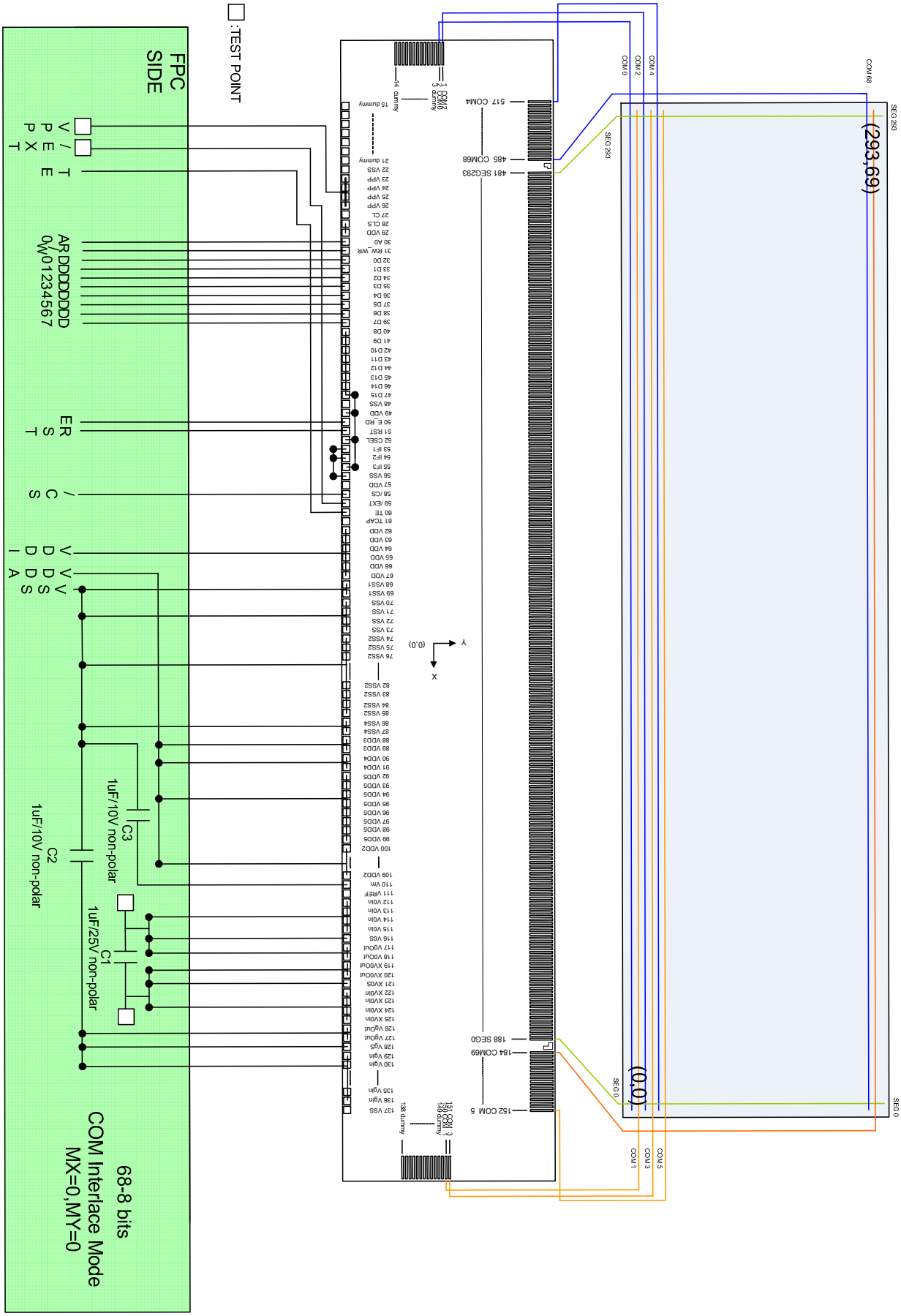
◆ A1 – Reference Circuit (4L SPI / COM interlace Mode)



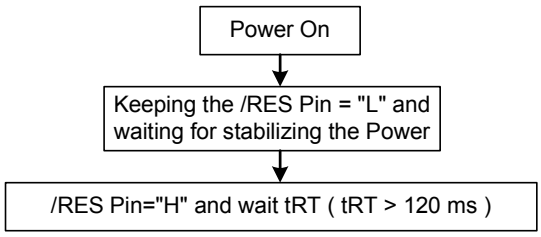
◆ A1 – Reference Circuit (80-8bits / COM interlace Mode)

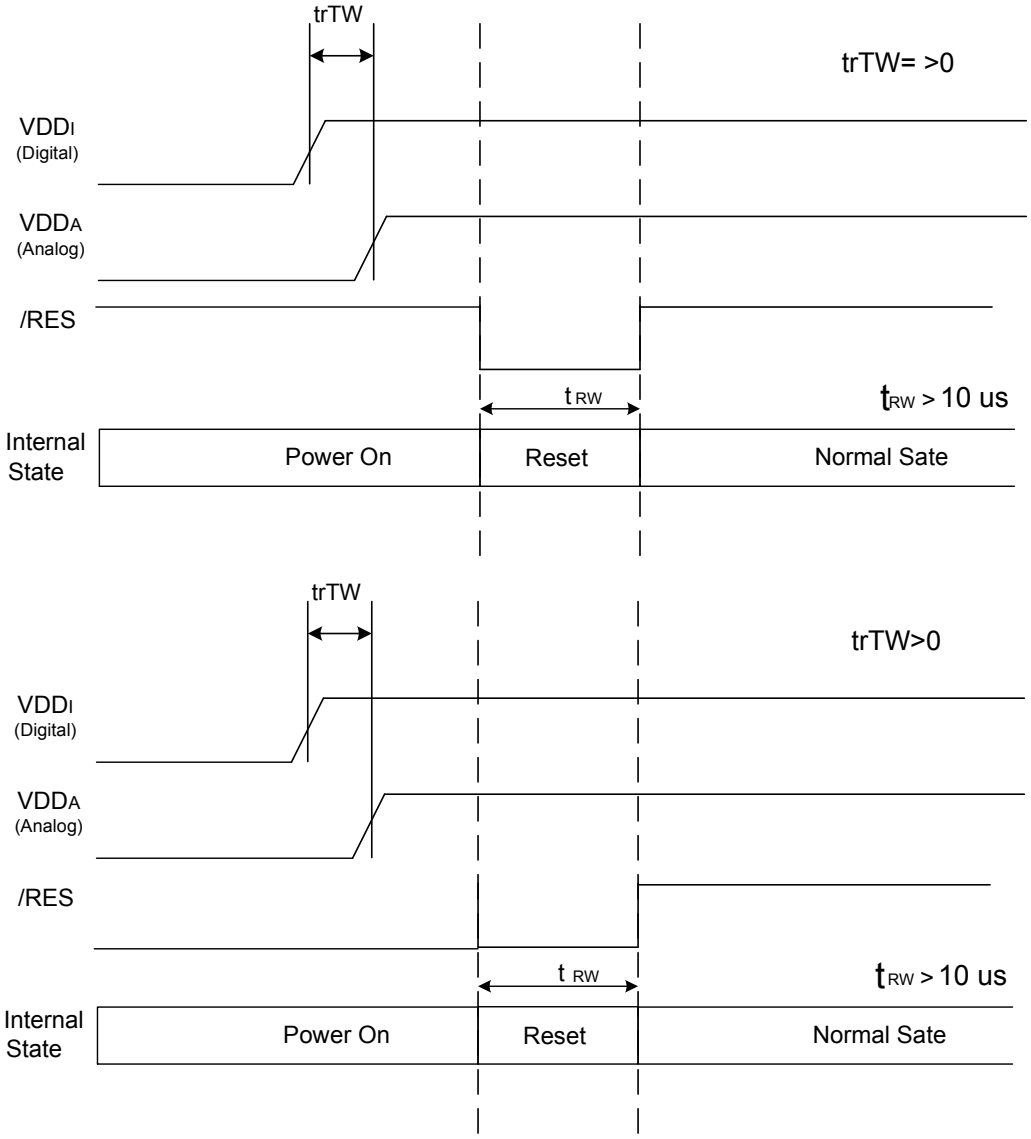


◆ A1 – Reference Circuit (68-8bits / COM interlace Mode)

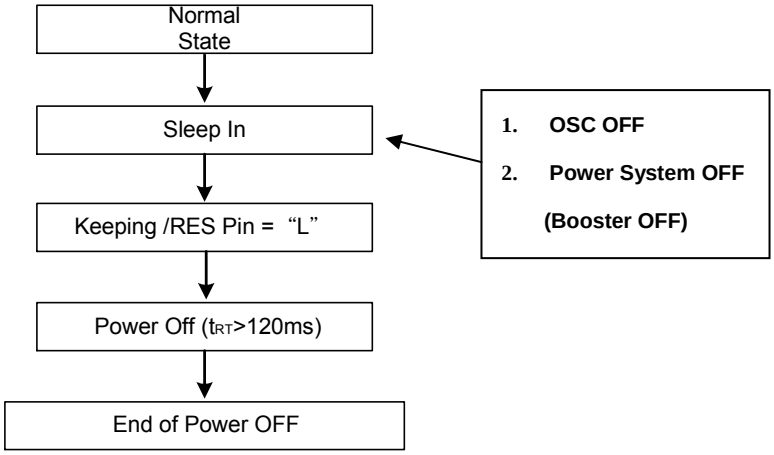


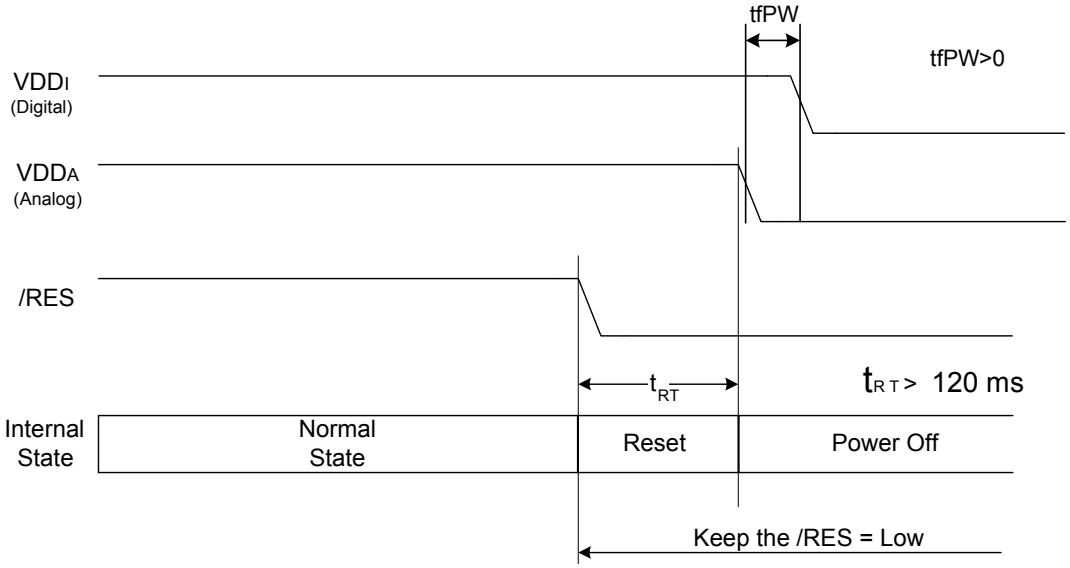
◆ A2 – Power On


Power On
Keeping the /RES Pin = "L" and waiting for stabilizing the Power
/RES Pin="H" and wait tRT (tRT > 120 ms)

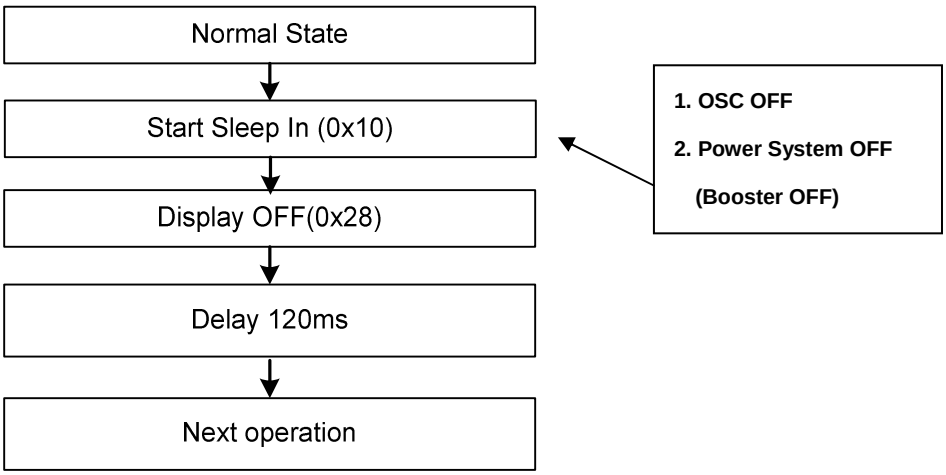

trTW
trTW= >0
VDDI
(Digital)
VDDA
(Analog)
/RES
t RW
tRW > 10 us
Internal State
Power On
Reset
Normal Sate
trTW
trTW>0
VDDI
(Digital)
VDDA
(Analog)
/RES
t RW
tRW > 10 us
Internal State
Power On
Reset
Normal Sate

◆ A3 – Power off

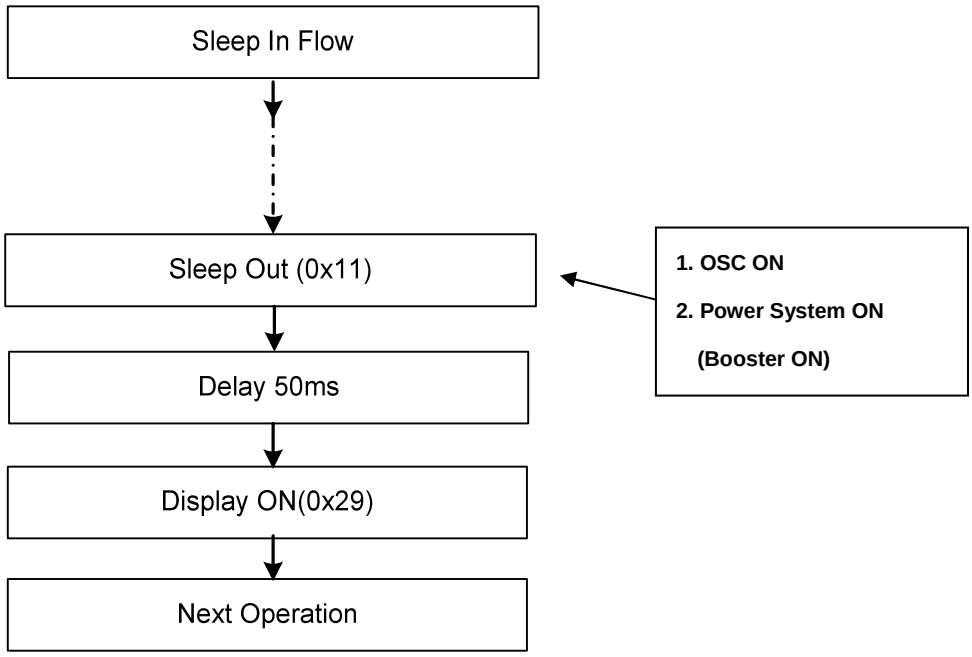

Normal State
Sleep In
Keeping /RES Pin = "L"
Power Off (tRT>120ms)
End of Power OFF
1. OSC OFF
2. Power System OFF
(Booster OFF)


tfPW
tfPW>0
VDDI
(Digital)
VDDA
(Analog)
/RES
tRT
tRT > 120 ms
Internal State
Normal State
Reset
Power Off
Keep the /RES = Low

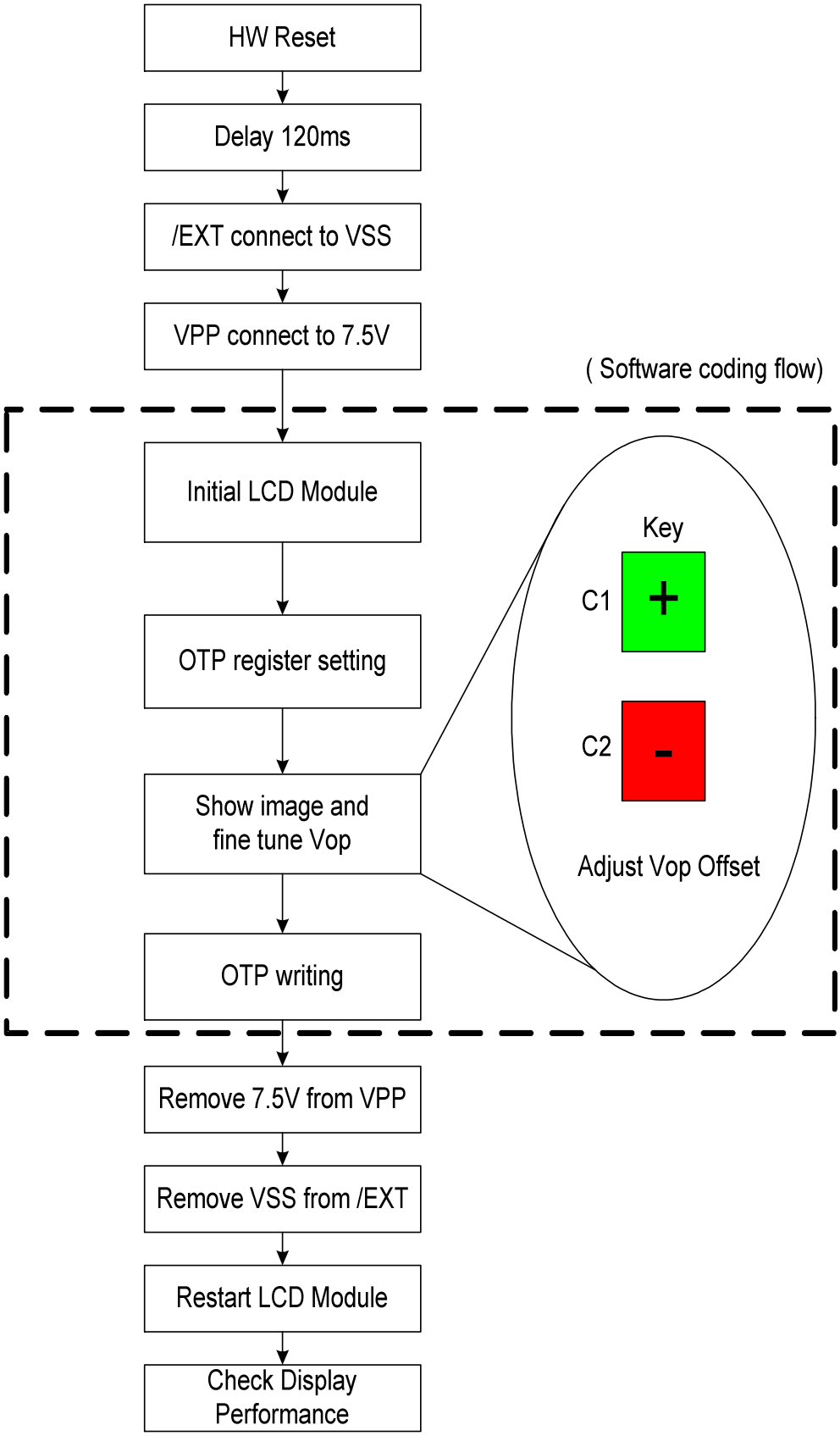
◆ A4 – Sleep In Flow



◆ A5 – Sleep Out Flow



◆ A6 – OTP Burning Flow:



◆ A7 – Software coding flow

void Initial_LCD_Module(void)			
{			
//----------disable autoread + Manual read once ----------			
	Write(COMMAND,0xd7);		// Auto Load Set
	Write(DATA,0xdf);		// Auto Load Disable
	Write(COMMAND,0xE0);		// EE Read/write mode
	Write(DATA,0x00);		// Set read mode
	delayms(10);		// Delay 10ms
	Write(COMMAND,0xE3);		// Read active
	delayms(20);		// Delay 20ms
	Write(COMMAND,0xE1);		// Cancel control
//---------- Sleep OUT ----------			
	Write(COMMAND, 0x11);		// Sleep Out
	delayms(50);		//Delay 50ms
//----------Vop setting----------			
	Write(COMMAND,0xC0);		//Set Vop by initial Module
	Write(DATA, 0xD2);		//Vop = 12V
	Write(DATA, 0x00);		//Base Vop voltage
//----------Set Register----------			
	Write(COMMAND,0xC3);		// Bias select
	Write(DATA,0x02);		
	Write(COMMAND,0xC4);		// Setting Booster times
	Write(DATA,0x07);		
	Write(COMMAND,0xC5);		// Booster efficiency
	Write(DATA,0x21);		// BE = 0x01 (Level 2)
	Write(COMMAND,0xCB);		// Vg with booster x2 control
	Write(DATA,0x01);		// Vg from Vdd2
	Write(COMMAND,0xCC);		// ID1 = 00
	Write(DATA,0x00);		//
	Write(COMMAND,0xCE);		// ID3 = 00
	Write(DATA,0x00);		
	Write(COMMAND,0xD0);		// Analog circuit setting
	Write(DATA,0x1D);		//

	Write(COMMAND,0x3A);		// Color mode = 65k
	Write(DATA,0x05);		//
	Write(COMMAND,0x36);		// Memory Access Control //
	Write(DATA,0x00);		
	Write(COMMAND,0xF7);		// command for temp sensitivity.
	Write(DATA,0x06);		//
	Write(COMMAND, 0xB5);		// N-Line
	Write(DATA, 0x01);		// RST, 2-line inversion
	1. Set Gamma table for Module, please refer spec setting. **2. Set Temp compensation for Module, please refer spec setting.**		
	Write(COMMAND,0x2A);		// COL//
	Write(DATA,0x00);		// Start address = 0
	Write(DATA,0x61);		// End address = 97
	Write(COMMAND,0x2B);		// ROW //
	Write(DATA,0x00);		// Start address = 0
	Write(DATA,0x45);		// End address = 69
}			
void Set_OTP_Register(void)			
{			
//----------Set OTP register----------			

	Write(COMMAND, 0xCD);		//ID2
	Write(DATA, 0x80);		
	Write(COMMAND, 0xB5);		// N-Line
	Write(DATA, 0x01);		// RST, 2-line inversion
	Write(COMMAND,0xD0);		// Analog circuit setting
	Write(DATA,0x1D);		//
	Write(COMMAND,0xD7);		//Auto read Set
	Write(DATA,0x9F);		//OTPB Disable
	Write(COMMAND,0xB4);		//PTL Mode Select
	Write(DATA,0x18);		//PTLMOD → Normal Mode
}			
void Fine_Tune_Vop(void)			
{			
//---------- Show Map ----------			
	Show_Image();		//Display a image
//---------- Display ON ----------			
	Write(COMMAND, 0x29);		// Display On
//----------Fine tune Vop offset----------			
	Write(COMMAND, 0xC1); or Write(COMMAND, 0xC2);		//Fine tuning Vop here by command 0xc1(VopOffsetInc),0xc2(VopOffsetDec).
	Note		
}			
void OTP_Writing(void)			
{			
//----------Display OFF----------			
	Write(COMMAND, 0x28);		// Display Off
	Delayms(50);		// delay 50ms
//----------OTP writing----------			
	Write(COMMAND, 0x00F0);		// Keep Frame Rate with 77Hz
	Write(DATA, 0x0012);		
	Write(DATA, 0x0012);		

	Write(DATA, 0x0012);		
	Write(DATA, 0x0012);		
	Write(COMMAND, 0x00E4);		//OTP selection
	Write(DATA, 0x0058);		// Select OTP
	Write(COMMAND, 0x00E5);		// Set OTP writing setup
	Write(DATA, 0x0009);		
	Write(COMMAND, 0x00E0);		// Read/write mode setting
	Write(DATA, 0x0020);		// Set Write mode
	Delayms(100);		// Delay 100ms
	Write(COMMAND, 0x00E2);		// Write active
	Delayms(100);		// Delay 100ms
	Write(COMMAND, 0x00E1);		// Cancel control
	Write(COMMAND, 0x10);		// Sleep In
}			

Note:

In this section"+" & "-" key button, please execute Write(COMMAND,0xC1) to increase one step at Vop and execute Write(COMMAND,0xC2) to decrease one step at Vop, if necessary.

Modification History

Version	Date	Description
0.X		Preliminary version.
1.0	2007/2/7	First issue.
1.1	2007/2/27	Modify command table list and descriptions.
1.2	2007/3/1	Add command 0x2E for memory reading.
1.3	2007/6/12	1. Redefine the programming mechanism of non-volatility memory. 2. Modify 6800 and 3-pin Serial timing