Sitronix

ST7522

17 x 96 Dot Matrix LCD Controller/Driver

OVERVIEW

The ST7522 family of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.
The drivers are available in two configurations
The ST7522 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages. These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.
The ST7522 which is able to drive 1 line of 6 Chinese characters or 2 lines of 12 Chinese characters each line
with two ST7522.

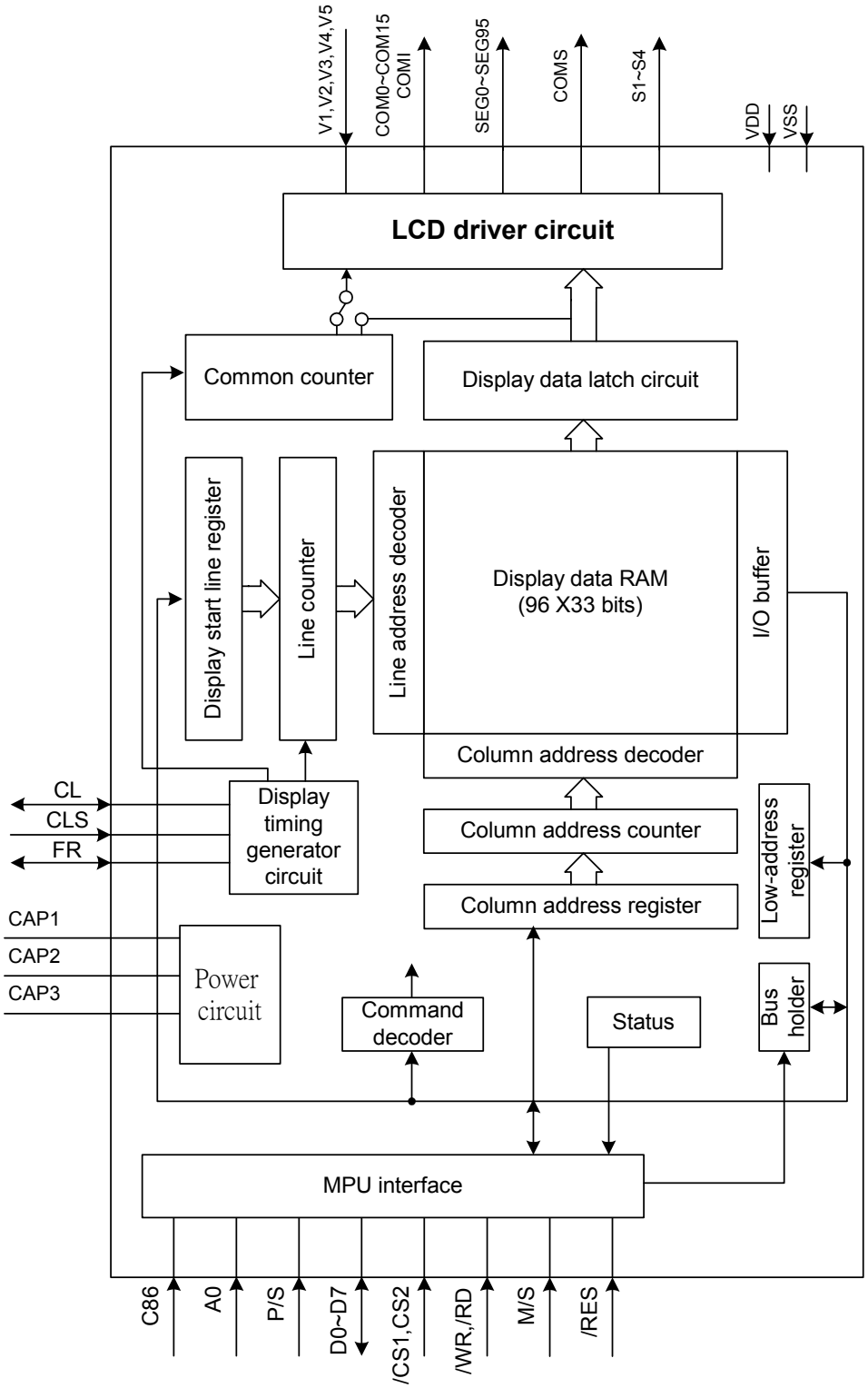
FEATURES

- Fast 8-bit MPU interface compatible with 80- and 68- family microcomputers and serial interface
- Clock synchronous serial interface
- Many command set
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set , column address set , status read , display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, static indicator, adjustable OSC frequency, booster input voltage select, follower input voltage and amplified ratio selectable
- 4 static indicator and 96 icon available
- Total 118 (segment + common + static) drive sets
- Wide range of supply voltages
  V_{DD} – V_{SS}：2.7 to 5.5 V
  V_{DD} – V_5：3.5 to 7.0 V
  V_{DD} – V_{CAP3} ：3.5 to 7.0 V
- Low-power CMOS
- 64 level digital contrast control

Product name	Clock frequency		Number of COM	Number of SEG	Bias	Duty
	On-Chip	External				
ST7522D	1.2KHz,2.4KHz (When VDD=3.0V)	2.8KHz	17	96	1/5,1/6	1/17,1/33

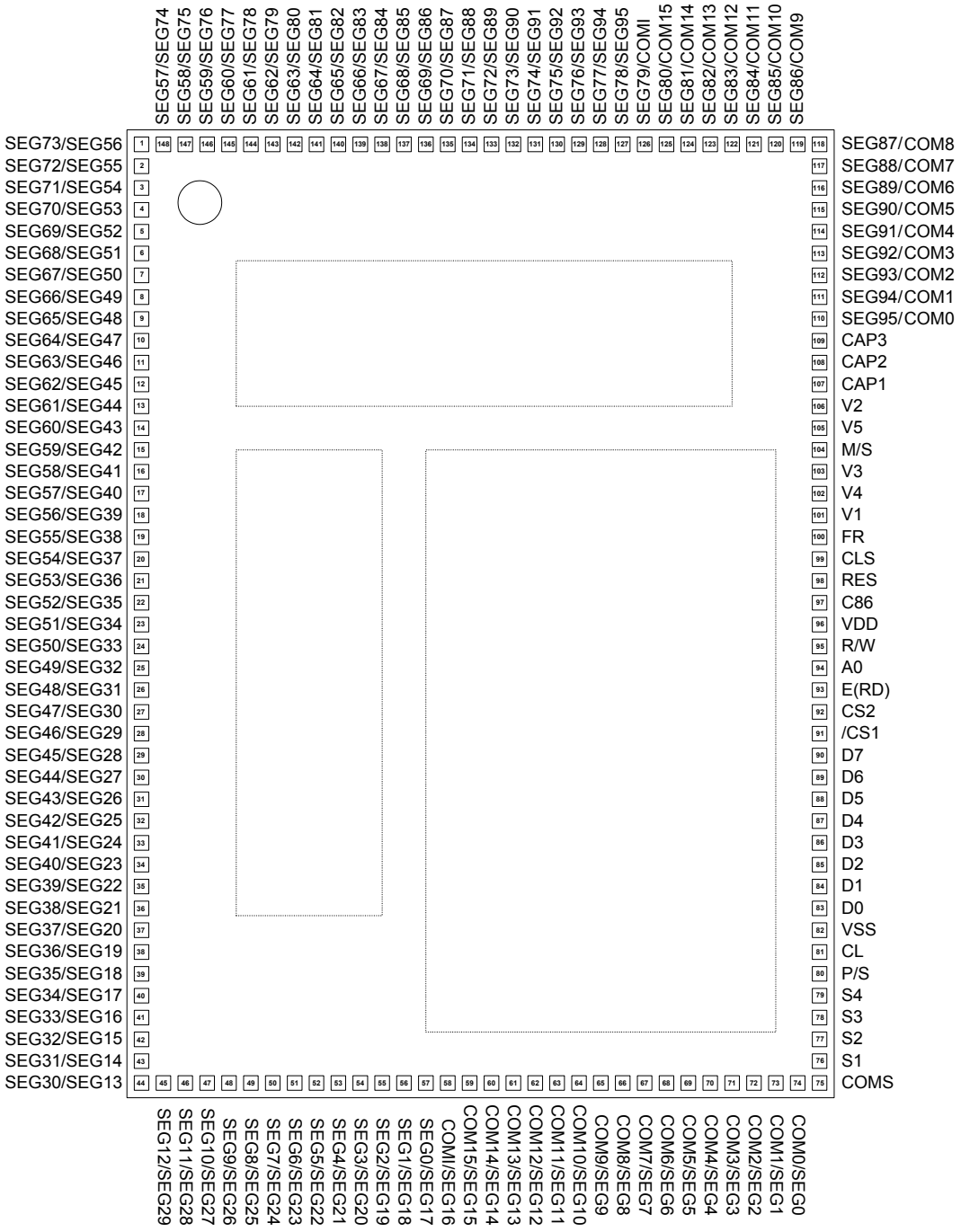
ST7522 Serial Specification Revision History		
Version	**Date**	**Description**
1.0	2002/01/30	New specification version
1.0a	2002/02/20	Modify cover page's product name
1.0b	2002/03/18	Adding FR frequency for "OSC frequency set" command
1.0c	2002/07/10	1. Adding "Slave chip notice" in application circuit 2. Adding "Software example" 3. Adding "Follower-contrast curve" 4. Adding "Master mode application circuit" 5. Adding "I/O pad configuration"

BLOCK DIAGRAM



PAD ARRANGEMENT

Chip specifications of AL pad package
Chip size : 3720 µm x 5040 µm
Minimum pad pitch : 110µm
Pad size : 90µm X 90µm



* Substrate connect to VDD.

PAD CENTER COORDINATES

(chip size : 3720 µm x 5040 µm)

Pad No.	Pin Name		X	Y
	Master	Slave		
1	SEG56	SEG73	-1745	2405
2	SEG55	SEG72	-1745	2275
3	SEG54	SEG71	-1745	2155
4	SEG53	SEG70	-1745	2035
5	SEG52	SEG69	-1745	1925
6	SEG51	SEG68	-1745	1815
7	SEG50	SEG67	-1745	1705
8	SEG49	SEG66	-1745	1595
9	SEG48	SEG65	-1745	1485
10	SEG47	SEG64	-1745	1375
11	SEG46	SEG63	-1745	1265
12	SEG45	SEG62	-1745	1155
13	SEG44	SEG61	-1745	1045
14	SEG43	SEG60	-1745	935
15	SEG42	SEG59	-1745	825
16	SEG41	SEG58	-1745	715
17	SEG40	SEG57	-1745	605
18	SEG39	SEG56	-1745	495
19	SEG38	SEG55	-1745	385
20	SEG37	SEG54	-1745	275
21	SEG36	SEG53	-1745	165
22	SEG35	SEG52	-1745	55
23	SEG34	SEG51	-1745	-55
24	SEG33	SEG50	-1745	-165
25	SEG32	SEG49	-1745	-275
26	SEG31	SEG48	-1745	-385
27	SEG30	SEG47	-1745	-495
28	SEG29	SEG46	-1745	-605
29	SEG28	SEG45	-1745	-715
30	SEG27	SEG44	-1745	-825
31	SEG26	SEG43	-1745	-935
32	SEG25	SEG42	-1745	-1045
33	SEG24	SEG41	-1745	-1155
34	SEG23	SEG40	-1745	-1265
35	SEG22	SEG39	-1745	-1375
36	SEG21	SEG38	-1745	-1485
37	SEG20	SEG37	-1745	-1595
38	SEG19	SEG36	-1745	-1705
39	SEG18	SEG35	-1745	-1815
40	SEG17	SEG34	-1745	-1925
41	SEG16	SEG33	-1745	-2035
42	SEG15	SEG32	-1745	-2155
43	SEG14	SEG31	-1745	-2275
44	SEG13	SEG30	-1745	-2405
45	SEG12	SEG29	-1615	-2405
46	SEG11	SEG28	-1495	-2405
47	SEG10	SEG27	-1375	-2405
48	SEG9	SEG26	-1265	-2405
49	SEG8	SEG25	-1155	-2405

Pad No.	Pin Name		X	Y
	Master	Slave		
50	SEG7	SEG24	-1045	-2405
51	SEG6	SEG23	-935	-2405
52	SEG5	SEG22	-825	-2405
53	SEG4	SEG21	-715	-2405
54	SEG3	SEG20	-605	-2405
55	SEG2	SEG19	-495	-2405
56	SEG1	SEG18	-385	-2405
57	SEG0	SEG17	-275	-2405
58	COMI	SEG16	-165	-2405
59	COM15	SEG15	-55	-2405
60	COM14	SEG14	55	-2405
61	COM13	SEG13	165	-2405
62	COM12	SEG12	275	-2405
63	COM11	SEG11	385	-2405
64	COM10	SEG10	495	-2405
65	COM9	SEG9	605	-2405
66	COM8	SEG8	715	-2405
67	COM7	SEG7	825	-2405
68	COM6	SEG6	935	-2405
69	COM5	SEG5	1045	-2405
70	COM4	SEG4	1155	-2405
71	COM3	SEG3	1265	-2405
72	COM2	SEG2	1375	-2405
73	COM1	SEG1	1495	-2405
74	COM0	SEG0	1615	-2405
75	COMS		1745	-2405
76	S1		1745	-2275
77	S2		1745	-2155
78	S3		1745	-2035
79	S4		1745	-1925
80	P/S		1745	-1815
81	CL		1745	-1705
82	VSS		1745	-1595
83	D0		1745	-1485
84	D1		1745	-1375
85	D2		1745	-1265
86	D3		1745	-1155
87	D4		1745	-1045
88	D5		1745	-935
89	D6		1745	-825
90	D7		1745	-715
91	/CS1		1745	-605
92	CS2		1745	-495
93	E(RD)		1745	-385
94	A0		1745	-275
95	R/W		1745	-165
96	VDD		1745	-55
97	C86		1745	55
98	RES		1745	165

Pad No.	Pin Name		X	Y
	Master	Slave		
99	CLS		1745	275
100	FR		1745	385
101	V1		1745	495
102	V4		1745	605
103	V3		1745	715
104	M/S		1745	825
105	V5		1745	935
106	V2		1745	1045
107	CAP1		1745	1155
108	CAP2		1745	1265
109	CAP3		1745	1375
110	SEG95	COM0	1745	1485
111	SEG94	COM1	1745	1595
112	SEG93	COM2	1745	1705
113	SEG92	COM3	1745	1815
114	SEG91	COM4	1745	1925
115	SEG90	COM5	1745	2035
116	SEG89	COM6	1745	2155
117	SEG88	COM7	1745	2275
118	SEG87	COM8	1745	2405
119	SEG86	COM9	1615	2405
120	SEG85	COM10	1495	2405
121	SEG84	COM11	1375	2405
122	SEG83	COM12	1265	2405
123	SEG82	COM13	1155	2405
124	SEG81	COM14	1045	2405
125	SEG80	COM15	935	2405
126	SEG79	COMI	825	2405
127	SEG78	SEG95	715	2405
128	SEG77	SEG94	605	2405
129	SEG76	SEG93	495	2405
130	SEG75	SEG92	385	2405
131	SEG74	SEG91	275	2405
132	SEG73	SEG90	165	2405
133	SEG72	SEG89	55	2405
134	SEG71	SEG88	-55	2405
135	SEG70	SEG87	-165	2405
136	SEG69	SEG86	-275	2405
137	SEG68	SEG85	-385	2405
138	SEG67	SEG84	-495	2405
139	SEG66	SEG83	-605	2405
140	SEG65	SEG82	-715	2405
141	SEG64	SEG81	-825	2405
142	SEG63	SEG80	-935	2405
143	SEG62	SEG79	-1045	2405
144	SEG61	SEG78	-1155	2405
145	SEG60	SEG77	-1265	2405
146	SEG59	SEG76	-1375	2405
147	SEG58	SEG75	-1495	2405
148	SEG57	SEG74	-1615	2405

PIN DESCRIPTION

(1) Power Pins

Name	I/O	Description
V_{DD}	-	Connected to the +5V 0r +3V dc power. Common to the Vcc MPU power pin.
V_{SS}	-	0V dc pin connected to the system ground.
CAP1~3	-	Capacitor connector pin for voltage booster
V1~V5	-	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: VDD≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧V5

(2) System Bus Connection Pins

Name	I/O	Description
D7 to D0 SI (D7) SCL (D6)	I/O	The 8-bit bidirectional data buses to be connected to the 8- or 16- bit standard MCU Data busses. When the serial interface is selected then D7 act as serial data input terminal and D6 act as serial clock input terminal. D5 ~ D0 become high impedance.
A0	I	Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. A0=0 : DO to D7 are display control data. A0=1 : DO to D7 are display data.
CLS	I	CLS=1 : internal oscillator enable CLS=0 : external clock operation mode
$\overline{RES}$	I	Input low active. System reset.
C86	I	High level: 68-series MPU interface Low level : 80-series MPU interface
P/S	I	This pin select the parallel / serial data input method. P/S = 1 : parallel, P/S = 0 : serial.
$\overline{CS1}$, CS2	I	Input. When $\overline{CS1}$ = 0 and CS2 = 1 the chip select become active
E($\overline{RD}$)	I	● If the 68-series MPU is connected: Input. Active high. Used as an enable clock input of the 68-series MPU. ● If the 80-series MPU is connected: Input. Active low. The RD signal of the 80-series MPU is entered in this pin. When this signal is kept low, the ST7522 data bus is in the output status.
R/W ($\overline{WR}$)	I	● If the 68-series MPU is connected: Input. Used as an input pin of read control signals (if R/W is high) or write control signals (if low). ● If the 80-series MPU is connected: Input. Active low. The WR signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of WR signal.

(3) LCD Driver Circuit Signals

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>CL</td><td>I/O</td><td>Input/output.
I/O selection
● M/S = “H” & CLS = “H” ：Output
● M/S = “L” & CLS = “H” ：Input
● M/S = “X” & CLS = “L” ：Input

This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges.</td></tr>
<tr><td>SEGn</td><td>O</td><td>Output.
A single level of VDD, V2, V3 and
V5 is selected by the combination of display RAM contents and FR signal.</td></tr>
<tr><td>COMn</td><td>O</td><td>Output.
The output pin for LCD common (row) driving. A single level of VDD, V1, V4 and V5 is selected by the combination of common counter output and FR signal. The slave LSI has the reverse common output scan sequence than the master LSI.</td></tr>
<tr><td>COMI</td><td>O</td><td>Output. ICON common signals(only use with SEGn)</td></tr>
<tr><td>FR</td><td>I/O</td><td>Input/output.
This is the liquid crystal alternating current signal I/O terminal
I/O selection
● M/S = “H”：Output
● M/S = “L”：Input</td></tr>
<tr><td>COMS</td><td>O</td><td>Output. Static scan line(only use with S1~S4)</td></tr>
<tr><td>S1~S4</td><td>O</td><td>Output. Static data (only use with COMS)</td></tr>
<tr><td>M/S</td><td>I</td><td>Input.
The master or slave LSI operation select pin for the ST7522 .
<u>Connected to VDD (to select the master LSI operation mode) or Vss (to select the slave LSI operation mode).</u>
<u>The slave driver has the reverse common/ segment output scan sequence than the master driver for the convenience of PCB and LCD layout.</u>
<table>
<tr><th>M/S</th><th>Operating Mode</th><th>FR</th><th>CL</th><th>V1~V5</th><th>Power Supply</th><th>Internal oscillator</th></tr>
<tr><td>High</td><td>Master</td><td>Output</td><td>See CLS</td><td>On</td><td>On</td><td>See CLS</td></tr>
<tr><td>Low</td><td>Slave</td><td>Input</td><td>Input</td><td>Off</td><td>Off</td><td>Off</td></tr>
</table>
<table>
<tr><th>M/S</th><th>COM0~COM15</th><th>SEG0~SEG95</th><th>COMI</th><th>COMS</th><th>S1~S4</th></tr>
<tr><td>High</td><td>Pad 74~59</td><td>Pad 57~110</td><td>Pad 58</td><td rowspan="2">Pad 75</td><td rowspan="2">Pad 76~79</td></tr>
<tr><td>Low</td><td>Pad 110~125</td><td>Pad 74~127</td><td>Pad 126</td></tr>
</table>
</td></tr>
</table>

DESCRIPTION OF FUNCTIONS

The MPU Interface

Selecting the Interface Type

With the ST7522 Series chips, data transfers are done through an 8-bit bi-directional data bus (D7 to D0) or through a serial data input (SI). Through selecting the P/S terminal polarity to the “H” or “L” it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5~D0
H: Parallel Input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5~D0
L: Serial Input	$\overline{CS1}$	CS2	A0	High level	High level	High level	SI	SCL	High level

The Parallel Interface

When the parallel interface has been selected (P/S =“H”), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (as shown in Table 2) by selecting the C86 terminal to either “H” or to “L”.

Table 2

C86	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7~D0
H: 6800 Series MPU Bus	$\overline{CS1}$	CS2	A0	E	R/W	D7~D0
L: 8080 MPU Bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7~D0

Moreover, data bus signals are recognized by a combination of A0, **$\overline{RD}$** (E), **$\overline{WR}$**(R/W) signals, as show in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

The Serial Interface

When the serial interface has been selected (P/S = “L”) then when the chip is in active state (CS1 = “L” and CS2 = “H”) the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing. The A0 input is used to determine whether or the serial data input is display data or command data; when A0 = “H”, the data is display data, and when A0 = “L” then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 1 is a serial interface signal chart.

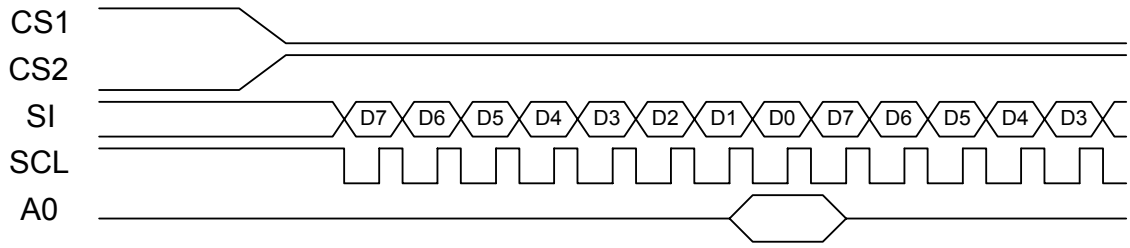


Figure 1

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

The Chip Select

The ST7522 Series chips have two chip select terminals: CS1 and CS2. The MPU interface or the serial interface is enabled only when CS1 = “L” and CS2 = “H”.

When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, RD, and WR inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

The Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (t_{CYC}) requirement alone in accessing the ST7522 Series. Wait time may not be considered.

And, in the ST7522 Series chips, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus. Internal data bus.

For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.

There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.

This relationship is shown in Figure 2.

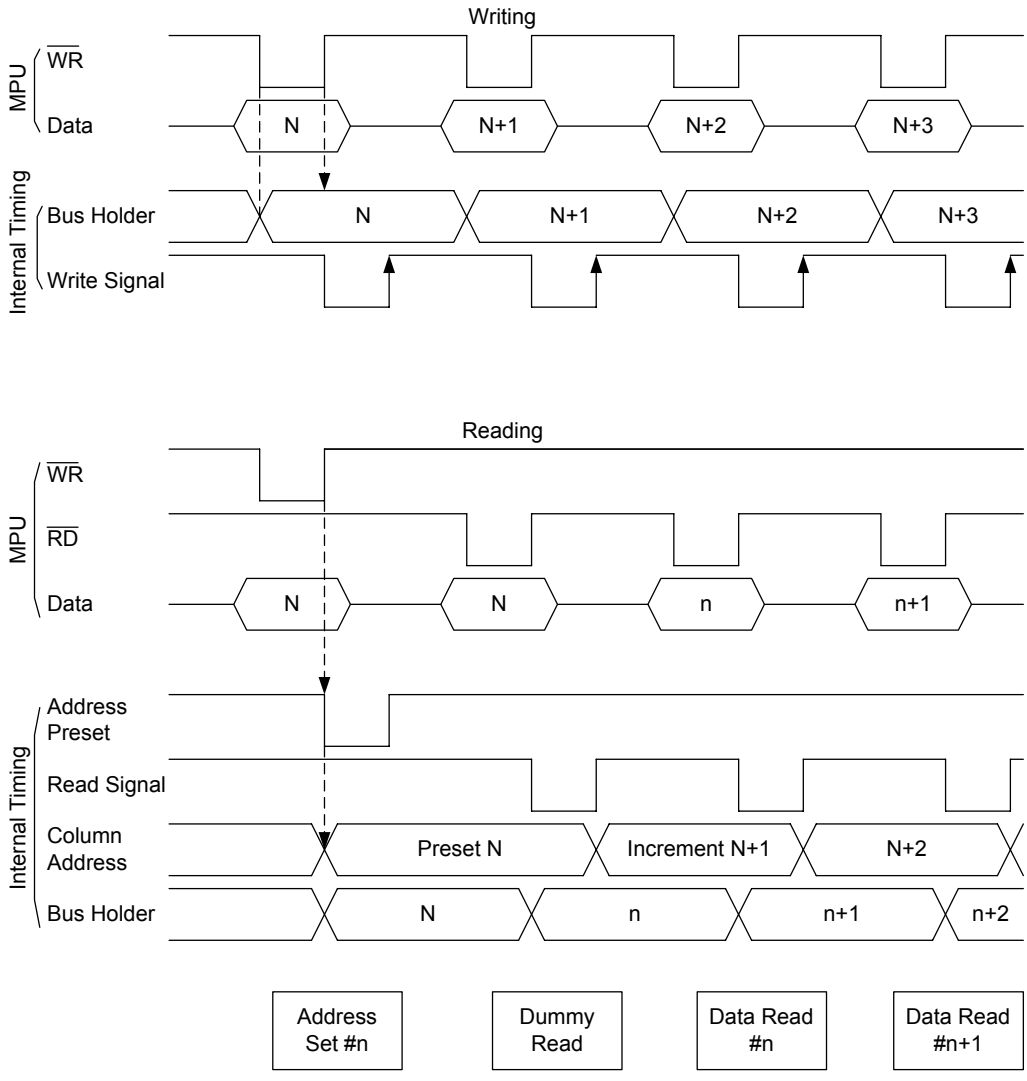


Figure 2

Display Data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 33 (4 page x 8 bit +1) x 96 bit structure. It is possible to access the desired bit by specifying the page address and the column address.
Because, as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display data transfer when multiple ST7522 series chips are used, thus and display structures can be created easily and with a high degree of freedom.
Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

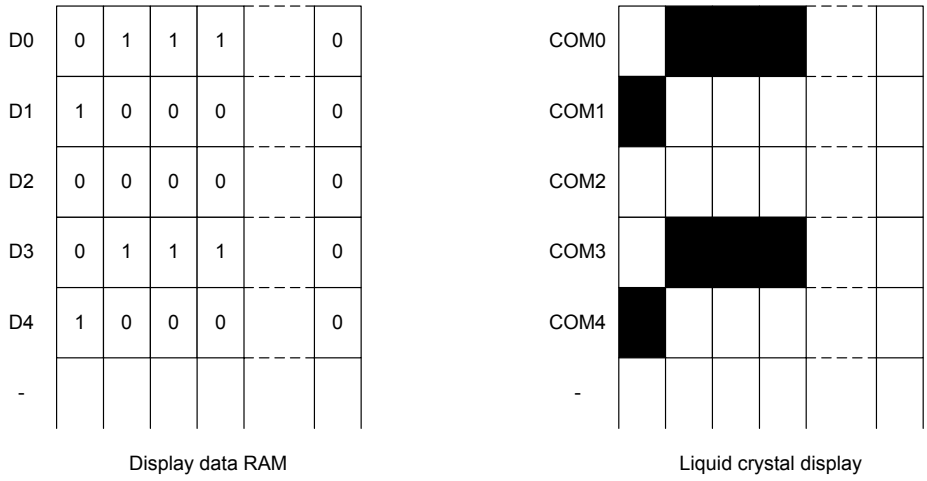


Figure 3

The Page Address Circuit

As shown in Figure 4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is the page for the RAM region used only by the indicators, and only display data D0 is used.

The Column Addresses

As is shown in Table 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the increment of column addresses stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to respecify both the page address and the column address.
Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output / ADC set	SEG0		SEG 95
ADC(D0)=0	0	→ Column Address →	95
ADC(D0)=1	95	← Column Address ←	0

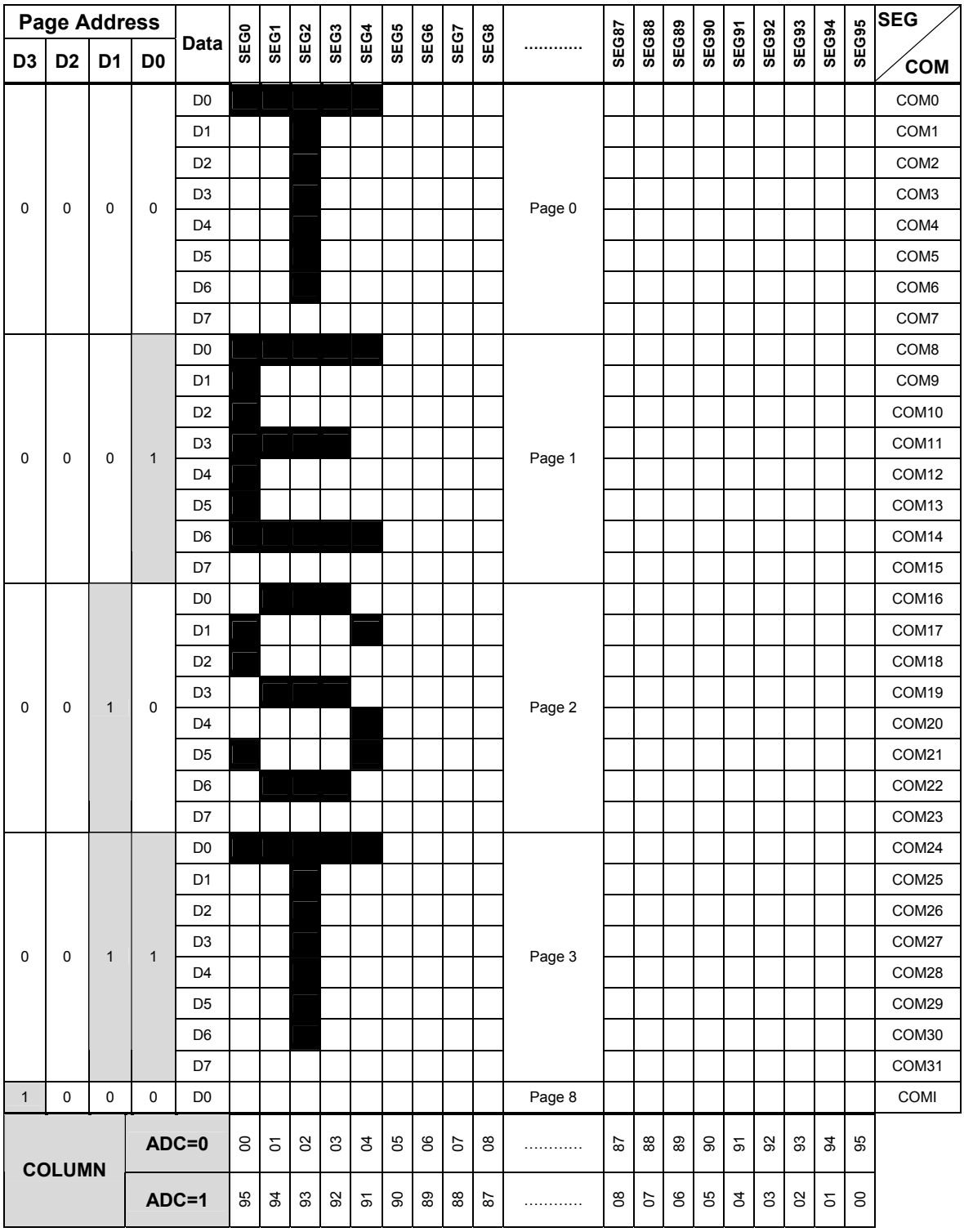

Page Address
D3 D2 D1 D0
Data
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7 SEG8 ..... SEG87 SEG88 SEG89 SEG90 SEG91 SEG92 SEG93 SEG94 SEG95
SEG / COM
0 0 0 0 D0 D1 D2 D3 D4 D5 D6 D7 Page 0 COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7
0 0 0 1 D0 D1 D2 D3 D4 D5 D6 D7 Page 1 COM8 COM9 COM10 COM11 COM12 COM13 COM14 COM15
0 0 1 0 D0 D1 D2 D3 D4 D5 D6 D7 Page 2 COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23
0 0 1 1 D0 D1 D2 D3 D4 D5 D6 D7 Page 3 COM24 COM25 COM26 COM27 COM28 COM29 COM30 COM31
1 0 0 0 D0 Page 8 COMI
COLUMN
ADC=0 00 01 02 03 04 05 06 07 08 ..... 87 88 89 90 91 92 93 94 95
ADC=1 95 94 93 92 91 90 89 88 87 ..... 08 07 06 05 04 03 02 01 00

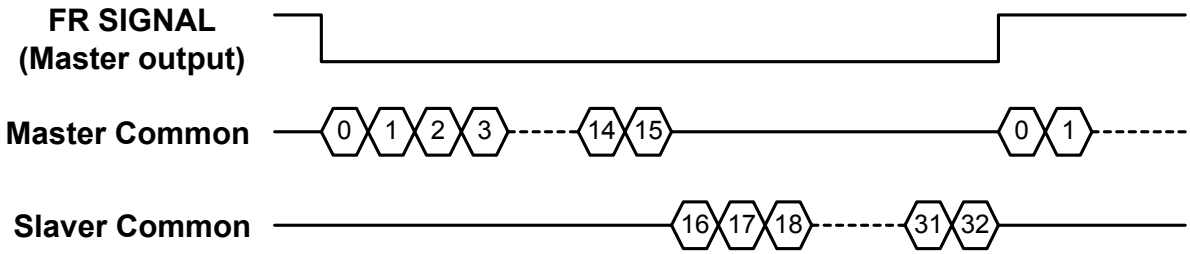
Figure 4

Common Timing Generator Circuit

Generates common timing signals and FR frame signals from the CL basic clock. The 1/17 or l/33 duty (for ST7522)can be selected by the Duty Select command. If the l/33 duty is selected for the ST7522 , the l/33 and l/ 17 duties are provided by two chips consisting of the master and slave chips in the common multi-chip mode.

Display Data Latch Circuit

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the Display ON/OFF.



Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Two-frame alternating current drive waveform

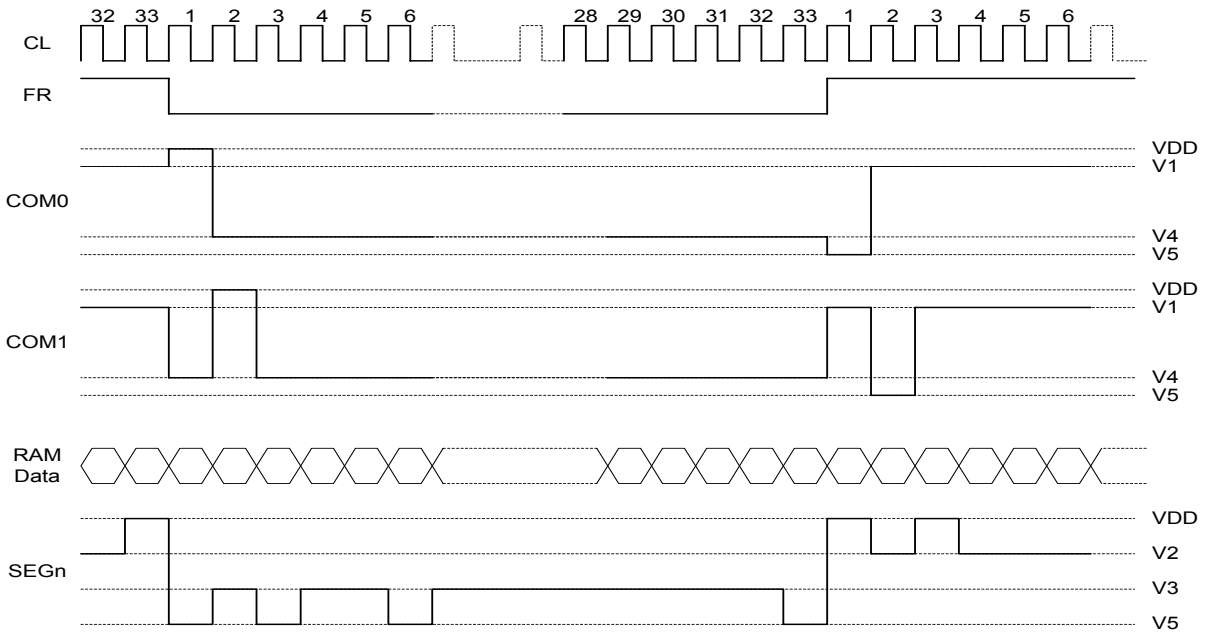


Figure 5

When multiple ST7522 Series chips are used, the slave chip must be supplied the display timing signals (FR, CL) from the master chip.

Table 5 shows the status of the FR and CL signals.

Table 5

Operating Mode		FR	CL
Master (M/S = “H”)	The internal oscillator circuit is enabled (CLS = “H”)	Output	Output
	The internal oscillator circuit is disabled (CLS = “L”)	Output	Input
Slave (M/S = “L”)	The internal oscillator circuit is enabled (CLS = “H”)	Input	Input
	The internal oscillator circuit is disabled (CLS = “L”)	Input	Input

The Liquid Crystal Driver Circuits

These are a 113-channel (ST7522), that generate four voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output. Figure 6 shows examples of the SEG and COM output wave form.

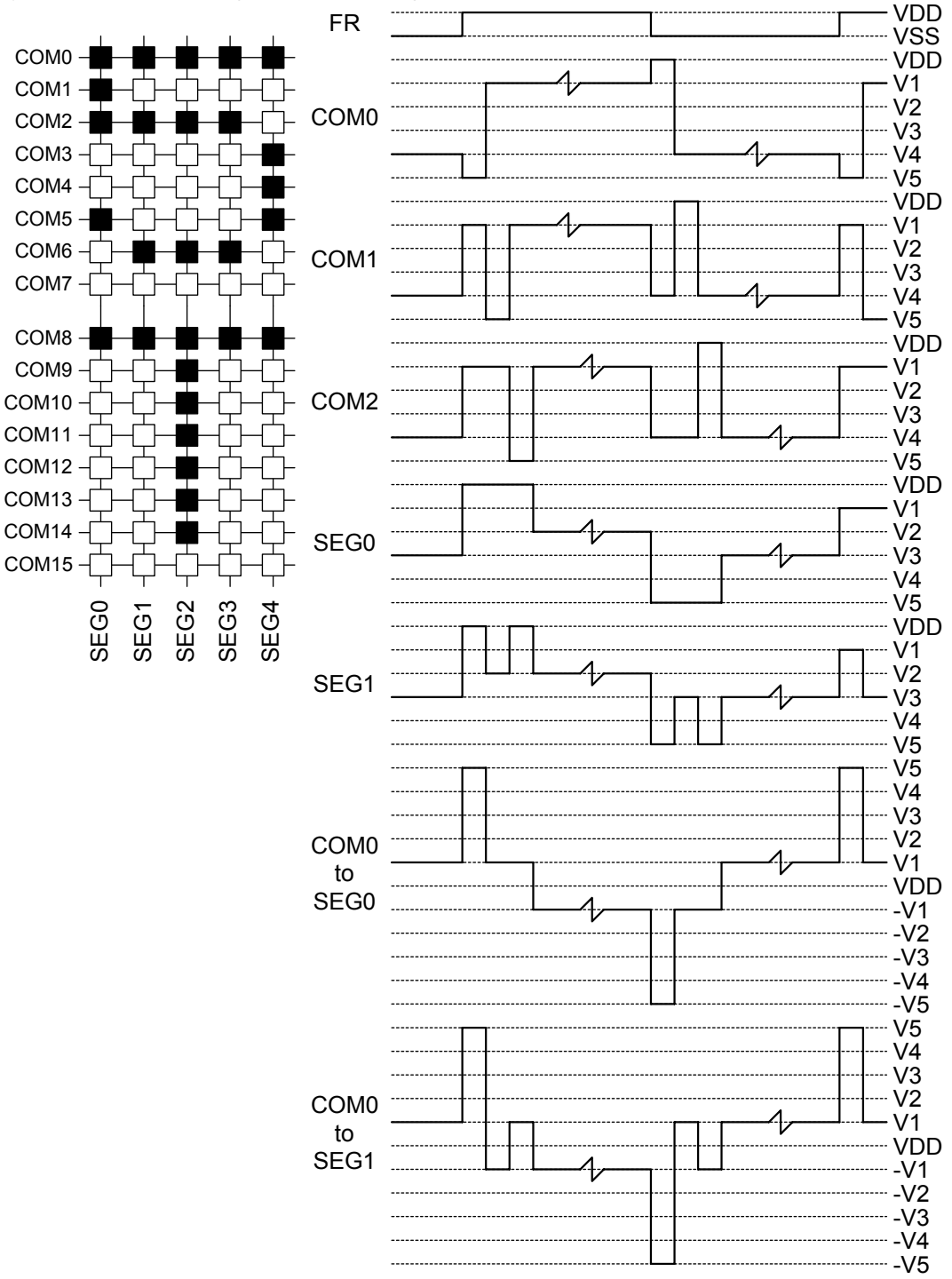


Figure 6

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise Booster circuits, and voltage follower circuits. **They are only enabled in master operation.**

The power supply circuits can turn the Booster circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 6 shows the Power Control Set Command 2-bit data control function,. **(if Booster is off, than the external LCD power supply CAP3 must connect to Vss or external power).**

Table 6

Item	Status "1"	Status "0"
D2 Booster circuit control bit	ON	OFF
D0 Voltage follower circuit control bit	ON	OFF

The Control Details of Each Bit of the Power Control Set Command

The Liquid Crystal Voltage Generator Circuit

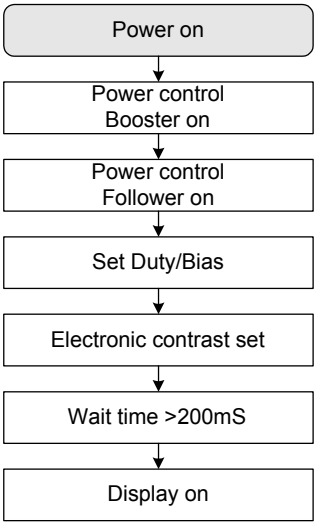
The V_5 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3, and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3 and V_4 to the liquid crystal drive circuit.

1/6 bias or 1/5 bias for ST7522, can be selected.

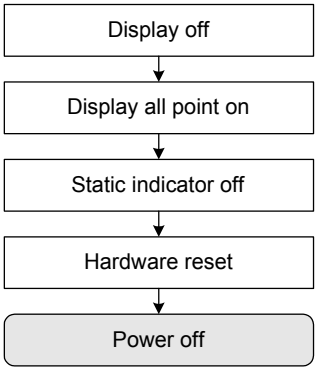
VDD-V5 maximum voltage is 7V, VDD-Vcap3 maximum voltage is 7V too.

If VDD < 3.5V , it can use the Booster circuit 2x, The booster voltage can follow the spec. condition (VDD-V5 ≦ 7V max. voltage.) if VDD >3.5V only use the 1X booster circuit, that can ensure the VDD-V5 voltage ≦ 7V. If use the VDD voltage 5V and 2X booster , it's over the spec. operation condition, although adjust the contrast control can make the V5 voltage small than 7V , but the Vcap3 booster voltage already over spec 7V. IC can not guarantee normally work in this condition.

To turn on built-in power(booster/follower) must waiting 200mS to display on for booster/follower stable. Therefore, power off must follow "power off sequence" too.



Power on sequence



Power off sequence

The Reset Circuit

When the RES input comes to the “L” level, these LSIs return to the default state. Their default states are as follows:

1. Display OFF
2. Static drive is turned OFF.
3. ADC select: Normal (ADC command D0 = 0)
4. Display all point on is select to normal
5. Display normal/reverse is select to normal
6. Power control register: (D2, D0) = (0, 0)
7. Serial interface internal register data clear
8. 1/6 bias is selected
9. 1/17 duty is selected.
10. Read modify write OFF
11. Column address set to Address 0
12. Page address set to Page 0
13. Start line set to first line
14. Electronic contrast register = 35H(max:3FH)
15. OSC frequency set = 08H
16. Follower input voltage set =02H
17. Follower amplified ratio = 06H
18. Booster input voltage set = 00H

When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the $\overline{RES}$ terminal. After the initialization, each input terminal should be controlled normally.

While $\overline{RES}$ is “L,” the oscillator works but the display timing generator stops, and the CL, FR, terminals are fixed to “H.” The terminals D0 to D7 are not affected.

TABLE OF ST7522 INSTRUCTIONS

Instructions	Instruction code											Function
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
Display on/off	0	1	0	1	0	1	0	1	1	1	D	D=1:Display on D=0:Display off
Page address set	0	1	0	1	0	1	1	Page address				Set display page
Column address set upper bits	0	1	0	0	0	0	1	MSB 4 bits				Set MSB 4 bits of column address
Column address set lower bits	0	1	0	0	0	0	0	LSB 4 bits				Set LSB 4 bits of column address
Status read	0	0	1	0	Status			0	0	0	0	Read status
Display data write	1	1	0	Write data								Write display data
Display data read	1	0	1	Read data								Read display data
Start line set	0	1	0	0	1	0	Display start address					Determines the RAM display line for COM 0
ADC select	0	1	0	1	0	1	0	0	0	0	A	Display RAM and Segment output correspondence A=1:Reverse A=0:Normal
Display normal/reverse	0	1	0	1	0	1	0	0	1	1	R	Set LCD display reverse R=1:Reverse R=0:Normal
Display all point on/off	0	1	0	1	0	1	0	0	1	0	L	Set display all point on L=1:All on L=0:Normal
Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment Wr:+1 Rd:+0
End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
Duty select	0	1	0	1	0	1	0	1	0	0	U	Select LCD duty U=1:1/33 duty U=0:1/17 duty
LCD bias set	0	1	0	1	0	1	0	0	0	1	I	Select LCD bias voltage I=1:1/5 bias I=0:1/6 bias
Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
Power control	0	1	0	0	0	1	0	1	B	0	F	B=1:Booster on B=0:Booster off F=1:Follower on F=0:Follower off

TABLE OF ST7522 INSTRUCTIONS(continued)

Instructions	Instruction code											Function
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
Electronic contrast set	0	1	0	1	0	0	0	0	0	0	1	Set contrast by 64 level (V5 fine adjust)
				0	0	Electronic volume						
OSC Frequency set	0	1	0	1	1	1	1	0	0	0	1	Internal OSC frequency adjust
				0	0	0	0	josc 3	josc 2	josc 1	josc 0	
Follower input voltage set	0	1	0	1	1	1	1	1	0	0	0	V5 follower input voltage select(V5 coarse adjust)
				0	0	0	0	0	0	jvref 1	jvref 0	
Follower amplified ratio	0	1	0	0	0	1	0	0	rarb 2	rarb 1	rarb 0	V5 follower amplified ratio
Booster input voltage set	0	1	0	1	1	1	1	0	0	0	0	Booster input voltage select
				jbst 1	jbst 0	0	0	0	0	0	0	
Static indicator on/off static indicator register set	0	1	0	1	0	1	0	1	1	0	S	S=1:Indicator on S=0:Indicator off Set the individual indicator on/off
				0	0	0	0	S4	S3	S2	S1	
Sleep	Display off + Display all point on + Static indicator off compound command											Sleep mode
Stand by	Display off + Display all point on + Static indicator on compound command											Stand by mode

Command Description

See the Table of ST7522 instructions. The ST7522 series identifies a data bus using a combination of A0 and R/W ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

➢ Display ON/FF

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

This command turns the display on and off.
D=1: Display ON
D=0: Display OFF(default)

➢ Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

This command loads the page address register.

A3	A2	A1	A0	Page
0	0	0	0	0(default)
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
1	0	0	0	8(Icon)

Page mapping see Figure 4.

➢ Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by I each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 95, and the page address is not changed continuously.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	0	A3	A2	A1	A0	Low column set

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	A7	A6	A5	A4	High column set

This command loads the column address register.

A7	A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0	0(default)
0	0	0	0	0	0	0	1	1
				.				.
				.				.
				.				.
				.				.
0	1	0	1	1	1	1	1	95

➢ Read Status

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.
The ADC bit indicates the way column addresses are assigned to segment drivers.

ADC=1 : Normal. Column address n = segment driver n.
ADC=0: Inverted. Column address 95-n = segment driver n.

The ON/OFF bit indicates the current status of the display.

It is the inverse of the polarity of the display ON/OFF command.
ON/OFF=1: Display OFF
ON/OFF=0: Display ON

The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode,

RESET=1: Currently executing reset command.
RESET=0: Normal operation

➢ Write Display Data

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page, address registers and then increments the column address register by one.

➢ Read Display Data

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

➢ Start line set

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	Display start address				

Loads the RAM line address of the initial display line, COM 0,into the initial display line register. The RAM display data becomes the top line of the LCD screen. It is followed by the higher number lines in ascending order, corresponding to the duty cycle. The screen can be scrolled using this command by incrementing the line address.(default value=”00H”)

➢ Select ADC

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	A

The command selects the relationship between display data RAM column addresses and segment drivers.
A=1: SEG0 ← column address 5FH, … inverted
A=0: SEG0 ← column address 00H, … normal (default)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit Board design. See Figure 4 for a table of segments and column addresses for the two values of D.

➢ Display Normal/Reverse

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	R

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM(with ICON). When this is done. the display data RAM contents are maintained

.

R=1: Reverse
R=0: Normal(default)

➢ Display All Points ON/OFF

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	L

This command makes it possible to force all display points ON regardless of the content of the display data RAM(with ICON). The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.
L=1: All display points ON.
L=0: Normal(default)

Compound command priority follow below table

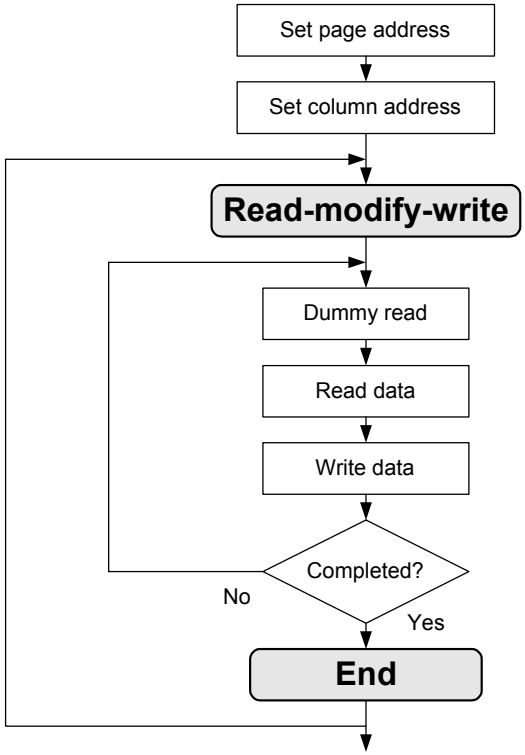
	Display all point on	Display reverse	Display on
Display on	All point black	Display reverse	Display on
Display reverse	All point white	Display reverse	Display reverse
Display all point on	Display all point on	All point white	All point black

➢ Read-Modify-Write

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

This command defeats column address register auto-increment after data reads. The current contents of the column Address register are saved. The mode remains active until an End command is received.

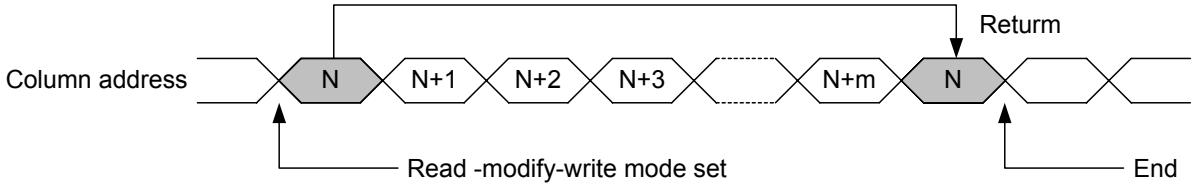
When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write Command. This function can reduce the load of MPU when data change is repeated as a specific display area.
*Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



➢ End

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



➢ Select Duty

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	U

U=1: 1/33 duty cycle (When double chip was be used, then both chip must set duty together)
U=0: 1/17 duty cycle (default)

➢ LCD bias set

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	I

I=1:1/5 bias
I=0:1/6 bias (default)

➢ Reset

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

This command initializes **the column address, the page address, the start line, the electric volume, and the static indicator are reset, and the read/modify/write mode are released. There is no impact on the display data RAM.** The reset operation is performed after the reset command is entered. Their default states are as follows:

1. Column address set to Address 0
2. Page address set to Page0
3. Start line set to first line
4. Electronic contrast register = 35H(max=3FH)
5. Static drive is turned OFF
6. Read modify write OFF

➢ Power control

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	B	x	F

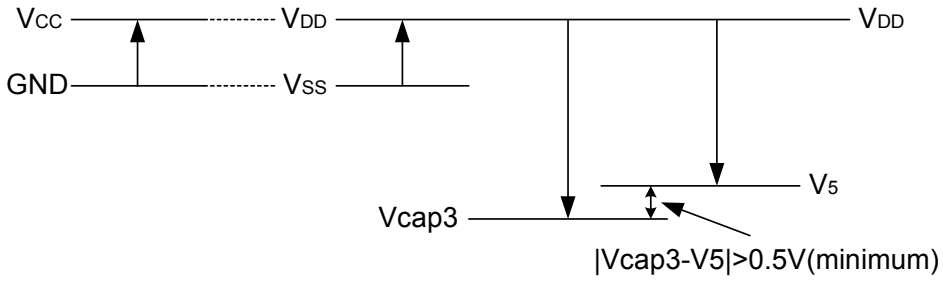
B=1: set booster circuit on, which makes Vcap3 has 2 time voltage
B=0: set booster circuit off, which make Vcap3 have 1 time voltage only. (default)

F=1: set follower circuit on, the V5 electric volume can adjust by internal follower circuit with command set.
F=0: set follower circuit off, the V1~V5 must connect to external voltage divider and adjust V5 level by external divider. (default)

B	F	Step- up circuit	Follower circuit	External input voltage
0	0	Open	Open	Vcap3 connect to V5 V1~V5 connect to external resistor
0	1	Open	Used	Vcap3 connect to external power supply
1	0	Used	Open	V1~V5 connect to external resistor
1	1	Used	used	-

Booster and follower on/off condition table

Note:
ensure V5 level stable, that must let |Vcap3-V5| over 0.5V(if panel size over 4.5",the |Vcap3-V5| propose over 0.8V).



(System side) (ST7522 Side)

➢ The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V5. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other. That command can operate in master chip for master + slave mode.

□ The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

□ Electronic Volume Register Set

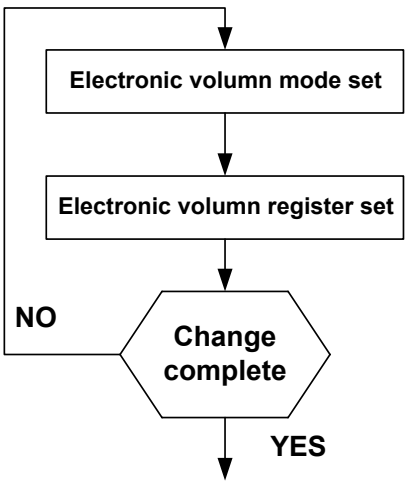
By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V_5 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	Electronic volume					

Default value="35H"

D7	D6	D5	D4	D3	D2	D1	D0	V5 level
0	0	0	0	0	0	0	0	Small
0	0	0	0	0	0	0	1	.
				.				.
				.				.
				.				.
				.				.
0	0	1	1	1	1	1	1	Large

The Electronic Volume Register Set Sequence



➢ OSC frequency set(Double Byte Command)

This command is designed for frame frequency adjustment, which can provide about 50% variation of frame frequency to avoid the interference with the frequency of daylight lamp in different countries. This command is a two byte command used as a pair with the OSC frequency mode set command and the OSC frequency register set command, and both commands must be issued one after the other.

□ The OSC frequency mode set

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	0	0	0	1

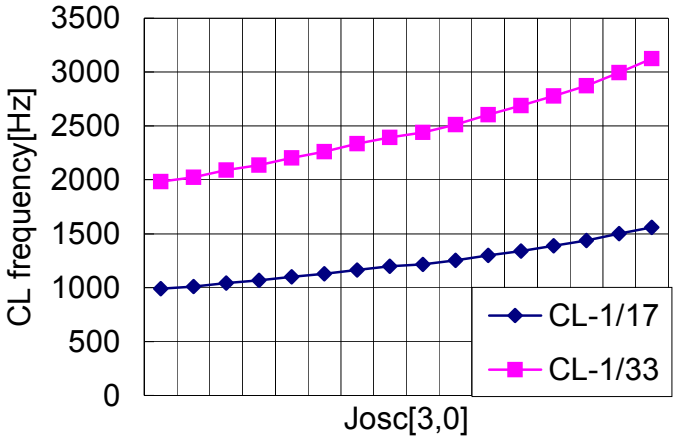
□ OSC frequency register set

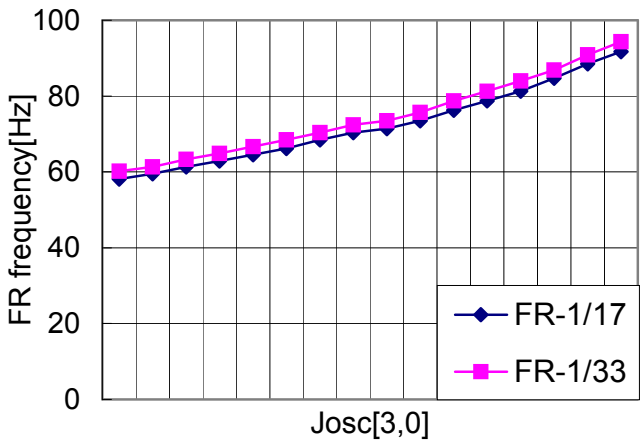
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	Josc3	Josc2	Josc1	Josc0

Default value="08H"

Josc3	Josc2	Josc1	Josc0	CL Frequency
0	0	0	0	Slow
0	0	0	1	
		.		.
		.		.
		.		.
		.		.
1	1	1	1	Fast

Frequency for "OSC frequency set" command





Conditions:

1. VDD=3.0V
2. Use internal OSC circuit

➢ Follower input voltage set(Double Byte Command)

V5 amplifier input voltage can be set by this command, which provide coarse adjustment only. This command needs to be used with the electric volume control command in order to get correct V5 output. This command is a two byte command used as a pair with the follower input voltage mode set command and the follower input voltage register set command, and both commands must be issued one after the other.
See the power control explanation for details.

□ The follower input voltage mode set

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

□ Follower input voltage register set

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	Jvref1	Jvref0

Default value="02H"

Jvref1	Jvref0	V5 input voltage
0	0	4/6*VSS
0	1	3/6*VSS
1	0	2/6*VSS(default)
1	1	1/6*VSS

Follower input voltage parameter

➢ Follower amplified ratio

This command sets the V5 voltage internal resistor ratio. that can control V5 level with follower input voltage set command and electric volume command.
See the power control explanation for details.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	RaRb2	RaRb1	RaRb0

Default value="06H"

Rarb2	Rarb1	Rarb0	V5 amplified ratio
0	0	0	2
0	0	1	2.5
0	1	0	3
0	1	1	3.5
1	0	0	4
1	0	1	4.5
1	1	0	5(default)
1	1	1	5.5

Follower amplified ratio parameter

The V5 level be generate by OPAmp with VDD-Vcap3 power supply, so that V5 level must to be smaller than Vcap3 over –0.5V.
Fine adjustment must to used EC[5:0] adjust of Electronic contrast set command.
Coarse adjustment must to used jvref[1:0] adjust of Follower input voltage set command.

For V5 voltage level setup formula:

(follower must on of power control command)
(used follower input voltage set and amplified ratio command)

Jvref[1,0]	[1,1]	[1,0]	[0,1]	[0,0]
Rvref	200K	400K (default)	600K	800K

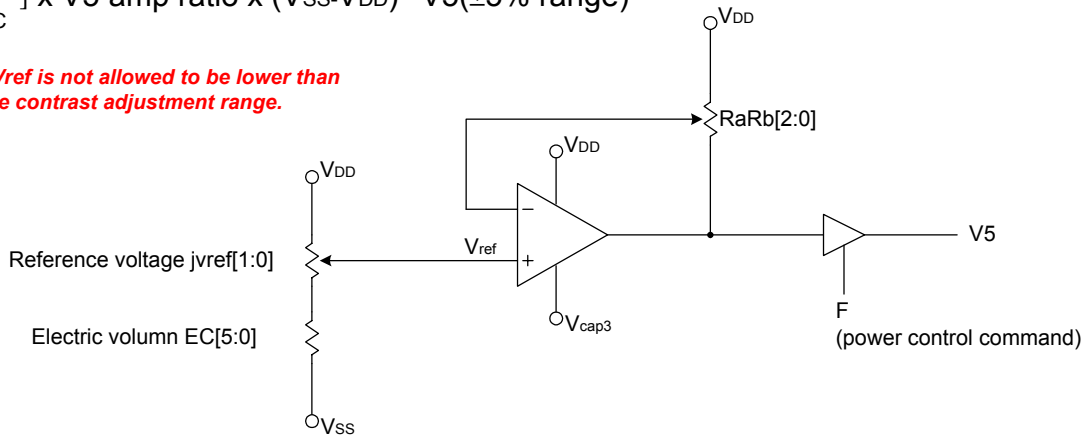
Rarb2	Rarb1	Rarb0	V5 amplified ratio
0	0	0	2
0	0	1	2.5
0	1	0	3
0	1	1	3.5
1	0	0	4
1	0	1	4.5
1	1	0	5(default)
1	1	1	5.5

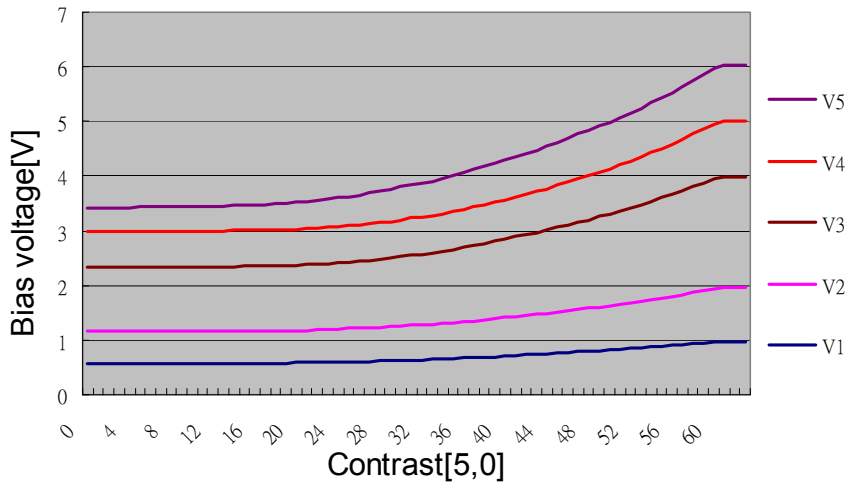
[3FH-EC volume] x 20KΩ=REC

$$\left[\frac{Rvref}{1M+R_{EC}}\right] \times (V_{SS}-V_{DD}) = V_{ref}$$

$$\left[\frac{Rvref}{1M+R_{EC}}\right] \times V5\ amp\ ratio \times (V_{SS}-V_{DD}) = V5(\pm 5\%\ range)$$

The value of Vref is not allowed to be lower than 1.2V within the contrast adjustment range.





Test condition:

1. VDD=3.0V
2. Booster/Follower=Default set
3. Bias=1/6
4. Only master chip

➢ Booster input voltage set (Double Byte Command)

This command is designed to select different level of the input voltage to booster. In 5V application system, it's better to reduce the input voltage of booster to make sure that the output voltage of booster will not be over the specification range of VDD-Vcap3. This command is a two byte command used as a pair with the booster input voltage mode set command and the booster input voltage register set command, and both commands must be issued one after the other.
See the power control explanation for details.

□ The booster input voltage mode set

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	0	0	0	0

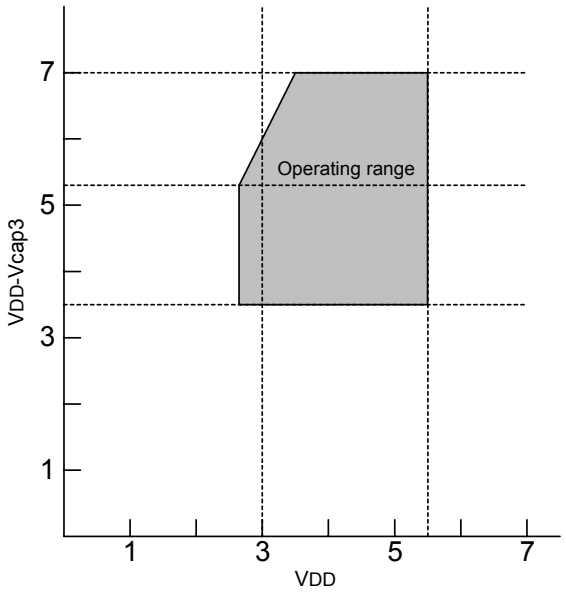
□ Booster input voltage register set.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	Jbst1	Jbst0	0	0	0	0	0	0

Default value="00H"

Jbst1	Jbst0	VSS2
0	0	1*VSS(default)
0	1	4/5*VSS
1	0	3/5*VSS
1	1	2/5*VSS

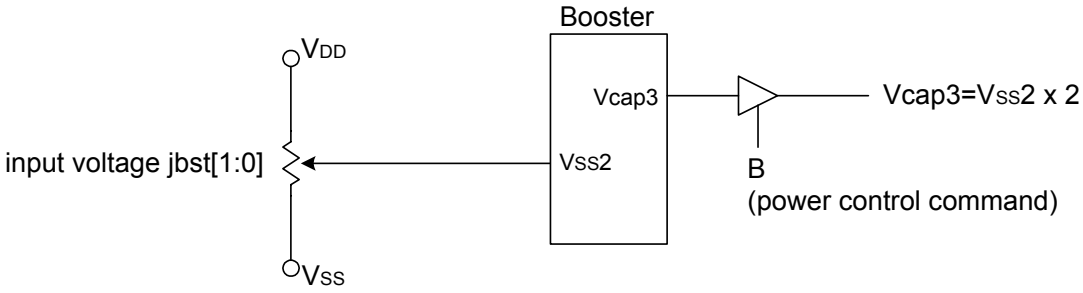
Booster input voltage parameter



Operating voltage range of Vss and Vcap3 system

For Vcap3 voltage level setup formula:
(booster must on of power control command)
(used booster input voltage set command)

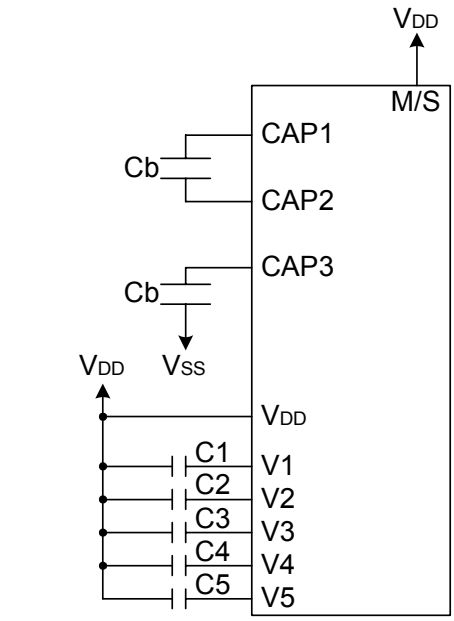
Vcap3=VSS2 x 2
(booster must on of power control command)

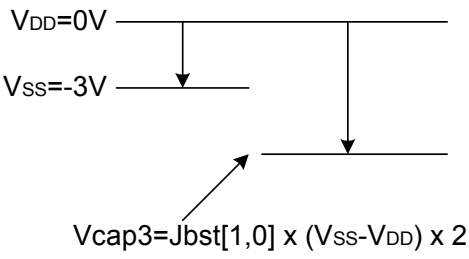


Reference circuit examples:

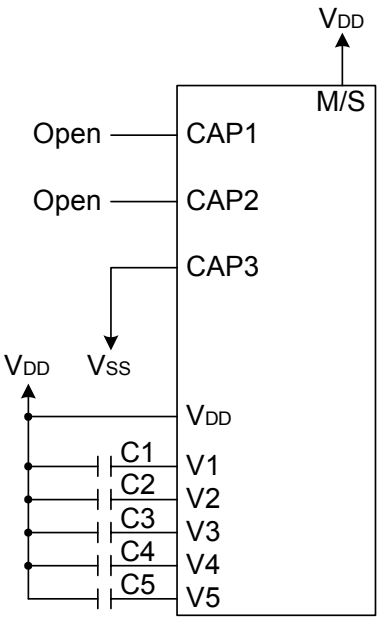
When used 2x step-up voltage circuit, the “Power control” command must set to 2DH and adjust “Booster input voltage set” command of Vcap3’ s full range.

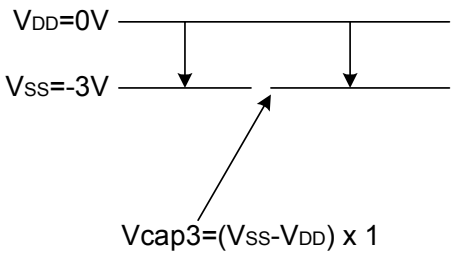
When used 1x step-up voltage circuit, the “Power control” command must set to 29H; the “Booster input voltage set” command is not action at this operation.





2x step-up voltage circuit
(Power control=2DH)





1x step-up voltage circuit
(Power control=29H)

➢ Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.
This is used when one of the static indicator liquid crystal drive electrodes is connected to the COMS terminal, and the other is connected to the S1~S4 terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.
The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

□ Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	S

S=1: Indicator on
S=0: Indicator off (default)

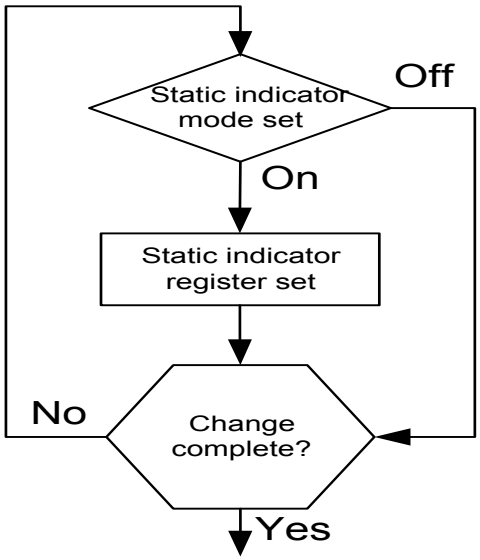
□ Static Indicator Register Set

This command sets four bits of data into the static indicator register, and is used to set the static indicator into a on/off mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	S1	S2	S3	S4

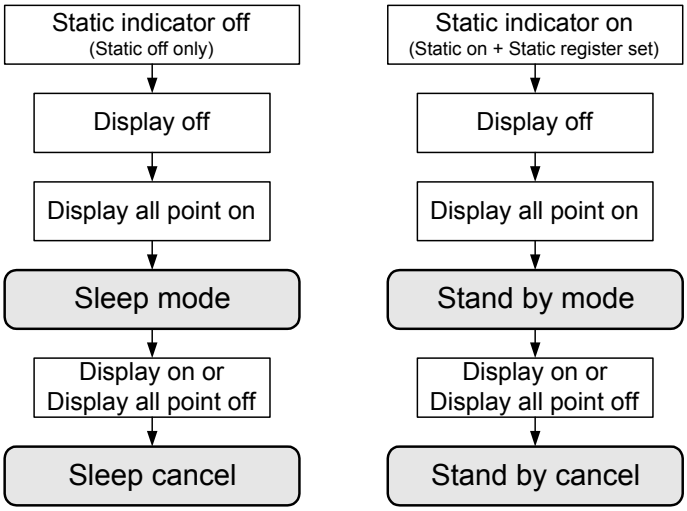
the command selection the S1-S4 static indicator on or off.
Sn=1: Sn -> on
Sn=0: Sn -> Off(default)

Static Indicator Register Set Sequence



➢ Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When all static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.
In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was ineffect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.



□ Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:
1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment and common drive outputs output a V_{DD} level.

□ Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.
1. The LCD power supply circuits are halted. The oscillator circuit continues to operate.
2. The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a V_{DD} level.

* When the master is turned on, the oscillator circuit is operable immediately after the powering on.
* When the master/slave mode, into Sleep or Standby mode have to at same time.

Software Example

Condition:

1. **VDD=5.0V**
2. Use Winbond W78E52-40 at 16MHz crystal(compatible intel 8051 MPU)
3. Use Mater and Slave mode(ST7522D x 2)
4. **|VCAP3|=(5x2)x3/5=6V**
5. **|V5|=[600KΩ/(1MΩ+200KΩ)]x2x5=5V**

```
;Reset
                CLR     RES             ;Reset ST7522D(Master & Slave)
                CALL    DELAY           ;
                SETB    RES
                CALL    DELAY           ;
;-------------------------------------------------------------------------------------------------------------------------------
;Initial LCD
                CLR     CS1             ;Enable chip 1(low active)
                CLR     CS2             ;Enable chip 2(low active)

                MOV     A,#11110001B    ;OSC frequency set
                CALL    WRINS           ;
                MOV     A,#10001000B    ;Frame about 80.6Hz/OSC frequency about 2.6KHz
                CALL    WRINS           ;

                MOV     A,#11111000B    ;Follower input voltage set
                CALL    WRINS           ;
                MOV     A,#00000001B    ;V5 input voltage=3/6*VSS
                CALL    WRINS           ;

                MOV     A,#00100000B    ;Follower amplified ratio
                CALL    WRINS           ;Ratio=2

                MOV     A,#11110000B    ;Booster input voltage set
                CALL    WRINS           ;
                MOV     A,#10000000B    ;VSS2=3/5 *VSS
                CALL    WRINS           ;

                MOV     A,#00101111B    ;Power control
                CALL    WRINS           ;

                MOV     A,#10101001B    ;Duty select
                CALL    WRINS           ;

                MOV     A,#10100010B    ;LCD bias set
                CALL    WRINS           ;

                MOV     A,#10000001B    ;Electronic contrast set
                CALL    WRINS           ;
                MOV     A,#00110101B    ;Contrast register=35H
                CALL    WRINS           ;

                CALL    DELAY200mS      ;Delay 200mS for booster & follower stable

                MOV     A,#10101111B    ;Display on
                CALL    WRINS           ;
                        .
                        .
                        .
                        .
```

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power supply voltage	V_{DD}	-0.3 to +7.0	V
LCD driver voltage	Vcap3	-7.0 to +0.3	V
Input voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Operating temperature	T_A	-40 to +85	℃
Storage temperature	T_{STO}	-55 to +125	℃

DC CHARACTERISTICS

Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V

Item		Symbol	Condition	Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage		VDD	-	2.7	3.0	5.5	V	V_{DD}*1
Step up output voltage		Vcap3	(Relative to V_{DD})	-7	-	-3.5	V	CAP3
Voltage follower circuit operating Voltage		V5	(Relative to V_{DD})	-7	-	-3.5	V	V5
V5 accuracy		V5	-	-7	-	7	%	V5
High-level Input Voltage Low-level Input Voltage		V_{IHC} V_{ILC}	-	0.7 V_{DD} Vss	-	V_{DD} 0.9	V	*2
High-level Output Voltage Low-level Output Voltage		V_{OHC} V_{OLC}	I_{OH} = –0.5 mA I_{OL} = 0.5 mA	0.8V_{DD} Vss	-	V_{DD} 0.2 V_{DD}	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	-1	-	2	uA	*4
Output leakage current		I_{LO}	-	-1		1	uA	*5
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C (Relative To V_{DD}) V_5 = –6.0 V	-	1.6	2.0	KΩ	SEGn COMn *6
Oscillator Frequency	Internal Oscillator	f_{OSC}	Ta = 25°C 1/33Duty	2	-	3	kHz	CL
	External Input RECOMMAND	f_{CL}		2	-	3.5		

• Dynamic Consumption Current, During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used.

Display Pattern OFF

Ta = 25°C Vcap3=-6V

Item	Symbol	Condition	Rating			Unit	Notes
			Min.	Typ.	Max.		
ST7522	IDD	VDD=3.0 V, VDD-V5=-5.0V	-	10	15	μA	*7
		VDD=5.0 V, VDD-V5=-5.0V	-	35	45		

-

Display Pattern Checker

Ta = 25°C Vcap3=-6V

Item	Symbol	Condition	Rating			Unit	Notes
			Min.	Typ.	Max.		
ST7522	IDD	VDD=3.0 V, VDD-V5=-5.0V	-	15	20	μA	*7
		VDD=5.0 V, VDD-V5=-5.0V	-	40	50		

• Dynamic Consumption Current, During Display, with the Internal Power Supply ON

Display Pattern OFF

Ta = 25°C Vcap3=-6V

Item	Symbol	Condition	Rating			Unit	Notes
			Min.	Typ.	Max.		
ST7522	IDD	VDD=3.0 V, VDD-V5=-5.0V	-	60	70	μA	*7
		VDD=5.0 V, VDD-V5=-5.0V	-	120	130		

Display Pattern Checker

Ta = 25°C Vcap3=-6V

Item	Symbol	Condition	Rating			Unit	Notes
			Min.	Typ.	Max.		
ST7522	IDD	VDD=3.0 V, VDD-V5=-5.0V	-	65	80	μA	*7
		VDD=5.0 V, VDD-V5=-5.0V	-	130	150		

• Consumption Current at Time of Power Saver Mode, VSS = 0 V, VDD = 3.0 V ± 10%

Ta = 25°C

Item	Symbol	Condition	Rating			Unit	Notes
			Min.	Typ.	Max.		
Sleep mode	IDD	-	-	5	10	μA	-
Standby Mode	IDD	-	-	10	15		

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The A0, D0 to D5, D6 (SCL), D7 (SI), RD (E), WR (R/W), CS1, CS2, CLS, CL, FR, M/S, C86, P/S , and RES terminals.

*3 The D0 to D7, FR and CL terminals.

*4 The A0, RD (E), WR (R/W), CS1, CS2, CLS, M/S, C86, P/S, and RES terminals.

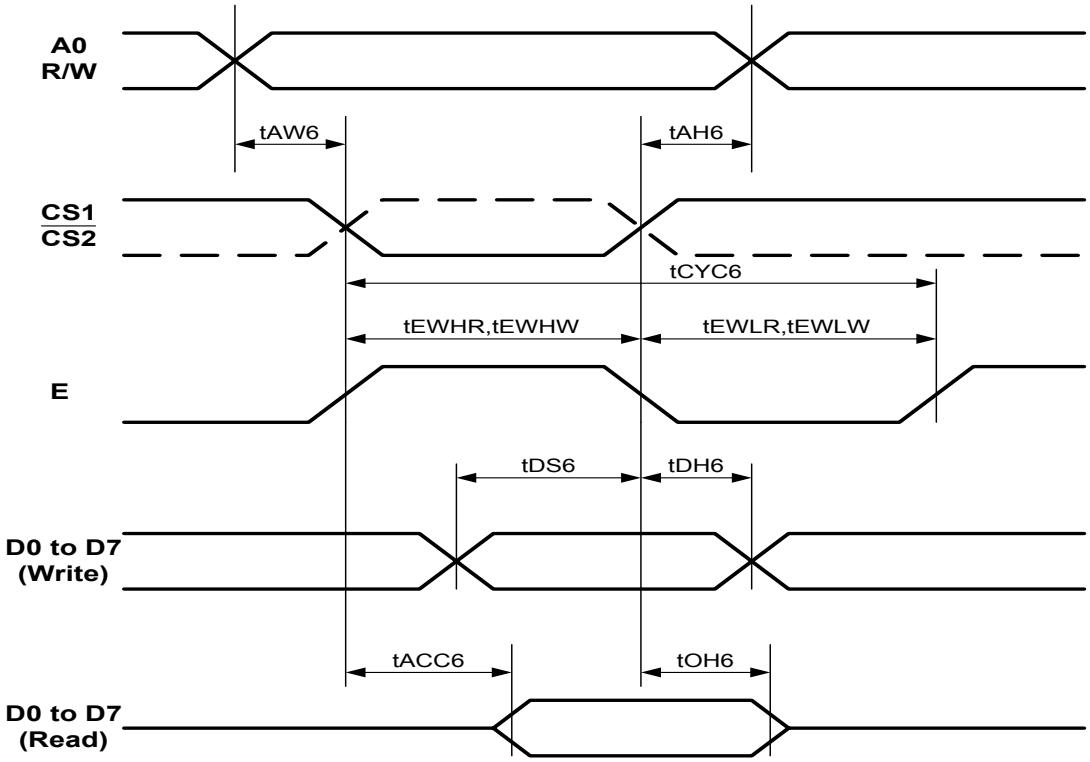
*5 Applies when the D0 to D5, D6 (SCL), D7 (SI), CL, and FR terminals are in a high impedance state.

*6 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V_1, V_2, V_3, and V_4). These are specified for the operating voltage (3) range. R_{ON} = 0.1 V / △I (Where △I is the current that flows when 0.1 V is applied while the power supply is ON.)

*7 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.
Does not include the current due to the LCD panel capacity and wiring capacity.
Applicable only when there is no access from the MPU.

TIMING CHARACTERISTICS

68 Interface



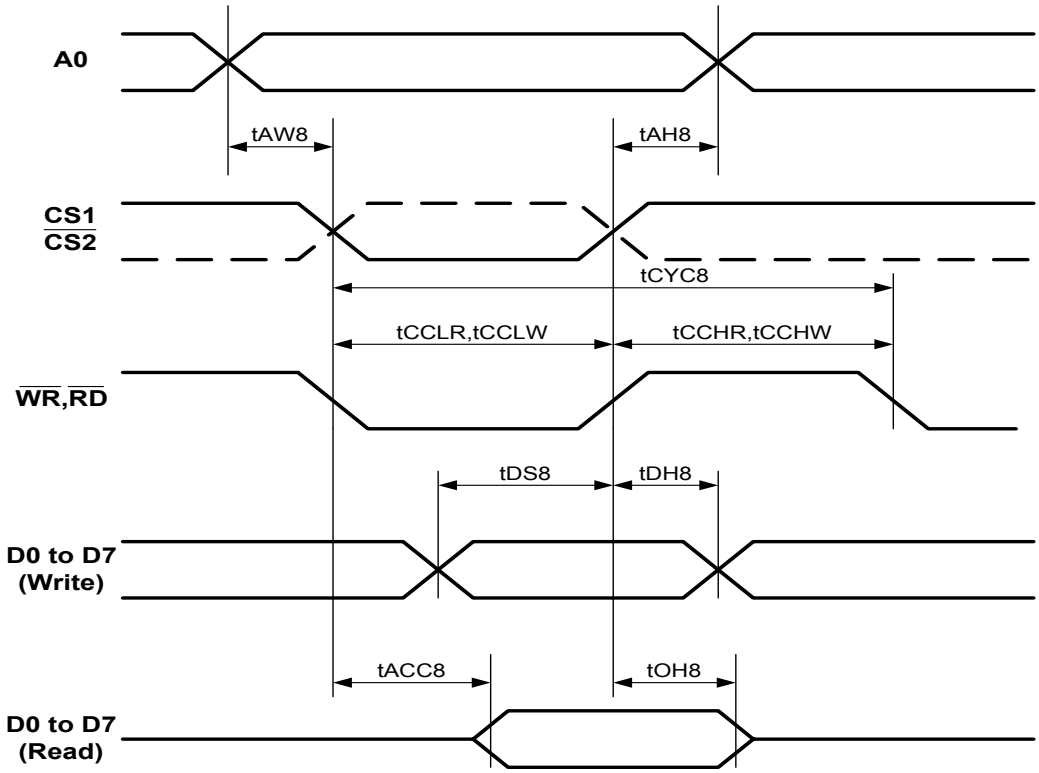
(Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
					Min.	Max.	Min.	Max.	
Address hold time		A0	t_{AH6}	—	10	—	10	—	ns
Address setup time		A0	t_{AW6}		25	—	10	—	
System cycle time		A0	t_{CYC6}	—	4400	—	3500	—	ns
Data setup time		D0 to D7	t_{DS6}	—	25	—	25	—	ns
Data hold time		D0 to D7	t_{DH6}		10	—	10	—	
Access time		D0 to D7	t_{ACC6}	C_L = 100 pF	—	90	—	60	ns
Output disable time		D0 to D7	t_{OH6}		—	1100	—	1100	
Enable H pulse time	Read	E	t_{EWHR}	—	260	—	160	—	ns
	Write		t_{EWHW}		260	—	160	—	
Enable L pulse time	Read	E	t_{EWLR}	—	200	—	140	—	ns
	Write		t_{EWLW}		2300	—	1200	—	

*1 All timing is specified using 20% and 80% of V_{DD} as the reference.

*2 t_{EWLW} and t_{EWLR} are specified as the overlap between CS1 being “L” (CS2 = “H”) and E.

80 Interface



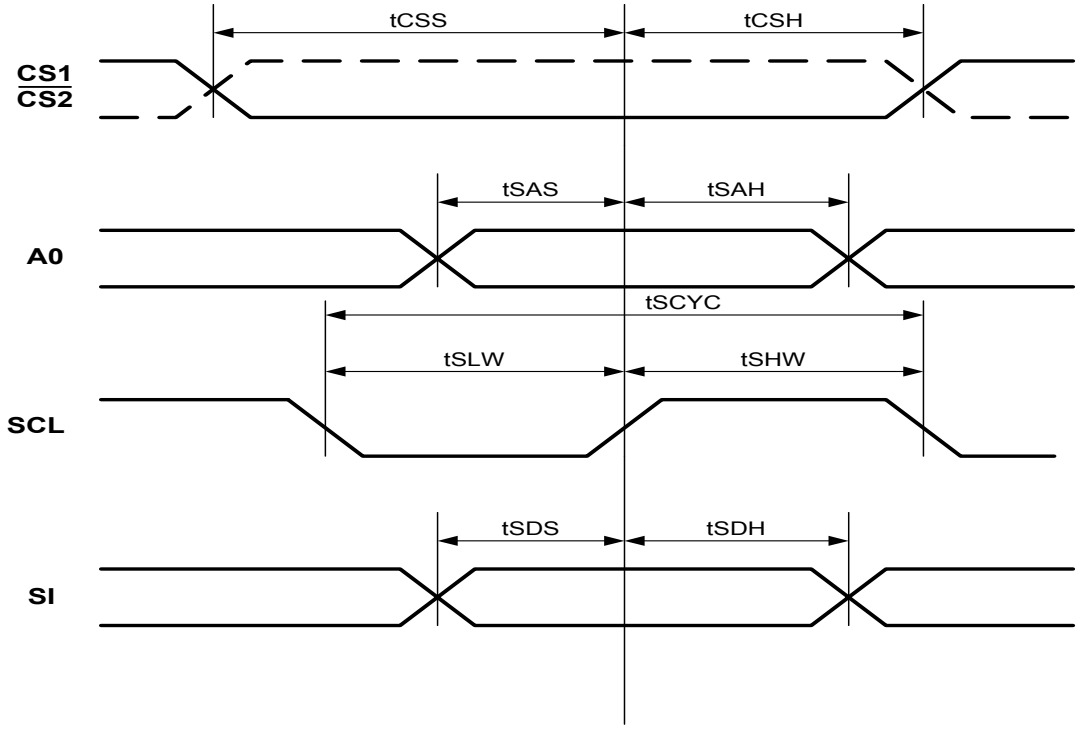
(Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
Address hold time	A0	t_{AH8}	—	10	—	10	—	ns
Address setup time		t_{AW8}		10	—	10	—	
System cycle time	A0	t_{CYC8}	—	3400	—	1300	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}	—	350	—	160	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		530	—	200	—	
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		1100	—	1100	—	
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		730	—	530	—	
Data setup time	D0 to D7	t_{DS8}	—	25	—	10	—	ns
Address hold time		t_{DH8}		10	—	10	—	
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L = 100 pF	—	70	—	70	ns
Output disable time		t_{OH8}		—	1200	—	1100	

*1 All timing is specified using 20% and 80% of V_{DD} as the reference.

*2 t_{CCLW} and t_{CCLR} are specified as the overlap between CS1 being “L” (CS2 = “H”) and $\overline{WR}$ and $\overline{RD}$ being at the “L” level.

Serial Interface



(Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}	—	500	—	400	—	ns
SCL “H” pulse width		t_{SHW}		100	—	300	—	
SCL “L” pulse width		t_{SLW}		200	—	120	—	
Address setup time	A0	t_{SAS}	—	0	—	0	—	ns
Address hold time		t_{SAH}		100	—	100	—	
Data setup time	SI	t_{SDS}	—	0	—	0	—	ns
Data hold time		t_{SDH}		120	—	100	—	
CS-SCL time	CS	t_{CSS}	—	60	—	40	—	ns
		t_{CSH}		2200	—	1000	—	

*1 All timing is specified using 20% and 80% of V_{DD} as the standard.

Reset Timing

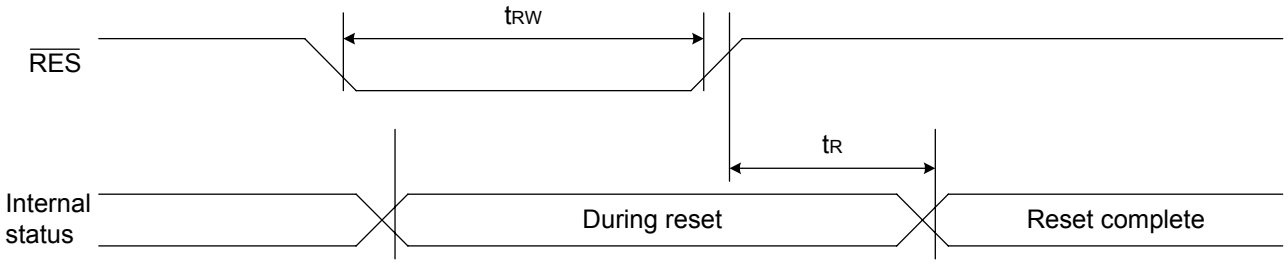


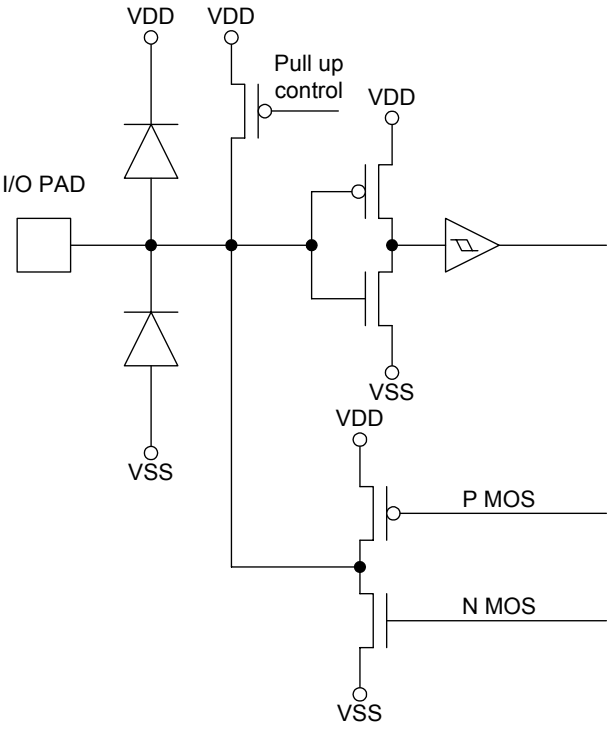
Figure 41

Table 36

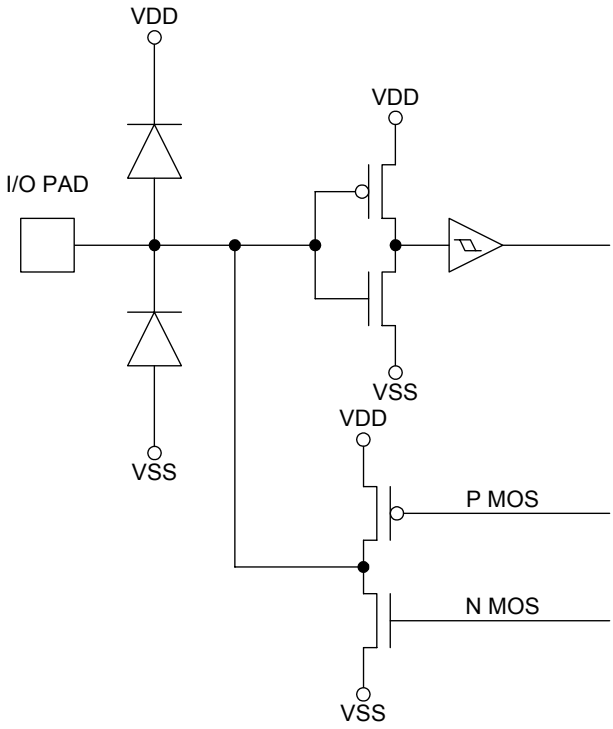
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	—	t_R	—	—	1	100	μs
Reset "L" pulse width	RES	t_{RW}	—	0.2	1	—	μs

*1 When double chip was be used, then the duty set command must be set between the t_R

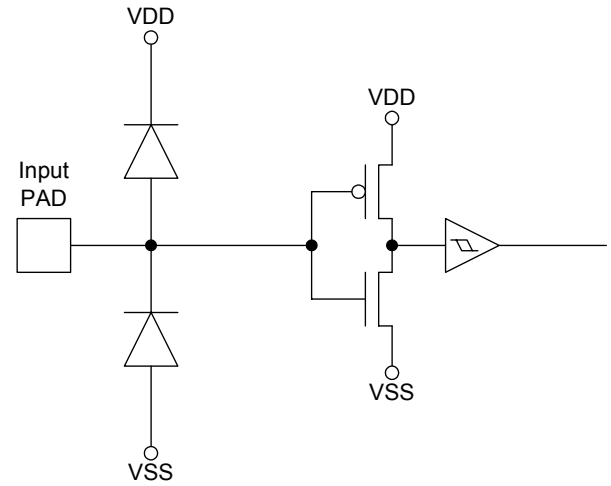
I/O PAD CONFIGURATION



I/O PAD:D0,D1,D2,D3,D4,D5



I/O PAD:D6,D7,FR,CL

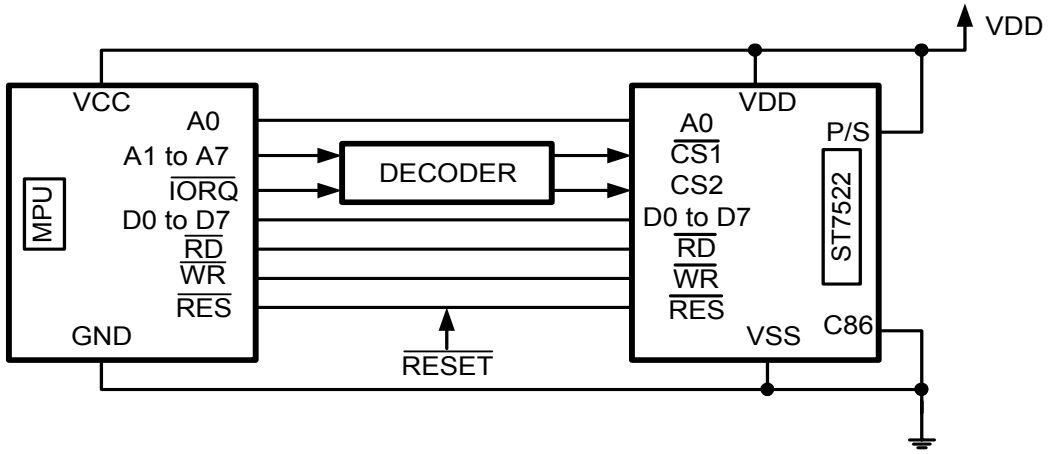


Input PAD:
RES,P/S,/CS1,CS2,CLS,
E(/RD),R/W(/WR),A0,C86,M/S

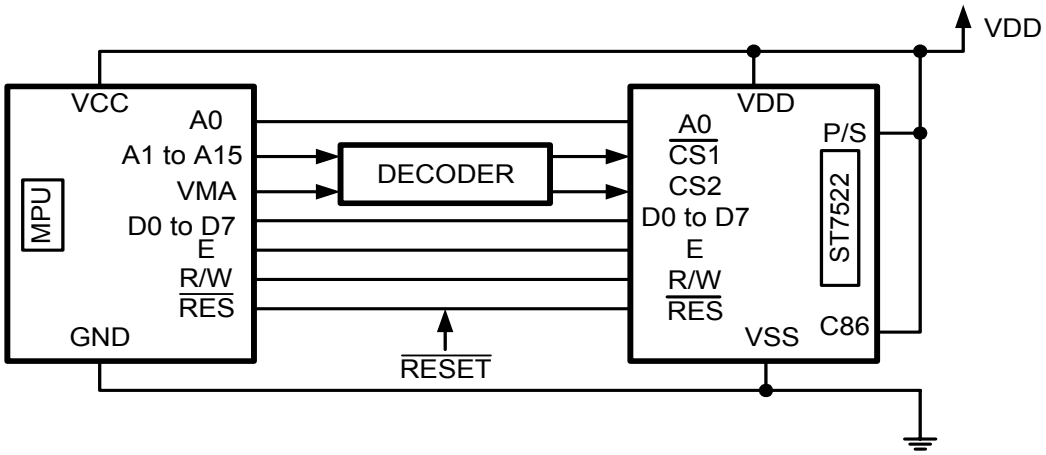
D0~D5 into pull up mode when P/S set to VSS(Serial interface), but P/S set to VDD(Parallel interface), D0~D5 will be without pull up MOS connected.

THE MPU INTERFACE (REFERENCE EXAMPLES)

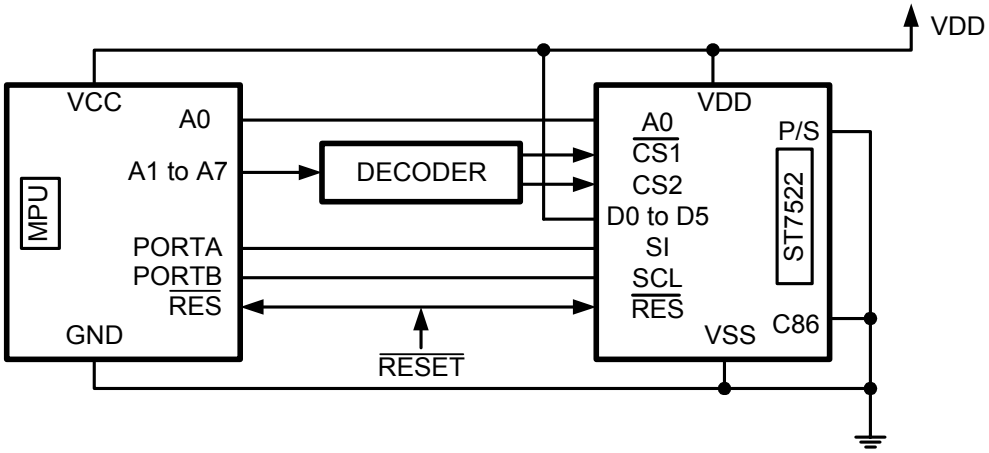
The ST7522 Series can be connected to either 80x86 Series MPUs or to 68000 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7522 series chips with fewer signal lines.
The display area can be enlarged by using multiple ST7522 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.
(1) 8080 Series MPUs



(2) 6800 Series MPUs



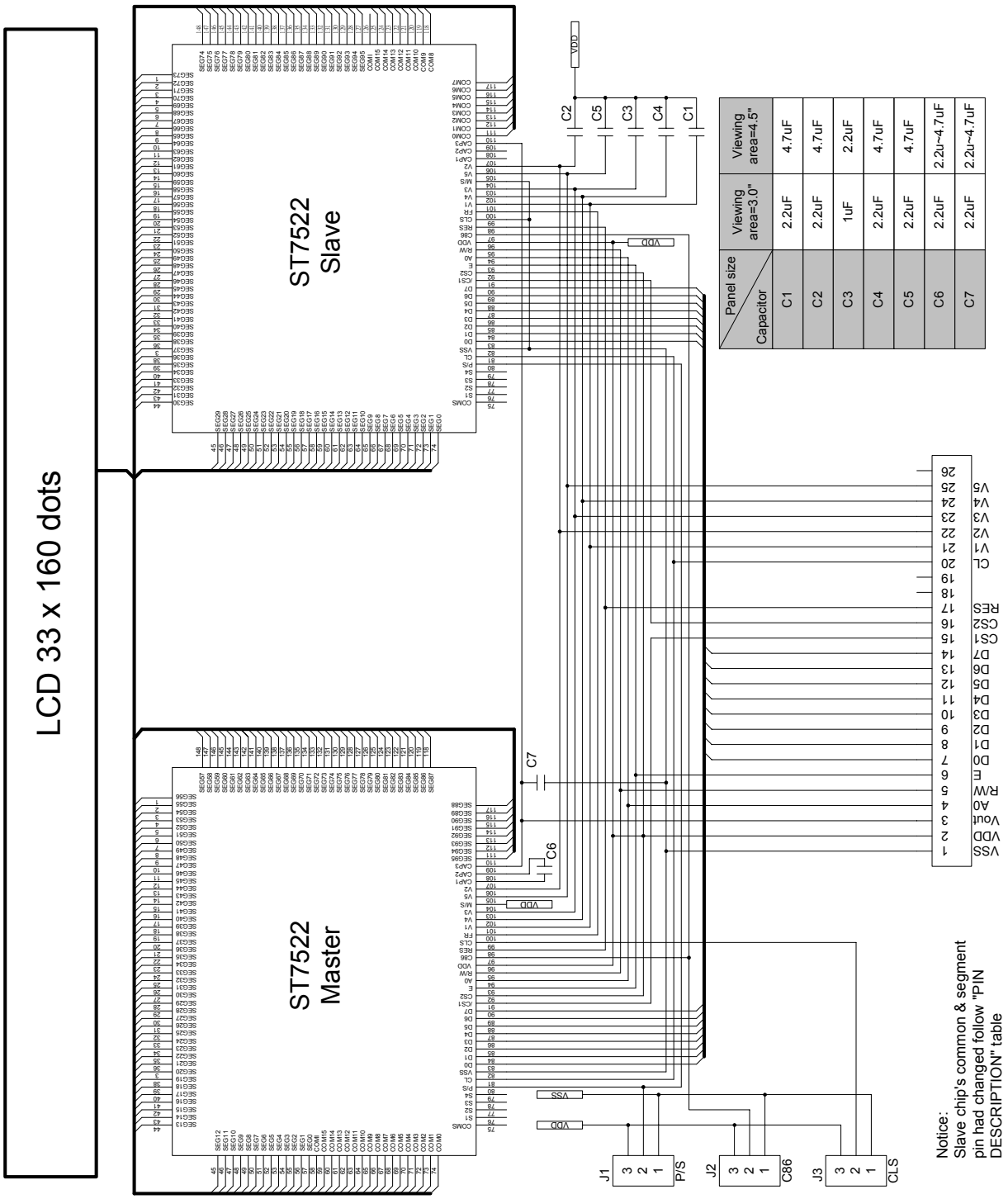
(3) Using the Serial Interface



APPLICATION (Master & Slave Mode)

Condition:

1. 2 time booster
2. internal follower
3. internal OSC frequency

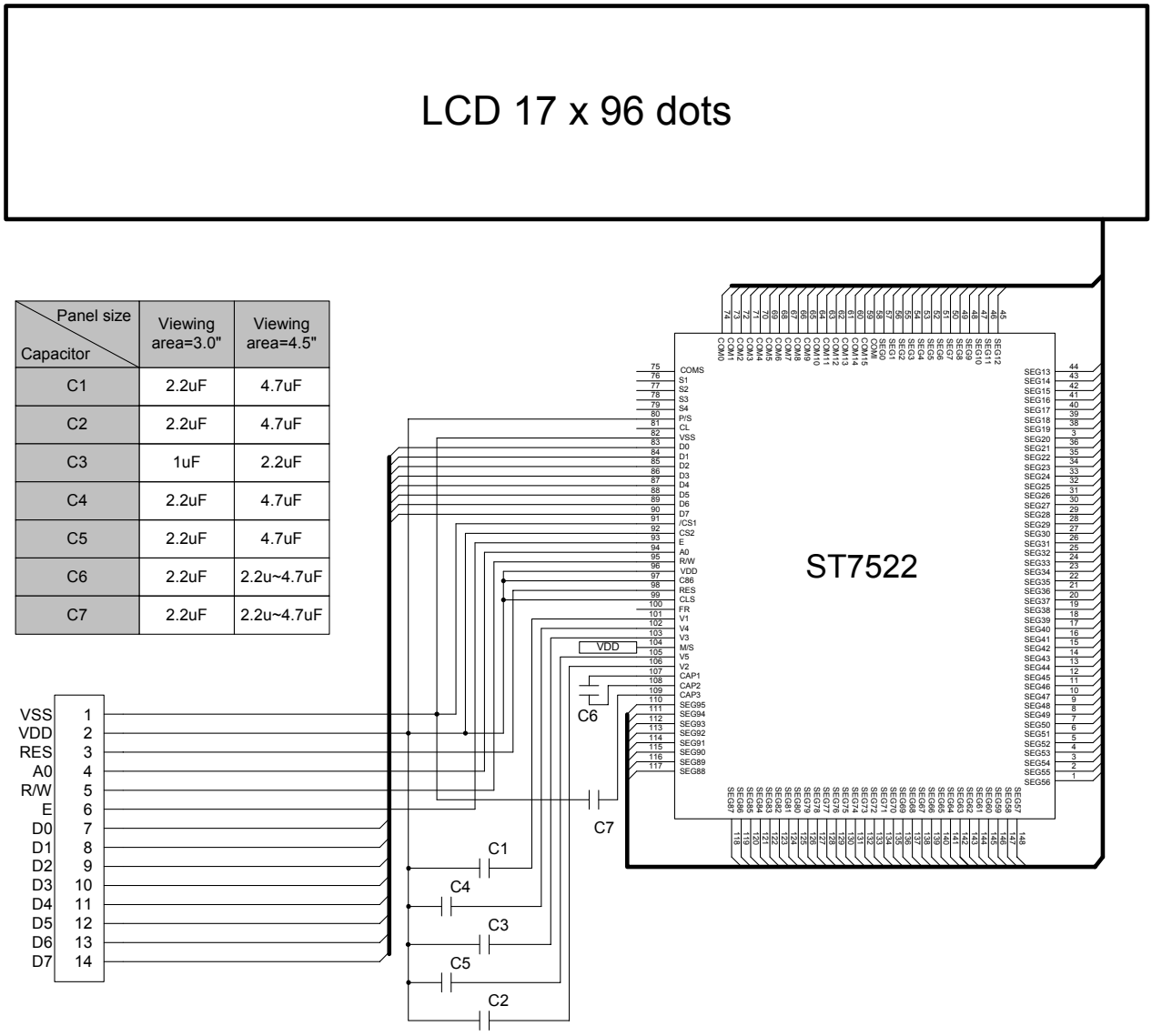


APPLICATION(Only use master mode)

Resemble ST7066U+ST7065C (2 line x 16 word with 14 pin assign application)

condition:

1. 68 interface
2. 2 time booster
3. internal follower
4. internal OSC frequency



Capacitor \ Panel size	Viewing area=3.0"	Viewing area=4.5"
C1	2.2uF	4.7uF
C2	2.2uF	4.7uF
C3	1uF	2.2uF
C4	2.2uF	4.7uF
C5	2.2uF	4.7uF
C6	2.2uF	2.2u~4.7uF
C7	2.2uF	2.2u~4.7uF