ST7282

720x544 System-On-Chip Driver

for 480RGBx272 TFT LCD

Datasheet

Version 1.5
2016/06

Sitronix Technology Corporation

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1. GENERAL DESCRIPTION

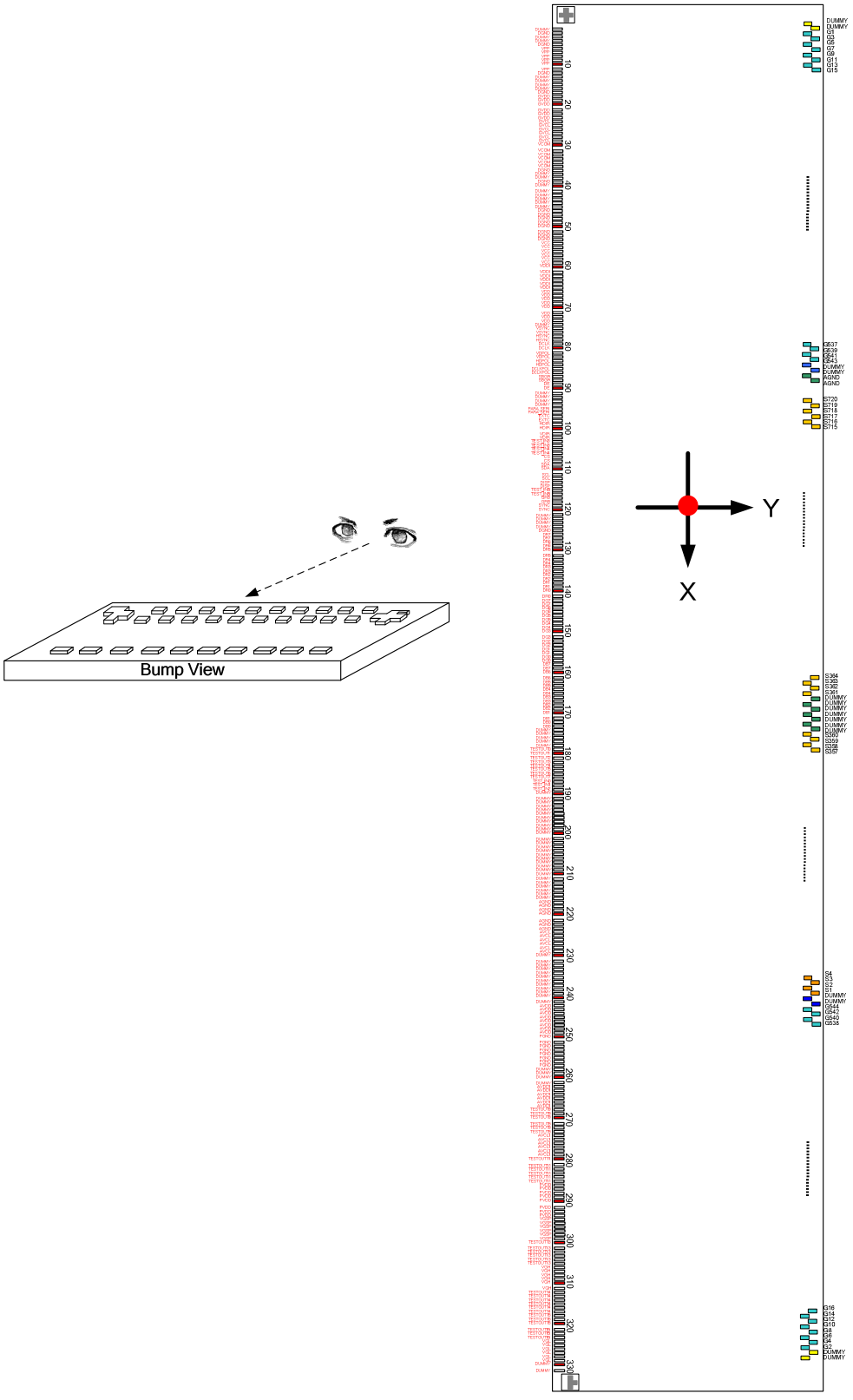
ST7282 offers all-in-one chip solution of 480RGBx272 for color TFT-LCD panel. This chip incorporated with digital timing generator, source and gate driver, power supply circuit and embedded serial communication interface for function setting. The source output support real 8-bit resolution and 256-gray scale with small output deviation are designed to support higher color resolution. The power supply circuit incorporated with step-up circuit, regulators and operational amplifiers to generate power supply voltages to drive TFT LCD.

2. FEATURES

- Display Resolution: 480*RGB (H) *272(V)
- LCD Driver Output Circuits
  - Source Outputs: 720 Channels
  - Gate Outputs: 544 Channels
  - Common Electrode Output
- 256 gray scale with true 8 bit DAC
- Support SYNC, SYNC-DE and DE mode RGB interface input timing
- Support 8-bit serial and 24-bit parallel RGB interface
- Support 3- wire Serial Peripheral Interface to config and control display
- On Chip Build-In Circuits
  - DC/DC Converter
  - Non-Volatile (NV) Memory to store initial Register setting and factory default value
  - Timing Controller
- Wide Supply Voltage Range
  - I/O Voltage (VDDI to DGND): 1.65V ~ VDD
  - Analog Voltage (VDD to AGND): 3.0V ~ 3.6V
  - Charge pump Voltage (PVDD to PGND): 3.0V ~ 3.6V
- On-Chip Power System
  - GVDD: +4.9600 ~ +5.9680V
  - GVCL: -4.4800V ~ -2.9600V
  - Gate driver HIGH level (VGH to AGND): +13V ~ +17.5V
  - Gate driver LOW level (VGL to AGND): -11.5V ~ -7V
- Optimized layout for COG Assembly
- Non-Volatile Memory (OTP) can only program one time for LCD VCOM calibration
- **Design for Consumer Applications; Automotive Related Products are Excluded**

3. PAD ARRANGEMENT

3.1 Output Bump Dimension

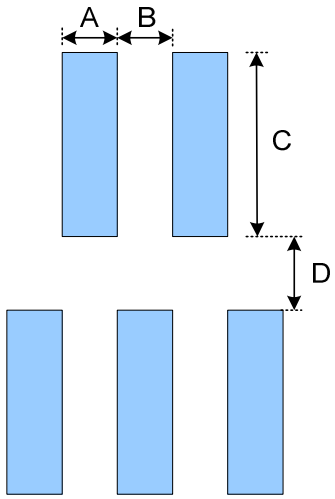


3.2 Bump Dimension

Output Pads

S1~S720、G1~G544、VCOM、DUMMY

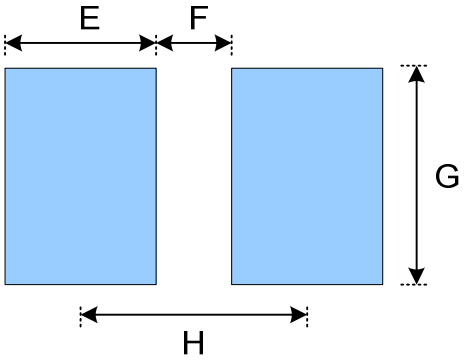
(No.332~1628)



Symbol	Item	Size
A	Bump Width	15 um
B	Bump Gap 1 (Horizontal)	15、30、75um
C	Bump Height	100 um
D	Bump Gap 2 (Vertical)	30 um

Input Pads

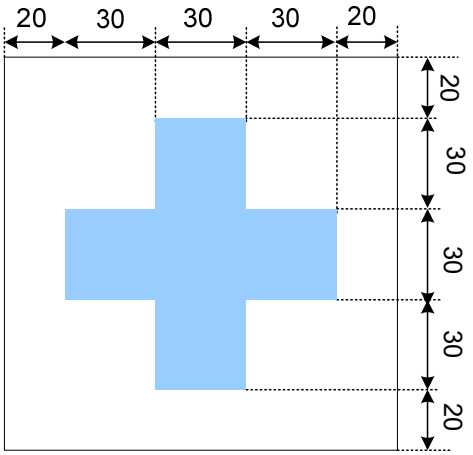
(No.1~331)



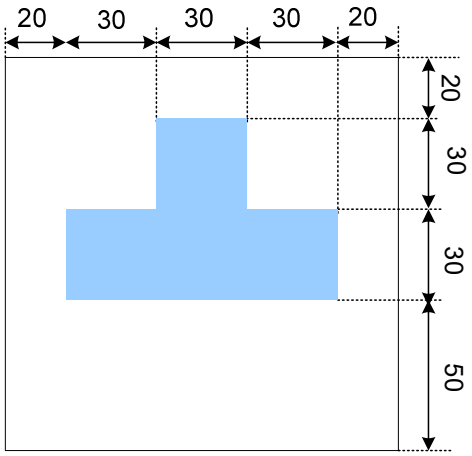
Symbol	Item	Size
E	Bump Width	35 um
F	Bump Gap	24 um
G	Bump Height	100 um
H	Bump Pitch	59 um

3.3 Alignment Mark Dimension

Alignment Mark: A1(X,Y)=(-9963,-235)



Alignment Mark: A2(X,Y)=(9963,-235)



3.4 Chip Information

Chip size	20200μm x730μm
Chip thickness	300μm
Pad Location	Pad center
Coordinate Origin	Chip center

4. PAD CENTER COORDINATES

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	DUMMY	-9735	-257	34	VCOM	-7788	-257
2	DGND	-9676	-257	35	VCOM	-7729	-257
3	DUMMY	-9617	-257	36	DGND	-7670	-257
4	DUMMY	-9558	-257	37	DUMMY	-7611	-257
5	DGND	-9499	-257	38	DUMMY	-7552	-257
6	VPP	-9440	-257	39	DGND	-7493	-257
7	VPP	-9381	-257	40	DUMMY	-7434	-257
8	VPP	-9322	-257	41	DUMMY	-7375	-257
9	VPP	-9263	-257	42	DUMMY	-7316	-257
10	VPP	-9204	-257	43	DUMMY	-7257	-257
11	VPP	-9145	-257	44	DUMMY	-7198	-257
12	DGND	-9086	-257	45	DUMMY	-7139	-257
13	DUMMY	-9027	-257	46	DGND	-7080	-257
14	DUMMY	-8968	-257	47	DGND	-7021	-257
15	DUMMY	-8909	-257	48	DGND	-6962	-257
16	DUMMY	-8850	-257	49	DGND	-6903	-257
17	DGND	-8791	-257	50	DGND	-6844	-257
18	GVDD	-8732	-257	51	DGND	-6785	-257
19	GVDD	-8673	-257	52	DGND	-6726	-257
20	GVDD	-8614	-257	53	DGND	-6667	-257
21	GVDD	-8555	-257	54	VCC	-6608	-257
22	GVDD	-8496	-257	55	VCC	-6549	-257
23	GVDD	-8437	-257	56	VCC	-6490	-257
24	GVCL	-8378	-257	57	VCC	-6431	-257
25	GVCL	-8319	-257	58	VCC	-6372	-257
26	GVCL	-8260	-257	59	VCC	-6313	-257
27	GVCL	-8201	-257	60	VDDI	-6254	-257
28	GVCL	-8142	-257	61	VDDI	-6195	-257
29	GVCL	-8083	-257	62	VDDI	-6136	-257
30	VCOM	-8024	-257	63	VDDI	-6077	-257
31	VCOM	-7965	-257	64	VDDI	-6018	-257
32	VCOM	-7906	-257	65	VDDI	-5959	-257
33	VCOM	-7847	-257	66	VDD	-5900	-257

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
67	VDD	-5841	-257	101	VDIR	-3835	-257
68	VDD	-5782	-257	102	VDIR	-3776	-257
69	VDD	-5723	-257	103	TEST_IN3	-3717	-257
70	VDD	-5664	-257	104	TEST_IN3	-3658	-257
71	VDD	-5605	-257	105	TEST_IN4	-3599	-257
72	VDD	-5546	-257	106	TEST_IN4	-3540	-257
73	VDD	-5487	-257	107	CS	-3481	-257
74	DUMMY	-5428	-257	108	CS	-3422	-257
75	VSYNC	-5369	-257	109	SDA	-3363	-257
76	VSYNC	-5310	-257	110	SDA	-3304	-257
77	HSYNC	-5251	-257	111	SCL	-3245	-257
78	HSYNC	-5192	-257	112	SCL	-3186	-257
79	DCLK	-5133	-257	113	DISP	-3127	-257
80	DCLK	-5074	-257	114	DISP	-3068	-257
81	VDPOL	-5015	-257	115	TEST_IN5	-3009	-257
82	VDPOL	-4956	-257	116	TEST_IN5	-2950	-257
83	HDPOL	-4897	-257	117	GRB	-2891	-257
84	HDPOL	-4838	-257	118	GRB	-2832	-257
85	DCLKPOL	-4779	-257	119	SYNC	-2773	-257
86	DCLKPOL	-4720	-257	120	SYNC	-2714	-257
87	SBGR	-4661	-257	121	DUMMY	-2655	-257
88	SBGR	-4602	-257	122	DUMMY	-2596	-257
89	DE	-4543	-257	123	DUMMY	-2537	-257
90	DE	-4484	-257	124	DUMMY	-2478	-257
91	DUMMY	-4425	-257	125	DGND	-2419	-257
92	DUMMY	-4366	-257	126	DR7	-2360	-257
93	DUMMY	-4307	-257	127	DR7	-2301	-257
94	DUMMY	-4248	-257	128	DR6	-2242	-257
95	PARA_SERI	-4189	-257	129	DR6	-2183	-257
96	PARA_SERI	-4130	-257	130	DR5	-2124	-257
97	EXTC	-4071	-257	131	DR5	-2065	-257
98	EXTC	-4012	-257	132	DR4	-2006	-257
99	HDIR	-3953	-257	133	DR4	-1947	-257
100	HDIR	-3894	-257	134	DR3	-1888	-257

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
135	DR3	-1829	-257	169	DB2	177	-257
136	DR2	-1770	-257	170	DB1	236	-257
137	DR2	-1711	-257	171	DB1	295	-257
138	DR1	-1652	-257	172	DB0	354	-257
139	DR1	-1593	-257	173	DB0	413	-257
140	DR0	-1534	-257	174	DUMMY	472	-257
141	DR0	-1475	-257	175	DUMMY	531	-257
142	DG7	-1416	-257	176	DUMMY	590	-257
143	DG7	-1357	-257	177	DUMMY	649	-257
144	DG6	-1298	-257	178	DUMMY	708	-257
145	DG6	-1239	-257	179	TESTOUT0	767	-257
146	DG5	-1180	-257	180	TESTOUT1	826	-257
147	DG5	-1121	-257	181	TESTOUT2	885	-257
148	DG4	-1062	-257	182	TESTOUT3	944	-257
149	DG4	-1003	-257	183	TESTOUT4	1003	-257
150	DG3	-944	-257	184	TESTOUT5	1062	-257
151	DG3	-885	-257	185	TESTOUT6	1121	-257
152	DG2	-826	-257	186	TESTOUT7	1180	-257
153	DG2	-767	-257	187	TEST_IN0	1239	-257
154	DG1	-708	-257	188	TEST_IN1	1298	-257
155	DG1	-649	-257	189	TEST_IN2	1357	-257
156	DG0	-590	-257	190	DUMMY	1416	-257
157	DG0	-531	-257	191	DUMMY	1475	-257
158	DB7	-472	-257	192	DUMMY	1534	-257
159	DB7	-413	-257	193	DUMMY	1593	-257
160	DB6	-354	-257	194	DUMMY	1652	-257
161	DB6	-295	-257	195	DUMMY	1711	-257
162	DB5	-236	-257	196	DUMMY	1770	-257
163	DB5	-177	-257	197	DUMMY	1829	-257
164	DB4	-118	-257	198	DUMMY	1888	-257
165	DB4	-59	-257	199	DUMMY	1947	-257
166	DB3	0	-257	200	DUMMY	2006	-257
167	DB3	59	-257	201	DUMMY	2065	-257
168	DB2	118	-257	202	DUMMY	2124	-257

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
203	DUMMY	2183	-257	237	DUMMY	4189	-257
204	DUMMY	2242	-257	238	DUMMY	4248	-257
205	DUMMY	2301	-257	239	DUMMY	4307	-257
206	DUMMY	2360	-257	240	DUMMY	4366	-257
207	DUMMY	2419	-257	241	DUMMY	4425	-257
208	DUMMY	2478	-257	242	AVDD	4484	-257
209	DUMMY	2537	-257	243	AVDD	4543	-257
210	DUMMY	2596	-257	244	AVDD	4602	-257
211	DUMMY	2655	-257	245	AVDD	4661	-257
212	DUMMY	2714	-257	246	AVDD	4720	-257
213	DUMMY	2773	-257	247	AVDD	4779	-257
214	DUMMY	2832	-257	248	AVDD	4838	-257
215	DUMMY	2891	-257	249	AVDD	4897	-257
216	DUMMY	2950	-257	250	PGND	4956	-257
217	AGND	3009	-257	251	PGND	5015	-257
218	AGND	3068	-257	252	PGND	5074	-257
219	AGND	3127	-257	253	PGND	5133	-257
220	AGND	3186	-257	254	PGND	5192	-257
221	AGND	3245	-257	255	PGND	5251	-257
222	AGND	3304	-257	256	PGND	5310	-257
223	AGND	3363	-257	257	PGND	5369	-257
224	AVCL	3422	-257	258	DUMMY	5428	-257
225	AVCL	3481	-257	259	DUMMY	5487	-257
226	AVCL	3540	-257	260	DUMMY	5546	-257
227	AVCL	3599	-257	261	DUMMY	5605	-257
228	AVCL	3658	-257	262	AVDD1	5664	-257
229	AVCL	3717	-257	263	AVDD1	5723	-257
230	DUMMY	3776	-257	264	AVDD1	5782	-257
231	DUMMY	3835	-257	265	AVDD1	5841	-257
232	DUMMY	3894	-257	266	AVDD1	5900	-257
233	DUMMY	3953	-257	267	AVDD1	5959	-257
234	DUMMY	4012	-257	268	TESTOUT9	6018	-257
235	DUMMY	4071	-257	269	TESTOUT9	6077	-257
236	DUMMY	4130	-257	270	TESTOUT9	6136	-257

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
271	TESTOUT9	6195	-257	305	TESTOUT13	8201	-257
272	TESTOUT9	6254	-257	306	VGH	8260	-257
273	TESTOUT9	6313	-257	307	VGH	8319	-257
274	AVCL1	6372	-257	308	VGH	8378	-257
275	AVCL1	6431	-257	309	VGH	8437	-257
276	AVCL1	6490	-257	310	VGH	8496	-257
277	AVCL1	6549	-257	311	VGH	8555	-257
278	AVCL1	6608	-257	312	TESTOUT14	8614	-257
279	AVCL1	6667	-257	313	TESTOUT14	8673	-257
280	TESTOUT11	6726	-257	314	TESTOUT14	8732	-257
281	TESTOUT11	6785	-257	315	TESTOUT14	8791	-257
282	TESTOUT11	6844	-257	316	TESTOUT14	8850	-257
283	TESTOUT11	6903	-257	317	TESTOUT14	8909	-257
284	TESTOUT11	6962	-257	318	TESTOUT15	8968	-257
285	TESTOUT11	7021	-257	319	TESTOUT15	9027	-257
286	PVDD	7080	-257	320	TESTOUT15	9086	-257
287	PVDD	7139	-257	321	TESTOUT15	9145	-257
288	PVDD	7198	-257	322	TESTOUT15	9204	-257
289	PVDD	7257	-257	323	TESTOUT15	9263	-257
290	PVDD	7316	-257	324	VGL	9322	-257
291	PVDD	7375	-257	325	VGL	9381	-257
292	PVDD	7434	-257	326	VGL	9440	-257
293	PVDD	7493	-257	327	VGL	9499	-257
294	VGSP	7552	-257	328	VGL	9558	-257
295	VGSP	7611	-257	329	VGL	9617	-257
296	VGSP	7670	-257	330	DUMMY	9676	-257
297	VGSP	7729	-257	331	DUMMY	9735	-257
298	VGSP	7788	-257	332	DUMMY	9945	127
299	VGSP	7847	-257	333	DUMMY	9930	257
300	TESTOUT13	7906	-257	334	G2	9900	127
301	TESTOUT13	7965	-257	335	G4	9885	257
302	TESTOUT13	8024	-257	336	G6	9870	127
303	TESTOUT13	8083	-257	337	G8	9855	257
304	TESTOUT13	8142	-257	338	G10	9840	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
339	G12	9825	257	373	G80	9315	257
340	G14	9810	127	374	G82	9300	127
341	G16	9795	257	375	G84	9285	257
342	G18	9780	127	376	G86	9270	127
343	G20	9765	257	377	G88	9255	257
344	G22	9750	127	378	G90	9240	127
345	G24	9735	257	379	G92	9225	257
346	G26	9720	127	380	G94	9210	127
347	G28	9705	257	381	G96	9195	257
348	G30	9690	127	382	G98	9180	127
349	G32	9675	257	383	G100	9165	257
350	G34	9660	127	384	G102	9150	127
351	G36	9645	257	385	G104	9135	257
352	G38	9630	127	386	G106	9120	127
353	G40	9615	257	387	G108	9105	257
354	G42	9600	127	388	G110	9090	127
355	G44	9585	257	389	G112	9075	257
356	G46	9570	127	390	G114	9060	127
357	G48	9555	257	391	G116	9045	257
358	G50	9540	127	392	G118	9030	127
359	G52	9525	257	393	G120	9015	257
360	G54	9510	127	394	G122	9000	127
361	G56	9495	257	395	G124	8985	257
362	G58	9480	127	396	G126	8970	127
363	G60	9465	257	397	G128	8955	257
364	G62	9450	127	398	G130	8940	127
365	G64	9435	257	399	G132	8925	257
366	G66	9420	127	400	G134	8910	127
367	G68	9405	257	401	G136	8895	257
368	G70	9390	127	402	G138	8880	127
369	G72	9375	257	403	G140	8865	257
370	G74	9360	127	404	G142	8850	127
371	G76	9345	257	405	G144	8835	257
372	G78	9330	127	406	G146	8820	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
407	G148	8805	257	441	G216	8295	257
408	G150	8790	127	442	G218	8280	127
409	G152	8775	257	443	G220	8265	257
410	G154	8760	127	444	G222	8250	127
411	G156	8745	257	445	G224	8235	257
412	G158	8730	127	446	G226	8220	127
413	G160	8715	257	447	G228	8205	257
414	G162	8700	127	448	G230	8190	127
415	G164	8685	257	449	G232	8175	257
416	G166	8670	127	450	G234	8160	127
417	G168	8655	257	451	G236	8145	257
418	G170	8640	127	452	G238	8130	127
419	G172	8625	257	453	G240	8115	257
420	G174	8610	127	454	G242	8100	127
421	G176	8595	257	455	G244	8085	257
422	G178	8580	127	456	G246	8070	127
423	G180	8565	257	457	G248	8055	257
424	G182	8550	127	458	G250	8040	127
425	G184	8535	257	459	G252	8025	257
426	G186	8520	127	460	G254	8010	127
427	G188	8505	257	461	G256	7995	257
428	G190	8490	127	462	G258	7980	127
429	G192	8475	257	463	G260	7965	257
430	G194	8460	127	464	G262	7950	127
431	G196	8445	257	465	G264	7935	257
432	G198	8430	127	466	G266	7920	127
433	G200	8415	257	467	G268	7905	257
434	G202	8400	127	468	G270	7890	127
435	G204	8385	257	469	G272	7875	257
436	G206	8370	127	470	G274	7860	127
437	G208	8355	257	471	G276	7845	257
438	G210	8340	127	472	G278	7830	127
439	G212	8325	257	473	G280	7815	257
440	G214	8310	127	474	G282	7800	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
475	G284	7785	257	509	G352	7275	257
476	G286	7770	127	510	G354	7260	127
477	G288	7755	257	511	G356	7245	257
478	G290	7740	127	512	G358	7230	127
479	G292	7725	257	513	G360	7215	257
480	G294	7710	127	514	G362	7200	127
481	G296	7695	257	515	G364	7185	257
482	G298	7680	127	516	G366	7170	127
483	G300	7665	257	517	G368	7155	257
484	G302	7650	127	518	G370	7140	127
485	G304	7635	257	519	G372	7125	257
486	G306	7620	127	520	G374	7110	127
487	G308	7605	257	521	G376	7095	257
488	G310	7590	127	522	G378	7080	127
489	G312	7575	257	523	G380	7065	257
490	G314	7560	127	524	G382	7050	127
491	G316	7545	257	525	G384	7035	257
492	G318	7530	127	526	G386	7020	127
493	G320	7515	257	527	G388	7005	257
494	G322	7500	127	528	G390	6990	127
495	G324	7485	257	529	G392	6975	257
496	G326	7470	127	530	G394	6960	127
497	G328	7455	257	531	G396	6945	257
498	G330	7440	127	532	G398	6930	127
499	G332	7425	257	533	G400	6915	257
500	G334	7410	127	534	G402	6900	127
501	G336	7395	257	535	G404	6885	257
502	G338	7380	127	536	G406	6870	127
503	G340	7365	257	537	G408	6855	257
504	G342	7350	127	538	G410	6840	127
505	G344	7335	257	539	G412	6825	257
506	G346	7320	127	540	G414	6810	127
507	G348	7305	257	541	G416	6795	257
508	G350	7290	127	542	G418	6780	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
543	G420	6765	257	577	G488	6255	257
544	G422	6750	127	578	G490	6240	127
545	G424	6735	257	579	G492	6225	257
546	G426	6720	127	580	G494	6210	127
547	G428	6705	257	581	G496	6195	257
548	G430	6690	127	582	G498	6180	127
549	G432	6675	257	583	G500	6165	257
550	G434	6660	127	584	G502	6150	127
551	G436	6645	257	585	G504	6135	257
552	G438	6630	127	586	G506	6120	127
553	G440	6615	257	587	G508	6105	257
554	G442	6600	127	588	G510	6090	127
555	G444	6585	257	589	G512	6075	257
556	G446	6570	127	590	G514	6060	127
557	G448	6555	257	591	G516	6045	257
558	G450	6540	127	592	G518	6030	127
559	G452	6525	257	593	G520	6015	257
560	G454	6510	127	594	G522	6000	127
561	G456	6495	257	595	G524	5985	257
562	G458	6480	127	596	G526	5970	127
563	G460	6465	257	597	G528	5955	257
564	G462	6450	127	598	G530	5940	127
565	G464	6435	257	599	G532	5925	257
566	G466	6420	127	600	G534	5910	127
567	G468	6405	257	601	G536	5895	257
568	G470	6390	127	602	G538	5880	127
569	G472	6375	257	603	G540	5865	257
570	G474	6360	127	604	G542	5850	127
571	G476	6345	257	605	G544	5835	257
572	G478	6330	127	606	DUMMY	5760	127
573	G480	6315	257	607	DUMMY	5745	257
574	G482	6300	127	608	DUMMY	5730	127
575	G484	6285	257	609	DUMMY	5715	257
576	G486	6270	127	610	DUMMY	5700	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
611	DUMMY	5685	257	645	S34	5115	257
612	S1	5610	127	646	S35	5100	127
613	S2	5595	257	647	S36	5085	257
614	S3	5580	127	648	S37	5070	127
615	S4	5565	257	649	S38	5055	257
616	S5	5550	127	650	S39	5040	127
617	S6	5535	257	651	S40	5025	257
618	S7	5520	127	652	S41	5010	127
619	S8	5505	257	653	S42	4995	257
620	S9	5490	127	654	S43	4980	127
621	S10	5475	257	655	S44	4965	257
622	S11	5460	127	656	S45	4950	127
623	S12	5445	257	657	S46	4935	257
624	S13	5430	127	658	S47	4920	127
625	S14	5415	257	659	S48	4905	257
626	S15	5400	127	660	S49	4890	127
627	S16	5385	257	661	S50	4875	257
628	S17	5370	127	662	S51	4860	127
629	S18	5355	257	663	S52	4845	257
630	S19	5340	127	664	S53	4830	127
631	S20	5325	257	665	S54	4815	257
632	S21	5310	127	666	S55	4800	127
633	S22	5295	257	667	S56	4785	257
634	S23	5280	127	668	S57	4770	127
635	S24	5265	257	669	S58	4755	257
636	S25	5250	127	670	S59	4740	127
637	S26	5235	257	671	S60	4725	257
638	S27	5220	127	672	S61	4710	127
639	S28	5205	257	673	S62	4695	257
640	S29	5190	127	674	S63	4680	127
641	S30	5175	257	675	S64	4665	257
642	S31	5160	127	676	S65	4650	127
643	S32	5145	257	677	S66	4635	257
644	S33	5130	127	678	S67	4620	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
679	S68	4605	257	713	S102	4095	257
680	S69	4590	127	714	S103	4080	127
681	S70	4575	257	715	S104	4065	257
682	S71	4560	127	716	S105	4050	127
683	S72	4545	257	717	S106	4035	257
684	S73	4530	127	718	S107	4020	127
685	S74	4515	257	719	S108	4005	257
686	S75	4500	127	720	S109	3990	127
687	S76	4485	257	721	S110	3975	257
688	S77	4470	127	722	S111	3960	127
689	S78	4455	257	723	S112	3945	257
690	S79	4440	127	724	S113	3930	127
691	S80	4425	257	725	S114	3915	257
692	S81	4410	127	726	S115	3900	127
693	S82	4395	257	727	S116	3885	257
694	S83	4380	127	728	S117	3870	127
695	S84	4365	257	729	S118	3855	257
696	S85	4350	127	730	S119	3840	127
697	S86	4335	257	731	S120	3825	257
698	S87	4320	127	732	S121	3810	127
699	S88	4305	257	733	S122	3795	257
700	S89	4290	127	734	S123	3780	127
701	S90	4275	257	735	S124	3765	257
702	S91	4260	127	736	S125	3750	127
703	S92	4245	257	737	S126	3735	257
704	S93	4230	127	738	S127	3720	127
705	S94	4215	257	739	S128	3705	257
706	S95	4200	127	740	S129	3690	127
707	S96	4185	257	741	S130	3675	257
708	S97	4170	127	742	S131	3660	127
709	S98	4155	257	743	S132	3645	257
710	S99	4140	127	744	S133	3630	127
711	S100	4125	257	745	S134	3615	257
712	S101	4110	127	746	S135	3600	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
747	S136	3585	257	781	S170	3075	257
748	S137	3570	127	782	S171	3060	127
749	S138	3555	257	783	S172	3045	257
750	S139	3540	127	784	S173	3030	127
751	S140	3525	257	785	S174	3015	257
752	S141	3510	127	786	S175	3000	127
753	S142	3495	257	787	S176	2985	257
754	S143	3480	127	788	S177	2970	127
755	S144	3465	257	789	S178	2955	257
756	S145	3450	127	790	S179	2940	127
757	S146	3435	257	791	S180	2925	257
758	S147	3420	127	792	S181	2910	127
759	S148	3405	257	793	S182	2895	257
760	S149	3390	127	794	S183	2880	127
761	S150	3375	257	795	S184	2865	257
762	S151	3360	127	796	S185	2850	127
763	S152	3345	257	797	S186	2835	257
764	S153	3330	127	798	S187	2820	127
765	S154	3315	257	799	S188	2805	257
766	S155	3300	127	800	S189	2790	127
767	S156	3285	257	801	S190	2775	257
768	S157	3270	127	802	S191	2760	127
769	S158	3255	257	803	S192	2745	257
770	S159	3240	127	804	S193	2730	127
771	S160	3225	257	805	S194	2715	257
772	S161	3210	127	806	S195	2700	127
773	S162	3195	257	807	S196	2685	257
774	S163	3180	127	808	S197	2670	127
775	S164	3165	257	809	S198	2655	257
776	S165	3150	127	810	S199	2640	127
777	S166	3135	257	811	S200	2625	257
778	S167	3120	127	812	S201	2610	127
779	S168	3105	257	813	S202	2595	257
780	S169	3090	127	814	S203	2580	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
815	S204	2565	257	849	S238	2055	257
816	S205	2550	127	850	S239	2040	127
817	S206	2535	257	851	S240	2025	257
818	S207	2520	127	852	S241	2010	127
819	S208	2505	257	853	S242	1995	257
820	S209	2490	127	854	S243	1980	127
821	S210	2475	257	855	S244	1965	257
822	S211	2460	127	856	S245	1950	127
823	S212	2445	257	857	S246	1935	257
824	S213	2430	127	858	S247	1920	127
825	S214	2415	257	859	S248	1905	257
826	S215	2400	127	860	S249	1890	127
827	S216	2385	257	861	S250	1875	257
828	S217	2370	127	862	S251	1860	127
829	S218	2355	257	863	S252	1845	257
830	S219	2340	127	864	S253	1830	127
831	S220	2325	257	865	S254	1815	257
832	S221	2310	127	866	S255	1800	127
833	S222	2295	257	867	S256	1785	257
834	S223	2280	127	868	S257	1770	127
835	S224	2265	257	869	S258	1755	257
836	S225	2250	127	870	S259	1740	127
837	S226	2235	257	871	S260	1725	257
838	S227	2220	127	872	S261	1710	127
839	S228	2205	257	873	S262	1695	257
840	S229	2190	127	874	S263	1680	127
841	S230	2175	257	875	S264	1665	257
842	S231	2160	127	876	S265	1650	127
843	S232	2145	257	877	S266	1635	257
844	S233	2130	127	878	S267	1620	127
845	S234	2115	257	879	S268	1605	257
846	S235	2100	127	880	S269	1590	127
847	S236	2085	257	881	S270	1575	257
848	S237	2070	127	882	S271	1560	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
883	S272	1545	257	917	S306	1035	257
884	S273	1530	127	918	S307	1020	127
885	S274	1515	257	919	S308	1005	257
886	S275	1500	127	920	S309	990	127
887	S276	1485	257	921	S310	975	257
888	S277	1470	127	922	S311	960	127
889	S278	1455	257	923	S312	945	257
890	S279	1440	127	924	S313	930	127
891	S280	1425	257	925	S314	915	257
892	S281	1410	127	926	S315	900	127
893	S282	1395	257	927	S316	885	257
894	S283	1380	127	928	S317	870	127
895	S284	1365	257	929	S318	855	257
896	S285	1350	127	930	S319	840	127
897	S286	1335	257	931	S320	825	257
898	S287	1320	127	932	S321	810	127
899	S288	1305	257	933	S322	795	257
900	S289	1290	127	934	S323	780	127
901	S290	1275	257	935	S324	765	257
902	S291	1260	127	936	S325	750	127
903	S292	1245	257	937	S326	735	257
904	S293	1230	127	938	S327	720	127
905	S294	1215	257	939	S328	705	257
906	S295	1200	127	940	S329	690	127
907	S296	1185	257	941	S330	675	257
908	S297	1170	127	942	S331	660	127
909	S298	1155	257	943	S332	645	257
910	S299	1140	127	944	S333	630	127
911	S300	1125	257	945	S334	615	257
912	S301	1110	127	946	S335	600	127
913	S302	1095	257	947	S336	585	257
914	S303	1080	127	948	S337	570	127
915	S304	1065	257	949	S338	555	257
916	S305	1050	127	950	S339	540	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
951	S340	525	257	985	S367	-105	257
952	S341	510	127	986	S368	-120	127
953	S342	495	257	987	S369	-135	257
954	S343	480	127	988	S370	-150	127
955	S344	465	257	989	S371	-165	257
956	S345	450	127	990	S372	-180	127
957	S346	435	257	991	S373	-195	257
958	S347	420	127	992	S374	-210	127
959	S348	405	257	993	S375	-225	257
960	S349	390	127	994	S376	-240	127
961	S350	375	257	995	S377	-255	257
962	S351	360	127	996	S378	-270	127
963	S352	345	257	997	S379	-285	257
964	S353	330	127	998	S380	-300	127
965	S354	315	257	999	S381	-315	257
966	S355	300	127	1000	S382	-330	127
967	S356	285	257	1001	S383	-345	257
968	S357	270	127	1002	S384	-360	127
969	S358	255	257	1003	S385	-375	257
970	S359	240	127	1004	S386	-390	127
971	S360	225	257	1005	S387	-405	257
972	DUMMY	150	127	1006	S388	-420	127
973	DUMMY	135	257	1007	S389	-435	257
974	DUMMY	120	127	1008	S390	-450	127
975	DUMMY	105	257	1009	S391	-465	257
976	DUMMY	90	127	1010	S392	-480	127
977	DUMMY	75	257	1011	S393	-495	257
978	DUMMY	60	127	1012	S394	-510	127
979	S361	-15	257	1013	S395	-525	257
980	S362	-30	127	1014	S396	-540	127
981	S363	-45	257	1015	S397	-555	257
982	S364	-60	127	1016	S398	-570	127
983	S365	-75	257	1017	S399	-585	257
984	S366	-90	127	1018	S400	-600	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1019	S401	-615	257	1053	S435	-1125	257
1020	S402	-630	127	1054	S436	-1140	127
1021	S403	-645	257	1055	S437	-1155	257
1022	S404	-660	127	1056	S438	-1170	127
1023	S405	-675	257	1057	S439	-1185	257
1024	S406	-690	127	1058	S440	-1200	127
1025	S407	-705	257	1059	S441	-1215	257
1026	S408	-720	127	1060	S442	-1230	127
1027	S409	-735	257	1061	S443	-1245	257
1028	S410	-750	127	1062	S444	-1260	127
1029	S411	-765	257	1063	S445	-1275	257
1030	S412	-780	127	1064	S446	-1290	127
1031	S413	-795	257	1065	S447	-1305	257
1032	S414	-810	127	1066	S448	-1320	127
1033	S415	-825	257	1067	S449	-1335	257
1034	S416	-840	127	1068	S450	-1350	127
1035	S417	-855	257	1069	S451	-1365	257
1036	S418	-870	127	1070	S452	-1380	127
1037	S419	-885	257	1071	S453	-1395	257
1038	S420	-900	127	1072	S454	-1410	127
1039	S421	-915	257	1073	S455	-1425	257
1040	S422	-930	127	1074	S456	-1440	127
1041	S423	-945	257	1075	S457	-1455	257
1042	S424	-960	127	1076	S458	-1470	127
1043	S425	-975	257	1077	S459	-1485	257
1044	S426	-990	127	1078	S460	-1500	127
1045	S427	-1005	257	1079	S461	-1515	257
1046	S428	-1020	127	1080	S462	-1530	127
1047	S429	-1035	257	1081	S463	-1545	257
1048	S430	-1050	127	1082	S464	-1560	127
1049	S431	-1065	257	1083	S465	-1575	257
1050	S432	-1080	127	1084	S466	-1590	127
1051	S433	-1095	257	1085	S467	-1605	257
1052	S434	-1110	127	1086	S468	-1620	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1087	S469	-1635	257	1121	S503	-2145	257
1088	S470	-1650	127	1122	S504	-2160	127
1089	S471	-1665	257	1123	S505	-2175	257
1090	S472	-1680	127	1124	S506	-2190	127
1091	S473	-1695	257	1125	S507	-2205	257
1092	S474	-1710	127	1126	S508	-2220	127
1093	S475	-1725	257	1127	S509	-2235	257
1094	S476	-1740	127	1128	S510	-2250	127
1095	S477	-1755	257	1129	S511	-2265	257
1096	S478	-1770	127	1130	S512	-2280	127
1097	S479	-1785	257	1131	S513	-2295	257
1098	S480	-1800	127	1132	S514	-2310	127
1099	S481	-1815	257	1133	S515	-2325	257
1100	S482	-1830	127	1134	S516	-2340	127
1101	S483	-1845	257	1135	S517	-2355	257
1102	S484	-1860	127	1136	S518	-2370	127
1103	S485	-1875	257	1137	S519	-2385	257
1104	S486	-1890	127	1138	S520	-2400	127
1105	S487	-1905	257	1139	S521	-2415	257
1106	S488	-1920	127	1140	S522	-2430	127
1107	S489	-1935	257	1141	S523	-2445	257
1108	S490	-1950	127	1142	S524	-2460	127
1109	S491	-1965	257	1143	S525	-2475	257
1110	S492	-1980	127	1144	S526	-2490	127
1111	S493	-1995	257	1145	S527	-2505	257
1112	S494	-2010	127	1146	S528	-2520	127
1113	S495	-2025	257	1147	S529	-2535	257
1114	S496	-2040	127	1148	S530	-2550	127
1115	S497	-2055	257	1149	S531	-2565	257
1116	S498	-2070	127	1150	S532	-2580	127
1117	S499	-2085	257	1151	S533	-2595	257
1118	S500	-2100	127	1152	S534	-2610	127
1119	S501	-2115	257	1153	S535	-2625	257
1120	S502	-2130	127	1154	S536	-2640	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1155	S537	-2655	257	1189	S571	-3165	257
1156	S538	-2670	127	1190	S572	-3180	127
1157	S539	-2685	257	1191	S573	-3195	257
1158	S540	-2700	127	1192	S574	-3210	127
1159	S541	-2715	257	1193	S575	-3225	257
1160	S542	-2730	127	1194	S576	-3240	127
1161	S543	-2745	257	1195	S577	-3255	257
1162	S544	-2760	127	1196	S578	-3270	127
1163	S545	-2775	257	1197	S579	-3285	257
1164	S546	-2790	127	1198	S580	-3300	127
1165	S547	-2805	257	1199	S581	-3315	257
1166	S548	-2820	127	1200	S582	-3330	127
1167	S549	-2835	257	1201	S583	-3345	257
1168	S550	-2850	127	1202	S584	-3360	127
1169	S551	-2865	257	1203	S585	-3375	257
1170	S552	-2880	127	1204	S586	-3390	127
1171	S553	-2895	257	1205	S587	-3405	257
1172	S554	-2910	127	1206	S588	-3420	127
1173	S555	-2925	257	1207	S589	-3435	257
1174	S556	-2940	127	1208	S590	-3450	127
1175	S557	-2955	257	1209	S591	-3465	257
1176	S558	-2970	127	1210	S592	-3480	127
1177	S559	-2985	257	1211	S593	-3495	257
1178	S560	-3000	127	1212	S594	-3510	127
1179	S561	-3015	257	1213	S595	-3525	257
1180	S562	-3030	127	1214	S596	-3540	127
1181	S563	-3045	257	1215	S597	-3555	257
1182	S564	-3060	127	1216	S598	-3570	127
1183	S565	-3075	257	1217	S599	-3585	257
1184	S566	-3090	127	1218	S600	-3600	127
1185	S567	-3105	257	1219	S601	-3615	257
1186	S568	-3120	127	1220	S602	-3630	127
1187	S569	-3135	257	1221	S603	-3645	257
1188	S570	-3150	127	1222	S604	-3660	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1223	S605	-3675	257	1257	S639	-4185	257
1224	S606	-3690	127	1258	S640	-4200	127
1225	S607	-3705	257	1259	S641	-4215	257
1226	S608	-3720	127	1260	S642	-4230	127
1227	S609	-3735	257	1261	S643	-4245	257
1228	S610	-3750	127	1262	S644	-4260	127
1229	S611	-3765	257	1263	S645	-4275	257
1230	S612	-3780	127	1264	S646	-4290	127
1231	S613	-3795	257	1265	S647	-4305	257
1232	S614	-3810	127	1266	S648	-4320	127
1233	S615	-3825	257	1267	S649	-4335	257
1234	S616	-3840	127	1268	S650	-4350	127
1235	S617	-3855	257	1269	S651	-4365	257
1236	S618	-3870	127	1270	S652	-4380	127
1237	S619	-3885	257	1271	S653	-4395	257
1238	S620	-3900	127	1272	S654	-4410	127
1239	S621	-3915	257	1273	S655	-4425	257
1240	S622	-3930	127	1274	S656	-4440	127
1241	S623	-3945	257	1275	S657	-4455	257
1242	S624	-3960	127	1276	S658	-4470	127
1243	S625	-3975	257	1277	S659	-4485	257
1244	S626	-3990	127	1278	S660	-4500	127
1245	S627	-4005	257	1279	S661	-4515	257
1246	S628	-4020	127	1280	S662	-4530	127
1247	S629	-4035	257	1281	S663	-4545	257
1248	S630	-4050	127	1282	S664	-4560	127
1249	S631	-4065	257	1283	S665	-4575	257
1250	S632	-4080	127	1284	S666	-4590	127
1251	S633	-4095	257	1285	S667	-4605	257
1252	S634	-4110	127	1286	S668	-4620	127
1253	S635	-4125	257	1287	S669	-4635	257
1254	S636	-4140	127	1288	S670	-4650	127
1255	S637	-4155	257	1289	S671	-4665	257
1256	S638	-4170	127	1290	S672	-4680	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1291	S673	-4695	257	1325	S707	-5205	257
1292	S674	-4710	127	1326	S708	-5220	127
1293	S675	-4725	257	1327	S709	-5235	257
1294	S676	-4740	127	1328	S710	-5250	127
1295	S677	-4755	257	1329	S711	-5265	257
1296	S678	-4770	127	1330	S712	-5280	127
1297	S679	-4785	257	1331	S713	-5295	257
1298	S680	-4800	127	1332	S714	-5310	127
1299	S681	-4815	257	1333	S715	-5325	257
1300	S682	-4830	127	1334	S716	-5340	127
1301	S683	-4845	257	1335	S717	-5355	257
1302	S684	-4860	127	1336	S718	-5370	127
1303	S685	-4875	257	1337	S719	-5385	257
1304	S686	-4890	127	1338	S720	-5400	127
1305	S687	-4905	257	1339	AGND	-5475	257
1306	S688	-4920	127	1340	AGND	-5490	127
1307	S689	-4935	257	1341	AGND	-5505	257
1308	S690	-4950	127	1342	AGND	-5520	127
1309	S691	-4965	257	1343	AGND	-5535	257
1310	S692	-4980	127	1344	AGND	-5550	127
1311	S693	-4995	257	1345	AGND	-5565	257
1312	S694	-5010	127	1346	AGND	-5580	127
1313	S695	-5025	257	1347	AGND	-5595	257
1314	S696	-5040	127	1348	AGND	-5610	127
1315	S697	-5055	257	1349	DUMMY	-5685	257
1316	S698	-5070	127	1350	DUMMY	-5700	127
1317	S699	-5085	257	1351	DUMMY	-5715	257
1318	S700	-5100	127	1352	DUMMY	-5730	127
1319	S701	-5115	257	1353	DUMMY	-5745	257
1320	S702	-5130	127	1354	DUMMY	-5760	127
1321	S703	-5145	257	1355	G543	-5835	257
1322	S704	-5160	127	1356	G541	-5850	127
1323	S705	-5175	257	1357	G539	-5865	257
1324	S706	-5190	127	1358	G537	-5880	127

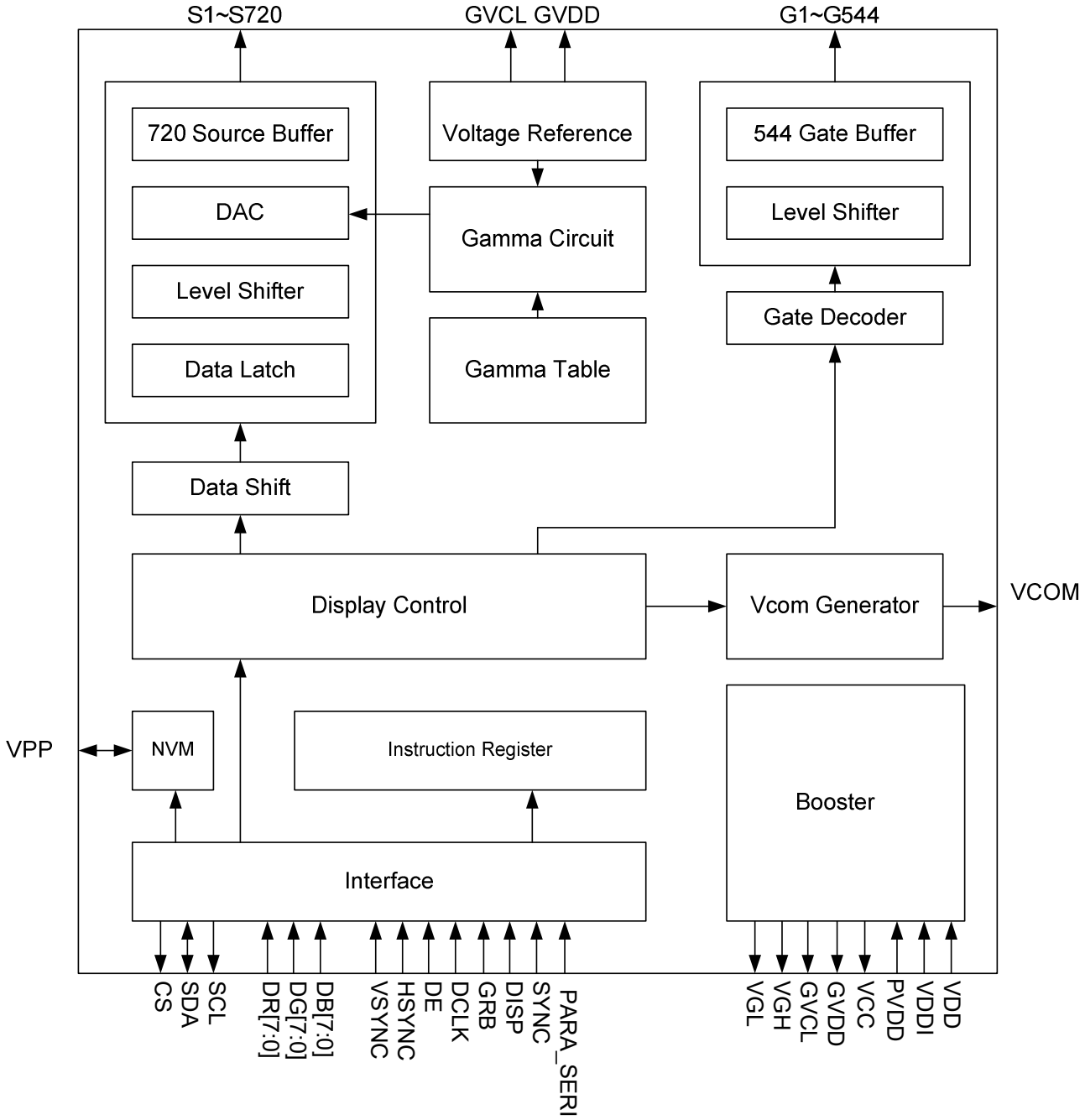
PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1359	G535	-5895	257	1393	G467	-6405	257
1360	G533	-5910	127	1394	G465	-6420	127
1361	G531	-5925	257	1395	G463	-6435	257
1362	G529	-5940	127	1396	G461	-6450	127
1363	G527	-5955	257	1397	G459	-6465	257
1364	G525	-5970	127	1398	G457	-6480	127
1365	G523	-5985	257	1399	G455	-6495	257
1366	G521	-6000	127	1400	G453	-6510	127
1367	G519	-6015	257	1401	G451	-6525	257
1368	G517	-6030	127	1402	G449	-6540	127
1369	G515	-6045	257	1403	G447	-6555	257
1370	G513	-6060	127	1404	G445	-6570	127
1371	G511	-6075	257	1405	G443	-6585	257
1372	G509	-6090	127	1406	G441	-6600	127
1373	G507	-6105	257	1407	G439	-6615	257
1374	G505	-6120	127	1408	G437	-6630	127
1375	G503	-6135	257	1409	G435	-6645	257
1376	G501	-6150	127	1410	G433	-6660	127
1377	G499	-6165	257	1411	G431	-6675	257
1378	G497	-6180	127	1412	G429	-6690	127
1379	G495	-6195	257	1413	G427	-6705	257
1380	G493	-6210	127	1414	G425	-6720	127
1381	G491	-6225	257	1415	G423	-6735	257
1382	G489	-6240	127	1416	G421	-6750	127
1383	G487	-6255	257	1417	G419	-6765	257
1384	G485	-6270	127	1418	G417	-6780	127
1385	G483	-6285	257	1419	G415	-6795	257
1386	G481	-6300	127	1420	G413	-6810	127
1387	G479	-6315	257	1421	G411	-6825	257
1388	G477	-6330	127	1422	G409	-6840	127
1389	G475	-6345	257	1423	G407	-6855	257
1390	G473	-6360	127	1424	G405	-6870	127
1391	G471	-6375	257	1425	G403	-6885	257
1392	G469	-6390	127	1426	G401	-6900	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1427	G399	-6915	257	1461	G331	-7425	257
1428	G397	-6930	127	1462	G329	-7440	127
1429	G395	-6945	257	1463	G327	-7455	257
1430	G393	-6960	127	1464	G325	-7470	127
1431	G391	-6975	257	1465	G323	-7485	257
1432	G389	-6990	127	1466	G321	-7500	127
1433	G387	-7005	257	1467	G319	-7515	257
1434	G385	-7020	127	1468	G317	-7530	127
1435	G383	-7035	257	1469	G315	-7545	257
1436	G381	-7050	127	1470	G313	-7560	127
1437	G379	-7065	257	1471	G311	-7575	257
1438	G377	-7080	127	1472	G309	-7590	127
1439	G375	-7095	257	1473	G307	-7605	257
1440	G373	-7110	127	1474	G305	-7620	127
1441	G371	-7125	257	1475	G303	-7635	257
1442	G369	-7140	127	1476	G301	-7650	127
1443	G367	-7155	257	1477	G299	-7665	257
1444	G365	-7170	127	1478	G297	-7680	127
1445	G363	-7185	257	1479	G295	-7695	257
1446	G361	-7200	127	1480	G293	-7710	127
1447	G359	-7215	257	1481	G291	-7725	257
1448	G357	-7230	127	1482	G289	-7740	127
1449	G355	-7245	257	1483	G287	-7755	257
1450	G353	-7260	127	1484	G285	-7770	127
1451	G351	-7275	257	1485	G283	-7785	257
1452	G349	-7290	127	1486	G281	-7800	127
1453	G347	-7305	257	1487	G279	-7815	257
1454	G345	-7320	127	1488	G277	-7830	127
1455	G343	-7335	257	1489	G275	-7845	257
1456	G341	-7350	127	1490	G273	-7860	127
1457	G339	-7365	257	1491	G271	-7875	257
1458	G337	-7380	127	1492	G269	-7890	127
1459	G335	-7395	257	1493	G267	-7905	257
1460	G333	-7410	127	1494	G265	-7920	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1495	G263	-7935	257	1529	G195	-8445	257
1496	G261	-7950	127	1530	G193	-8460	127
1497	G259	-7965	257	1531	G191	-8475	257
1498	G257	-7980	127	1532	G189	-8490	127
1499	G255	-7995	257	1533	G187	-8505	257
1500	G253	-8010	127	1534	G185	-8520	127
1501	G251	-8025	257	1535	G183	-8535	257
1502	G249	-8040	127	1536	G181	-8550	127
1503	G247	-8055	257	1537	G179	-8565	257
1504	G245	-8070	127	1538	G177	-8580	127
1505	G243	-8085	257	1539	G175	-8595	257
1506	G241	-8100	127	1540	G173	-8610	127
1507	G239	-8115	257	1541	G171	-8625	257
1508	G237	-8130	127	1542	G169	-8640	127
1509	G235	-8145	257	1543	G167	-8655	257
1510	G233	-8160	127	1544	G165	-8670	127
1511	G231	-8175	257	1545	G163	-8685	257
1512	G229	-8190	127	1546	G161	-8700	127
1513	G227	-8205	257	1547	G159	-8715	257
1514	G225	-8220	127	1548	G157	-8730	127
1515	G223	-8235	257	1549	G155	-8745	257
1516	G221	-8250	127	1550	G153	-8760	127
1517	G219	-8265	257	1551	G151	-8775	257
1518	G217	-8280	127	1552	G149	-8790	127
1519	G215	-8295	257	1553	G147	-8805	257
1520	G213	-8310	127	1554	G145	-8820	127
1521	G211	-8325	257	1555	G143	-8835	257
1522	G209	-8340	127	1556	G141	-8850	127
1523	G207	-8355	257	1557	G139	-8865	257
1524	G205	-8370	127	1558	G137	-8880	127
1525	G203	-8385	257	1559	G135	-8895	257
1526	G201	-8400	127	1560	G133	-8910	127
1527	G199	-8415	257	1561	G131	-8925	257
1528	G197	-8430	127	1562	G129	-8940	127

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1563	G127	-8955	257	1597	G59	-9465	257
1564	G125	-8970	127	1598	G57	-9480	127
1565	G123	-8985	257	1599	G55	-9495	257
1566	G121	-9000	127	1600	G53	-9510	127
1567	G119	-9015	257	1601	G51	-9525	257
1568	G117	-9030	127	1602	G49	-9540	127
1569	G115	-9045	257	1603	G47	-9555	257
1570	G113	-9060	127	1604	G45	-9570	127
1571	G111	-9075	257	1605	G43	-9585	257
1572	G109	-9090	127	1606	G41	-9600	127
1573	G107	-9105	257	1607	G39	-9615	257
1574	G105	-9120	127	1608	G37	-9630	127
1575	G103	-9135	257	1609	G35	-9645	257
1576	G101	-9150	127	1610	G33	-9660	127
1577	G99	-9165	257	1611	G31	-9675	257
1578	G97	-9180	127	1612	G29	-9690	127
1579	G95	-9195	257	1613	G27	-9705	257
1580	G93	-9210	127	1614	G25	-9720	127
1581	G91	-9225	257	1615	G23	-9735	257
1582	G89	-9240	127	1616	G21	-9750	127
1583	G87	-9255	257	1617	G19	-9765	257
1584	G85	-9270	127	1618	G17	-9780	127
1585	G83	-9285	257	1619	G15	-9795	257
1586	G81	-9300	127	1620	G13	-9810	127
1587	G79	-9315	257	1621	G11	-9825	257
1588	G77	-9330	127	1622	G9	-9840	127
1589	G75	-9345	257	1623	G7	-9855	257
1590	G73	-9360	127	1624	G5	-9870	127
1591	G71	-9375	257	1625	G3	-9885	257
1592	G69	-9390	127	1626	G1	-9900	127
1593	G67	-9405	257	1627	DUMMY	-9930	257
1594	G65	-9420	127	1628	DUMMY	-9945	127
1595	G63	-9435	257				
1596	G61	-9450	127				

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 Pin Function

Name	Type	Description
CS	I (VDDI)	Serial communication chip select, Internal pull high
SDA	I/O (VDDI)	Serial communication data input and output ,Internal pull low
SCL	I (VDDI)	Serial communication clock input, Internal pull low
PARA_SERI	I (VDDI)	PARA_SERI="Low", Serial 8-bit RGB input through DG0~DG7. PARA_SERI="High", Parallel 24-bit RGB input through DR0~7, DB0~DB7, DG0~DG7
DR0~DR7	I (VDDI)	8-bit digital Red data input
DG0~DG7	I (VDDI)	8-bit digital Green data input
DB0~DB7	I (VDDI)	8-bit digital Blue data input
DCLK	I (VDDI)	Clock signal; latching data at the falling edge
HSYNC	I (VDDI)	Horizontal sync signal; negative polarity When not used, user should connect it to "Low".
VSYNC	I (VDDI)	Vertical sync signal; negative polarity When not used, user should connect it to "Low".
DE	I (VDDI)	Data input enable. Active High to enable the data input When not used, user should connect it to "Low".
SYNC	I (VDDI)	No Function. User should connect it to "Low"
HDIR	I (VDDI)	Horizontal scan direction control.. HDIR = "High": Shift from left to right. HDIR = "Low" : Shift from right to left. When not used, user should connect it to "High" (Please refer to the register setting : HDIR)
VDIR	I (VDDI)	Vertical scan direction control. VDIR = "High": Shift from up to down. VDIR = "Low": Shift from down to up. When not used, user should connect it to "High"

Name	Type	Description
VDPOL	I (VDDI)	VSYNC polarity control. VDPOL=”High”, negative polarity VDPOL=Low, positive polarity When not used, user should connect it to “High” (Please refer to the register setting : VDPOL)
HDPOL	I (VDDI)	HSYNC polarity control. HDPOL=”High”, negative polarity HDPOL=”Low”, positive polarity When not used, user should connect it to “High” (Please refer to the register setting : VDPOL)
DCLKPOL	I (VDDI)	DCLK polarity control. DCLKPOL=”High”, negative polarity DCLKPOL=”Low”, positive polarity (Please refer to the register setting : DCLKPOL)
SBGR	I (VDDI)	Data R[7:0] & B[7:0] exchanged internally SBGR=”1” R[7:0]→B[7:0] B[7:0]→R[7:0] SBGR=”0” R[7:0]→R[7:0] B[7:0]→B[7:0]
GRB	I (VDDI)	Global reset. Active low, Internal pull high
DISP	I (VDDI)	Display control / standby mode selection. Internal pull low DISP = “Low” : Standby. DISP = “High” : Normal display
EXTC	I (VDDI)	Control OTP trim function. Internal pull low. The pin should be floating for enabling the function of auto-refresh register. EXTC = “High”: Enable OTP trim function and disable register refresh automatically. EXTC = “Low”: Disable OTP trim function and enable register refresh automatically.
Source / Gate Driver		
S1~S720	O	Source driver output signals
G1~G544	O	Gate driver output signals

VCOM Generator		
VCOM	O	A power supply for the TFT-LCD common electrode. Frame polarity output for VCOM.
Power Supply		
VDD	P	Power supply for digital circuit
VDDI	P	Power supply for digital interface I/O pins
PVDD	P	Power supply for charge pump circuit
DGND	P	Ground pin for digital circuit
AGND	P	Ground pin for analog circuit
PGND	P	Ground pin for charge pump circuit
VPP	P	Power input pin for NVM. When writing NVM, it needs external power supply voltage (7.5V). If not used, let this pin open.
AVDD	C	A power supply pin for generating GVDD. Connect a capacitor for stabilization. (Default NC)
AVDD1	PO	A power supply pin for generating positive Gamma reference voltage.
AVCL	C	A power supply pin for generating GVCL. Connect a capacitor for stabilization. (Default NC)
AVCL1	C	A power supply pin for generating negative Gamma reference voltage. Connect a capacitor for stabilization. (Default NC)
VCC	PO	Monitoring pin of internal digital power
VGH	C	Positive power supply for gate driver output. Connect a capacitor for stabilization. (Default NC)
VGL	C	Negative power supply for gate driver output. Connect a capacitor for stabilization. (Default NC)
GVDD	PO	A reference positive voltage of grayscale voltage generator.
GVCL	PO	A reference negative voltage of grayscale voltage generator.
Others		
VGSP	T	Internal VCOM offset monitor pin for feed-through voltage.
TESTOUT[0:7] TESTOUT9 TESTOUT11 TESTOUT13 TESTOUT14 TESTOUT15	T	Test pins for internal testing only. User should leave it open.
TEST_IN[0:4]	T	Test pins for internal testing only. Internal pull low. User should leave it open or connect it to “Low”.

TEST_IN5	T	Test pins for internal testing only. Internal pull high. User should leave it open or connect it to “High”
DUMMY	D	Dummy pin. User should leave it open.

Note..

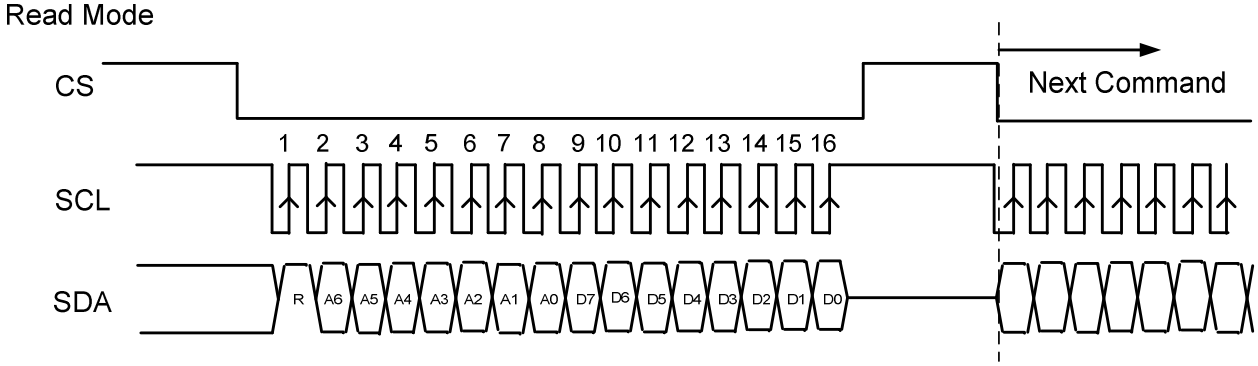
I: input, O: output, I/O: input/output, P: power input, PO: power out, D: dummy, T: test pin, C: capacitor pin

If unused pin don’t floating, the pin fix to VDDI or DGND.

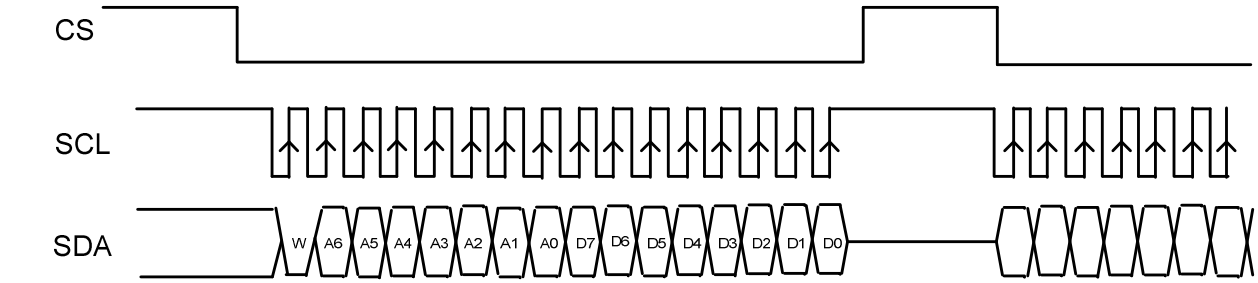
7. 3-WIRE SERIAL INTERFACE

R/W: Read/Write mode control bit.
R/W=1: Read mode
R/W=0: Write mode

Read Mode



Write Mode



a. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.

b. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.

c. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.

d. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.

e. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before the rising edge of CS pulse are valid data.

f. Serial block operates with the SCL clock

g. Serial data can be accepted in the power save mode.

h. After power on reset or GRB reset, it is required 100ms delay to begin SPI communication.

8. REGISTER LIST

8.1 Register Summary

No.	TYP	B7	B6	B5	B4	B3	B2	B1	B0	Default
R0	R/W	-	VDIR	HDIR	-	-	-	-	-	60h
R1	R/W	-	-	-	-	GRB	-	-	DISP	08h
R2	R/W	CONTRAST								40h
R3	R/W	-	SUB_CONTRAST_R							40h
R4	R/W	-	SUB_CONTRAST_B							40h
R5	R/W	BRIGHTNESS								40h
R6	R/W	-	SUB_BRIGHTNESS_R							40h
R7	R/W	-	SUB_BRIGHTNESS_B							40h
R8	R/W	H_BLANKING								2Bh
R9	R/W	VDPOL	HDPOL	V_BLANKING						CCh
R10	R/W	-	DCLKPOL	-	-	-	-	-	-	40h
COMMAND TABLE2										
No.	TYP	B7	B6	B5	B4	B3	B2	B1	B0	Default
R20	W	PKP7[4]	PKP6[4]	PKP5[4]	PKP4[4]	PKP3[4]	PKP2[4]	PKP1[4]	PKP0[4]	3Eh
R21	W	-	-	-	-	VOS0P[4]	VRF0P[4]	PKP9[4]	PKP8[4]	03h
R22	W	PKP1[3:0]				PKP0[3:0]				ECh
R23	W	PKP3[3:0]				PKP2[3:0]				97h
R24	W	PKP5[3:0]				PKP4[3:0]				45h
R25	W	PKP7[3:0]				PKP6[3:0]				87h
R26	W	PKP9[3:0]				PKP8[3:0]				50h
R27	W	VOS0P[3:0]				VRF0P[3:0]				DAh
R28	W	PKN7[4]	PKN6[4]	PKN5[4]	PKN4[4]	PKN3[4]	PKN2[4]	PKN1[4]	PKN0[4]	FEh
R29	W	-	-	-	-	VOS0N[4]	VRF0N[4]	PKN9[4]	PKN8[4]	03h
R2A	W	PKN1[3:0]				PKN0[3:0]				78h
R2B	W	PKN3[3:0]				PKN2[3:0]				30h
R2C	W	PKN5[3:0]				PKN4[3:0]				43h
R2D	W	PKN7[3:0]				PKN6[3:0]				30h
R2E	W	PKN9[3:0]				PKN8[3:0]				A5h
R2F	W	VOS0N[3:0]				VRF0N[3:0]				DAh
R40	R/W	VMF_SET	VMF[6:0]							C0h
R4A	W	0	0	0	0	0	0	OTP_EN	0	00h
R4B	W	OTP_DUMP	OTP_ADDR[6:0]							00h
R4C	W	OTP_DATA[7:0]								00h
R4D	W	OTP_CONTROL[7:0]								00h

R50	R/W	1	VRHP[6:0]							D0h
R51	R/W	0	VRHN[6:0]							51h
R52	R/W	1	VGSP [6:0]							C2h
R54	W	0	0	NO[1:0]		VGLSEL[1:0]		VGHSEL[1:0]		1Fh
R5B	W	T4[1:]		T3[1:0]		T2[1:0]		T1[1:0]		
R5D	W	1	1	1	1	1	REV	1	1	
R5E	W	1	GATE_WIDTH[2:0]			0	0	0	0	

Note:

When GRB is low, all registers reset to default values.

All commands will be executed at next VSYNC.

8.2 Command Table 1 Register description

8.2.1 R0: Direction setting

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R0	R/W	-	VDIR	HDIR	-	-	-	-	-	60h

<table>
<tr><th>Designation</th><th>Address</th><th>Description</th></tr>
<tr><td>VDIR</td><td>R0[6]</td><td>Vertical shift direction setting
VDIR=0: Shift from bottom to top, last line=L1← L2…L543←L544=first line
VDIR=1: Shift from top to bottom, first line=L1→ L2…L543→L544=last line (default)
* Hardware pin setting (VDIR) with R0[6] interaction
<table>
<tr><th>HW PIN</th><th>SW-R0[6]</th><th>Vertical shift direction</th></tr>
<tr><td>0</td><td>0</td><td>Shift from up to down</td></tr>
<tr><td>0</td><td>1</td><td>Shift from down to up</td></tr>
<tr><td>1</td><td>0</td><td>Shift from down to up</td></tr>
<tr><td>1</td><td>1</td><td>Shift from up to down</td></tr>
</table>
</td></tr>
<tr><td>HDIR</td><td>R0[5]</td><td>Horizontal shift direction setting
HDIR=0: Shift from right to left, last data=Y1← Y2…Y719←Y720=first data
HDIR=1: Shift from left to right, first data=Y1→ Y2…Y719→Y720=last data (default)
* Hardware pin setting (HDIR) with R0[5] interaction
<table>
<tr><th>HW PIN</th><th>SW-R0[5]</th><th>Horizontal shift direction</th></tr>
<tr><td>0</td><td>0</td><td>Shift from left to right</td></tr>
<tr><td>0</td><td>1</td><td>Shift from right to left</td></tr>
<tr><td>1</td><td>0</td><td>Shift from right to left</td></tr>
<tr><td>1</td><td>1</td><td>Shift from left to right</td></tr>
</table>
</td></tr>
</table>

8.2.2 R1: GRB、DISP

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R1	R/W	-	-	-	-	GRB	-	-	DISP	08h

Designation	Address	Description
GRB	R1[3]	Register reset setting GRB=0: Reset all registers to default value GRB=1: Normal operation(default)
DISP	R1[0]	Standby(power saving) mode setting

		DISP=0: Standby, timing control, DAC, and DC/DC converter are off, and register data should be kept (default) DISP=1: Normal operation with power on/off sequence

8.2.3 R2: CONSTRAST

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R2	R/W	CONTRAST								40h

Designation	Address	Description
CONTRAST	R2[7:0]	RGB contrast level setting, the gain changes (1/64)/ bit CONTRAST=00h: contrast gain=0 CONTRAST=40h: contrast gain=1 (default) CONTRAST=FFh: contrast gain=3.984

8.2.4 R3: SUB-CONTRAST_R

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R3	R/W	-	SUB_CONTRAST_R							40h

Designation	Address	Description
SUB_CONTRAST_R	R3[6:0]	R sub-contrast level setting, the gain changes (1/256) / bit Sub_CONTRAST_R=00h: contrast gain=0.75 Sub_CONTRAST_R=40h: contrast gain=1 (default) Sub_CONTRAST_R=7Fh: contrast gain=1.246

8.2.5 R4: SUB-CONTRAST_B

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R4	R/W	-	SUB_CONTRAST_B							40h

Designation	Address	Description
SUB_CONTRAST_B	R4[6:0]	B sub-contrast level setting, the gain changes (1/256) / bit Sub_CONTRAST_B=00h: contrast gain=0.75 Sub_CONTRAST_B=40h: contrast gain=1 (default) Sub_CONTRAST_B=7Fh: contrast gain=1.246

8.2.6 R5: BRIGHTNESS

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R5	R/W	BRIGHTNESS								40h

Designation	Address	Description
BRIGHTNESS	R5[7:0]	RGB brightness level setting, the accuracy 1 step/ bit. BRIGHTNESS =00h: -64 BRIGHTNESS =40h: 0 (default) BRIGHTNESS =FFh: +191

8.2.7 R6: SUB-BRIGHTNESS_R

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R6	R/W	-	SUB_BRIGHTNESS_R							40h

Designation	Address	Description
SUB_BRIGHTNESS_R	R6[6:0]	R sub-brightness level setting, the accuracy 1 step / bit. SUB_BRIGHTNESS_R=00h: -64 SUB_BRIGHTNESS_R=40h: 0 (default) SUB_BRIGHTNESS_R=7Fh: +63

8.2.8 R7: SUB-BRIGHTNESS_B

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R7	R/W	-	SUB_BRIGHTNESS_B							40h

Designation	Address	Description
SUB_BRIGHTNESS_B	R7[6:0]	B sub-brightness level setting, the accuracy 1 step / bit. SUB_BRIGHTNESS_B=00h: -64 SUB_BRIGHTNESS_B=40h: 0 (default) SUB_BRIGHTNESS_B=7Fh: +63

8.2.9 R8: H_BLANKING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R8	R/W	H_BLANKING								2Bh

Designation	Address	Description
H_BLANKING	R8[7:0]	H back porch setting (unit: DCLK)

		H_BLANKING=00h: 0 H_BLANKING=2Bh: 43(default) H_BLANKING=FFh: 255

8.2.10 R9: VDPOL、HDPOL、V_BLANKING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R9	R/W	VDPOL	HDPOL	V_BLANKING						CCh

Designation	Address	Description
VDPOL	R9[7]	VSYNC polarity select VDPOL=0: Positive polarity VDPOL=1: Negative polarity (default) * Hardware pin setting (VDPOL) with R9[7] interaction
HDPOL	R9[6]	HSYNC polarity select HDPOL=0: Positive polarity HDPOL=1: Negative polarity (default) * Hardware pin setting (HDPOL) with R9[6] interaction
V_BLANKING	R9[5:0]	V back porch setting (unit: H) V_BLANKING=00h: 0 V_BLANKING=0Ch: 12(default) V_BLANKING=3Fh: 63

HW PIN	SW-R9[7]	VDPOL Polarity
0	0	Negative
0	1	Positive
1	0	Positive
1	1	Negative

HW PIN	SW-R9[6]	HDPOL Polarity
0	0	Negative
0	1	Positive
1	0	Positive
1	1	Negative

8.2.11 R10: DCLKPOL

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R10	R/W	-	DCLKPOL	-	-	-	-	-	-	40h

Designation	Address	Description
DCLKPOL	R10[6]	DCLK Polarity Select DCLKPOL=0: Positive Polarity DCLKPOL=1: Negative Polarity(default) * Hardware pin setting (DCLKPOL) with R10[6] interaction

HW PIN	SW-R10[6]	DCLKPOL Polarity
0	0	Negative
0	1	Positive
1	0	Positive
1	1	Negative

8.3 Command Table 2 Register description

8.3.1 R7F: COMMAND2_ENABLE

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R7F	R/W	-	-	-	-	-	-	-	CMD2_EN	00h

Designation	Address	Description
CMD2_EN	R7F[0]	Command 1 table and Command 2 table switch CMD2_EN = 0: Command 1 table enable (default) CMD2_EN = 1: Command 2 table enable

8.3.2 R20~R2F: GAMMA SELECTION

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R20	W	PKP7[4]	PKP6[4]	PKP5[4]	PKP4[4]	PKP3[4]	PKP2[4]	PKP1[4]	PKP0[4]	3Eh
R21	W	-	-	-	-	VOS0P[4]	VRF0P[4]	PKP9[4]	PKP8[4]	03h
R22	W	PKP1[3:0]				PKP0[3:0]				ECh
R23	W	PKP3[3:0]				PKP2[3:0]				97h
R24	W	PKP5[3:0]				PKP4[3:0]				45h
R25	W	PKP7[3:0]				PKP6[3:0]				87h
R26	W	PKP9[3:0]				PKP8[3:0]				50h
R27	W	VOS0P[3:0]				VRF0P[3:0]				DAh
R28	W	PKN7[4]	PKN6[4]	PKN5[4]	PKN4[4]	PKN3[4]	PKN2[4]	PKN1[4]	PKN0[4]	FEh
R29	W	-	-	-	-	VOS0N[4]	VRF0N[4]	PKN9[4]	PKN8[4]	03h
R2A	W	PKN1[3:0]				PKN0[3:0]				78h
R2B	W	PKN3[3:0]				PKN2[3:0]				30h
R2C	W	PKN5[3:0]				PKN4[3:0]				43h
R2D	W	PKN7[3:0]				PKN6[3:0]				30h
R2E	W	PKN9[3:0]				PKN8[3:0]				A5h
R2F	W	VOS0N[3:0]				VRF0N[3:0]				DAh

Designation	Address	Description
VRF0P[4:0]	R21[2], R27[3:0]	V8 Gamma selection
VRF0N[4:0]	R29[2], R2F[3:0]	
PKP0[4:0]	R20[0], R22[3:0]	V16 Gamma selection
PKN0[4:0]	R28[0], R2A[3:0]	
PKP1[4:0]	R20[1], R22[7:4]	V32 Gamma selection
PKN1[4:0]	R28[1], R2A[7:4]	
PKP2[4:0]	R20[2], R23[3:0]	V48 Gamma selection

PKN2[4:0]	R28[2], R2B[3:0]	
PKP3[4:0]	R20[3], R23[7:4]	V80 Gamma selection
PKN3[4:0]	R28[3], R2B[7:4]	
PKP4[4:0]	R20[4], R24[3:0]	V112 Gamma selection
PKPN4[4:0]	R28[4], R2C[3:0]	
PKP5[4:0]	R20[5], R24[7:4]	V144 Gamma selection
PKN5[4:0]	R28[5], R2C[7:4]	
PKP6[4:0]	R20[6], R25[3:0]	V176 Gamma selection
PKN6[4:0]	R28[6], R2D[3:0]	
PKP7[4:0]	R20[7], R25[7:4]	V208 Gamma selection
PKN7[4:0]	R28[6], R2D[7:4]	
PKP8[4:0]	R21[0], R26[3:0]	V224 Gamma selection
PKN8[4:0]	R29[0], R2E[3:0]	
PKP9[4:0]	R21[1], R26[7:4]	V240 Gamma selection
PKN9[4:0]	R29[1], R2E[7:4]	
VOS0P[4:0]	R21[3], R27[7:4]	V248 Gamma selection
VOS0N[4:0]	R29[3], R2F[7:4]	

8.3.3 R50: GVDD SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R50	R/W	1	1	VRHP[5:0]						D0h

Designation	Address	Description
VRHP[5:0]	R50[5:0]	GVDD level adjustment

VRHP[5:0]	GVDD	VRHP[5:0]	GVDD	VRHP[5:0]	GVDD	VRHP[5:0]	GVDD
000000	5.9680	010000	5.7120	100000	5.4560	110000	5.2000
000001	5.9520	010001	5.6960	100001	5.4400	110001	5.1840
000010	5.9360	010010	5.6800	100010	5.4240	110010	5.1680
000011	5.9200	010011	5.6640	100011	5.4080	110011	5.1520
000100	5.9040	010100	5.6480	100100	5.3920	110100	5.1360
000101	5.8880	010101	5.6320	100101	5.3760	110101	5.1200
000110	5.8720	010110	5.6160	100110	5.3600	110110	5.1040
000111	5.8560	010111	5.6000	100111	5.3440	110111	5.0880
001000	5.8400	011000	5.5840	101000	5.3280	111000	5.0720
001001	5.8240	011001	5.5680	101001	5.3120	111001	5.0560
001010	5.8080	011010	5.5520	101010	5.2960	111010	5.0400
001011	5.7920	011011	5.5360	101011	5.2800	111011	5.0240
001100	5.7760	011100	5.5200	101100	5.2640	111100	5.0080
001101	5.7600	011101	5.5040	101101	5.2480	111101	4.9920
001110	5.7440	011110	5.4880	101110	5.2320	111110	4.9760
001111	5.7280	011111	5.4720	101111	5.2160	111111	4.9600

8.3.4 R51: GVCL SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R51	R/W	0	VRHN[6:0]							51h

Designation	Address	Description
VRHN[6:0]	R51[6:0]	GVCL level adjustment

VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL
0100000	-4.4800	0111000	-4.0960	1010000	-3.7120	1101000	-3.3280
0100001	-4.4640	0111001	-4.0800	1010001	-3.6960	1101001	-3.3120
0100010	-4.448	0111010	-4.0640	1010010	-3.6800	1101010	-3.2960
0100011	-4.4320	0111011	-4.0480	1010011	-3.6640	1101011	-3.2800
0100100	-4.4160	0111100	-4.0320	1010100	-3.6480	1101100	-3.2640

0100101	-4.4000	0111101	-4.0160	1010101	-3.6320	1101101	-3.2480
0100110	-4.3840	0111110	-4.0000	1010110	-3.6160	1101110	-3.2320
0100111	-4.3680	0111111	-3.9840	1010111	-3.6000	1101111	-3.2160
0101000	-4.3520	1000000	-3.9680	1011000	-3.5840	1110000	-3.2000
0101001	-4.3360	1000001	-3.9520	1011001	-3.5680	1110001	-3.1840
0101010	-4.3200	1000010	-3.9360	1011010	-3.5520	1110010	-3.1680
0101011	-4.3040	1000011	-3.9200	1011011	-3.5360	1110011	-3.1520
0101100	-4.2880	1000100	-3.9040	1011100	-3.5200	1110100	-3.1360
0101101	-4.2720	1000101	-3.8880	1011101	-3.5040	1110101	-3.1200
0101110	-4.2560	1000110	-3.8720	1011110	-3.4880	1110110	-3.1040
0101111	-4.2400	1000111	-3.8560	1011111	-3.4720	1110111	-3.0880
0110000	-4.2240	1001000	-3.8400	1100000	-3.4560	1111000	-3.0720
0110001	-4.2080	1001001	-3.8240	1100001	-3.4400	1111001	-3.0560
0110010	-4.1920	1001010	-3.8080	1100010	-3.4240	1111010	-3.0400
0110011	-4.1760	1001011	-3.7920	1100011	-3.4080	1111011	-3.0240
0110100	-4.1600	1001100	-3.7760	1100100	-3.3920	1111100	-3.0080
0110101	-4.1440	1001101	-3.7600	1100101	-3.3760	1111101	-2.9920
0110110	-4.1280	1001110	-3.7440	1100110	-3.3600	1111110	-2.9760
0110111	-4.1120	1001111	-3.7280	1100111	-3.3440	1111111	-2.9600

8.3.5 R52: VGSP SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R52	R/W	1	VGSP[6:0]							C2h

Designation	Address	Description
VGSP[6:0]	R52[6:0]	VGSP level adjustment

VGSP[6:0]	VGSP	VGSP[6:0]	VGSP	VGSP[6:0]	VGSP	VGSP[6:0]	VGSP
0100000	1.5520	0111000	1.1680	1010000	0.7840	1101000	0.4000
0100001	1.5360	0111001	1.1520	1010001	0.7680	1101001	0.3840
0100010	1.5200	0111010	1.1360	1010010	0.7520	1101010	0.3680
0100011	1.5040	0111011	1.1200	1010011	0.7360	1101011	0.3520
0100100	1.4880	0111100	1.1040	1010100	0.7200	1101100	0.3360
0100101	1.4720	0111101	1.0880	1010101	0.7040	1101101	0.3200
0100110	1.4560	0111110	1.0720	1010110	0.6880	1101110	0.3040
0100111	1.4400	0111111	1.0560	1010111	0.6720	1101111	0.2880
0101000	1.4240	1000000	1.0400	1011000	0.6560	1110000	0.2720
0101001	1.4080	1000001	1.0240	1011001	0.6400	1110001	0.2560

0101010	1.3920	1000010	1.0080	1011010	0.6240	1110010	0.2400
0101011	1.3760	1000011	0.9920	1011011	0.6080	1110011	0.2240
0101100	1.3600	1000100	0.9760	1011100	0.5920	1110100	0.2080
0101101	1.3440	1000101	0.9600	1011101	0.5760	1110101	0.1920
0101110	1.3280	1000110	0.9440	1011110	0.5600	1110110	0.1760
0101111	1.3120	1000111	0.9280	1011111	0.5440	1110111	0.1600
0110000	1.2960	1001000	0.9120	1100000	0.5280	1111000	0.1440
0110001	1.2800	1001001	0.8960	1100001	0.5120	1111001	0.1280
0110010	1.2640	1001010	0.8800	1100010	0.4960	1111010	0.1120
0110011	1.2480	1001011	0.8640	1100011	0.4800	1111011	0.0960
0110100	1.2320	1001100	0.8480	1100100	0.4640	1111100	0.0800
0110101	1.2160	1001101	0.8320	1100101	0.4480	1111101	0.0640
0110110	1.2000	1001110	0.8160	1100110	0.4320	1111110	0.0480
0110111	1.1840	1001111	0.8000	1100111	0.4160	1111111	0.0320

8.3.6 R54: VGH, VGL SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R54	R/W	0	0	NO[1:0]		VGLSEL[1:0]		VGSEL[1:0]		1Fh

Designation	Address	Description
NO[1:0]	R54[5:4]	Gate non-overlap adjustment NO[1:0] / Non-overlap (DCLK) 00 / 20 01 / 30 10 / 40 11 / 50
VGLSEL[1:0]	R54[3:2]	VGL level adjustment VGLSEL[1:0] / VGL(V) 00 / -7 01 / -8 10 / -11.5 11 / -10
VGHSEL[1:0]	R54[1:0]	VGH level adjustment VGHSEL[1:0] / VGH(V) 00 / 13 01 / 15

		10	17.5
		11	15

8.3.7 R55: SOURCE OP-AMP POWER SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R55	W	1	0	1	0	1	SOURCE_AP[2:0]			

Designation	Address	Description
SOURCE_AP [2:0]	R55[2:0]	Source driving capability selection. When setting OP capability to a higher level, the source output current will be increased.

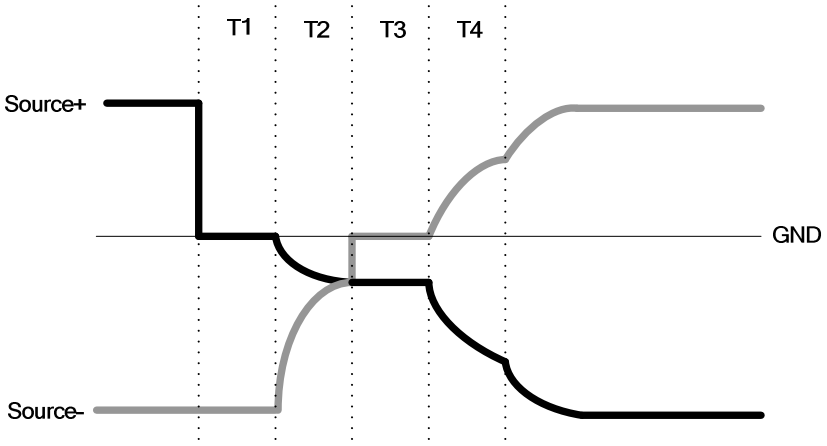
SOURCE_AP[2:0]	Source Op-amp power
000	Level1 (Least)
001	Level2 (Small)
010	Level3 (Small to Medium)
011	Level4 (Medium)
100	Level5 (Medium to Large)
101	Level6 (Large)
110	Level7 (Large to Maximum)
111	Level8 (Maximum)

Note: Setting SOURCE_AP level for turning source output current, and adjusting for a better display quality.

8.3.8 R5B: SOURCE EQUALIZE TIME SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R5B	R/W	T4[1:0]		T3[1:0]		T2[1:0]		T1[1:0]		

Designation	Address	Description
T4[1:0]	R5B[7:6]	Source equalizing time diagram:
T3[1:0]	R5B[5:4]	
T2[1:0]	R5B[3:2]	
T1[1:0]	R5B[1:0]	



Source equalizing T4 time adjustment

T4[1:0]	T4(DCLK)
00	0
01	5
10	10
11	15

Source equalizing T3 time adjustment

T3[1:0]	T3(DCLK)
00	0
01	5
10	10
11	15

Source equalizing T2 time adjustment

T2[1:0]	T2(DCLK)
00	0
01	5
10	10
11	15

Source equalizing T1 time adjustment

T1[1:0]	T1(DCLK)
00	0
01	5
10	10
11	15

Note: By the different panel condition, Adjusting source equalizing time for a better display quality.

8.3.9 R5D: LC TYPE SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R5D	W	1	1	1	1	1	REV	1	1	

Designation	Address	Description
REV	R5D[2]	Define LC type of panel selection

REV	Panel type
0	Normally White
1	Normally Black

8.3.10 R5E: GATE WIDTH SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R5E	W	1	GATE_WIDTH[2:0]			0	0	0	0	

Designation	Address	Description
GATE_WIDTH [2:0]	R5E[6:4]	Gate width adjusting

GATE_WIDTH[2:0]	Gate(n) width (DCLK)
000	207
001	223
010	239
011	255
100	271
101	287
110	303
111	319

Gate width formula:

Gate(n+1) = Th (HSYNC period time) – Nonoverlap time – Gate(n) width

Example: Th=531DCLK , Non-overlap=30DCLK

GATE_WIDTH[2:0]	G(n) width (DCLK)	G(n+1) width (DCLK)
000	207	294
001	223	278
010	239	262
011	255	246
100	271	230
101	287	214
110	303	198
111	319	182

8.3.11 R40: VMF OFFSET SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R40	R/W	VMF_SET	VMF[6:0]							C0h

Designation	Address	Description
VMF_SET	R40[7]	VMF_SET=0: Enable VMF setting function
VMF[6:0]	R40[6:0]	VMF setting adjustment

VMF[6]	VMF[5:0]	VGSP	GVDD	GVCL
0	000000	VCOMS[6:0]+64d	VRHP[6:0]+64d	VRHN[6:0]+64d
0	000001	VCOMS[6:0]+63d	VRHP[6:0]+63d	VRHN[6:0]+63d
0	000010	VCOMS[6:0]+62d	VRHP[6:0]+62d	VRHN[6:0]+62d
0	|	|	|	|
0	111110	VCOMS[6:0]+2d	VRHP[6:0]+2d	VRHN[6:0]+2d
0	111111	VCOMS[6:0]+1d	VRHP[6:0]+1d	VRHN[6:0]+1d
1	000000	VCOMS[6:0]	VRHP[6:0]	VRHN[6:0]
1	000001	VCOMS[6:0]-1d	VRHP[6:0]-1d	VRHN[6:0]-1d
1	000010	VCOMS[6:0]-2d	VRHP[6:0]-2d	VRHN[6:0]-2d
1	|	|	|	|
1	111110	VCOMS[6:0]-62d	VRHP[6:0]-62d	VRHN[6:0]-62d
1	111111	VCOMS[6:0]-63d	VRHP[6:0]-63d	VRHN[6:0]-63d

Note: d=16mV

8.3.12 R4A: OTP FUNCTION CONTROL

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R4A	W	0	0	0	0	0	0	OTP_EN	0	00h

Designation	Address	Description
CMD2_EN	R4A[1]	OTP Function switch OTP_EN = 0:Disable OTP Function (default) OTP_EN = 1: Enable OTP Function

8.3.13 R4B: OTP ADDRESS SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R4B	W	0	OTP_ADDR[6:0]							00h

Designation	Address	Description

OTP_ADDR[6:0]	R4B[6:0]	OTP_ADDR[6:0]=0x01: VCOM Offset register OTP address.

8.3.14 R4C: OTP DATA SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	default
R4C	W/R	OTP_DATA[7:0]								00h

Designation	Address	Description
OTP_DATA[7:0]	R4C[7:0]	OTP DATA

8.3.15 R4D: OTP CONTROL

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	default
R4D	W	OTP_CONTROL[7:0]								00h

Designation	Address	Description
OTP_CONTROL[7:0]	R4D[7:0]	OTP_CONTROL[7:0]=0xCA: Write OTP

9. ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	VDD	- 0.3 ~ +4.6	V
IO Supply Voltage	VDDI	- 0.3 ~ +4.6	V
Charge Pump Supply Voltage	PVDD	- 0.3 ~ +4.6	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Output Voltage Range	VO	-0.3 ~ VDDI + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Note:

1. That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/AC Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.

2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

3. VIN should be less than or equal to 3.6V. (VIN ≤ 3.6V)

9.2 DC Characteristics

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

9.2.1 Recommended Operating Range

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VDD	3.0	3.3	3.6	V	
IO Supply Voltage	VDDI	1.65	-	VDD	V	
Charge Pump Supply Voltage	PVDD	3.0	3.3	3.6	V	
NVM Supply Voltage	VPP	7.4	7.5	7.6	V	

9.2.2 DC Characteristics for Digital Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic-High Input Voltage	Vih	0.7VDDI	-	VDDI	V	
Logic-Low Input Voltage	Vil	DGND	-	0.3VDDI	V	
Logic-High Output Voltage	Voh	VDDI-0.4	-	VDDI	V	
Logic-Low Output Voltage	Vol	DGND	-	DGND+0.4	V	

9.2.3 DC Characteristics for Analog Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Positive High-voltage power	VGH	13	15	17.5	V	
Negative High-voltage power	VGL	-11.5	-10	-7	V	
Output Voltage Deviation	Vod		±35	±45	mV	
Standby Current	Isc			50	uA	
Operation Current	Ioc		20		mA	No Load@ FR=60Hz

9.3 AC Characteristics

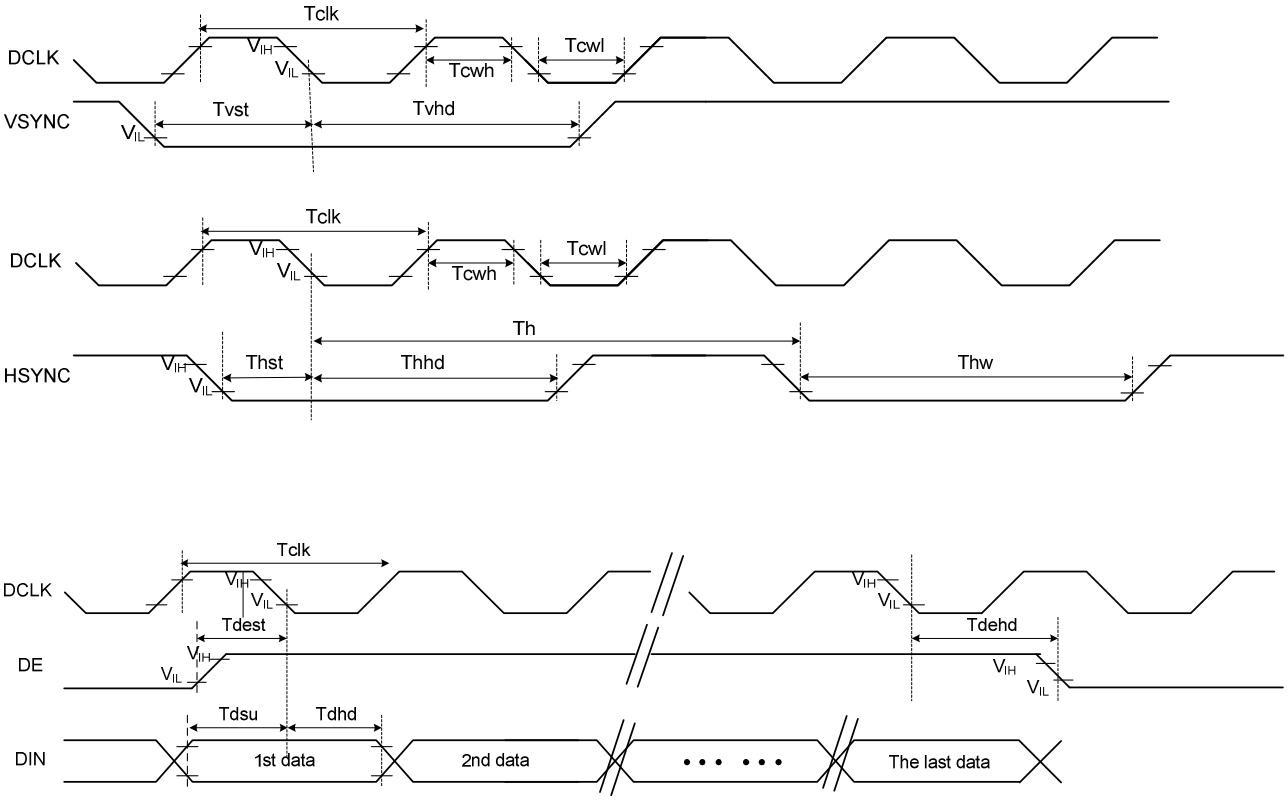
AC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
System operation timing						
VDD power source slew time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB pulse width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
Input/ Output timing						
CLK pulse duty	Tcw	40	50	60	%	
Hsync width	Thw	1	-	-	DCLK	
Hsync period	Th	55	60	65	us	
Vsync setup time	Tvst	12	-	-	ns	
Vsync hold time	Tvhd	12	-	-	ns	
Hsync setup time	Thst	12	-	-	ns	
Hsync hold time	Thhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	
Data hold time	Tdhd	12	-	-	ns	
DE setup time	Tdest	10	-	-	ns	
DE setup time	Tdehd	10	-	-	ns	
SD output stable time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD output rise and fall time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF
3-wire serial communication						
Delay between CSB and VSYNC	Tcv	1			us	
CS input setup time	Ts0	50			ns	
Serial data input setup time	Ts1	50			ns	
CS input hold time	Th0	50			ns	
Serial data input hold time	Th1	50			ns	

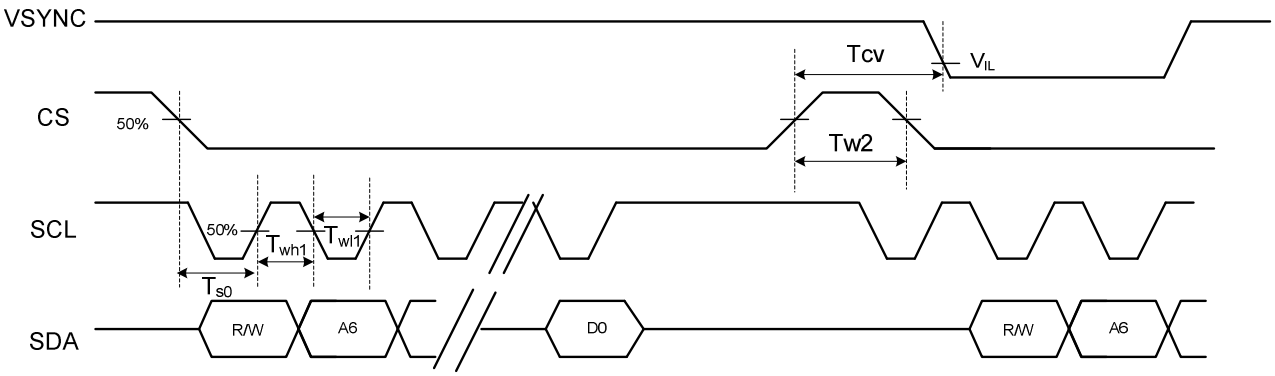
SCL pulse high width	Twh1	50			ns	
SCL pulse low width	Twl1	50			ns	
CS pulse high width	Tw2	400			ns	

9.4 AC Timing Diagram

9.4.1 Clock and Data Input Timing Diagram



9.4.2 3-Wire Communication Timing Diagram



10. INPUT DATA FORMAT

10.1 RGB Input Timing Table

RGB input timing table (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

10.1.1 Parallel 24-bit RGB Timing Table

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	8	9	12	MHz	
DCLK Period		Tclk	83	111	125	ns	
HSYNC	Period Time	Th	485	531	598	DCLK	
	Display Period	Thdisp		480		DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	75	DCLK	
VSYNC	Period Time	Tv	276	292	321	H	
	Display Period	Tvdisp		272		H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	37	H	

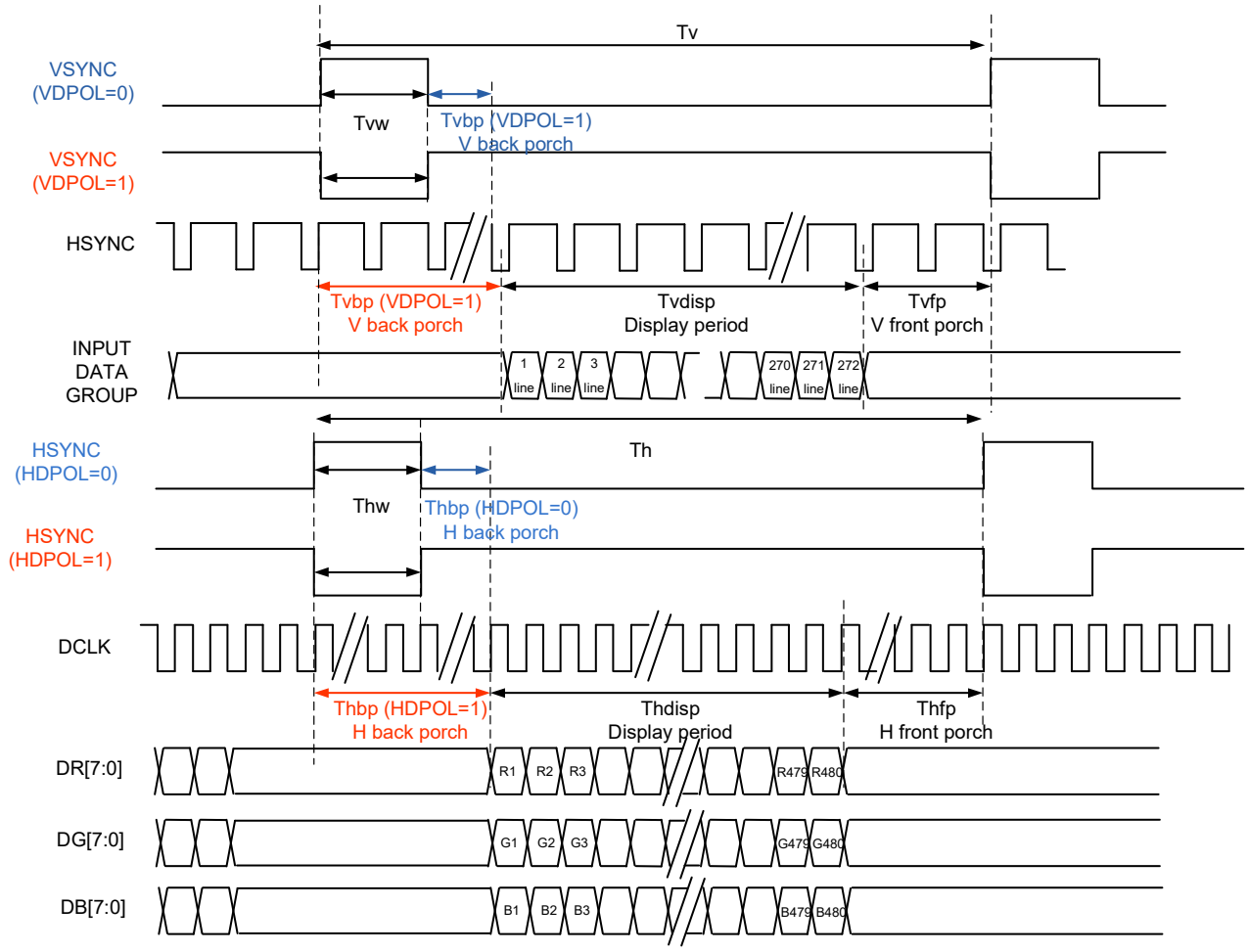
Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

10.1.2 Serial 8-bit RGB Timing Table

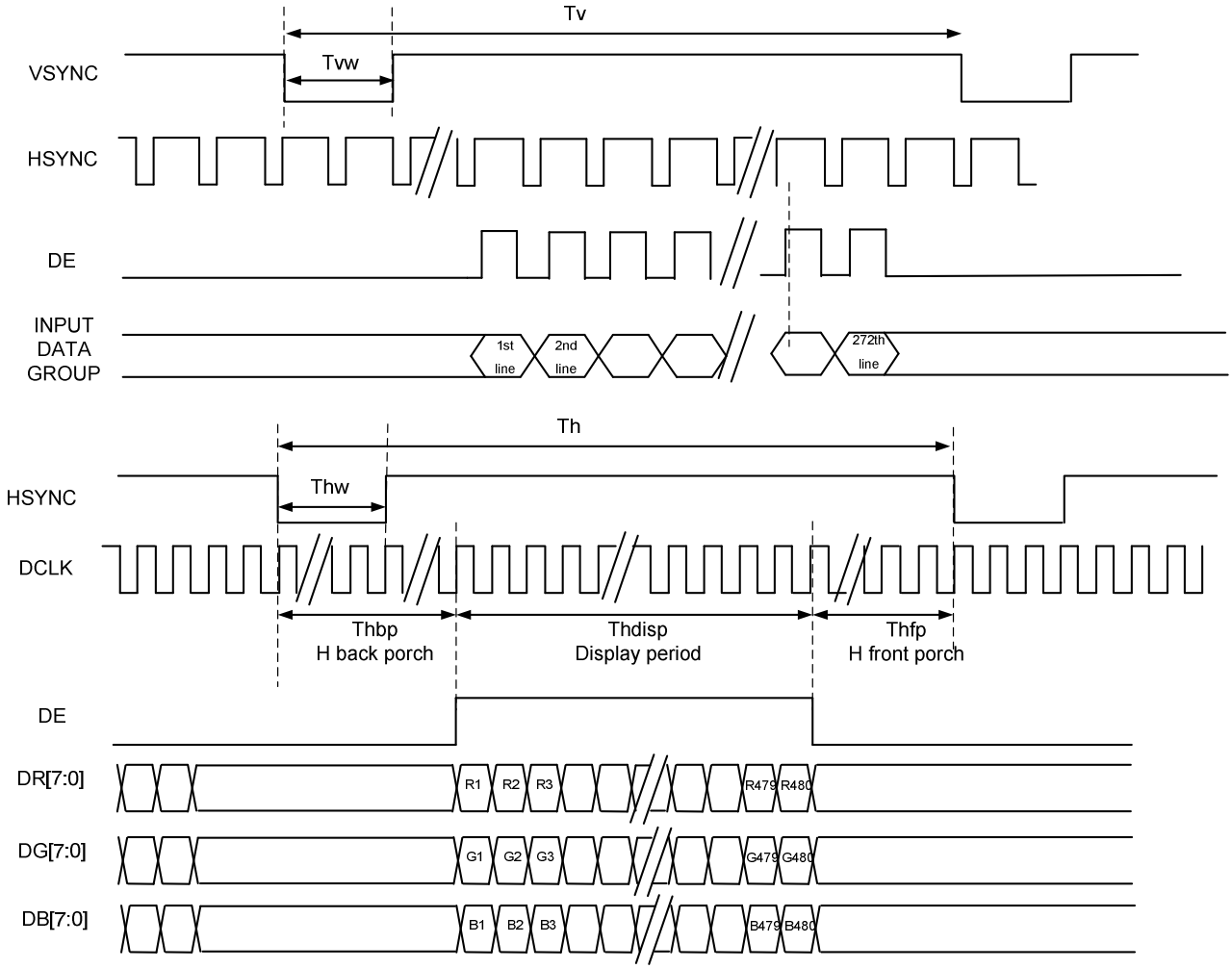
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	24	27	30	MHz	
DCLK Period		Tclk	33	37	42	ns	
HSYNC	Period Time	Th	1445	1491	1558	DCLK	
	Display Period	Thdisp		1440		DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	75	DCLK	
VSYNC	Period Time	Tv	276	292		H	
	Display Period	Tvdisp		272		H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	37	H	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

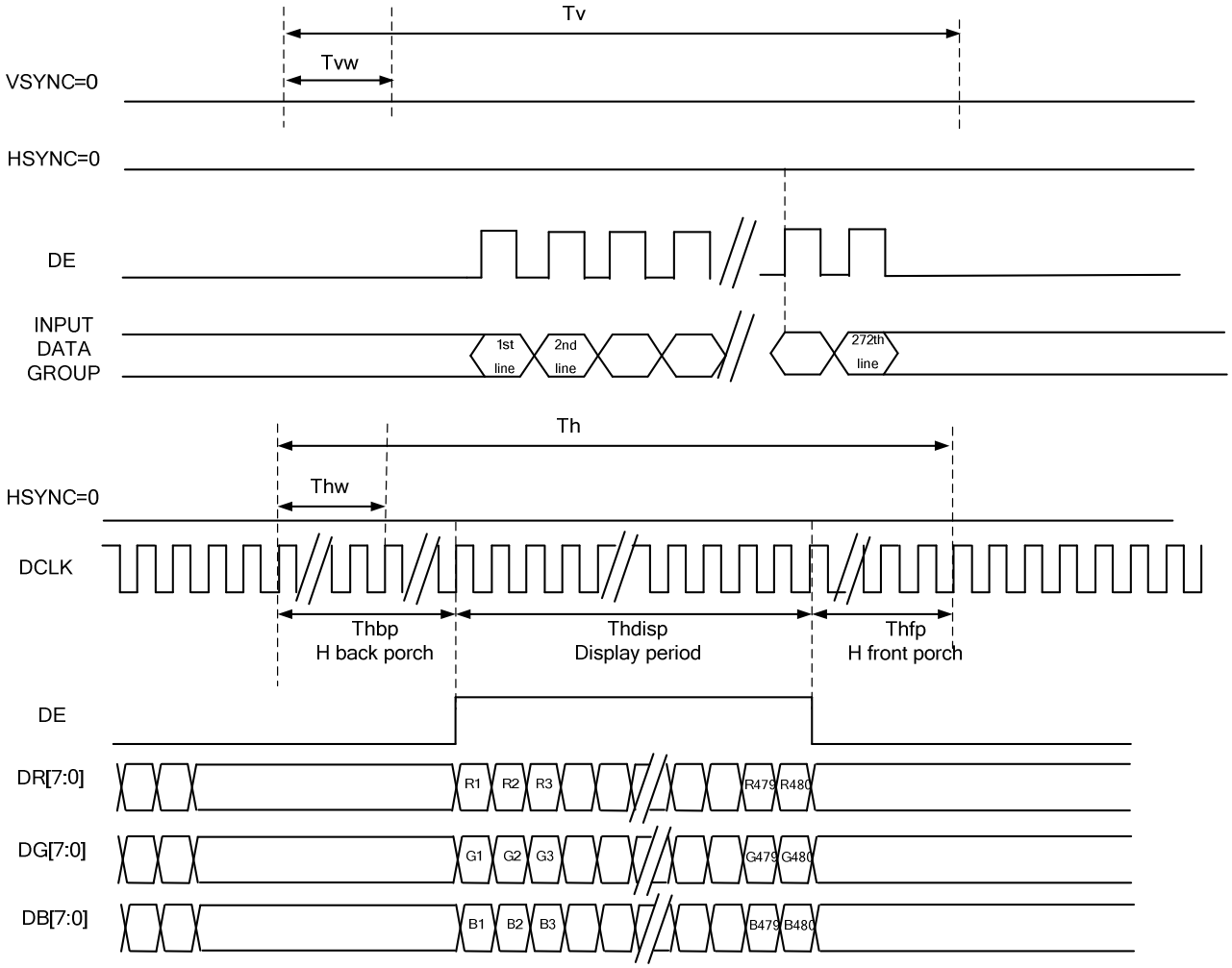
10.2 SYNC Mode Timing Diagram



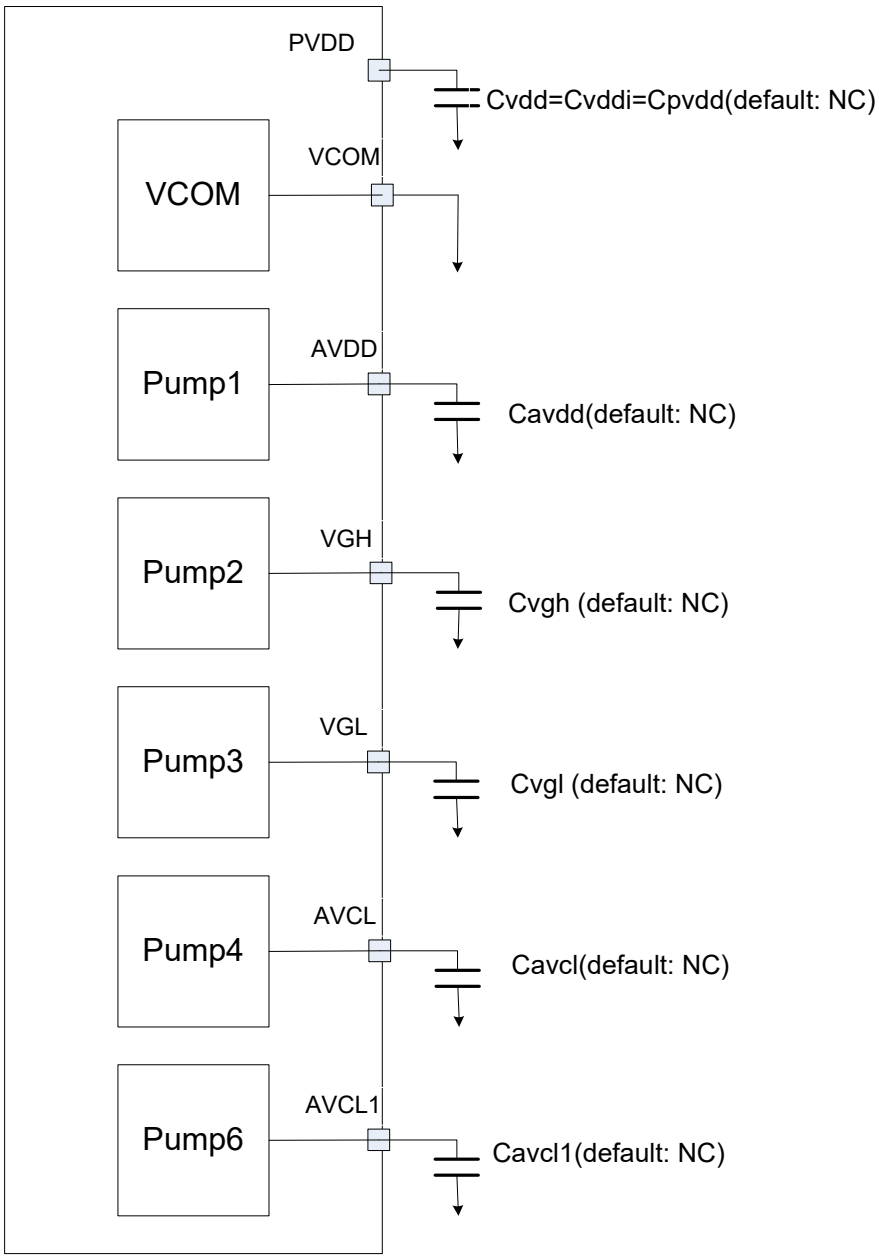
10.3 SYNC-DE Mode Timing Diagram



10.4 DE Mode Timing Diagram



11. POWER APPLICATION CIRCUIT



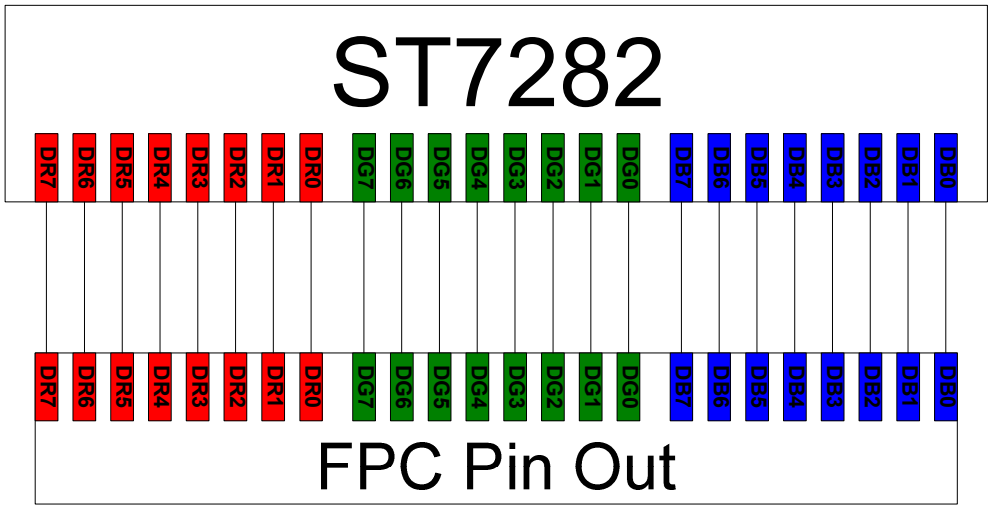
Suggestion of external component

Component	Recommended Value	Voltage proof
Cvdd=Cvddi=Cpvdd	1uF	> 6.3V (default: NC)
Cavdd	1uF	> 10V (default: NC)
Cavcl	1uF	> 10V (default: NC)
Cavcl1	1uF	> 10V (default: NC)
Cvgh	1uF	> 25V (default: NC)
Cvgl	1uF	> 16V (default: NC)

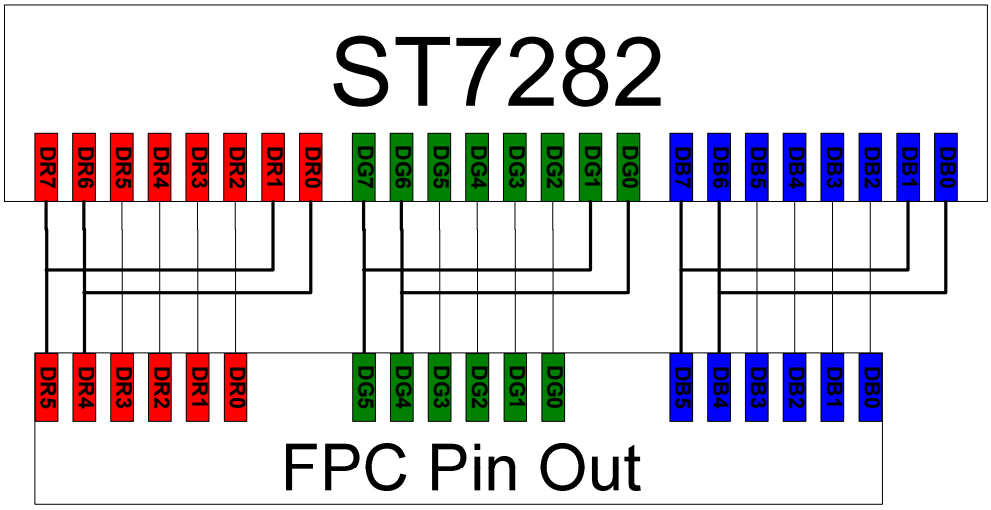
Note: Default NC, The components would be needed depend on the system power, panel loading and display quality.

12. INPUT COLOR FORMAT APPLICATION CIRCIT

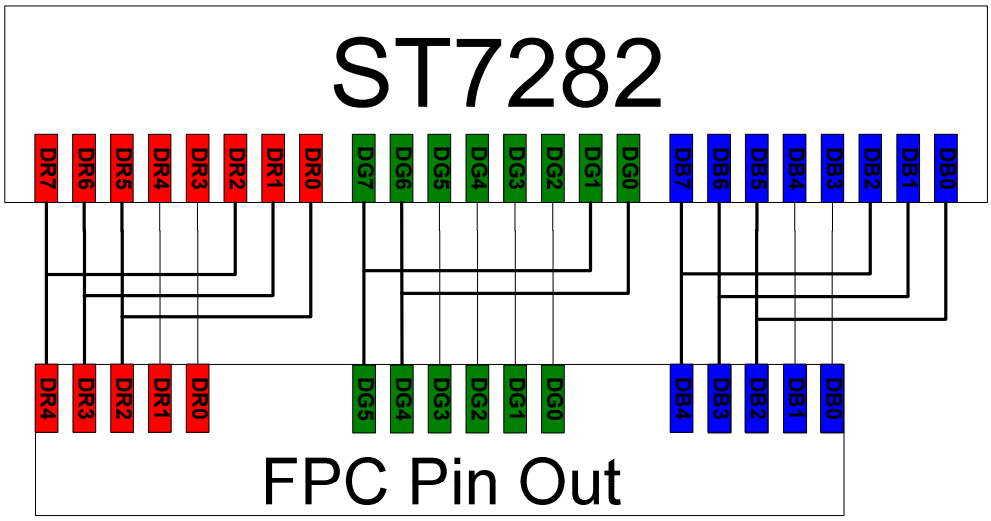
12.1 16.7M Input Color Format



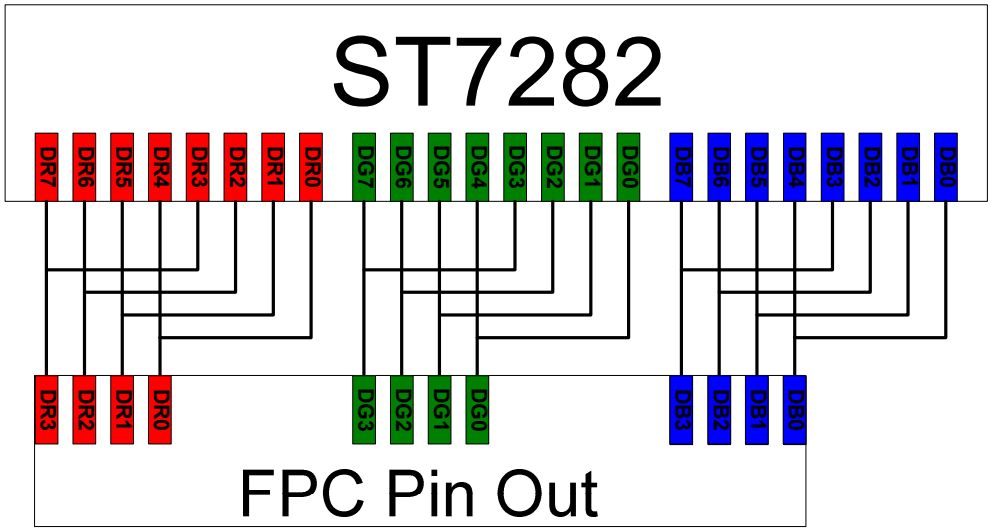
12.2 262K Input Color Format



12.3 65K Input Color Format



12.3 4K Input Color Format



13. FPC APPLICATION CIRCUIT

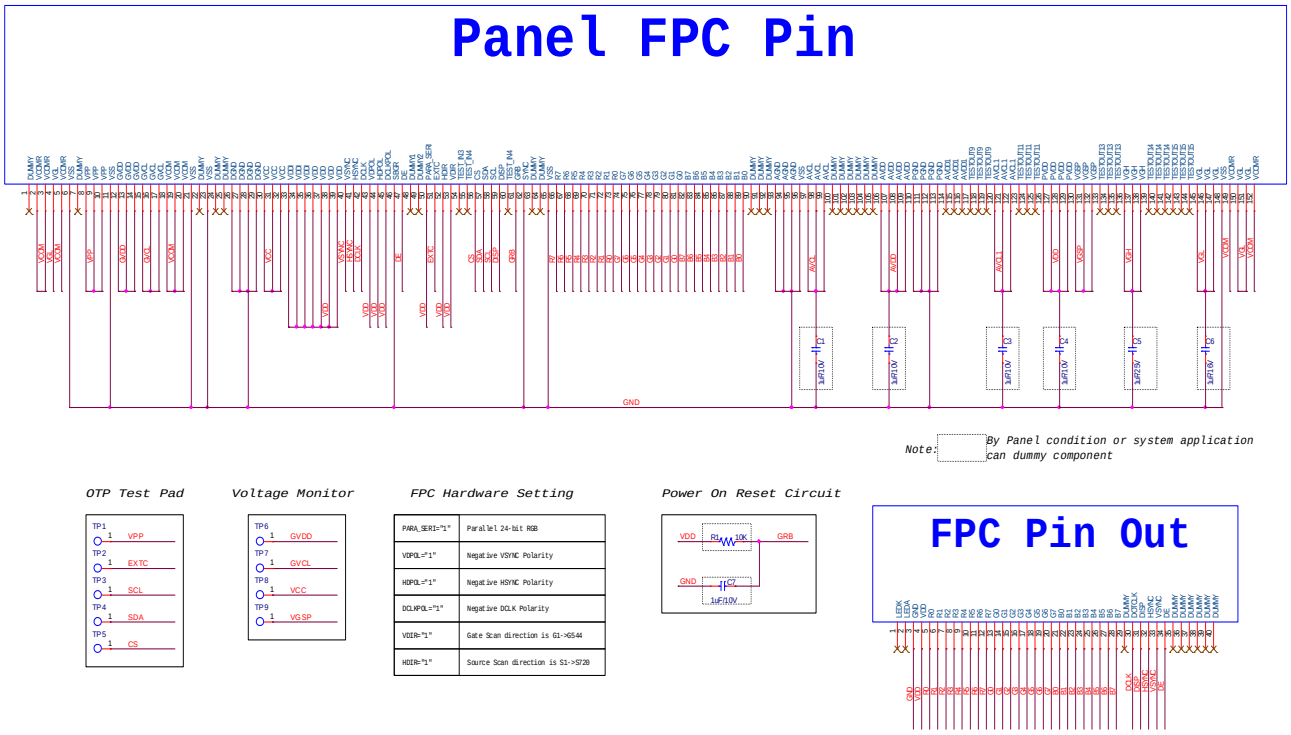
13.1 RGB Mode Selection Table

RGB Mode	DCLK	HSYNC	VSYNC	DE	DR[0:7]	DG[0:7]	DB[0:7]
Parallel RGB SYNC-DE Mode	Input	Input	Input	Input	Input	Input	Input
Parallel RGB SYNC Mode	Input	Input	Input	DGND	Input	Input	Input
Parallel RGB DE Mode	Input	DGND	DGND	Input	Input	Input	Input
Serial RGB SYNC-DE Mode	Input	Input	Input	Input	DGND	Input	DGND
Serial RGB SYNC Mode	Input	Input	Input	DGND	DGND	Input	DGND
Serial RGB DE Mode	Input	DGND	DGND	Input	DGND	Input	DGND

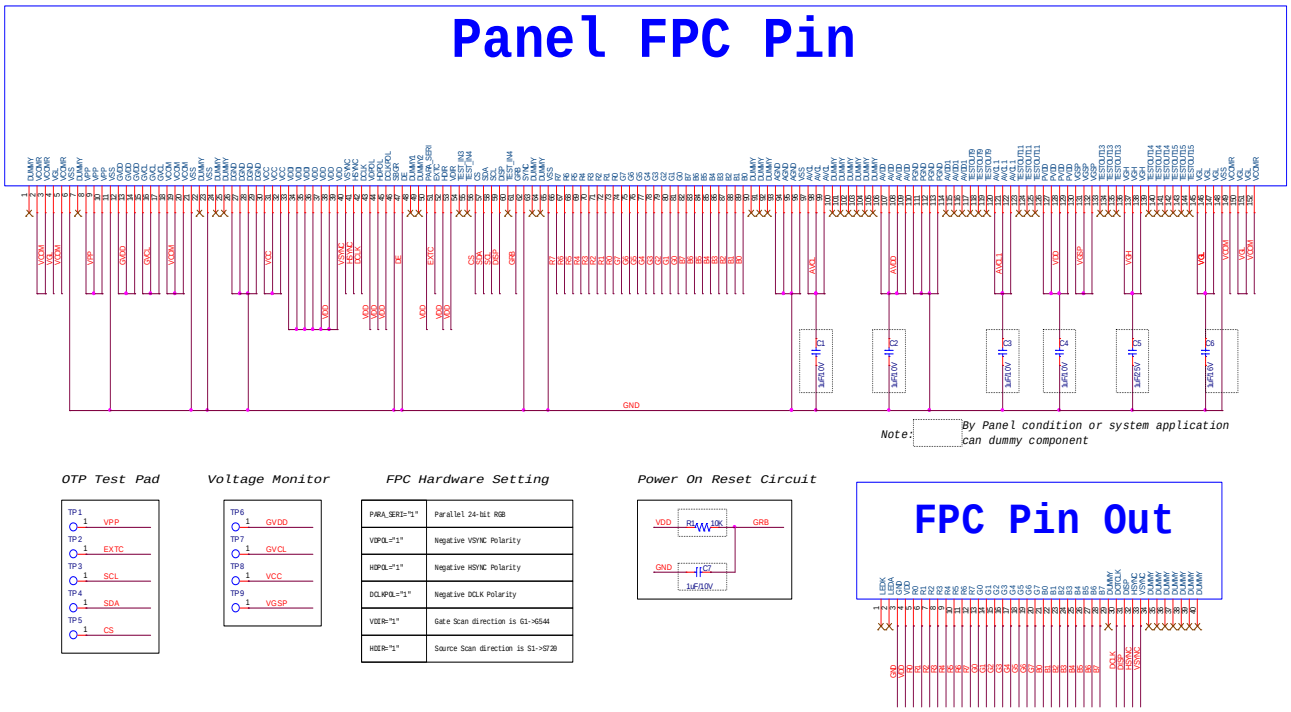
Input: IC input pins are driven by system RGB interface signal.

13.2 Type A Panel (C-company panel)

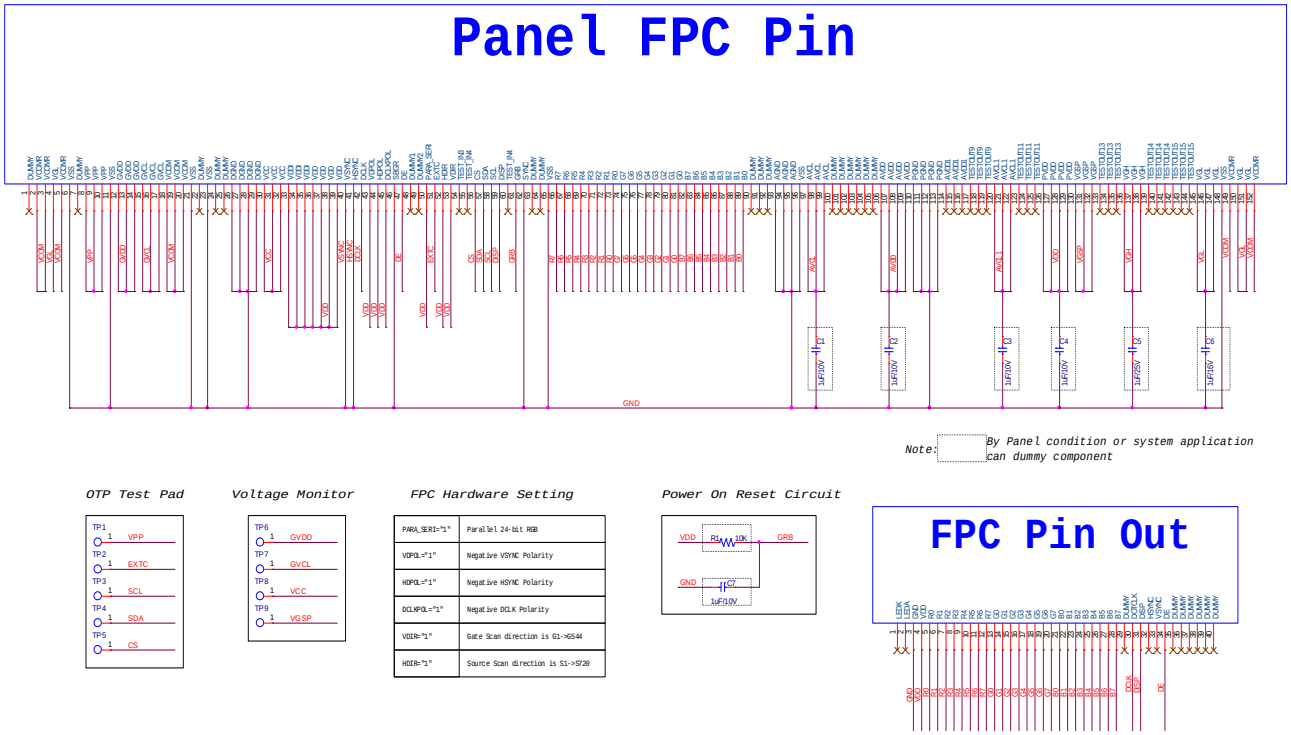
13.2.1 Parallel RGB SYNC-DE Mode Reference Circuit



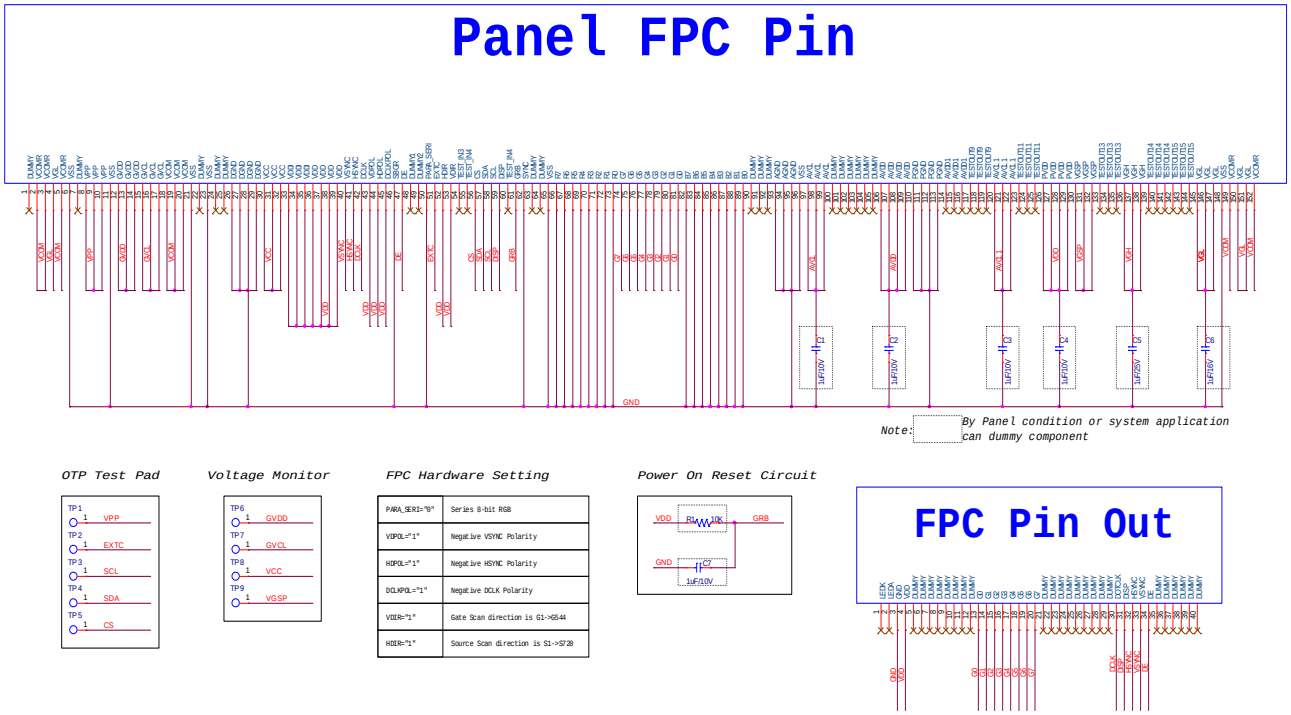
13.2.2 Parallel RGB SYNC Mode Reference Circuit



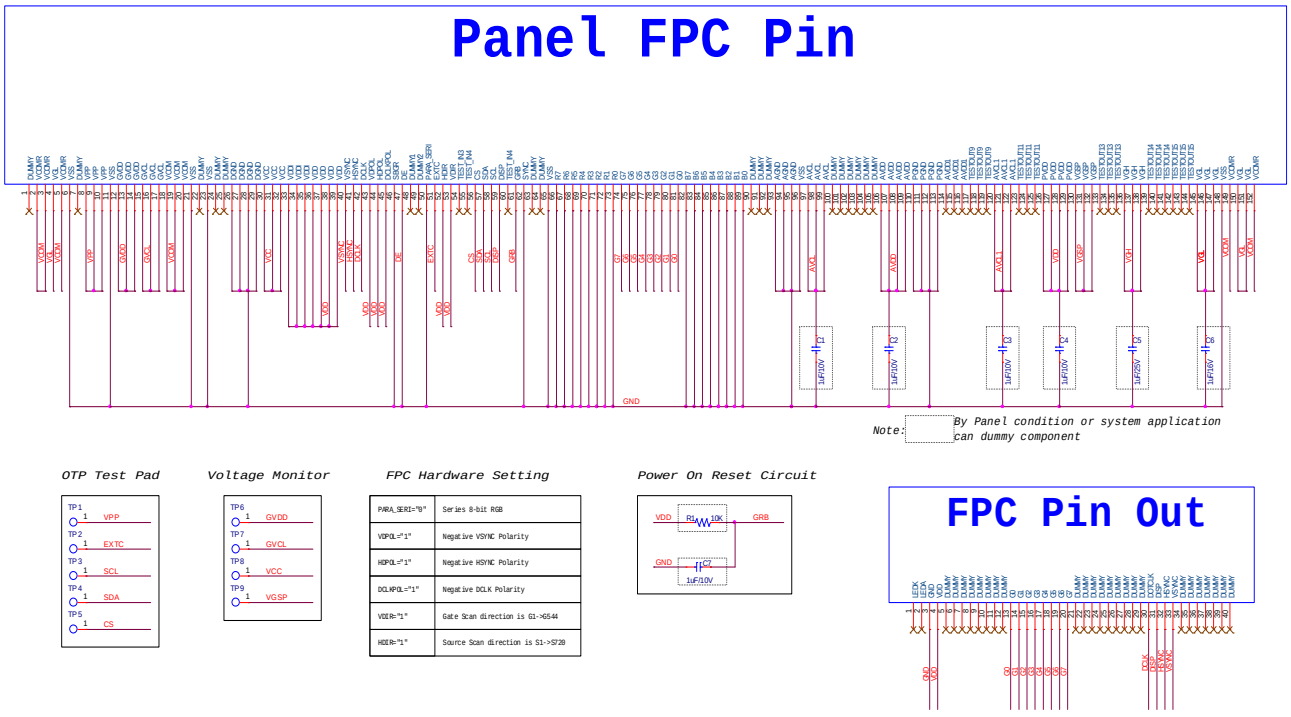
13.2.3 Parallel RGB DE Mode Reference Circuit



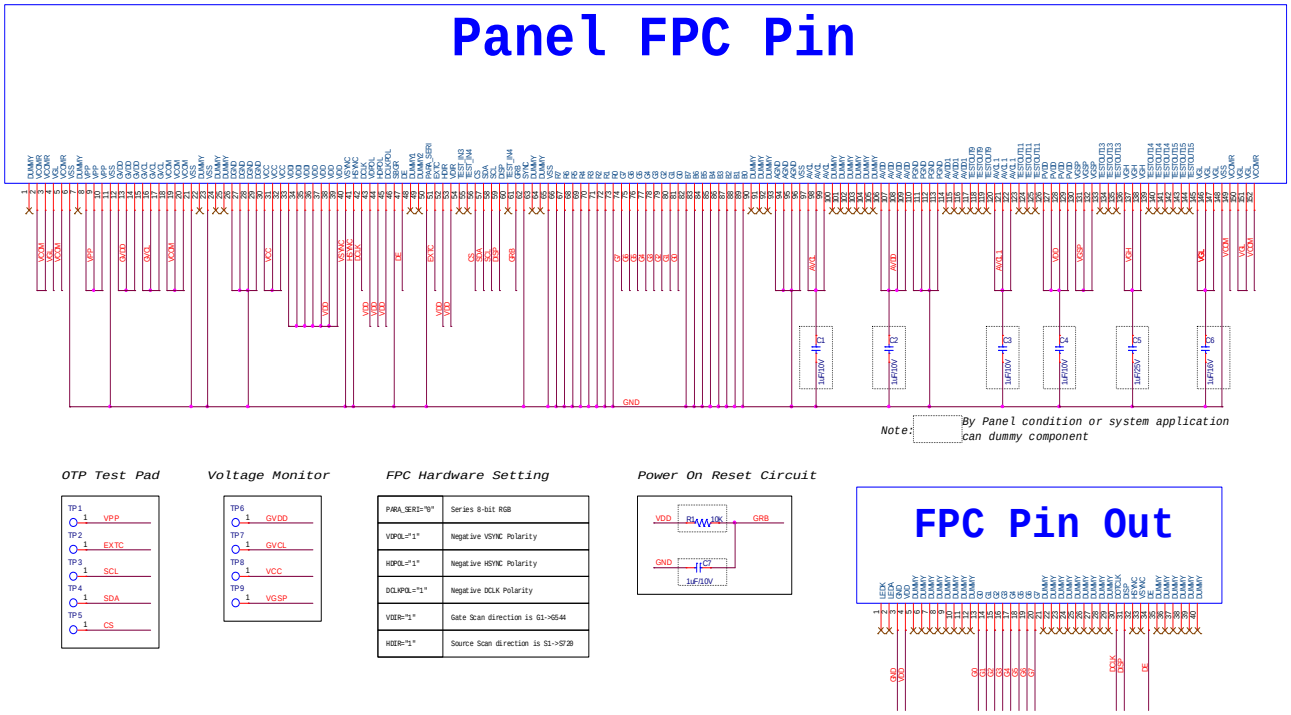
13.2.4 Serial RGB SYNC-DE Mode Reference Circuit



13.2.5 Serial RGB SYNC Mode Reference Circuit



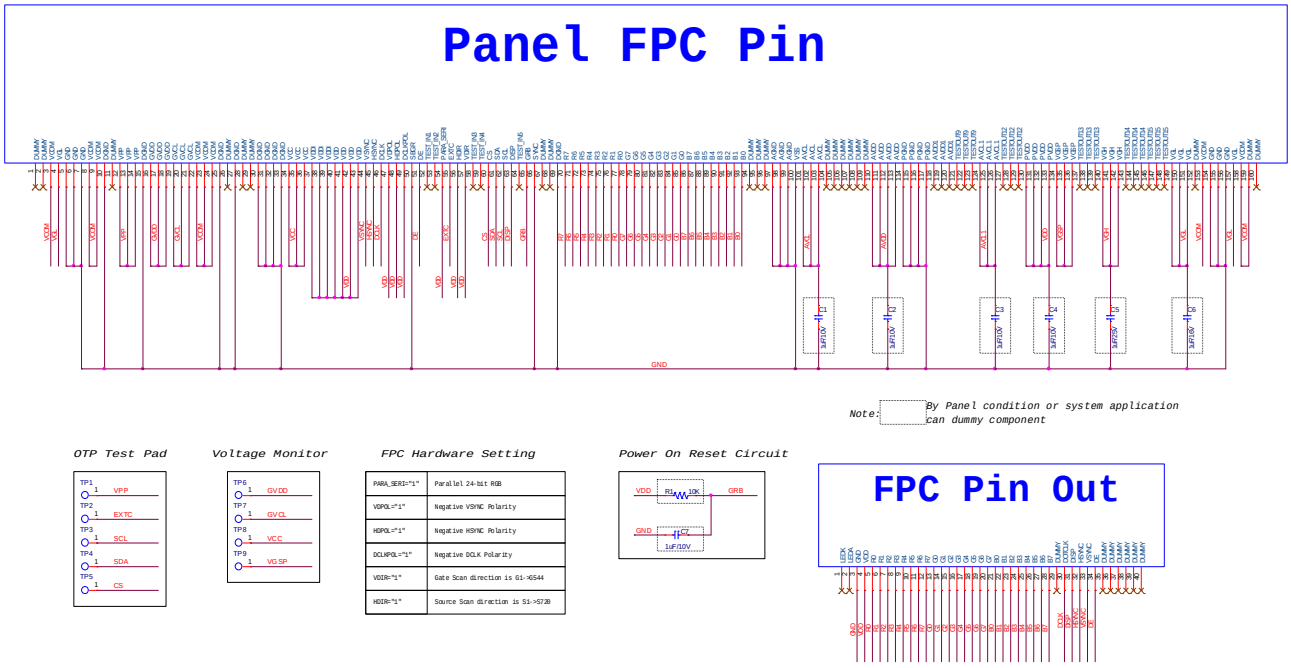
13.2.6 Serial RGB DE Mode Reference Circuit



PARA_SERI="0"	Series 8-bit RGB
VSPOL="1"	Negative VSYNC Polarity
HSPOL="1"	Negative HSYNC Polarity
DCLKPOL="1"	Negative DCLK Polarity
VDIR="1"	Gate Scan direction is G1->G544
HDIR="1"	Source Scan direction is S1->S720

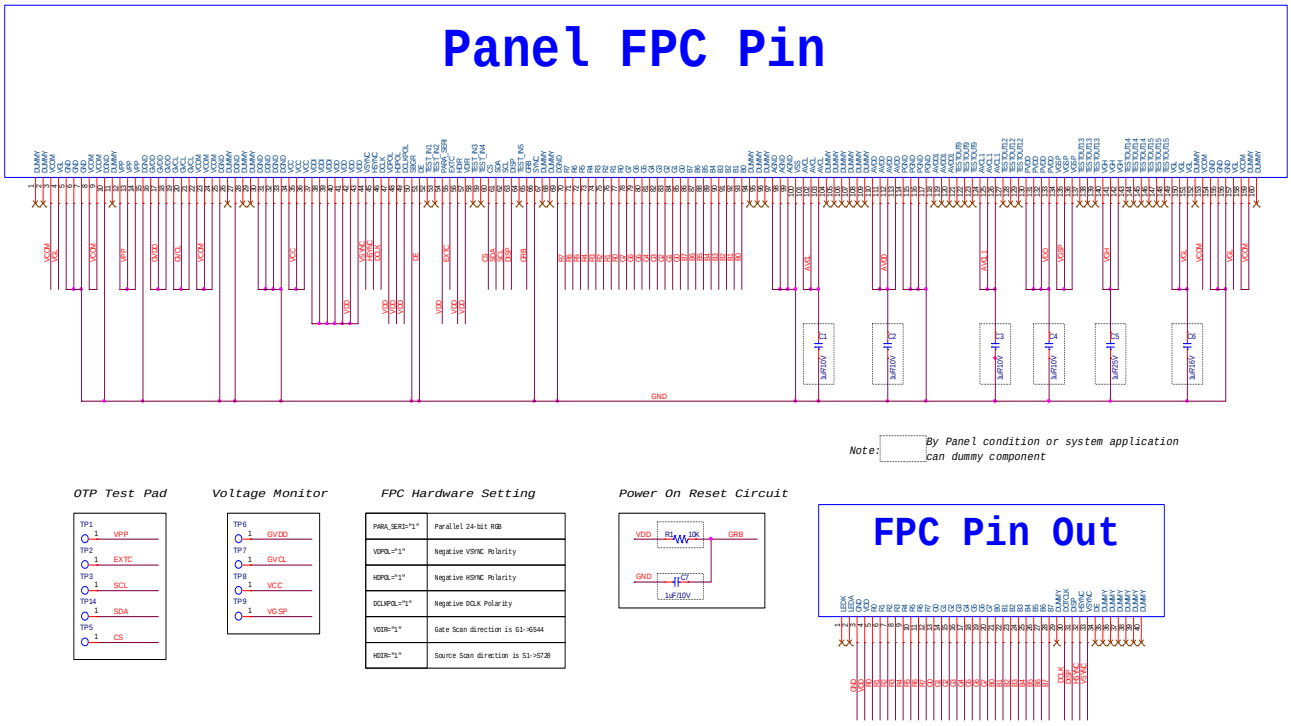
13.3 Type B Panel (B-company panel)

13.3.1 Parallel RGB SYNC-DE Mode Reference Circuit

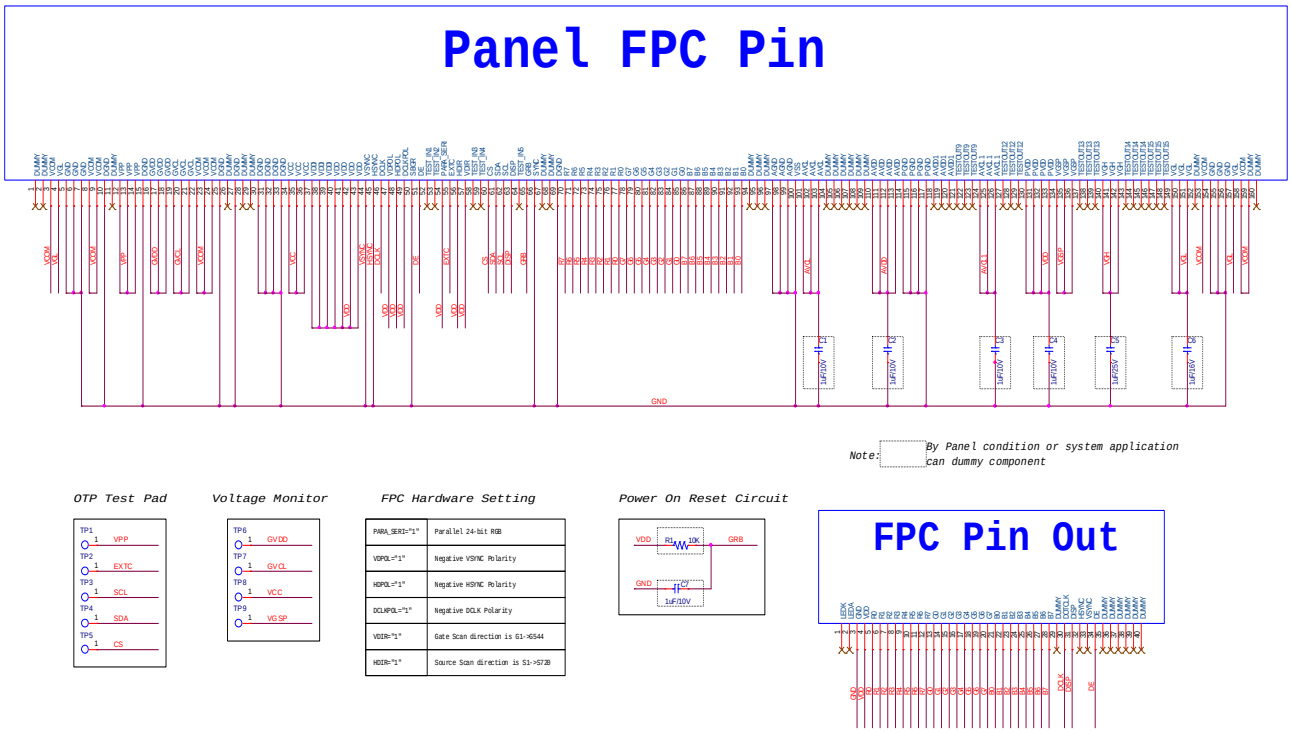


PARA_SERI="1"	Parallel 24-bit RGB
VSPOL="1"	Negative VSYNC Polarity
HSPOL="1"	Negative HSYNC Polarity
DCLKPOL="1"	Negative DCLK Polarity
VDIR="1"	Gate Scan direction is G1->G544
HDIR="1"	Source Scan direction is S1->S720

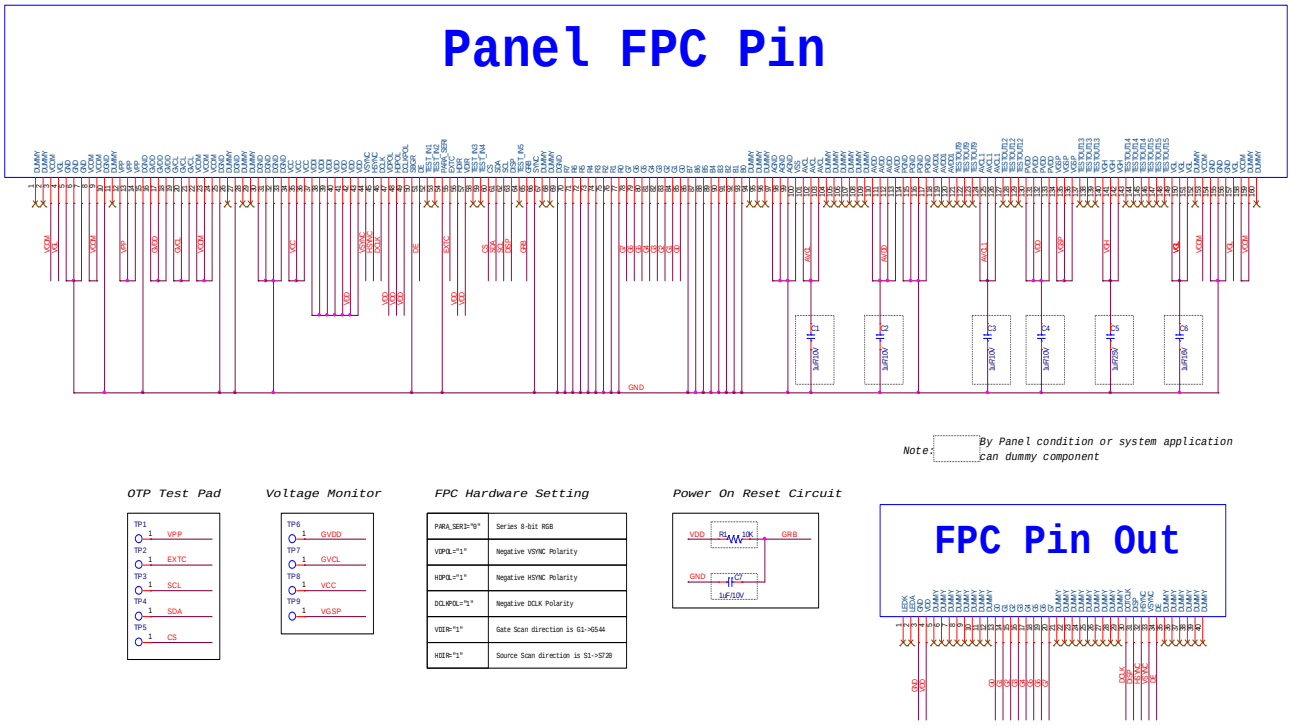
13.3.2 Parallel RGB SYNC Mode Reference Circuit



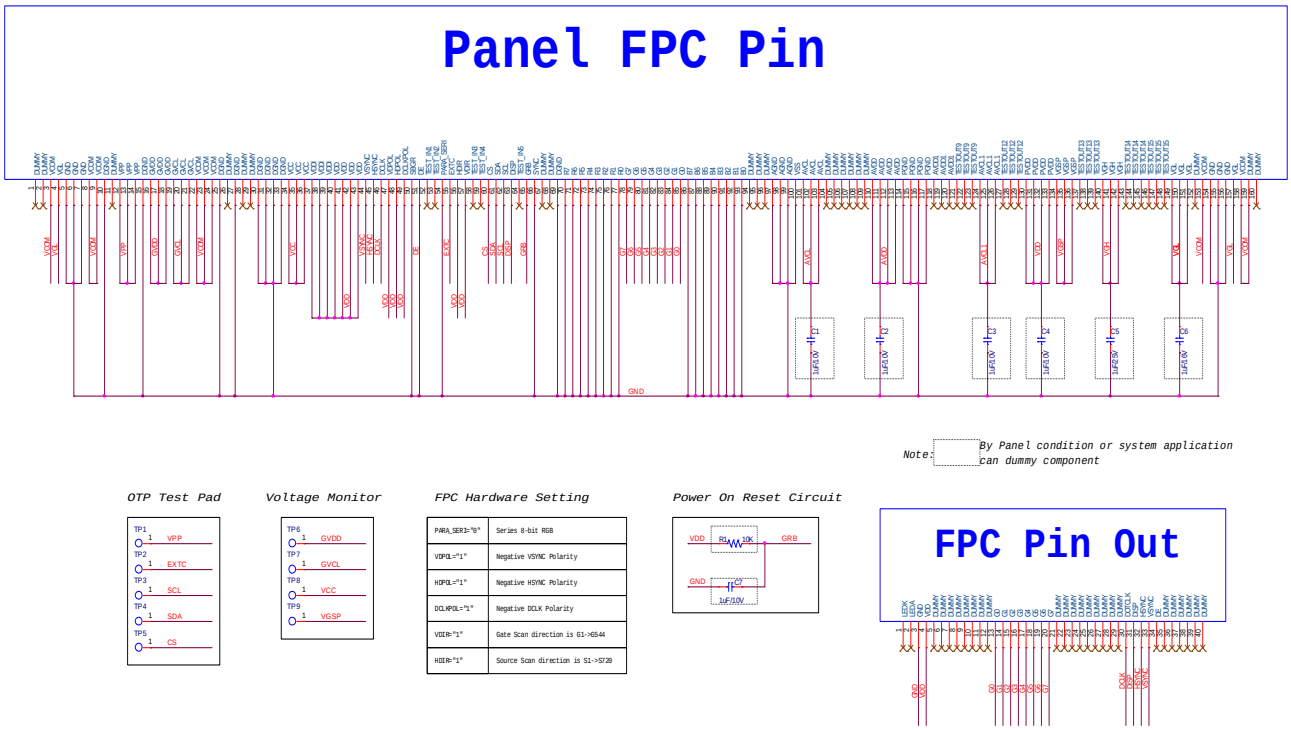
13.3.3 Parallel RGB DE Mode Reference Circuit



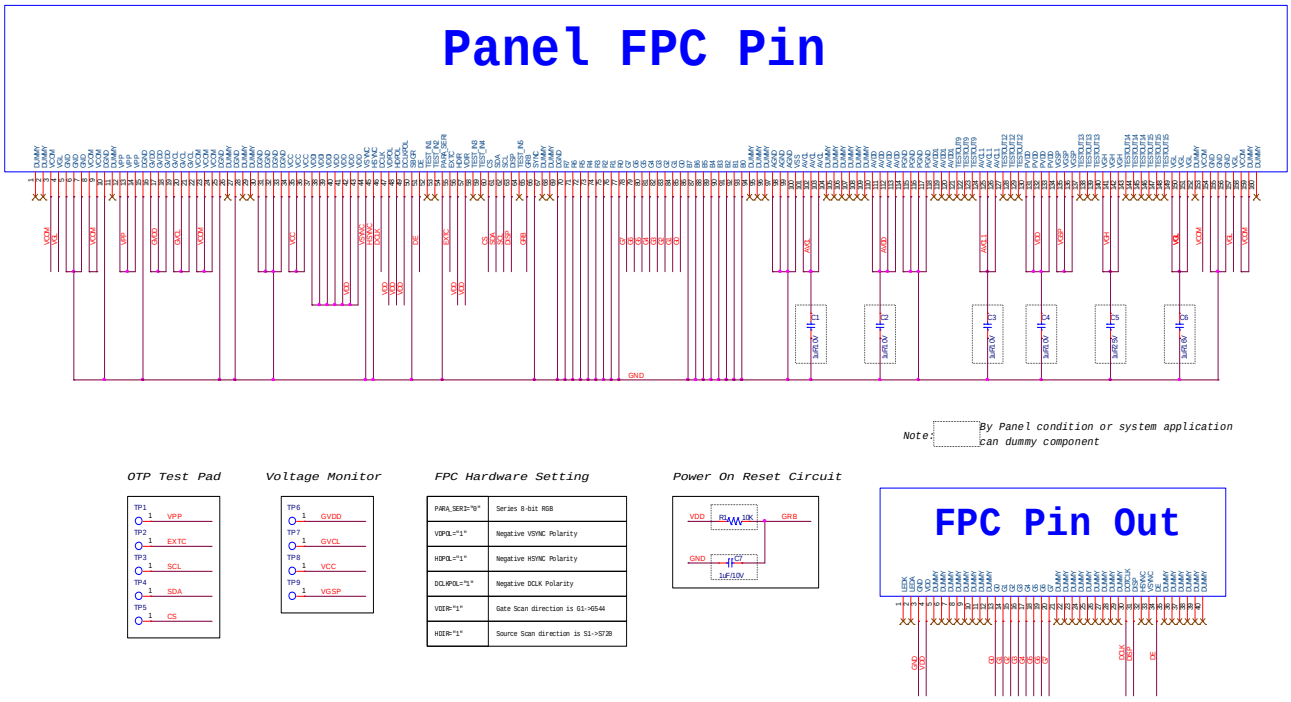
13.3.4 Serial RGB SYNC-DE Mode Reference Circuit



13.3.5 Serial RGB SYNC Mode Reference Circuit

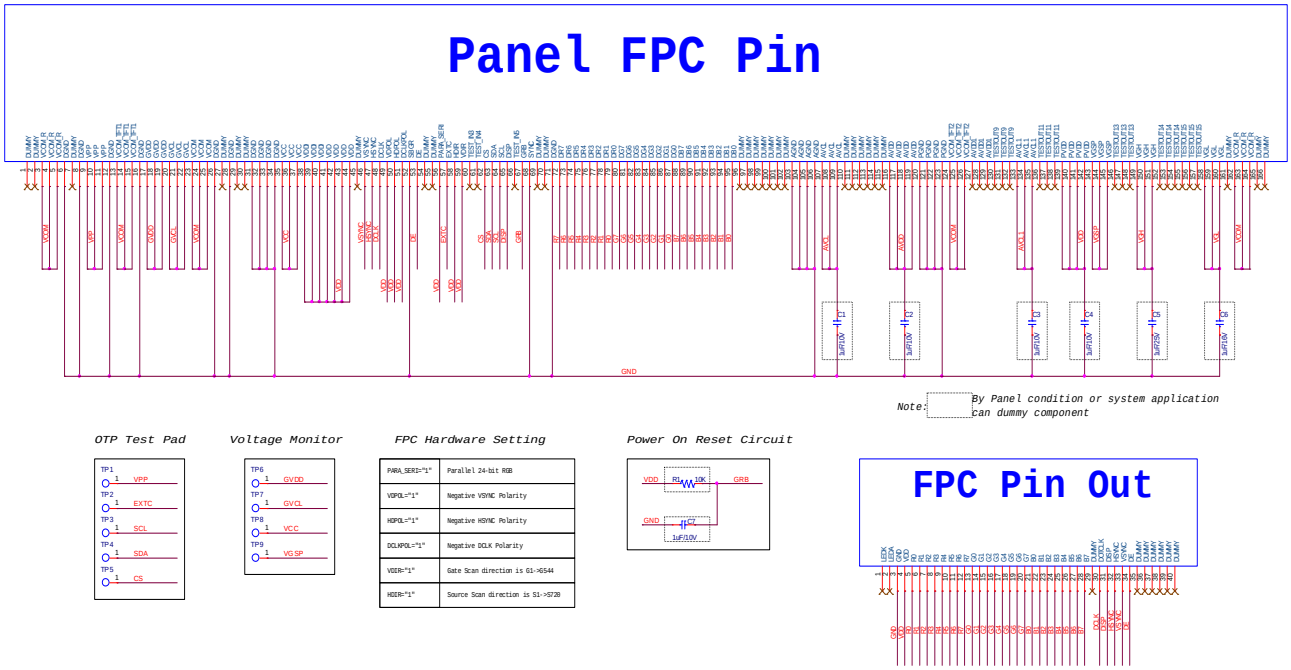


13.3.6 Serial RGB DE Mode Reference Circuit

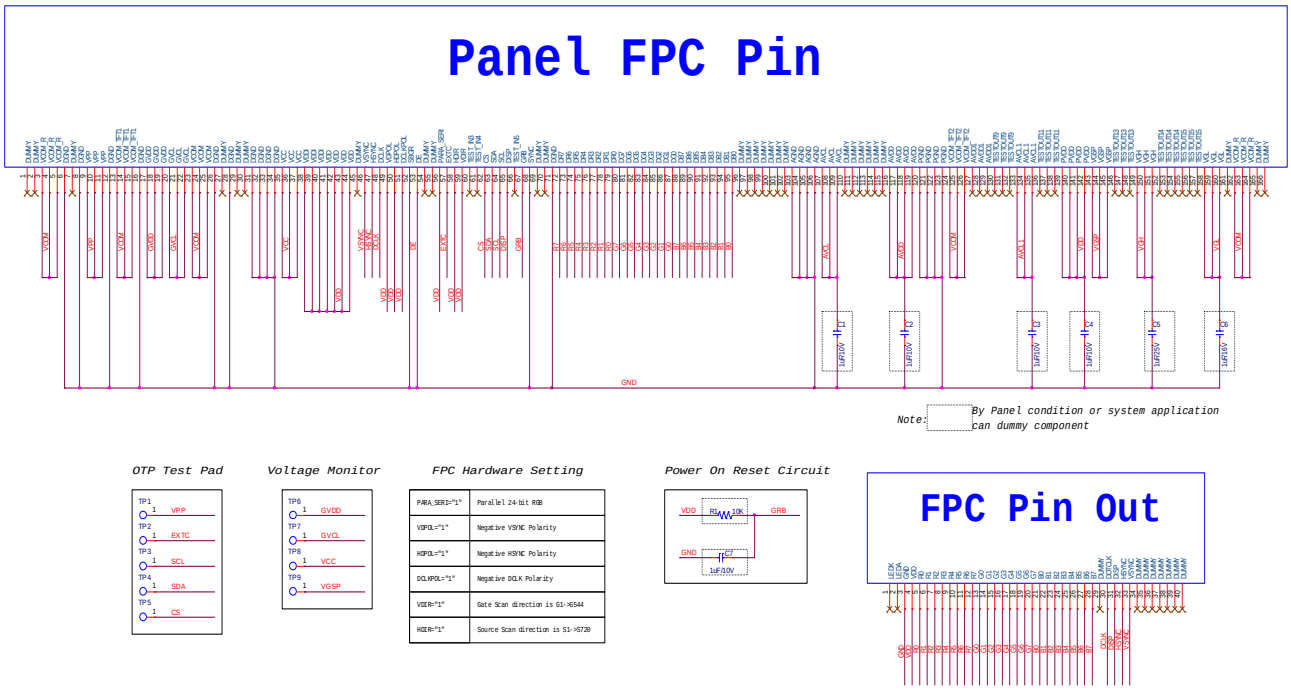


13.4 Type C Panel (I-company panel)

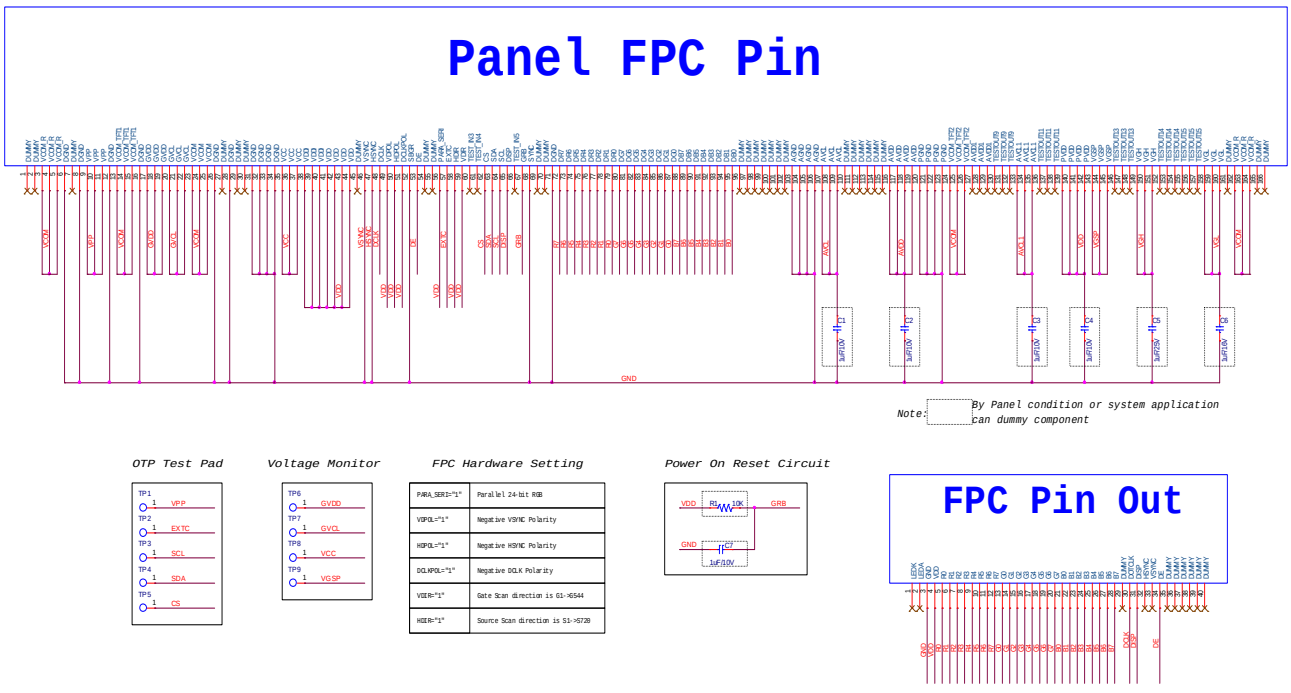
13.4.1 Parallel RGB SYNC-DE Mode Reference Circuit



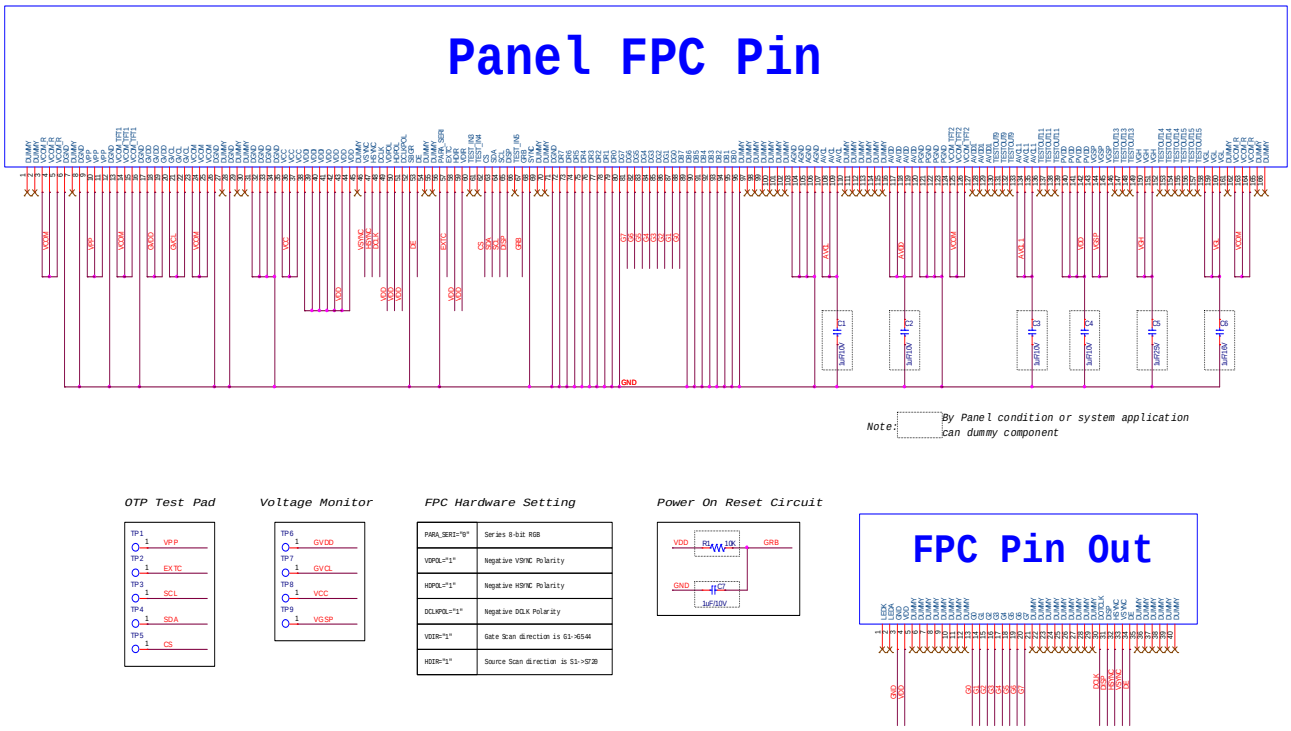
13.4.2 Parallel RGB SYNC Mode Reference Circuit



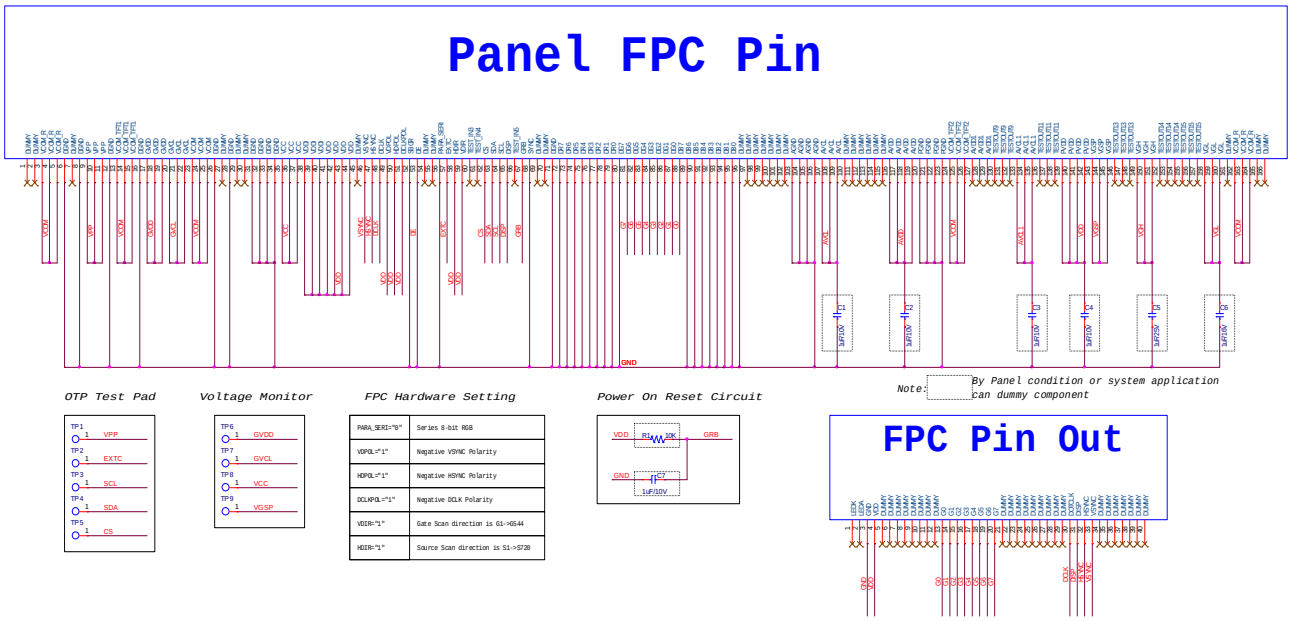
13.4.3 Parallel RGB DE Mode Reference Circuit



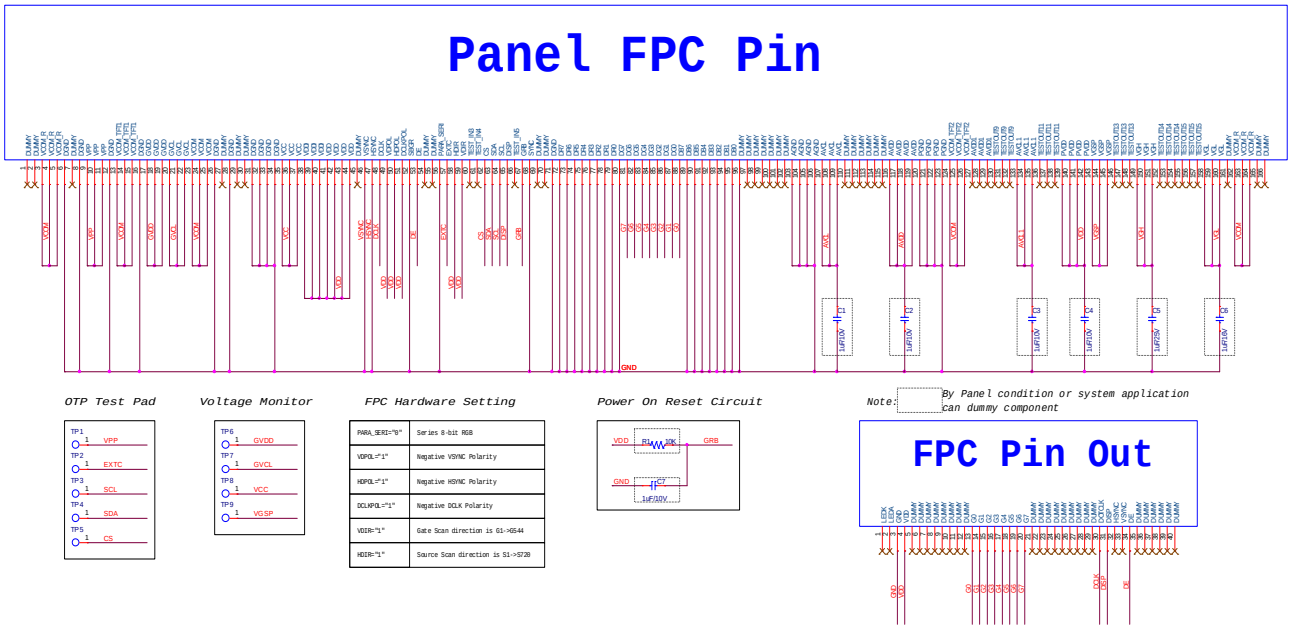
13.4.4 Serial RGB SYNC-DE Mode Reference Circuit



13.4.5 Serial RGB SYNC Mode Reference Circuit

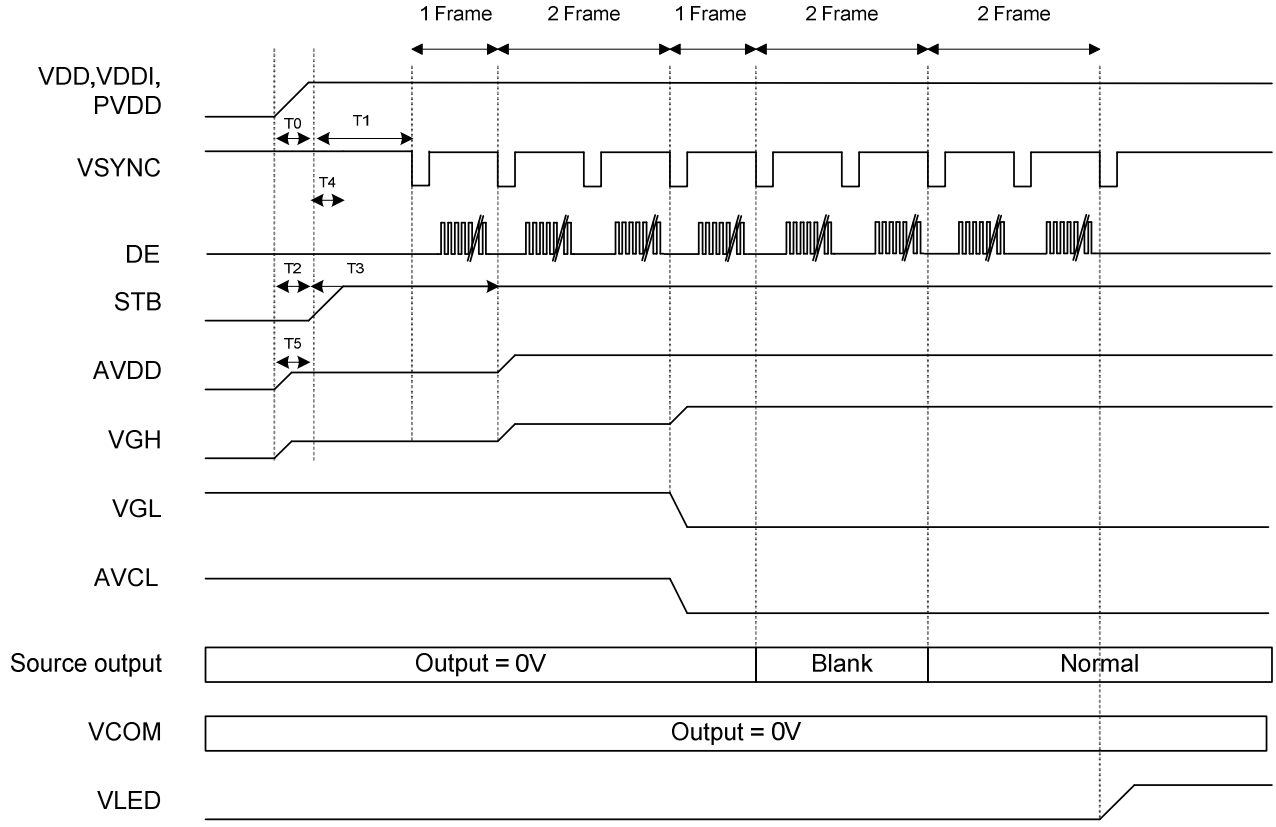


13.4.6 Serial RGB DE Mode Reference Circuit



14. POWER ON/OFF SEQUENCE

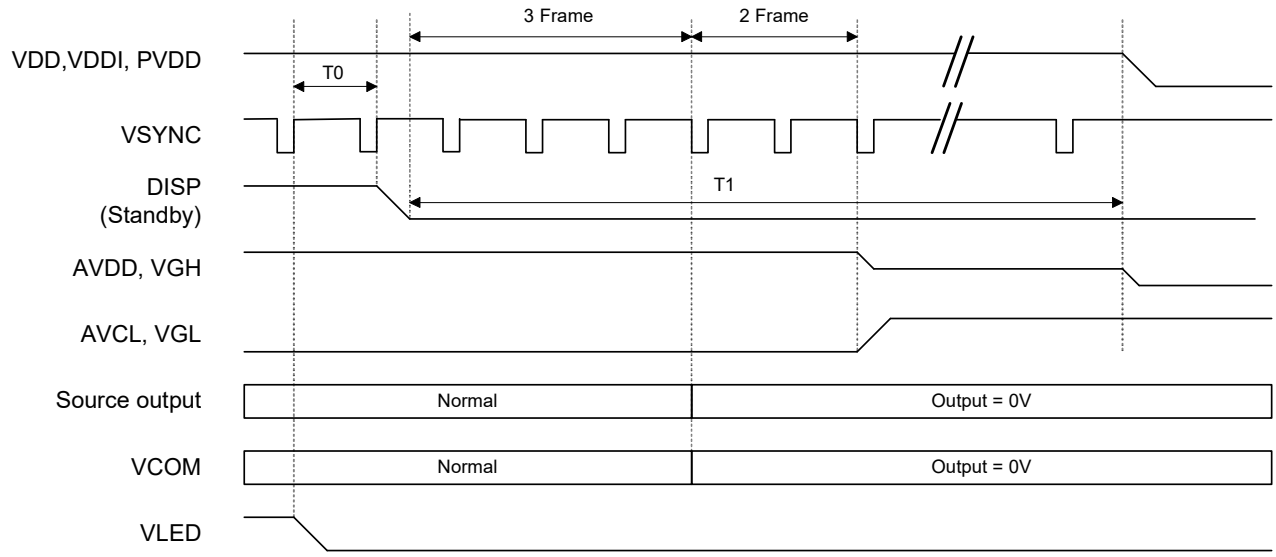
14.1 Power On Sequence



	Description	Min. Time
T0	Determined by the external power	
T1	Time from stable VDD, VDDI, PVDD set-up to the first VSYNC	T1=0
T2	Time from AVDD=0V to AVDD=3.3V	T2=T0
T3	Time from AVDD=3.3V to AVDD=6.0V	T3=T1+ (1*Frame)
T4	Time from stable VDD, VDDI, PVDD set-up to DISP asserted	T4=0
T5	Time from VGH=0V to VGH=3.3V	T5=T0

Note: Recommend the LCM power on rise time T0= 0~ 1ms

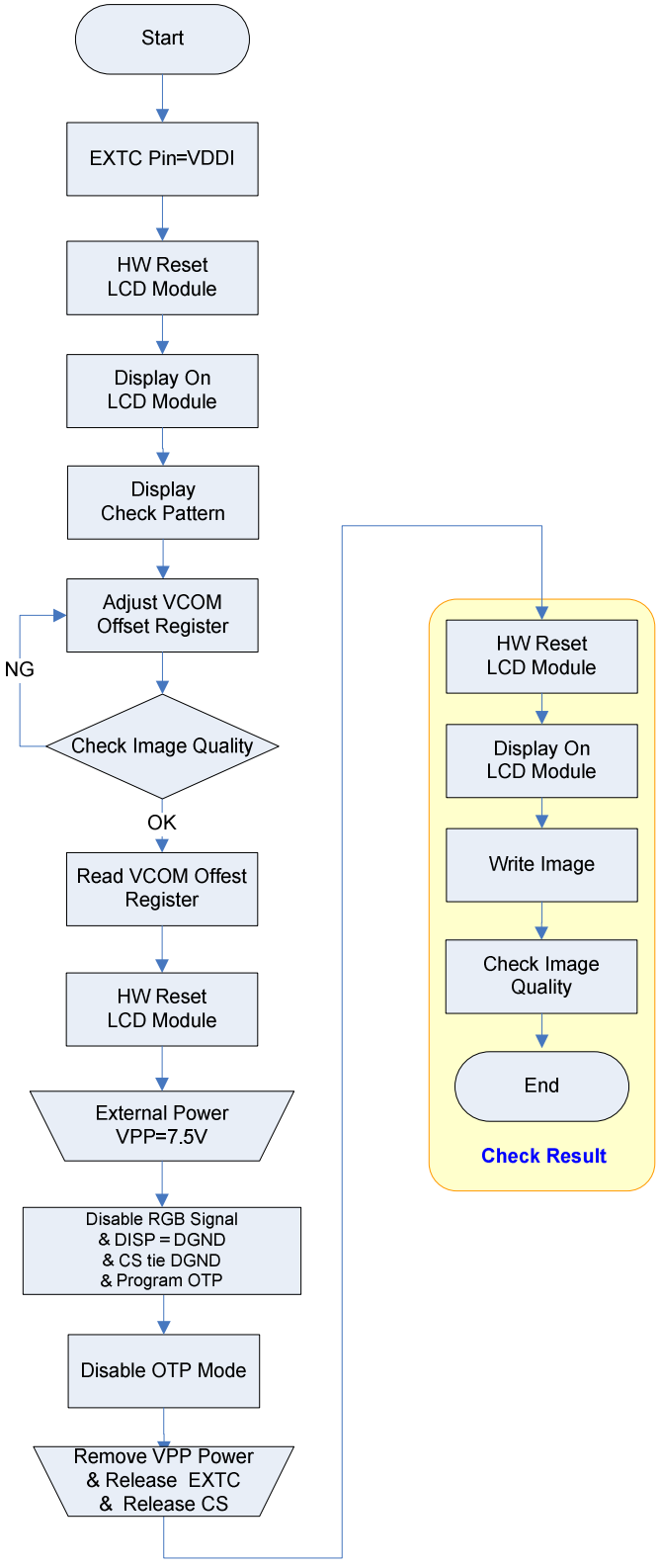
14.2 Power Off Sequence



	Description	Min. Time
T0	Time from backlight power off to DISP=”L”	1*Frame
T1	Time from DISP=”L” to LCM Power off	5*Frame

15. OTP Flow

Non-Volatile Memory (OTP) can only program one time for LCD VCOM calibration .The figure below shows program flow



Step 1: Attach LCD module on OTP programming machine.

LCD module condition	
VDD(V)	3.3
EXTC	VDD

Step 2: Initialize the non-programmed module by software.

Function	W/R	CMD	Par	Note
HW reset	--	--	--	HW reset sequence
Waiting 100ms	--	--	--	
Display On LCD Module	--	--	--	Refer Power On Sequence
Display Check Pattern	--	--	--	Recommend Flicker Pattern
Enable Command 2	W	7F	01	
Adjust VCOM	W	40	XX	Fine tune VMF to reduce flicker

Step 3: Check the image quality of display module. If flicker can be still observed on the panel, repeat the command 40h until the flicker disappearance.

Step 4: Read Optimization VCOM Value

Function	W/R	CMD	Par	Note
Read Optimization VMF	R	40	--	VMF=Read(0x40);
Waiting 100ms				

Step 5:. HW reset LCD Module

Function	W/R	CMD	Par	Note
HW reset	--	--	--	HW reset sequence
Waiting 100ms	--	--	--	

Step 6: Hardware setting

Action	Note
RGB signal OFF	
DISP Pin = GND	
CS Pin tie GND	
External Power 7.5V to VPP Pin	

Step 7: Enable OTP programming Mode and parameter setup

Function	W/R	CMD	Par	Note
Enable Command 2	W	7F	01	
OTP Enable	W	4A	02	
OTP parameter setup	W	4B	01	
OTP parameter setup	W	4C	VMF	
Waiting 100ms				

Step 8: Program OTP.

Function	W/R	CMD	Par	Note
OTP Write Command	W	4D	CA	Program OTP
Waiting 100ms				

Step 9: Hardware setting

Action	Note
Release EXTC Pin	
Release CS Pin	
Remove 7.5V form VPP Pin	

Step 10: Disable OTP programming Mode.

Function	W/R	CMD	Par	Note
Disable OTP Programming Mode	W	4A	00	
Waiting 100ms				

Step 11: Turn off VDD and VDDI, waiting for 200ms then and turn on again.

Step 12: Execute normal display on sequence.

Function	W/R	CMD	Par	Note
HW reset	--	--	--	HW reset sequence
Waiting 100ms	--	--	--	
Display On LCD Module	--	--	--	Refer Power On Sequence
Display Check Pattern	--	--	--	Recommend Flicker Pattern

Step 13: Check the image quality.

16. RECOMMENDED PANEL ROUTING RESISTANCE

The recommended wiring resistance values are given below. The wiring resistance values affect the current capability of the power supply blocks and thus must be designed within the given range.

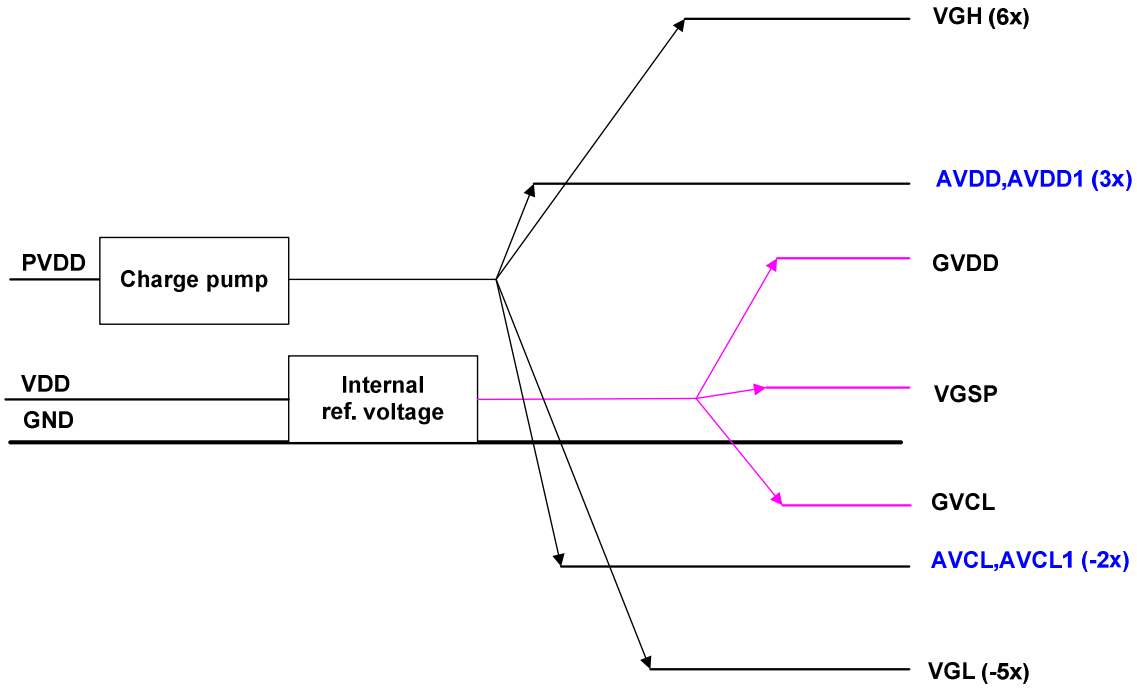
	Pin Name	Unit: ohm
1	VPP	<3
2	GVDD	<50
3	GVCL	<50
4	VCOM	<3
5	DGND	<3
6	VCC	<50
7	VDDI	<3
8	VDD	<3
9	VSYNC	<50
10	HSYNC	<50
11	DCLK	<50
12	VDPOL	<50
13	HDPOL	<50
14	DCLKPOL	<50
15	SBGR	<50
16	DE	<50
17	PARA_SERI	<50
18	EXTC	<50
19	HDIR	<50
20	VDIR	<50
21	CS	<50
22	SDA	<50
23	SCL	<50
24	DISP	<50
25	GRB	<50
26	SYNC	<50
27	DR7-DR0	<50
28	DG7-DG0	<50
29	DB7-DB0	<50
30	AGND	<3

	Pin Name	Unit: ohm
31	AVCL	<50
32	AVCL1	<50
33	AVDD	<50
34	AVDD1	<50
35	VGSP	<50
36	PGND	<3
37	PVDD	<3
38	VGH	<50
39	VGL	<50

17. POWER STRUCTURE

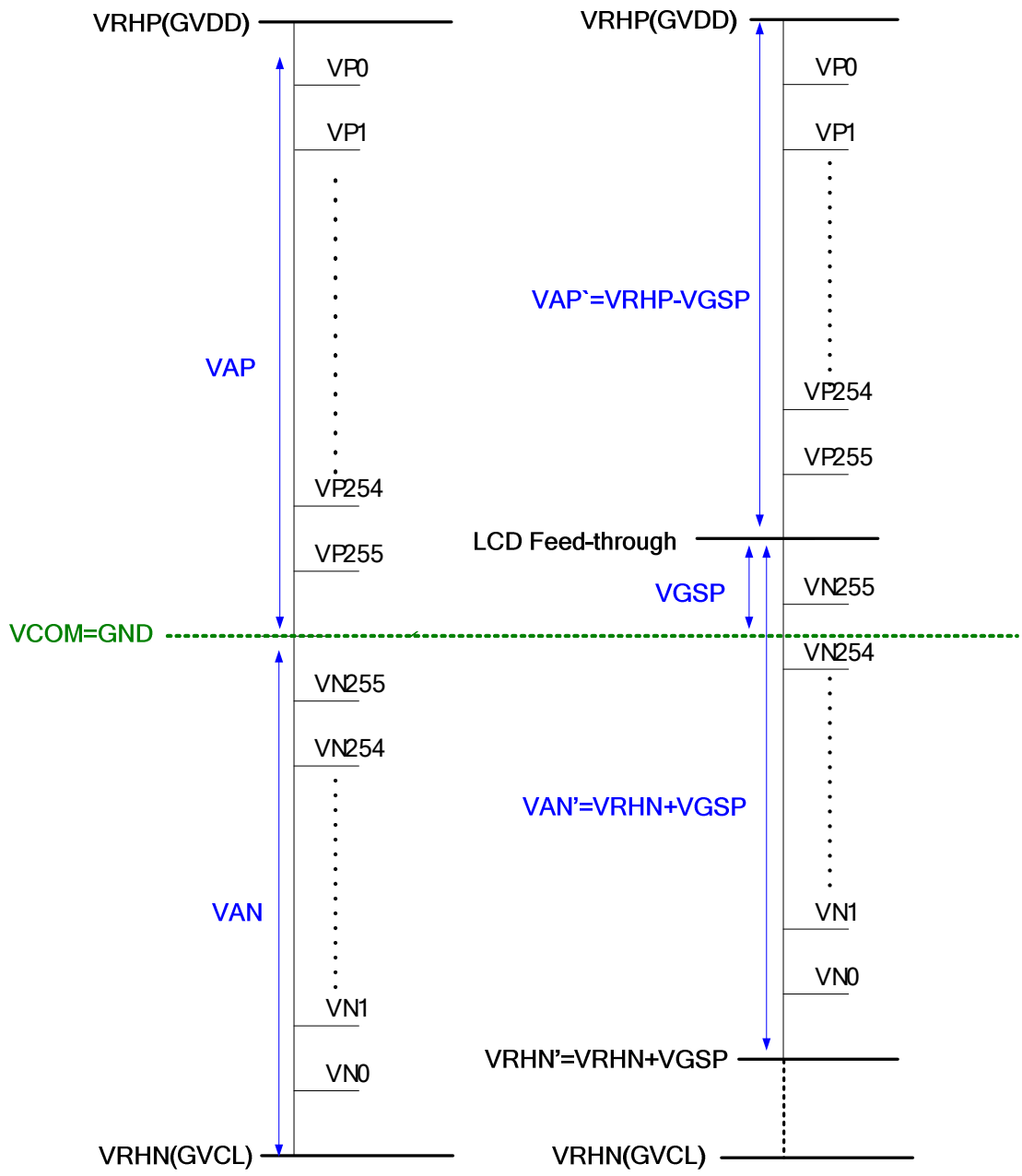
17.1 Voltage Generation

The following figure is relations of analog voltage



17.2 Source Voltage Relations

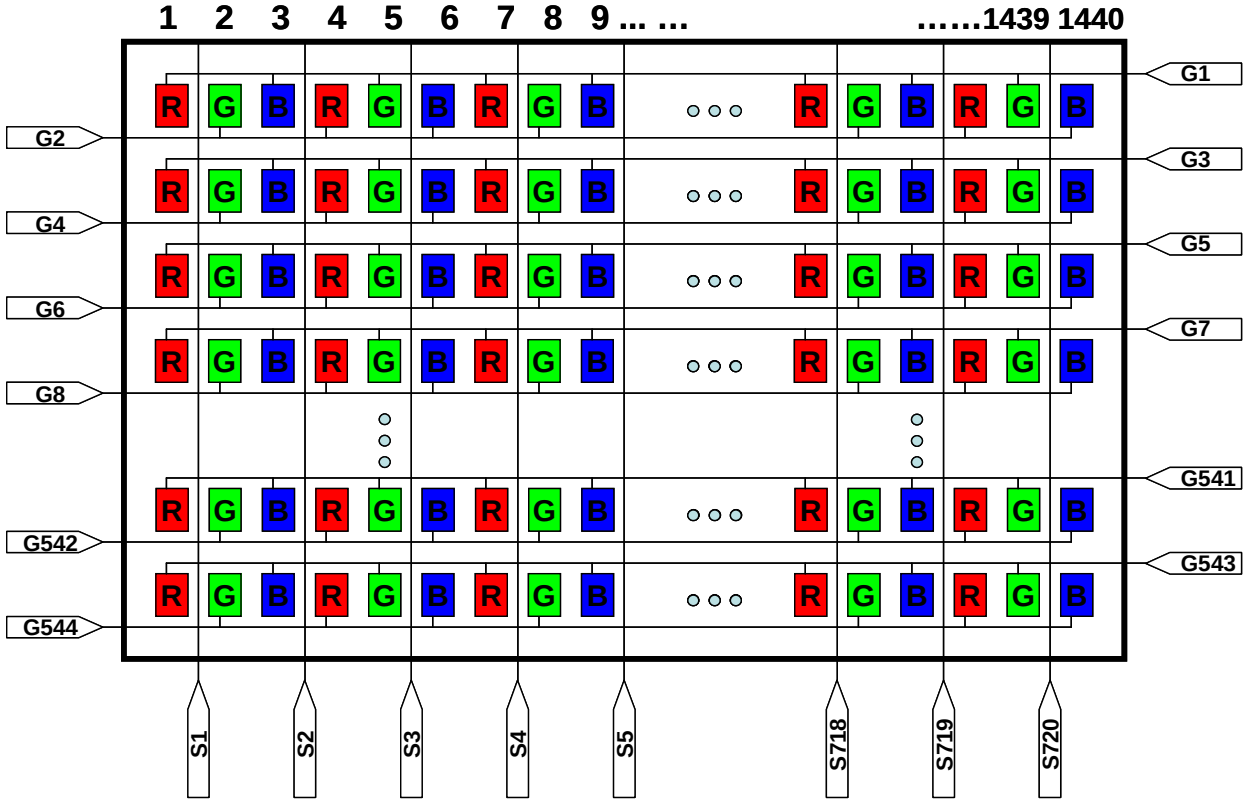
The relations between VCOM and Source voltage is shown as below:



Note: VAP' = VRHP-VGSP and VAN'= VRHN+VGSP is LC voltage. Applied voltage between LC is 5.46~ 4.46V, and the difference depends on panel feed-through voltage (panel feed-through voltage estimation is 0.5~ 1.5V).

18. COLOR FILTER ARRANGEMENT

The Driver supports the stripe color filter of dual-gate application. The color filter arrangement on panel is shown below.



19. REVISION HISTORY

Revision	Description	Date
preliminary	1st edition	2013/12
0.1	Modify PAD arrangement (P6) Modify PIN name, No.91,92,93,94,103,104,105,106,330 (P10,P13,P23,P28) Modify PIN description (P36) Modify RGB input timing table (P48) Modify timing diagram (P49) Modify recommended panel routing resistance (P52)	2013/12/18
0.2	Modify RGB input timing table (P48)	2014/02
0.3	Modify RGB input timing table (P48)	2014/04
0.4	Modify Alignment Mark Position (P8)	2014/05
0.5	Modify PARA_SERI PIN default description (P34)	2014/06
0.6	Modify RGB input timing table (P48)	2014/08
0.7	Modify DE pin description (P34) Modify TEST_IN3 pin description (P36) Add AVCL1 pin function (P13,P36,P52) Modify RGB input timing table (P48)	2014/09
1.0	Modify GVDD/GVCL voltage range(P5) Modify Output Bump Dimension PIN name(P6) Add power application circuit (P51) Modify Power on and Power off sequence (P52,P53)	2014/10
1.1	Modify TESTOUT8 pin name(P6,P12) Modify TESTOUT12 pin name(P6,P13) Add AVDD1 pin description(P36) Add VGSP pin description(P36) Modify RGB input timing table(P49) Add FPC application circuit(P53,P54,P55,P56) Modify Power On/Off Squence (P58,P59) Modify recommand panel routing resistance table(P60)	2015/02
1.2	Modify HSYNC, VSYNC, SYNC ,VDPOL, HDPOL, SBGR pin Description (P34,P35) Modify Register R9, R10 Description (P44,P45) Remove Register R16 (P39,P45) Add Command Table 2 Register Description (P39,P40,P46-P52) Modify AC Characteristics (P54) Modify AC Timing Diagram (P55)	2015/05

	Add RGB input timing in sync mode description (P56) Modify SYNC Mode Timing Diagram (P57) Add Chap.12 Input Color Format Application Circuit (P60,P61) Add Chap.15 OTP flow (P68,P69,P70)	
1.2a	Modify Title Page Description Modify Features Description (P5) Modify Note Description (P59)	2015/06
1.3	Modify Features Description (P5) Modify Output Bump Dimension(P6) Modify HSYNC,VSYNC,DE,VDIR,HDIR pin description(P34) Modify register R0 description (P39) Modify suggestion of external component table (P59) Add DE Mode Timing Diagram (P60) Modify FPC application circuit (P64,P65,P66) Add VGSP recommended panel routing resistance (P72)	2015/10
1.4	Modify general description(P4) Modify HSYNC,VSYNC and DE pin description (P34) Modify VGSP pin description (P36) Add SPI communication Note (P38) Modify register summary table(P39) Remove register R53 (P51) Modify register R54 description (P51) Add register R55 (P52) Add register R5B (P52) Add register R5D (P5D) Add register R5E (P5E) Modify absolute maximum rating note(P59) Modify DC characteristics for digital circuit table(P59) Modify DC characteristics for analog circuit(P60) Modify RGB timing table (P62) Add RGB mode selection table (P69) Add type B panel FPC reference circuit (P72) Add type C panel FPC reference circuit (P75) Add power on sequence note(P78) Modify power off sequence (P79) Add power structure chapter (P84) Add color filter arrangement chapter(P86)	2016/05

1.5	Modify type A/B/C reference circuit (P68~P77)	2016/06