Sitronix

ST2608B

8-bit Integrated Microcontroller

Datasheet

Version 1.1

2009/03/06

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SITRONIX Technology Corporation

1   GENERAL DESCRIPTION

The ST2608B is a 8-bit integrated microcontroller designed with CMOS silicon gate technology. The true static CPU core, power down modes and dual oscillators design makes the ST2608B suitable for power saving and long battery life designs. The ST2608B integrates various logic to support functions on-chip which are needed by system designers.

The ST2608B features the capacity of memory access of maximum 44M bytes and DMA function for fast memory transfer. Six chip-select pins are equipped for direct connection to external ROM, SRAM, Flash memory or other devices. The maximum size for a single external memory device can be 16M bytes.

The ST2608B has 56 I/Os grouped into 6 ports. They are Port-A ~ Port-F and Port-L, where the Port-F is 8 open drain output pins shared with LCD COMs. Each I/O pins can be programmed to input or output individually. Port-C inputs have both pull-up and pull-down options. The other input pins have only pull-up options. In the case of output mode, Port-C outputs have open-drain type and CMOS type options; while the other ports are fixed at CMOS type. The Port-A and Port-B are designed for keyboard scan function. The Port-A inputs are further equipped with de-bounce and transition triggered interrupt function. The Port-C/D/E/L are shared with other system functions. All the properties of I/O pins are still programmable when they are configured to be other special functional signals. This enlarges the flexibility of the usage of the functional signals.

The ability of driving large LCD panels, up to 240x160, and hardware gray-level support rich the display information and the diversity of contents as well. By the patented sharing mechanism design of internal memory, the LCD display function can be done without the need of external display RAM. The variable LCD buffer design also makes it feasible to use small internal display RAM as the buffer of large-sized display. User may free major internal RAM for computing or temporary access while keeping the display content. The clock of LCD (LCDCK) is not only sourced from main-frequency (OSC), it can also be sourced by OSCX (32KHz crystal) to make current consumption to be minimum.

The ST2608B equips serial communication ports, one UART and one SPI, to perform different communications, ex.: RS-232 and IrDA, with system components or other products such as PC, Notebook, and popular PDA. Three clocking outputs can produce synthesized PWM signals or high frequency carrier for IR remote control. This helps products become more useful in our daily life.

The built-in four-channel PSG are designed to generate key tone, melody, voice, and speech. Two dedicated pins with large driving capacity can drive a buzzer/speaker directly.

The ST2608B has a Low Voltage Detector (LVD) for power management usage. The status of internal or external power can be detected and reported to the management software.

Power bouncing during power-on is a major problem when designing a reliable system. The ST2608B equips a Low Voltage Reset function to keep the whole system in reset status when power is low. After the power returns to normal level, the system may recover its original states and keeps working correctly.

With these integrated functions inside, the ST2608B single chip microcontroller is a right solution for PDA, translator, databank and other consumer products.

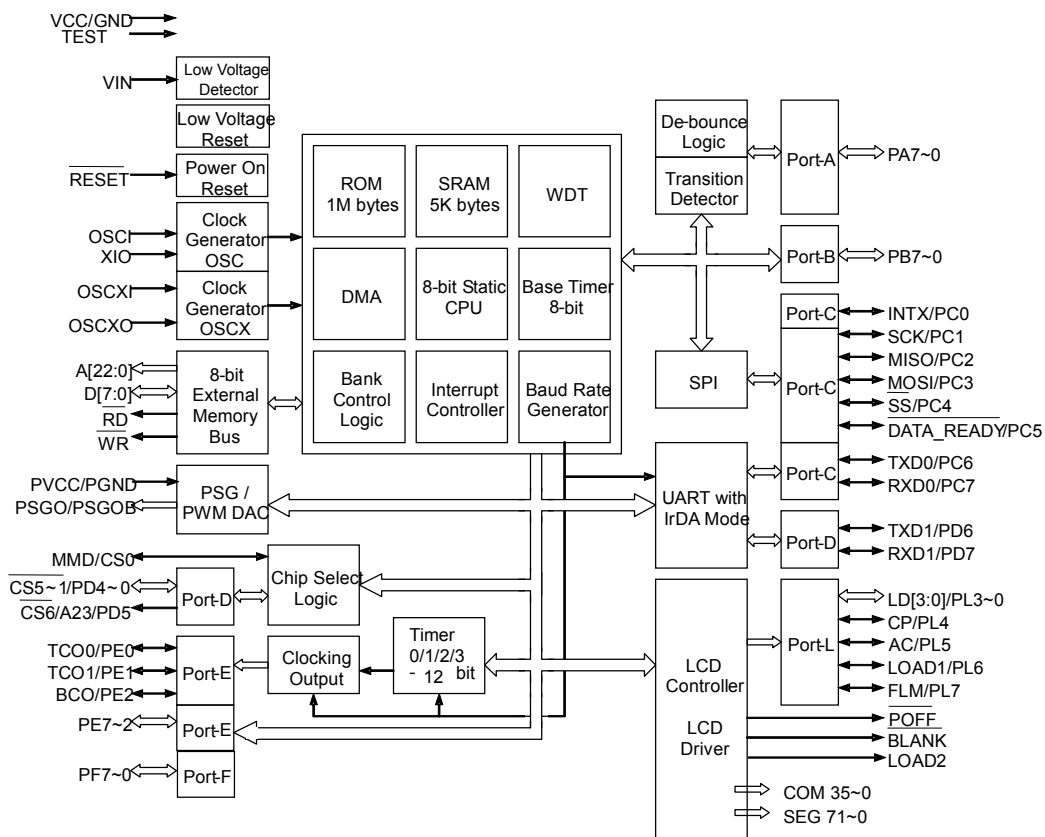The block diagram of ST2608B is shown in the following figure.

2 BLOCK DIAGRAM

FIGURE 2-1 ST2608B Block Diagram

3 FEATURES

- Totally static 8-bit CPU
- ROM: 1M x 8-bit
- RAM: 5K x 8-bit
- Stack: Up to 128-level deep
- Operation voltage: 2.4V ~ 3.6V
- Operation frequency:
  – 3.0Mhz@2.4V(Min.)
  – 4.0Mhz@2.7V(Min.)
- LCD Drives
  – COM: 36 outputs. Eight shared with one output port
  – SEG: 72 outputs. Shared with 3 I/O ports and memory bus signals.
- One 8x8 Signed Multiplier
- Low Voltage Reset (LVR)
  – Two levels by code option
- Low Voltage Detector (LVD)
  – Programmable 4 levels
  – System power or external battery level can be detected.
- Programmable Watchdog Timer (WDT)
- Memory interface to ROM, RAM, Flash
- Memory configuration
  – Three kinds of banks for program, data and interrupt
  – 12-bit bank registers support up to 44M bytes
  – Six programmable chip-selects with 4 modes
  – Maximum single device of 16M bytes
- General-Purpose I/O (GPIO) ports
  – Up to 56 bit programmable CMOS I/Os
    32 shared with LCD drives
  – 8 open drain output pins shared with LCD COMs
  – Hardware de-bounce option for Port-A
  – Bit programmable pull-up for input pins
  – Pull-up/down and open-drain/CMOS control for Port-C
- Timer/Counter
  – Four 12-bit timers.
  – One 8-bit base timer
  – Seven fixed base timers
- Three clocking outputs
  – Clock sources including Timer0/1, baud rate generator
- Eleven prioritized interrupts with dedicated exception vectors
  – External interrupt (edge triggered)
  – PortA interrupt (transition triggered)
  – LCD buffer interrupt
  – Base timer interrupt
  – Timer0~3 interrupts (x4)
  – SPI interrupts (x2)
  – UART interrupts (x2)

- Dual clock sources with warm-up timer
  – Low frequency crystal oscillator (OSCX)
    .... 32768 Hz
  – High frequency resistor or crystal/resonator oscillator (OSC) selected by pin option .... 455K~4M Hz
- Direct Memory Access (DMA)
  – Block-to-Block transfer
  – Block to Single port
- LCD Power Management
  – DC-DC converter with 8-level output control
  – LC driving voltage regulator with 16-level control
  – 1/4, 1/5, 1/6 bias options with 4 voltage followers
- LCD Driver
  – 32x28~72x36 resolution, maximum 2592 dots
  – Clock source from OSC/OSCX.
  – Internal bias resistors(1/4, 1/5, 1/6 bias).
- LCD Controller (LCDC)
  – Software programmable display size up to 240X160
  – B/W, Hardware 4/16 gray levels with 5-bit palette
  – Support 1-/4-/8-bit LCD data bus
  – Share system memory with display buffer and with no loss of the CPU time
  – LCD buffer extension function to combine both internal and external RAM for larger display
  – Diverse functions including virtual screen, panning, scrolling, contrast control and alternating signal generator
- Programmable Sound Generator (PSG)
  – Four channels with three playing modes:
    9-bit ADPCM, 8-bit PCM and 8-bit melody
  – One 16-byte buffer and 6-bit volume control per channel
  – Wavetable melody support
  – Two dedicated PWM outputs for direct driving
  – One 12-bit current DAC
- Universal Asynchronous Receiver/Transmitter (UART)
  – Full-duplex operation
  – Baud rate generator with one digital PLL
  – Standard baud rates of 600 bps to 115.2 kbps
  – Both transmitter and receiver buffers supported
  – Direct glueless support of IrDA physical layer protocol
  – Two sets of I/Os (TX,RX) for two independent devices
- Serial Peripheral Interface (SPI)
  – Master and slave modes
  – Five serial signals including enable and data-ready
  – Both transmitter and receiver buffers supported
  – Programmable data length from 7-bit to 16-bit
- Three power down modes
  – WAI0 mode
  – WAI1 mode
  – STP mode
- Vlcd/LVD trimming fuse function:
  – Vlcd default voltage variation trimming.
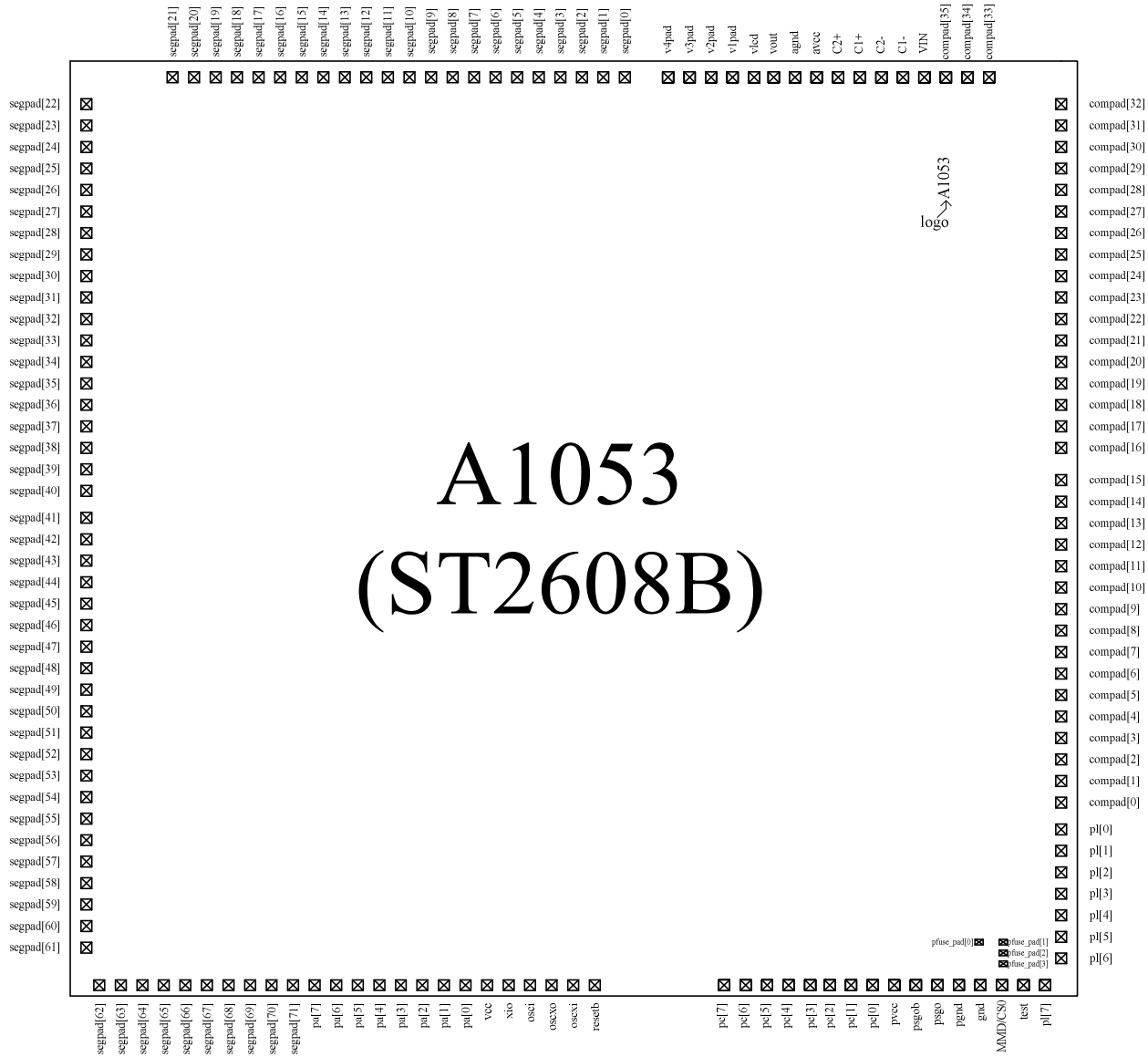 – 4-level LVD voltage variation trimming.

4   SIGNAL DESCRIPTIONS

1.   Signal Function Groups

Function Group	Pad No.	Designation	Description
Power		VCC , PVCC, AVCC	**VCC:** Power supply for system **AVCC:** Power supply for LCD function **PVCC:** Power supply for PSGO and PSGOB **NOTE: PVCC level must not be higher than VDD level.**
Ground		GND , PGND	**GND:** System power ground **PGND:** Power ground for PSGO and PSGOB

System control		$\overline{\text{RESET}}$,
		TEST,
		MMD/$\overline{\text{CS0}}$
			$\overline{\text{RESET}}$: Active low system reset signal input
			TEST: Leave this pin open when normal operation
			MMD/$\overline{\text{CS0}}$: Memory modes selection pin
			Normal mode: Enable internal ROM.
			  MMD/$\overline{\text{CS0}}$ is connected to GND.
			Emulation mode: Disable internal ROM.
			  MMD/$\overline{\text{CS0}}$ is connected to the chip-select pin of external ROM. During reset period, the MMD/$\overline{\text{CS0}}$ is an internally pulled-up input pin. After reset cycles, MMD/$\overline{\text{CS0}}$ is changed to be an output pin. It will output signal $\overline{\text{CS0}}$.

Clock		XIO,OSCI OSCXO,OSCXI, ,	High frequency oscillator (OSC) mode selected by code-option **Crystal mode:** One crystal or resonator should be connected between OSCI and XIO **Resistor oscillator mode:** One resistor should be connected between OSCI and VCC **OSCXI, OSCXO:** Connect one 32768Hz crystal between these two pins when using low frequency oscillator
External memory bus signals / LCD drivers		$\overline{\text{WR}}$ / SEG9, $\overline{\text{RD}}$ / SEG8	External memory R/W control signals / LCD Segment drivers
		A[22:0]/SEG32~SEG10	External memory address bus / LCD Segment drivers
		D[7:0]/SEG7~SEG0	External memory data bus / LCD Segment drivers
PSG/PWM DAC		PSGO, PSGOB	PSG outputs. Connect to one buzzer or speaker
Keyboard scan signal (return line)		PA7~0	I/O port A
GPIO / LCD drivers		PB7~0/SEG63~SEG56	I/O port B / LCD Segment drivers
Chip selects / LCD drivers		$\overline{\text{CS5}} \sim \overline{1}$/PD4~0 / SEG37~SEG33, $\overline{\text{CS6}}$ /A23/PD5 /SEG38	I/O port D and chip-select outputs / LCD Segment drivers
UART		RXD0/PC7,TXD0/PC6, RXD1/PD7/SEG40,TXD1/ PD6/SEG39	UART signals and I/Os / LCD Segment drivers
SPI		$\overline{\text{DATA\_READY}}$ /PC5 , $\overline{\text{SS}}$ /PC4 , SDO/PC3 , SDI/PC2 , SCK/PC1	SPI signals and I/Os

Function Group	Pad No.	Designation	Description
External clock/signal interrupt		INTX/PC0	External interrupt inputs
Clocking output		BCO/PE2/SEG66 , TCO1/PE1/SEG65 , TCO0/PE0/SEG64	Clocking outputs / LCD Segment drivers
GPIO / LCD drivers		PE7~3/SEG71~SEG67	I/O port E/ LCD Segment drivers
LCD control signals (for controller mode)		BLANK/COM0, POFF/COM1, FLM/COM2, LOAD1/COM3, LOAD2/COM4, AC/COM5,CP/COM6, EIO/COM7, LD7~LD0/COM15/COM8	LCD control signals
LCD voltage source		Vout, Vlcd, V1, V2, V3, V4	LCD voltage sources
LCD voltage booster		C1+, C1-, C2+, C2-	Connect a 0.1 uF between C1+ and C1-, C2+ and C2- repectively.
Low Voltage Detector		VIN	Analog input pin of Low Voltage Dector module

5 PAD DIAGRAM

A1053
(ST2608B)

logo A1053

Left side (top to bottom): segpad[22], segpad[23], segpad[24], segpad[25], segpad[26], segpad[27], segpad[28], segpad[29], segpad[30], segpad[31], segpad[32], segpad[33], segpad[34], segpad[35], segpad[36], segpad[37], segpad[38], segpad[39], segpad[40], segpad[41], segpad[42], segpad[43], segpad[44], segpad[45], segpad[46], segpad[47], segpad[48], segpad[49], segpad[50], segpad[51], segpad[52], segpad[53], segpad[54], segpad[55], segpad[56], segpad[57], segpad[58], segpad[59], segpad[60], segpad[61]

Top side (left to right): segpad[21], segpad[20], segpad[19], segpad[18], segpad[17], segpad[16], segpad[15], segpad[14], segpad[13], segpad[12], segpad[11], segpad[10], segpad[9], segpad[8], segpad[7], segpad[6], segpad[5], segpad[4], segpad[3], segpad[2], segpad[1], segpad[0], v4pad, v3pad, v2pad, v1pad, vlcd, vout, agnd, avcc, C2+, C1+, C2-, C1-, VIN, compad[35], compad[34], compad[33]

Right side (top to bottom): compad[32], compad[31], compad[30], compad[29], compad[28], compad[27], compad[26], compad[25], compad[24], compad[23], compad[22], compad[21], compad[20], compad[19], compad[18], compad[17], compad[16], compad[15], compad[14], compad[13], compad[12], compad[11], compad[10], compad[9], compad[8], compad[7], compad[6], compad[5], compad[4], compad[3], compad[2], compad[1], compad[0], pl[0], pl[1], pl[2], pl[3], pl[4], pl[5], pl[6]

pfuse_pad[0], pfuse_pad[1], pfuse_pad[2], pfuse_pad[3]

Bottom side (left to right): segpad[62], segpad[63], segpad[64], segpad[65], segpad[66], segpad[67], segpad[68], segpad[69], segpad[70], segpad[71], pd[7], pd[6], pd[5], pd[4], pd[3], pd[2], pd[1], pd[0], vca, xir, osc1, osc0, oscei, resetb, pc[7], pc[6], pc[5], pc[4], pc[3], pc[2], pc[1], pc[0], pvcc, psgob, psgo, pgnd, gnd, MMD/CS0, test, pl[7]

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rations

DC Supply Voltage ----------------------------- -0.3V to +4.5V
Operating Ambient Temperature ---------- -10°C to +60°C
Storage Temperature ----------------------- -10°C to +125°C

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. All the ranges are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

6.2 DC Electrical Characteristics

Standard operation conditions: VCC = 3.0V, GND = 0V, T_A = 25°C, OSC = 4M Hz, unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	VCC	2.4	3.0	3.6	V	Fosc = 3MHz
		2.7	3.0	3.6	V	Fosc = 4MHz
Operating Frequency	F_1	-	-	3	MHz	VCC = 2.4V ~ 3.6V
Operating Frequency	F_2	-	-	4	MHz	VCC = 2.7 ~ 3.6V
Operating Current	I_{OP}		2.5	3	mA	All I/O port are input and pull-up, execute NOP instruction, LCDC on
Standby Current	I_{SB0}		450	550	μA	All I/O port are input and pull-up, OSCX on, LCDC off (WAIT0 mode)
Standby Current	I_{SB1}		3.5	5	μA	All I/O port are input and pull-up, OSCX on, LCDC off (WAIT1 mode)
Standby Current	I_{SB2}		0.5	1	μA	All I/O port are input and pull-up, OSCX off, LCDC off (WAIT1 mode)
Standby Current	I_{SB3}		100	130	υA	LCD on, LCDCK=32Kz, Wait0, no panel
Input High Voltage	V_{IH}	0.7Vcc		Vcc+0.3	V	Port-C/D/E/L
		0.85Vcc			V	$\overline{RESET}$
Input Low Voltage	V_{IL}	GND-0.3		0.3Vcc	V	Port-C/D/E/L
				0.15Vccc	V	$\overline{RESET}$
Pull-up resistance	R_{IH}		150		KΩ	Port-C/D/E/L (input Voltage=0.7VCC)
Output high voltage	V_{OH1}	0.7Vcc			V	Port-C/D/L (I_{OH} =-6mA)
Output low voltage	V_{OL1}			0.3Vcc	V	Port-C/D/E/L (I_{OL} =9mA)
Output high voltage	V_{OH2}	0.7Vcc			V	PSG0/PSG0B(in PWM mode), I_{OH} = 35mA.
Output low voltage	V_{OL2}			0.3Vcc	V	PSG0/PSG0B(in PWM mode), I_{OL} = -65mA.
DAC current		2.4mA	3.0	3.6mA		DAC output current of maximum digital input value
Low Voltage Detector current	I_{LVR}		30	60	μA	Total LVD current consumption
Vlcd variation		-3%		+3%		
INT LVD variation		-4%		+4%		
EXT LVD variation		-4%		+4%		
SPI clock frequency				4.0	MHz	SPI slave mode

6.3 AC Electrical Characteristics
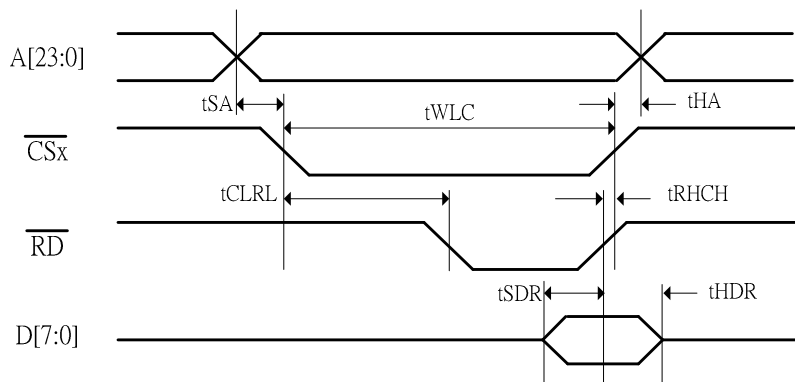
External Read Timing Diagram
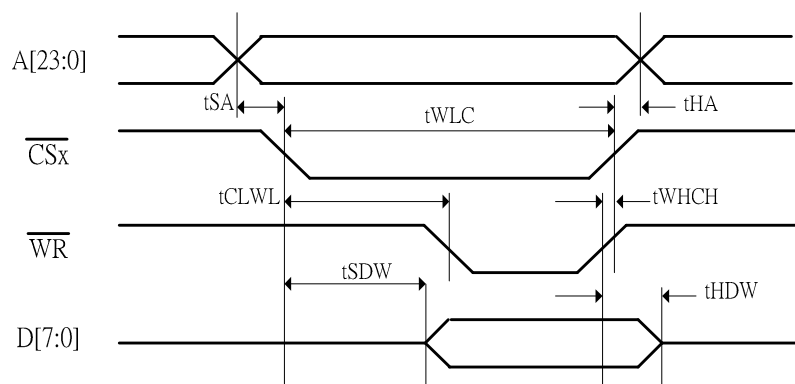
External Write Timing Diagram

TABLE 6-1 Timing parameters for 0 and 0

Standard operation conditions: VCC = 3.0V, GND = 0V, T_A = 25°C

Symbol	Characteristic	Rating			Unit
		Min.	Typ.	Max.	
tSA	Address setup time	—	—	10	ns
tHA	Address hold time	0	—	—	ns
tWLC	CS "L" pulse width	166	—	—	ns
tCLWL	CS asserted to $\overline{WR}$ asserted	—	1/2 tWLC	—	ns
tWHCH	CS negated after $\overline{WR}$ is negated	10	—	—	ns
tSDW	CS asserted to data-out is valid	—	1/2 tWLC	—	ns
tHDW	Data-out hold time after $\overline{WR}$ is negated	20	—		ns
tCLRL	CS asserted to $\overline{RD}$ asserted	—	1/2 tWLC	—	ns
tRHCH	CS negated after $\overline{RD}$ is negated	10	—	—	ns
tSDR	Data-in valid before $\overline{RD}$ is negated	30	—	—	ns
tHDR	Data-in hold time after $\overline{RD}$ is negated	10	—	—	ns
tR	Signal rise time	—	20	—	ns
tF	Signal fall time	—	10	—	ns

6.4   Characteristic Charts

Frequency of R-OSC as a function of VCC
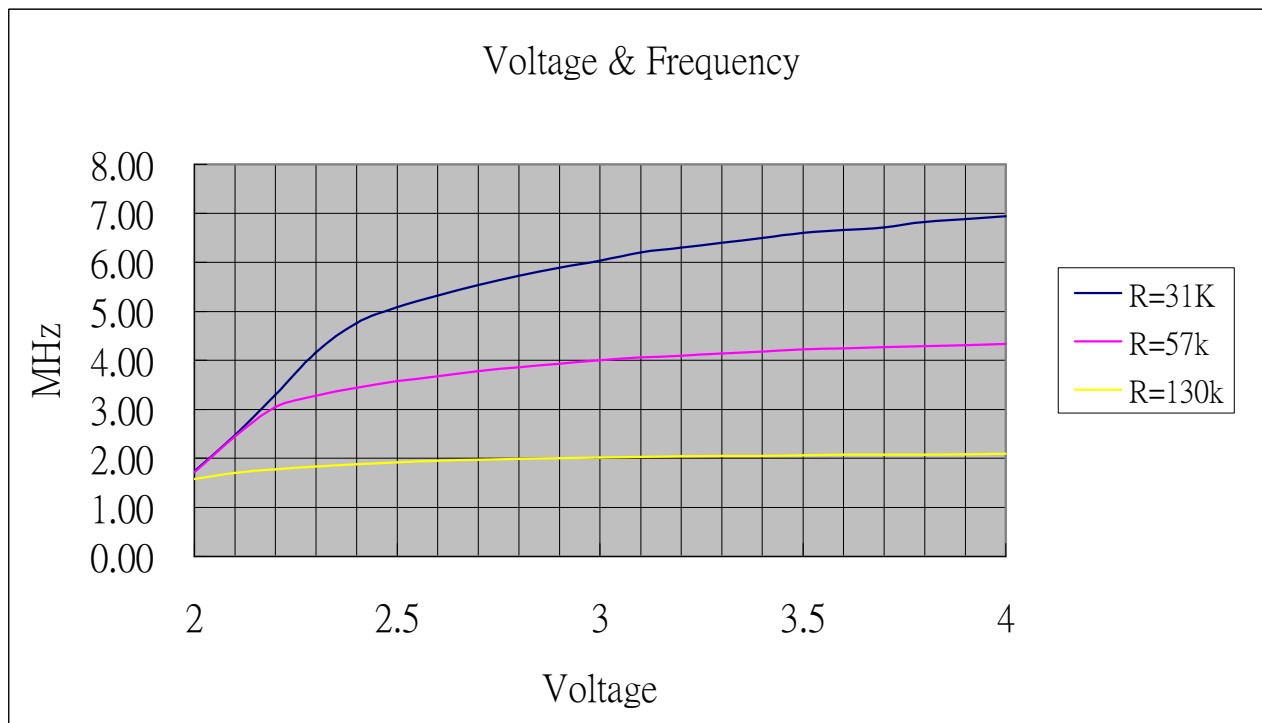
Frequency of R-OSC as a function of Resistor

Fosc VS. Rosc
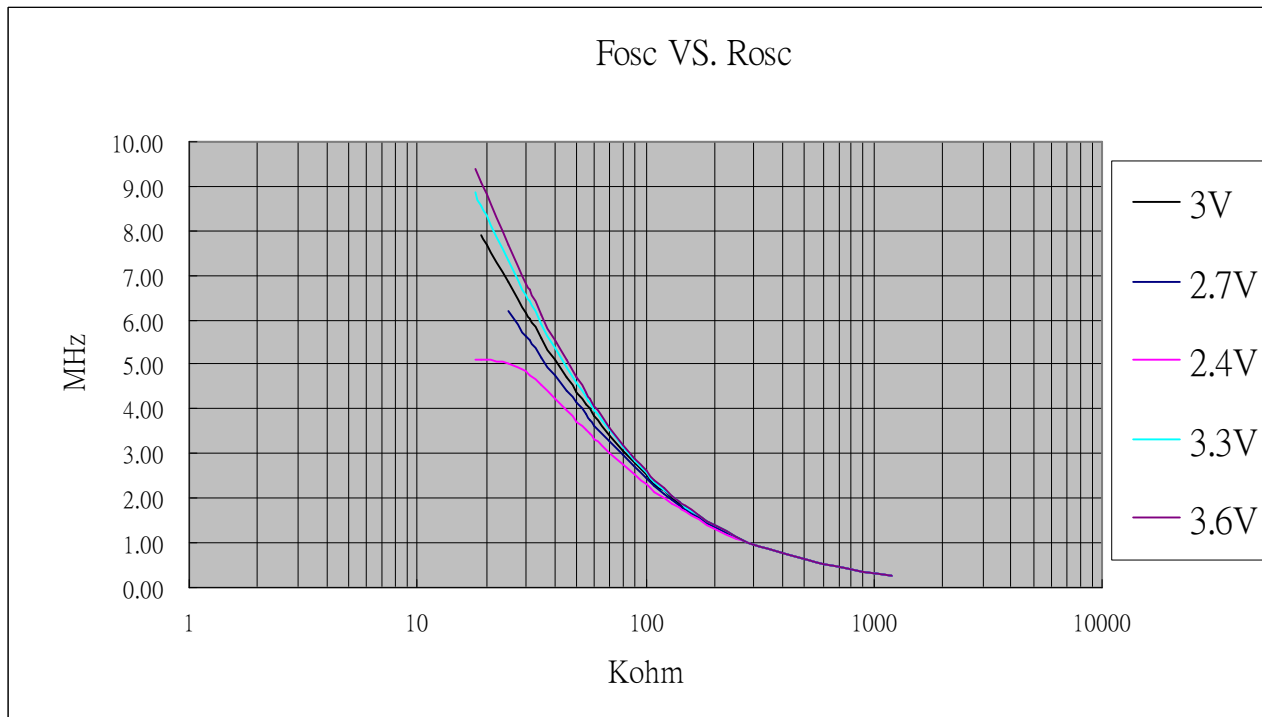
Voltage / Frequency	3V
4MHz	57K Ohm
3MHz	80K Ohm
2MHz	130K Ohm
1MHz	300K Ohm
0.5MHz	600K Ohm

7   APPLICATION CIRCUITS
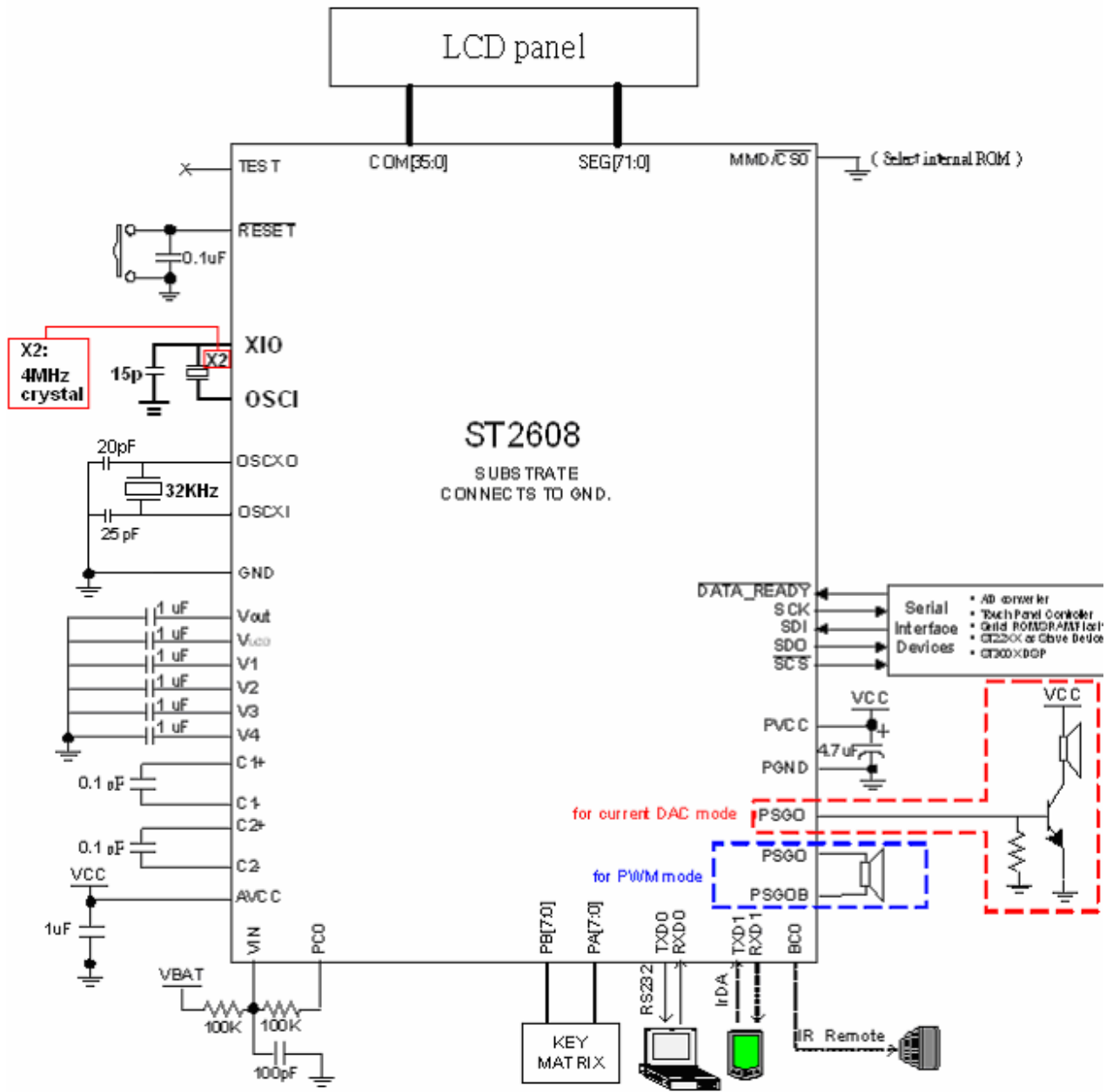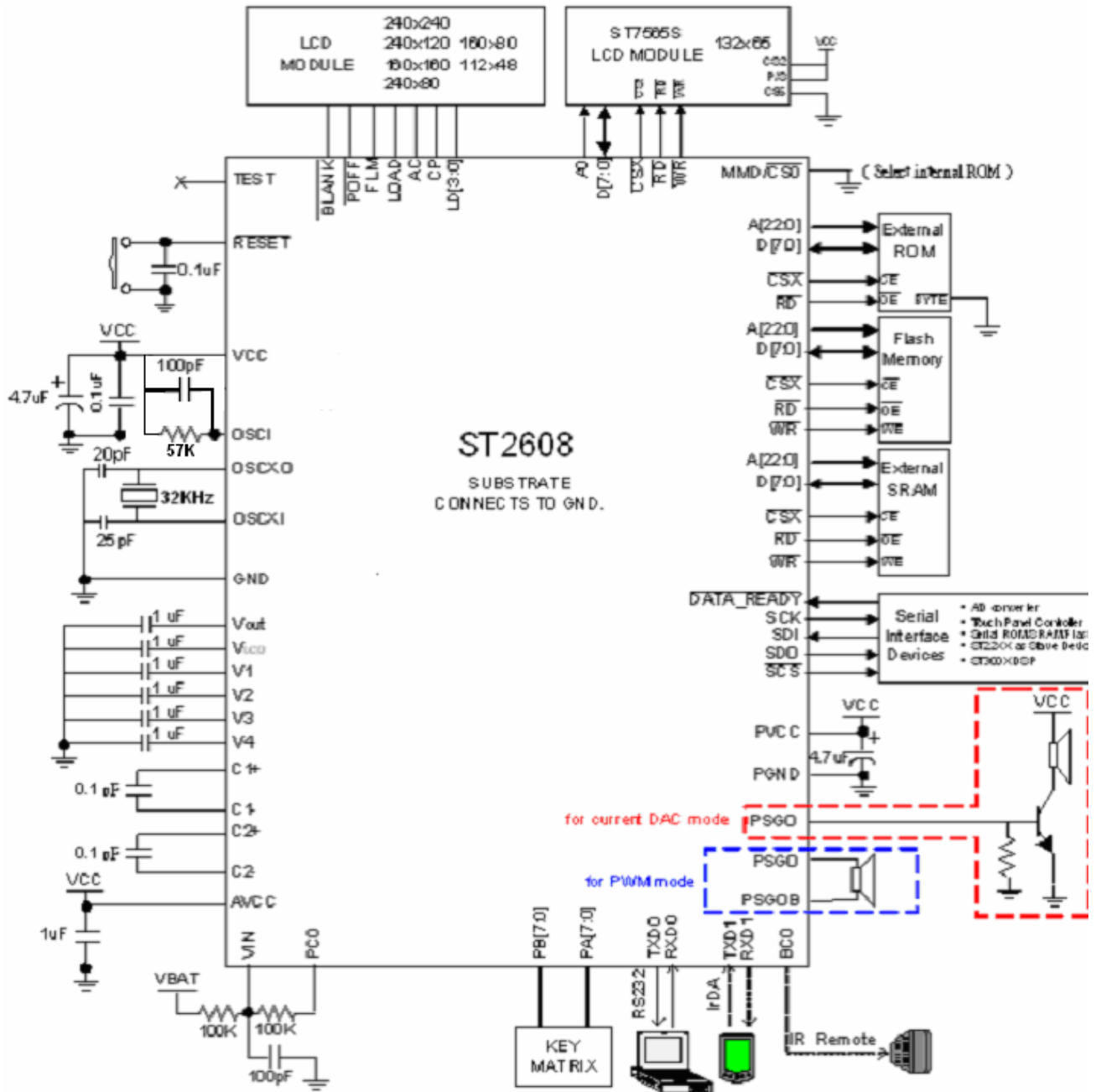
ST2608B+ST8008+ST8009 Application Circuit
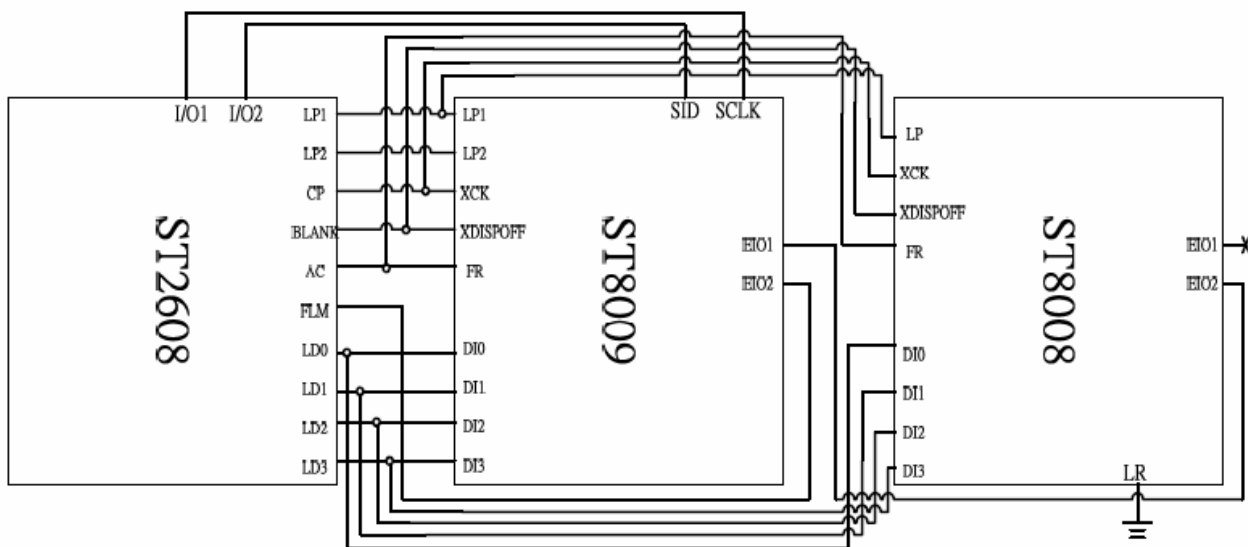
Feature comparison of st2600B series

Part Number	ST2608B	ST2604B	ST2602B	ST2601B
ROM	1M Byte	512K Byte	256K Byte	128K Byte
RAM	5K Byte	3.5K Byte	2.5K Byte	1.5K Byte
Built-in LCD Driver	36 COMs X 72 SEGs	36 COMs X 64 SEGs	36 COMs X 56 SEGs	36 COMs X 56 SEGs
Driving LCD with ext. driver	~9000 dots (16 gray) ~36000 dots (mono)	~6000 dots (16 gray) ~24000 dots (mono)	~4000 dots (16 gray) ~16000 dots (mono)	~2500 dots (16 gray) ~10000 dots (mono)
Dedicated I/O	24 (PA, PC, PL)	16 (PA, PC)	8 (PC)	8 (PC)
LCD-Shared I/O	32 (PB, PD, PE, PF)	39 (PB[6:0], PD, PE, PL, PF)	31 (PD, PE[6:0], PL, PF)	31 (PD, PE[6:0], PL, PF)
LCD gray level	16 gray levels			
PSG / volume-control	4-channel wavetable / 64 levels			
DAC	9-bit PWM, 12-bit current DAC			
Low voltage detector	4 levels			
Low voltage reset	Yes			
Watchdog timer	Yes			
Serieal interface	UART, SPI, IrDA			
Trimming fuse	YES			

Feature comparison of st2608 and ST2608B:

Part Number	ST2608	ST2608B
ROM	1M Byte	1M Byte
RAM	5K Byte	5K Byte
Built-in LCD Driver	36 COMs X 72 SEGs	36 COMs X 72 SEGs
Driving LCD with ext. driver	~9000 dots (16 gray) ~36000 dots (mono)	~9000 dots (16 gray) ~36000 dots (mono)
Dedicated I/O	24 (PA, PC, PL)	24 (PA, PC, PL)
LCD-Shared I/O	32 (PB, PD, PE, PF)	32 (PB, PD, PE, PF)
Basically functions	The same	The same
LCDCK = 32KHz	NO	YES
PSG volume maximum	normal	2-time larger than ST2608
Vlcd variation(VDD=2.4~3.6)	~300mV	~50mV
Current consumption of LVD	200uA	30uA
DAC	10-bit	12-bit
Trimming fuse	No	Yes

7.1   LCFG Setting Difference of ST260xx series IC

ST2608 / ST2608B

CFGS[2~0]	Pad Definition								
	SEG0~31	SEG32	SEG33~38	SEG39	SEG40	SEG41~47	SEG48~55	SEG56~63	SEG64~71
00X	SEG0~71								
010	SEG0~63								PE0~PE7
011	SEG0~55							PB0~PB7	PE0~PE7
100	SEG0~47						No Use	PB0~PB7	PE0~PE7
101	SEG0~31	No Use	PD0~PD7			No Use		PB0~PB7	PE0~PE7
110	A/D Bus	PD0~PD6		SEG0~31					
111	A/D Bus	PD0~PD7			No Use			PB0~PB7	PE0~PE7

ST2604 / ST2604B

CFGS[2~0]	Pad Definition						
	SEG0~31	SEG32	SEG33~39	SEG40	SEG41~47	SEG48~55	SEG56~63
000	SEG0 ~ 63						
001	SEG0 ~ 39			PD7	PB0 ~ 6	PE0 ~ 7	PL0 ~ 7
010	SEG0 ~ 63						
011	SEG0 ~ 55						PL0 ~ 7
100	SEG0 ~ 47					PE0 ~ 7	PL0 ~ 7
101	SEG0 ~ 31	A22	PD0 ~ 7		PB0 ~ 6	PE0 ~ 7	PL0 ~ 7
110	A/D bus	PD0 ~ 7			PB0 ~ 6	PE0 ~ 7	PL0 ~ 7
111	A/D bus	PD0 ~ 7			PB0 ~ 6	PE0 ~ 7	PL0 ~ 7

ST2602 / ST2604B

CFGS[2~0]	Pad Definition					
	SEG0~31	SEG32	SEG33~39	SEG40	SEG41~47	SEG48~55
000	SEG0 ~ 55					
001	SEG0 ~ 39			PD7	PE0 ~ 6	PL0 ~ 7
010	SEG0 ~ 55					
011	SEG0 ~ 55					
100	SEG0 ~ 47					PL0 ~ 7
101	SEG0 ~ 31	A22	PD0 ~ 7		PE0 ~ 6	PL0 ~ 7
110	A/D bus	PD0 ~ 7			PE0 ~ 6	PL0 ~ 7
111	A/D bus	PD0 ~ 7			PE0 ~ 6	PL0 ~ 7

8   CHECK LIST

CHECK LIST of ST2608B-□□□□	
8-Bit Microcontroller With 1M Bytes ROM	
CODE OPTION LOW VOLTAGE RESET	□1.4 Volt □2.1 Volt
OSCILLATOR	□32768 Hz Crystal □R-OSC _____ MHz (Resistor = _____ KΩ) □Resonator □Crystal _____ MHz
OPERATING VOLTAGE	□2.4V ~ 3.6V □2.7V ~ 3.6V □Regulator _____V □Other Range _____ ~ _____V <u>Note</u>: Maximum operating frequency = <u>4.0 Mhz@2.7~3.6V</u>, <u>3.0 Mhz@2.4~3.6V</u>
BATTERY	□CR20____x ____ □AAx ____ □AAAx ____ □ others _____
POWER DOWN MODES	□WAI-0 □WAI-1
LOW VOLTAGE DETECTOR	Disabled □Internal-LVD level1(2.4V) □Internal-LVD level2(2.6V) □Internal-LVD level3(2.8V) □Internal-LVD level4(3.0V) □External-LVD level1(1.2V) □External-LVD level2(1.3V) □External-LVD level3(1.4V) □External-LVD level4(1.5V)
UART	□Enabled, Baud Rate: _____ bps □Disabled
SPI	□Enabled, Bit Rate: _____ bps □Disabled
ST2600B EV mode Selection Please check ST2600B DVB (PCB-300)	□ ST2602B EV mode: JP58 2→3 JP59 1→2 □ ST2604B EV mode: JP58 1→2 JP59 2→3 □ ST2608B EV mode: JP58 2→3 JP59 2→3 SITRONIX PCB-300 JP58 JP59 □ □ ST2600B COB
LCD SPECIFICATIONS	Resolution: _____x_____ Duty: 1/____ Bias: 1/____ VLCD: ____V Frame Rate: ____Hz Driver: □ST8012x___ □ST8008x___ □ST8009x___ □ST8011x_____
LCD Gray-level	□Black and White □4 Gray-level □16 Gray-level
PSG mode	Current-type DAC PWM-single pin □ PWM-two pin push pull □PWM-two pin two end
Register Value	When playing sound: the PSGC = _____ , When LCD is on: LCKR= _____ , LCTR= _____ , LFRA = _____ ,LXMAX= _____ , LYMAX= _____ , LPOW = _____ LREG = _____ , LCFG = _____ When LVD is on: LVCTR = _____ When power down: SYS = _____ (WAIT0 or WAIT1)
Data sheet	ST2608B user's manual Ver_____
CODE FILE: _____ .BIN	DATE(Y/M/D): 20____/ ____/ ____

CHECK SUM: ☐☐☐☐H (Byte Mode)

Note: File format must be binary and the extension should be ".BIN".
b. File should be wrapped in ZIP format for transferring or e-mailing.
c. Only single file is allowed.
d. File length is 1M bytes.
e. Functions should be checked on the emulation board or by real chip.
f. Electric characteristics of the emulation board are not identical with those of the real chip.

CUSTOMER	
COMPANY	
SIGNATURE	
SITRONIX	
FAE/SA	
SALSE	

Project Name _____   DATE: _____

	ITEM	CHECK	NOTE
1.	Make sure the resistor of R-OSC matches the desired frequency and VCC		
2.	Make sure the referenced data sheet is the most updated version		
3.	After power on, enter wait-0 mode for0.5 second before normal operation		
4.	Initialize user RAM and every related control register		
5.	Confirm Vlcd level, duty, bias, frame rate, alternating rate and the display quality of LCD		
6.	Make sure to set LCKR=00h before turning off LCD function		
7.	Make sure to implement a mechanism to fine-tune LCD contrast level. The mechanism could be pin-option or keying-adjustment.		
8.	Confirm PSG output mode: Current DAC or one of three PWM modes		
9.	Before entering power down mode, turn off unused peripheral such as LCD controller, PSG, Current DAC and LVD		
10.	Confirm I/O direction, default state and function-enable bits. Enable pull-up for unused input pins		
11.	Read from an input port after the signals are stable. Ex. when doing key scan, delay 12 us from a new scan value then read the return lines.		
12.	If an input connects to VCC or GND directly, make sure to remove any DC current from internal pull-up/down resistor after the status is read.		
13.	Do not use "read-modify-write" instructions, e.g. ROR and SMB0, to the registers that are read-only, write-only or have different functions for read and write. The registers at least include PA ~ PF, PL, PCL, PSGxA, PSGxB, TxCH, TxCL, PRS, BTSR, BTC, MULL, MULH, MISC, SYS, IREQL, IREQH, LSSAL, LSSAH, LVPW, LCKR, LFRA, LPAL, SDATAH, SDATAL, SSR, DMSL, DMSH, DMDL, DMDH, DCNTL, DCNTH, LVCTR, UDATA and USR.		
14.	Disable unused functions and reserve "RTI" instruction for unused interrupt vectors		
15.	Always disable interrupt function (by an 'SEI' instruction) when modifying the IENAL, IENAH, IREQL and IREQH registers.		
16.	Check stack memory is limited within 256 bytes.		
17.	Design a test mode to check every possible function		
18.	Follow the standard operation flow of using LCDCK=32KHz.		
19.	Use ST2600B (enable ST2608B EV mode), to develop the whole system., and verify every functions, especially sound quality and LCD performance.		
20.	RC-type OSC has inter-sample variation. For frequency-sensitive application (for example:IR communication and speech sampling rate), please use 32KHz_OSC to calibrate RC-type OSC by firmware		
21.	Fill up ROM until there has no empty place. (total 1048576 bytes (1MB))		
22.	Make sure LCKR[5]=0		

Engineer _____   Manager _____

ST26xxB application note:

Content:

Version 1.09

<PSG: Current-DAC and PWM application circuit>

Description:
(These AP circuits are suitable for ST26xx series IC)
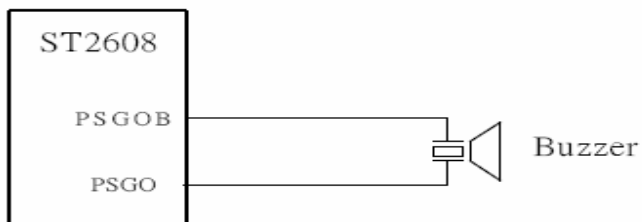
Figure 1 PWM mode application circuit
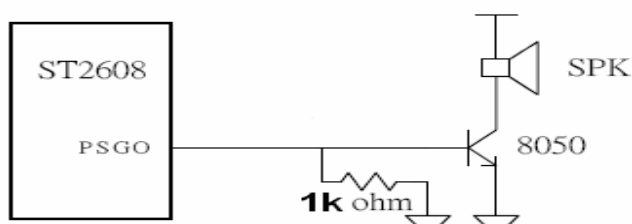
Figure 2 Current-DAC mode application circuit

<Methods to make up LCD voltage deviation >

Notice1: In order to cover the variation of VLCD of LCD panel, be sure to reserve pin-option by GPIO to change the status of VLCD(bit0:3 of register LREG). Here we suggest that there are at least 5-level of voltage pin-option for VLCD. If the GPIO is not enough to make pin-option, programmer can use key-return-line method for power on pin-option.

For example: make pin-option for change VLCD at…/5.6/5.8/**6.0V**/6.2V/6.4/…

Notice2: Programmer should add a contrast controller function to adjust VLCD for the convenience of end-user to change the contrast as they like.

For example: VLCD is pre-set at **6.2** by pin-option, end-users can also adjust the contrast…/5.8/5.9V/6.0V/**6.2V**/6.2V/6.3/6.4/…by using contrast controller function.

Notice3: Verifying the performance of voice on ST2602/2604/2608 DEMO boards.   Because ST2600B DVB can not provide the totally voice efficacy, such like the volume and the quality of voice. So we strongly suggest to verify voice playing on ST2602B/ST2608B DEMO boards before MASK.
(Ps…Because LCD SEG pins are shared with external EPROM, so the picture can not be verified on DEMO boards.)

<Vertical Cross talk on LCD display>

Description: Vertical Cross talk on LCD display
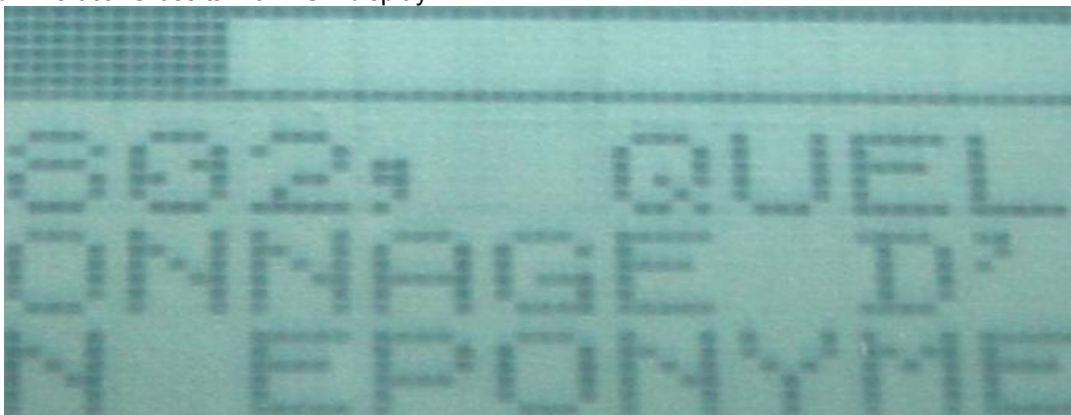
Solution: Vertical cross talk usually happens when the differential voltage of V0~V4 are not closely. In this case, increase C0~C4 (recommend > 1uF) will eliminate this problem. Fine tuning the value of capacitance to get the best LCD quality.

<How to use IrDA mode to generate 38kHz carrier with data?>
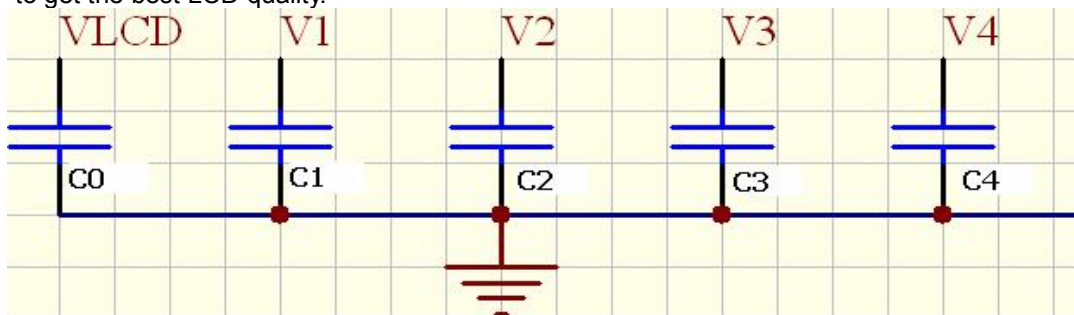
Port-E-2(PE2) is shared with clock signal output function, and the frequency of this pin is programmable. Programmer can define which signal pattern is "0", and which signal is "1"

For example, using Timer_interrupt to enable/disable PE2 function, and programmers can produce the signal pattern which means "0" or "1"
The same way, receive side can decode the signal by encode information.

<LCDCK=32k clock source on ST2602B/ST2608B display>
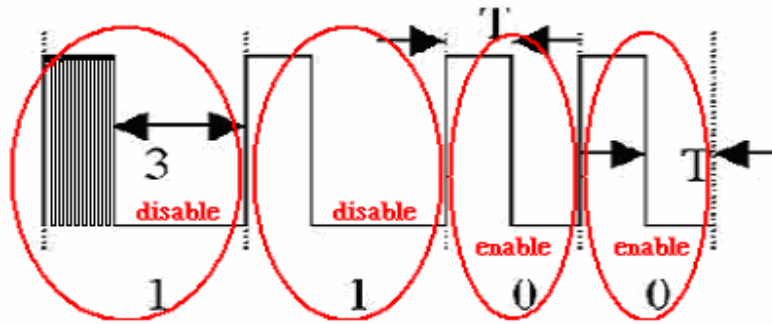
(1) Control register

Address	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
$047	LCTR	R/W	LPWR	BLNK	REV	CAS	GL[3]	GL[2]	GL[1]	GL[0]	1000 0000

Bit 3~2:   **GL[3:2]** : LCD gray-level selection bit
00 = B/W.
01 = 4 gray
10 = 16gray
11 = fast B/W mode

(2)

Address	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
$048	LCKR	W	-	-	LMOD[1]	LMOD[0]	LCK[3]	LCK[2]	LCK[1]	LCK[0]	- - 00 0000

Bit [5:4]:   **LMOD** : LCD data bus mode selection
00 = 1-bit mode
01 = 4-bit mode
1X = 8-bit mode

Bit 3~0: **LCKR[3:0]** : LCD clock selection (when SYSCK=OSCK)

LCKR[3:0]	LCDCK (B/W, 4G, 16G mode)			LCDCK (fast B/W mode)		
	1-bit mode (**LMOD**=00)	4-bit mode (**LMOD**=01)	8-bit mode (**LMOD**=1X)	1-bit mode (**LMOD**=00)	4-bit mode (**LMOD**=01)	8-bit mode (**LMOD**=1X)
0000	SYSCK			SYSCK/8		
0001	SYSCK/2			SYSCK/16		
0010	SYSCK /4			SYSCK /32		
0011	SYSCK /6			SYSCK /48		
0100	SYSCK /8			SYSCK /64		
0101	SYSCK /10			SYSCK /80		
0110	SYSCK /12			SYSCK /96		
0111	SYSCK /14			SYSCK /112		
1000	SYSCK /16			SYSCK /128		
1001	SYSCK /18			SYSCK /144		
1010	SYSCK /20			SYSCK /160		
1011	SYSCK /22			SYSCK /176		
1100	SYSCK /24			SYSCK /192		
1101	SYSCK /26			SYSCK /208		
1110	SYSCK /28			SYSCK /224		
1111	SYSCK /30			SYSCK /240		

(3) Sysclk is RC:
1.   Lcd clock source is Sysclk. If Sysclk is RC, LCD clock source will be RC.
2.   In ST2602B, if LCD clock source is RC, B/W, 4G, 16G mode are the same as ST2602.
3.   The fast B/W mode is added. In fast B/W mode, the LCDCK will be divided by 8.
4.   IF Sysclk is RC and in fast B/W mode, the frame rate is determined as below.

$$Frame\ Rate = \frac{LCDCK}{(LXMAX + LFRA + 1) \cdot (LYMAX * 2)}$$

(4) Sysclk is 32K:
1.   If Sysclk is 32k, LCD clock source will be 32k.
2.   If Sysclk is 32k, LCD can only display B/W.
3.   If LCD clock source is 32k, please set GL[3:2]=11(fash B/W mode) . In this condition, LCKR and LPAN control registers will avoid. LCDCK is always 32k hz and the frame rate is only controlled by LFRA control register.
4.   If LCD clock source is 32k, DC-DC converter clock (LPCK) will also become 32k. So, user must to change LPCK register to get higher pump frequency(We will provide a macro to take care this part).
5.   IF Sysclk is 32K and in fast B/W mode, the frame rate is determined by below equation.

$$Frame\ Rate = \frac{LCDCK}{(LXMAX + LFRA + 1) \cdot (LYMAX * 2)}$$, where LCDCK is 32K hz.

(5) change Sysclk from RC to 32K
Step1: let LCD in fast B/W mode
Step2: use the macro "SWITCH_SYSCLK_RC_TO_32K" to change Sysclk to 32K

(6) change Sysclk from 32K to RC

Step1: use the macro "SWITCH_SYSCLK_32K_TO_RC " to change Sysclk to RC

(7) sample code

1. When B/W, 4G, 16G mode change to fast B/W mode or fast B/W mode change to B/W, 4G, 16G mode, must turn off LCD.

for example: B/W, 4G, 16G mode change to fast B/W mode.

```
;====Step1 LCD OFF ===
     LDA  LCTR
     ORA  #10000000B
     STA       LCTR

;====Step2 set GL[3:2]=11, fast B/W mode ===
     LDA  LCTR
     ORA  #00001100B
     STA       LCTR

;=== Step3 set Frame rate about 65 Hz ===
LDA  #6                  ;when Sysclk is changed to 32k, LFRA can't be modified. Thus LFRA
STA       LFRA          ;is determined by equation2. Let the frame rate in sysclk=32k mode is
                            ;about 65hz
LDA  #00001000B         ;since LFRA has been determined, LCKR is determined by frame rate equation.
STA       LCKR          ;Let the frame rate in Sysclk=RC mode is about 65hz

;===Step4 LCD ON ===
     LDA  LCTR
     AND  #~10000000B
     STA       LCTR
```

[After setting up fast B/W mode, then switch SYSCK from RC to 32k]

2. Sysck from RC change to 32k…

Please use the macro "SWITCH_SYSCLK_RC_TO_32K".

This macro will use 4 bytes RAM. They are show below.

```
;===== used ram ====
LCD_FLAG        DS   1
IENAL_BAK            DS    1
IENAH_BAK            DS    1
LPCK_BAK        DS    1
```

And this macro will also use LCD interrupt. Please copy below program in LCD interrupt service routine.

```
;==== LCD interrupt service routine ===
LCDFR_ISR:
     PHA
     LDA  #FFH
     STA       LCD_FLAG
     RMB7      IENAL               ;DISABPLE LCD INTERRUPT
     PLA
     RTI
```

The declaration of this macro is show below (please don't modify this macro)

```
SWITCH_SYSCLK_RC_TO_32K          .MACRO

;=== backup LPCK ===
     LDA  LPCK
     STA       LPCK_BAK
     LDA  #2
     STA       LPCK

;=== BACKUP IENAL/H AND ONLY ENABLE LCD INT ===
     SEI
     LDA  IENAL
     STA       IENAL_BAK
     LDA  IENAH
     STA       IENAH_BAK
     LDA  #10000000B              ;ONLY ENABLE LCD INT
     STA       IENAL
```

```
        STZ     IENAH
        LDA #01111111B
        STA     IREQL               ;CLEAR LCD INT REQUEST
        STZ     LCD_FLAG
        CLI
?WAIT_LCD_INT_RC232K:
        LDA LCD_FLAG
        BEQ ?WAIT_LCD_INT_RC232K

        ;=== change SYSCLK = 32K ===
        LDA SYS
        ORA #10000000B
        STA     SYS
        NOP
        NOP
        NOP
        BBR7 SYS,$
        ;=== RECOVERY IENAL/H ===
        SEI
        LDA IENAL_BAK
        STA     IENAL
        LDA IENAH_BAK
        STA     IENAH
        CLI
        .ENDM
```

3. Sysck from 32K change to RC. (After changing to RC, LCD must be in fast B/W mode.)
Please use the macro "SWITCH_SYSCLK_32K_TO_RC".

```
SWITCH_SYSCLK_32K_TO_RC            .MACRO
        ;=== BACKUP IENAL/H AND ONLY ENABLE LCD INT ===
        SEI
        LDA IENAL
        STA     IENAL_BAK
        LDA IENAH
        STA     IENAH_BAK
        LDA #10000000B              ;ONLY ENABLE LCD INT
        STA     IENAL
        STZ     IENAH
        LDA #01111111B
        STA     IREQL               ;CLEAR LCD INT REQUEST
        STZ     LCD_FLAG
        CLI

?WAIT_LCD_INT_32K2RC:
        LDA LCD_FLAG
        BEQ ?WAIT_LCD_INT_32K2RC

;=== change SYSCLK = RC ===
        LDA SYS
        AND #~10000000B
        STA     SYS
        NOP
        NOP
        NOP
        BBS7 SYS,$
        ;=== RECOVERY IENAL/H ===
        SEI
        LDA IENAL_BAK
        STA     IENAL
        LDA IENAH_BAK
        STA     IENAH
        CLI
        LDA LPCK_BAK
```

```
STA        LPCK
.ENDM
```

<System clock switching from OSC to OSCX>

Cause warm-up time is different when OSC is RC-OSC or X'tal.
To make sure the system clock has switched to OSCX, or error will happen.
Sample code, please follow up…

```
LDA    SYS
ORA    #80H
STA    SYS     ;switch OSC to OSCX
NOP
NOP
NOP
BBR7  SYS,$   ; branch self until OSC is changed to OSCX
```

<Measure RC-OSC system clock>

Since programmer wants to measure the system clock when using RC-OSC, please follow up.

Please connect a 3K-Ohm resistor between Vdd and XIO. You can get a periodic signal output from the XIO pin. It's RC osc signal.

## <IrDA mode application note>

Since IrDA has strictly protocol when transmit/receive data.
We suggest programmers use **X'tal** to be system clock instead of RC-OSC if IrDA signals are needed.
Programmer can use ceramic-OSC to gain some profit since it's cheaper than X'tal.

<ST26xx UART details>

BGRCK: **BGRCK is used to produce UART baud rate, and BGRCK comes from OSC(main frequency) and fine tuning by 32768Hz crystal(REF) to make output baud rate is a stable frequency signal and will not effected by VDD variation.(RC-OSC frequency will change when VDD changes.)**
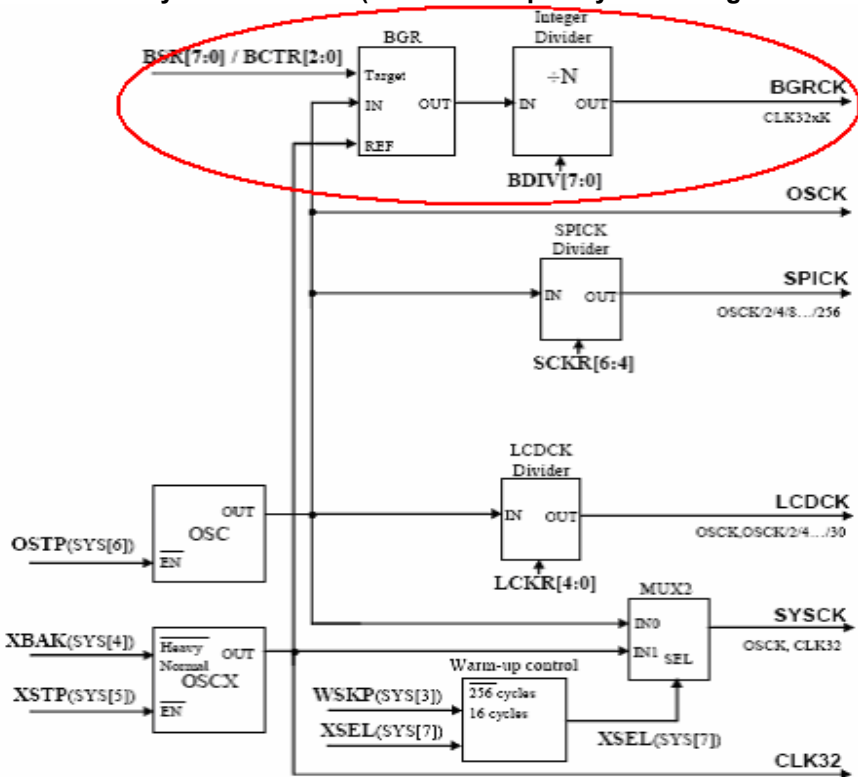
Baud rate: **Baud rate comes from BGRCK, and is determined by BDIV and BRS registers. The "Error rate" of baud rate is the maximum positive/negative inaccuracy of output baud rate.**
For example: If baud rate = 9600bps and OSC is in the rage of 3.72~4.28MHz, programmer should set BRS=61, BDIV=13 to get the best output baud rate which has error of 0.1%.So the real output baud rate will be in the range of [9600x0.999:9600x1.001].
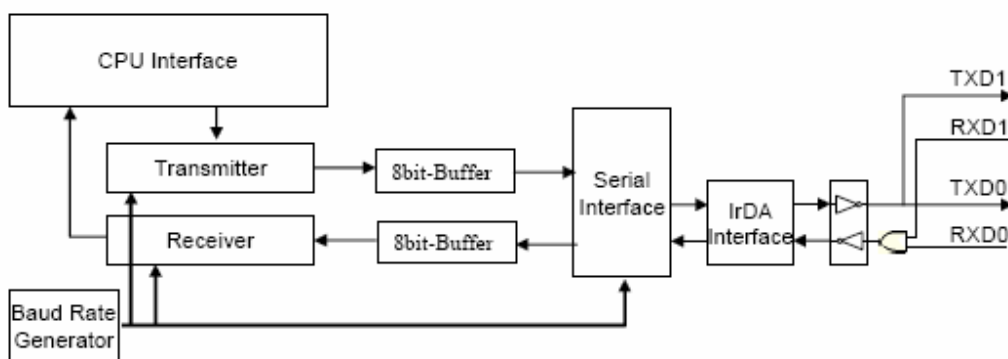
< IrDA BGRCK generation source >

BGRCK can be generated by two ways.

1. When bit7 of BCTR is 0,Haredware PLL which is used to stable BGRCK output will be operated. Cause BGRCK comes from OSC, since RC-OSC can't produce stable frequency, ST26xx hardware will fine tune BGRCK output frequency referenced from 32768Hz crystal to make BGRCK is in the range no matter VDD variation.
2. When bit7 of BCTR is 1:

It's used when OSC is X'tal. Since X'tal can produce stable frequency, and BGRCK comes from OSC, so BGRCK will also be stable if OSC is X'tal. Programmer can get better BGRCK output to make UART signal much more accurate by this way.

When bit7 of BCTR is 1, UART baud rate will be get in the following formula:

baud rate = Sysclk/(BDIV*16) (no need to set "BRS")

< How to avoid LCD blink caused by PSG >

Description:

LCD display may blink when LCD function and PSG function are playing in the same time. LCD blink caused by CPU can 't stand the load of calculation. So the LCD display my lag. And We can find there has blink problem.

Solution:

By using internal DMA function to move LCD data instead of programming method can solve part of this kind of problem. If there still has the same problem, we can separate LCD data into 16 parts and use DMA method to move into LCD RAM. The LCD blink problem can be totally solved.

Example program can be found by SA engineer. !!Please email us!!!

< How to measure the internal current of ST2600B?>

When finish developing program by ST2600B, programmer should measure the current consumption of totally possible situations. In that time programmer can use ST2600B stand alone mode with running external ROM. In order to only measure the current from IC, the power for External ROM should be independent. And then we can measure the current from IC only!!

< Ways to save power consumption >

There are some factors which can effect current consumption…

(1) Main-frequency : Higher frequency needs more current
(2) DAC mode cost much current than PWM mode
(3) Vlcd voltage level : Higher Vlcd pays higher current.
(4) Using EPROM will cost more current than no use.
(5) Input without any connection will randomly cost power
(6) WAIT mode with considerable program can save lots of power
(7) Larger panel will pay more current.
(8) Un-ideal hardware connection will cause unknown current waste.

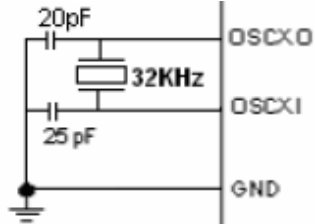## <32KHz (OSCX) application circuit >

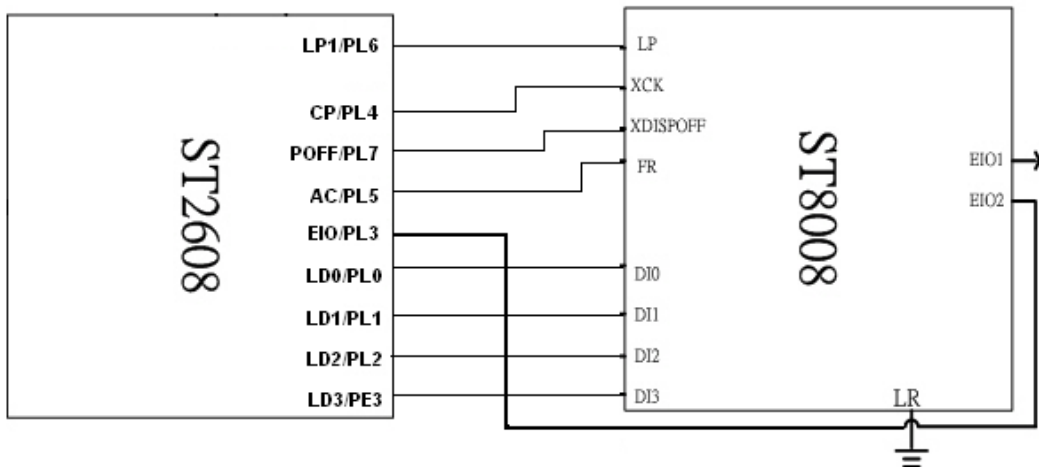Below shows the application circuit of 32KHz X'tal connection. Please follow it.

The original application circuit as below:
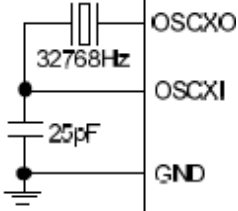
The modified circuit as follow:

<ST26XX+ST8008 CASCADE MODE CONNECTION>

This interface is suitable for ST26xx series IC.

Notice: ST26xxB can only output common signal when cascade mode.

User **can not mix** the segment from ST26xxB and the segment from other LCD drivers. It's because the LCD driving ability of ST26xxB and other LCD drivers are not the same. If user mix them, the performance of LCD display may be bad. (Color block or cross-talk)

< Standard flow for switching I/O and segment >

We know that there are many I/O which are shared with LCD segment.
And the configure is determined by **LCFG** register.
Here is the standard flow of configure I/O or segment, please follow up. Or programmer will not configure I/O possibly.
(1) Please configure **LCFG** first!!
(2) And then configure **PCA/PCB/PCC/PCD/PCE/PCL**
(3) Finally configure **PA/PB/PC/PD/PE/PL**

Sample code:
```
        LDA      #FFH
        STA      LCFG       ; enable all I/O
        STA      PCL        ; configure PL as output
        STA      PL         ; PL0~PL7 high status
```

< LCDCK=32K with cascade mode >

**There has some limit when programmer use LCDCK=32K and cascade.**
Programmer can use ST26 with LCD cascade mode, it's no doubt. Also, programmer can use cascade mode combine with LCDCK from 32KHz(OSCX).
But user should take care one thing as following:
We know ST26 can support Cascade 1/2/4-bit data bus mode, however, LCDCK=32K function can only support 8-bit mode!!
So, when programmer use these two functions in the same time, MCU will push 8-bit data per clock cause LCDCK=32K function, but cascade mode maximum push 4-bit data out to LCD driver per clock, so you will lose 4-bit data(bit4~bit7) and make display data wrong.
The solution is to modify the picture, let MCU push 8-bit every clock, and we separate it every 4-bit data into 8 bit data as picture 2. and we can solve it. Mention that because LCDCK=32K can maximum load 36 x 80 dots picture, by above condition, we finally can push 36x40 dots picture to show on LCD since we only use half of data (first 4-bit).
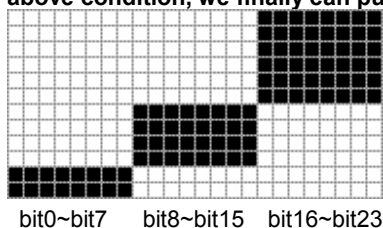
←The original picture information

bit0~bit7   bit8~bit15   bit16~bit23
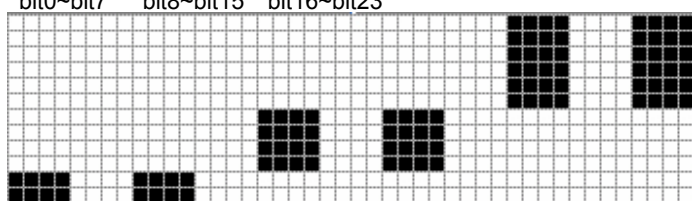
←picture 2 : modified picture

Notice: ST26xxB can only output common signal when cascade mode.
User **can not mix** the segment from ST26xxB and the segment from other LCD drivers. It's because the LCD driving ability of ST26xxB and other LCD drivers are not the same. If user mix them, the performance of LCD display may be bad. (Color block or cross-talk)

< User Manual for ST2600B external bus usage >
[Description]

Since users may use external memory bus to access external ROM, FLASH, or LCD driver, we draw this manual to tell the details and notice when using external bus by ST2600B in two mode: (1)Stand alone mode (2) ICE-mode

(1) When using ST2600B Stand alone mode:
External memory bus can be output directly by ST2600B DVB (PCB-300) J22 pin-1 to pin-32

(2) When using ST2600B ICE mode:
Because external data can be controlled by PC through ST-ICE, so the external bus will be shared with ICE connector pins (PCB-300 - J15)
(a) Please first amount 74hc32 on U11 and U12.
(b) PCB-300 J15 pins allocation as following:

J15

2	vcc	A18	A19	A20	A21	A22	A23	D0	D1	D2	D3	D4	D5	D6	D7	WR	RD	gnd
1	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17

(c) ST2600B DVB should be connected to ST-ICE by J15, and also be connected to external bus by above table

< Pull-up resistance of D0~D7 for current issue when using ST75xx >
Description: When entering sleep mode, D0~D7 of ST75xx will be floating, and make current consumption (about 120uA). It can be solved by adding 8 1M-ohm resistance on D0~D7.
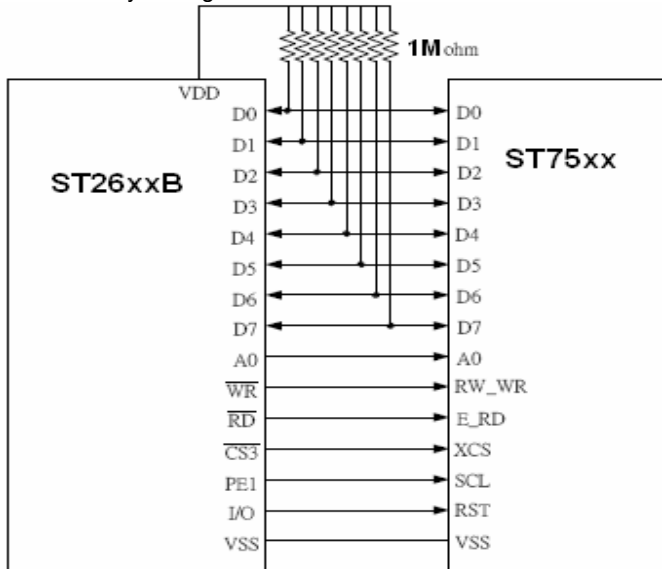
Note: The pull up resister of D7~ D0 are necessary to avoid the current issue.

9   REVISIONS

REVISION	DESCRIPTION	PAGE	DATE
V1.0			
V1.1	Add ST26xx application note		2009/3