ST2101C

Dot Matrix LCD Driver

80 COMMON/SEGMENT

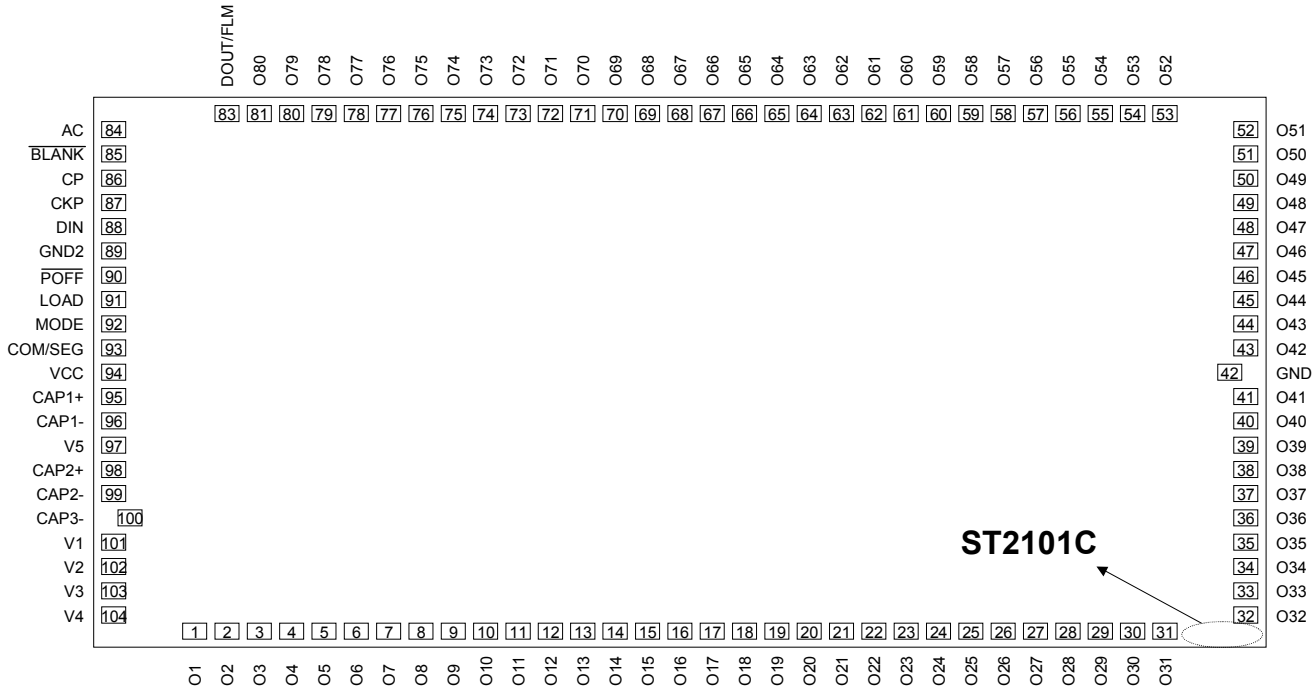
1. Features

- Number of LCD drive outputs: 80
- Programmable duty ratio: 1/32, 1/48, and 1/80
- Maximum LCD drive voltage: 13.0V
- Logic operation voltage: 2.4 to 5.5V
- Built-in double/triple/quad DC-DC voltage converter
- Low power consumption
- Low output impedance
- 1-bit serial data input
- Interface with ST2100 LCD controller
- Software programmable PWM contrast control
- Support cascade function to drive large size and high resolution panels

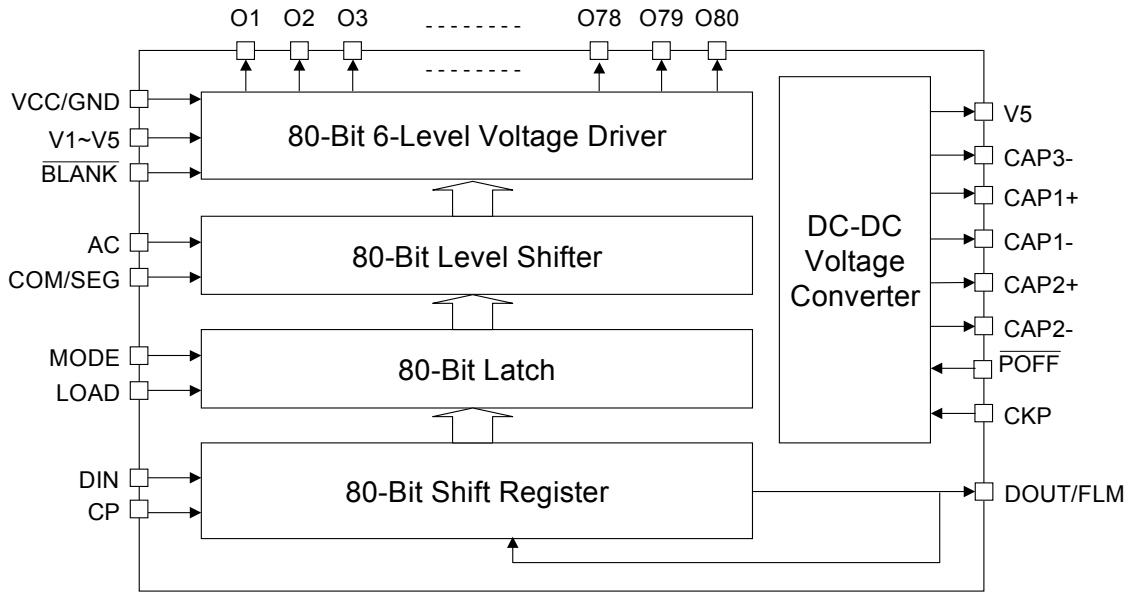
2. General Description

The ST2101C is a dot matrix common/segment LCD driver LSI that is fabricated by advanced low power CMOS silicon gate technology. It is suitable for driving various small/medium scale and different display resolution LCD panels, and is useful for personal equipments or other consumer applications. This chip consists of 80-bit shift register, 80-bit data latch, 80-bit level shifter and 80-bit 6-level driver. It converts serial data, which is received from LCD controller (ex: ST2100) to parallel data and outputs LCD driving waveform to the LCD panel. This LSI can drive a variety of LCD panels because of various segment/common combination modes, cascade capability, and also the flexibility of bias voltages which are provided externally. The built-in DC-DC converter is useful for generating a high level liquid crystal driving voltage and also saves additional components. Moreover, the PWM contrast control logic provides the ability of contrast adjustment via one PWM signal input.

3. Pad Diagram



4. Block Diagram



5. Function Description

5.1 Pin Description

Pin Number	Designation	I/O	Description
1~41,43~81	O1~O80	O	LCD common/segment drives
82	NC		
83	DOUT/FLM	I	- MODE="H": Connect to frame marker signal (FLM). Common data is input and shift at the falling edge of LOAD signal.
		O	- MODE="L": Segment (or common) data is shift and output from this pin. Connect to next ST2101C data input if two ST2101C are cascaded. Leave it open (NC) when there is no further connection.
84	AC	I	Alternating signal input for LCD drive waveform
85	$\overline{\text{BLANK}}$	I	Dual functions of display off and PWM contrast control signals input. - Display off: "L" pulse lasts for more than 2 lines will make all drives to output VCC level to turn the display off. - Contrast control: "L" pulse asserted during each line will makes the selected common drive to output non-selected level to disable this line and lower the effective driver voltage output.
86	CP	I	Clock pulse input pin for 80-bit shift register. Data is shifted at falling edge of clock. - Connect to LCD pixel clock for LCD segment data - Connect to line latch pulse (LOAD) for common data when 80-common mode is selected. Note: Must keep at GND level after power down
87	CKP	I	Clock is inputted from this pin and is divided by 32 to be the booster clock. Tie to VCC if voltage converter is not used.
88	DIN	I	80-bit shift register data input. - Connect to 1-bit LCD serial data input at segment function - Connect to frame marker signal (FLM) when 80-common mode is selected
90	$\overline{\text{POFF}}$	I	Voltage converter circuit on/off switch. - "H": Turn on voltage converter, and display on/off control will be masked to be off until 2 AC cycle is passed. - "L": Turn off voltage converter and force display to be off Note: To ensure the same display-on time, if two or more ST2101C are connected, all $\overline{\text{POFF}}$ must be connected together even those don't use their voltage converters.

<table>
<tr><td>91</td><td>LOAD</td><td>I</td><td>Latch pulse of the 80-bit display data latch at segment function. Shift clock input of shift register at common function. Data is latched when LOAD=”H”

Note: Must keep at GND level after power down</td></tr>
<tr><td>92,93</td><td>MODE, COM/SEG</td><td>I</td><td>- MODE=”H”: Mixed common and segment functions
- MODE=”L”: Either common or segment function is selected
<table>
<tr><td colspan="2" rowspan="2"></td><td colspan="2">COM/SEG</td></tr>
<tr><td>L</td><td>H</td></tr>
<tr><td rowspan="2">MODE</td><td>L</td><td>80 segments</td><td>80 commons</td></tr>
<tr><td>H</td><td>32 seg / 48 com</td><td>48 seg / 32 com</td></tr>
</table></td></tr>
<tr><td>94</td><td>VDD</td><td>P</td><td>Power supply for logic and voltage converter circuit</td></tr>
<tr><td>42,89</td><td>GND, GND2</td><td>P</td><td>Ground</td></tr>
<tr><td>95</td><td>CAP1+</td><td>O</td><td>Connect to booster capacitor 1 positive(+) terminal</td></tr>
<tr><td>96</td><td>CAP1-</td><td>O</td><td>Connect to booster capacitor 1 negative(-) terminal</td></tr>
<tr><td>98</td><td>CAP2+</td><td>O</td><td>Connect to booster capacitor 2 positive(+) terminal</td></tr>
<tr><td>99</td><td>CAP2-</td><td>O</td><td>Connect to booster capacitor 2 negative(-) terminal</td></tr>
<tr><td>97</td><td>V5</td><td>O</td><td>Negative voltage output of booster circuit
Power supply for LCD drives</td></tr>
<tr><td>100</td><td>CAP3-</td><td>O</td><td>Connect to booster capacitor 3 negative(-) terminal</td></tr>
<tr><td>101~104</td><td>V1~V4</td><td>I</td><td>Inputs of external power supply for LCD drives</td></tr>
</table>

Note: P=power pin, I=input pin, O=output pin

5.2 Display Modes

There are four kinds of display modes selected by the combination of two pins, MODE and COM/SEG. Refer to TABLE 5-1 for all the options and the order of com/seg drives in every mode.

TABLE 5-1 Display Mode Options

MODE	COM/SEG	O1 – O32	O33 – O48	O49 – O80	Note
L	L	Last input data	----------	First input data	80 segments
L	H	com1	----------	com80	80 commons
H	L	Last ----- First	com1 ----------	com48	32seg / 48com
H	H	Last ---------- First	com1 -----	com32	48seg / 32com

5.3 Output Voltage Level

All 80 bit latched data directly map to driver outputs O1~O80. Each has a 6-level voltage driver. One of 6 levels is outputted according to the combination of latched data, com/seg modes, and the alternating signal (AC). The relation is shown in TABLE 5-2 .

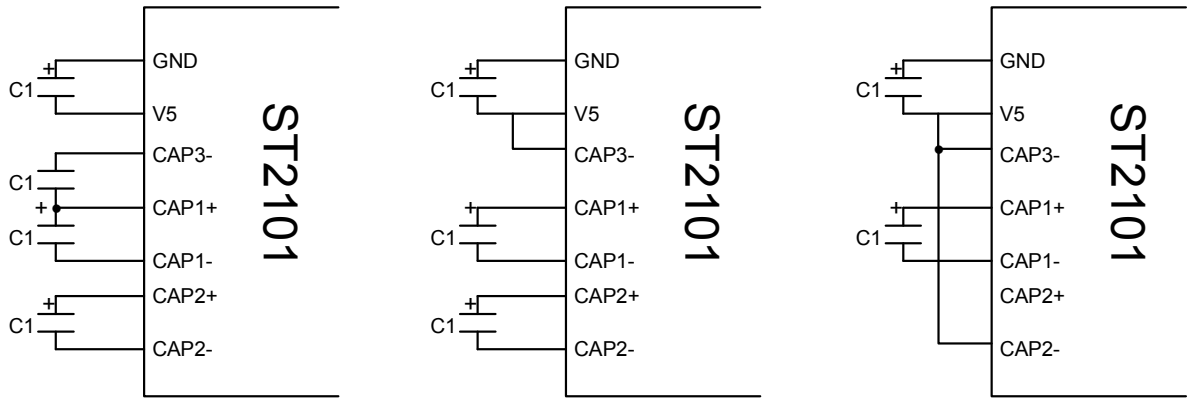
TABLE 5-2 Driver Output Levels “X”: don’t care

Drive Mode	$\overline{POFF}$	$\overline{BLANK}$	Status	AC	Output Levels
Common	H^1	H	Selected	H	VCC
				L	V5
			Non-Selected	H	V4
				L	V1
		L (contrast control)	X	H	V4
				L	V1
		L^2 (display off)	X	X	VCC
	L	X	X	X	VCC
Segment	H^1	H / L (contrast control)	Selected (“H”)	H	V5
				L	VCC
			Non-Selected (“L”)	H	V3
				L	V2
		L^2 (display off)	X	X	VCC
	L	X	X	X	VCC

Note: 1: Changes will be made after two AC cycle
2: Changes will be made after two LOAD cycle

5.4 Voltage Converter

It is possible and convenient by using the voltage converter equipped within ST2101C to produce a liquid crystal driving voltage of two, three or four times of power supply voltage level. The voltage converter can provide a negative voltage equal to VCC, two times of or three times of VCC with four capacitors at most. FIGURE 5-1 shows the connections between capacitors and ST2101C for different modes.



a. 4X step-up circuit b. 3X step-up circuit c. 2X step-up circuit

FIGURE 5-1 Voltage Converter Connections

5.5 Operation Timing

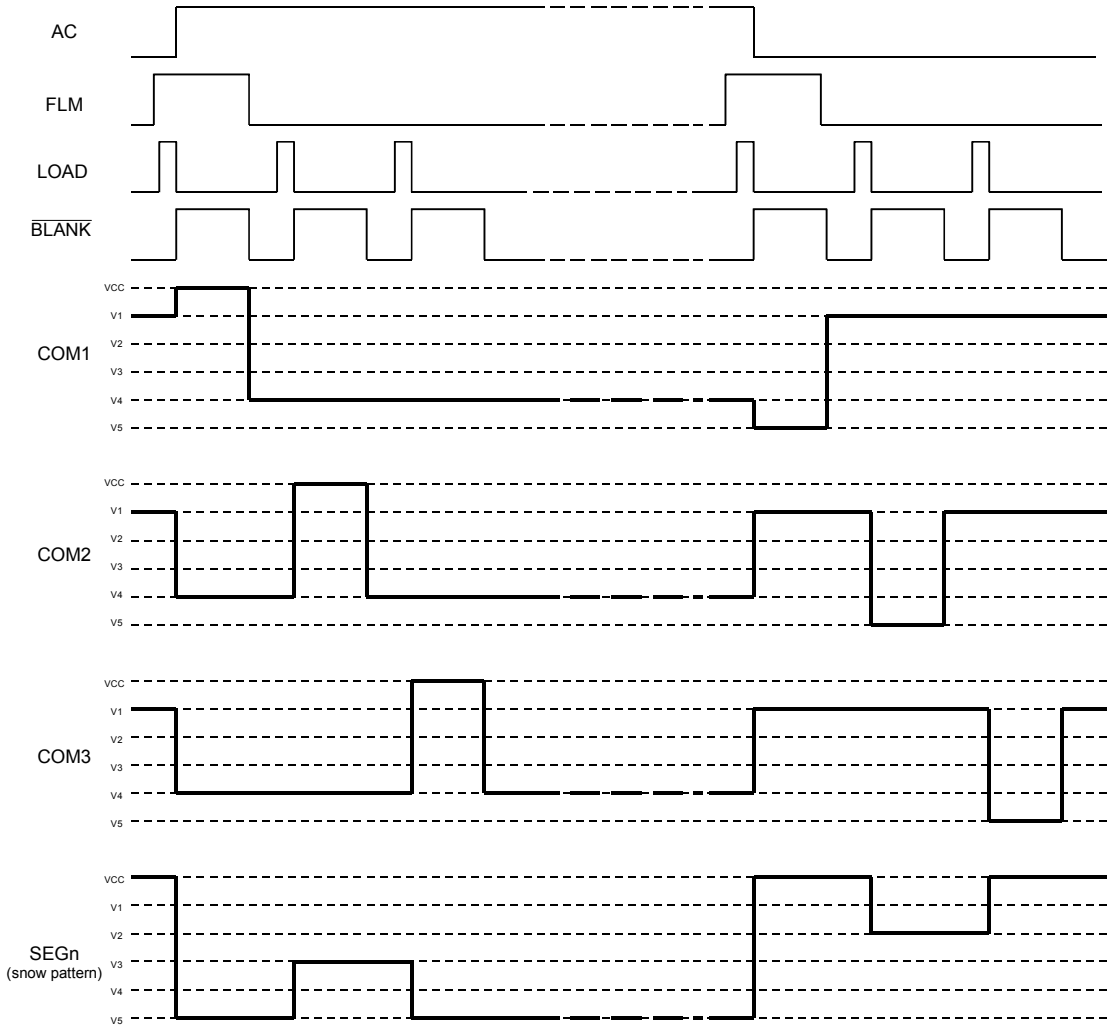


FIGURE 5-2 Driver Timing 1

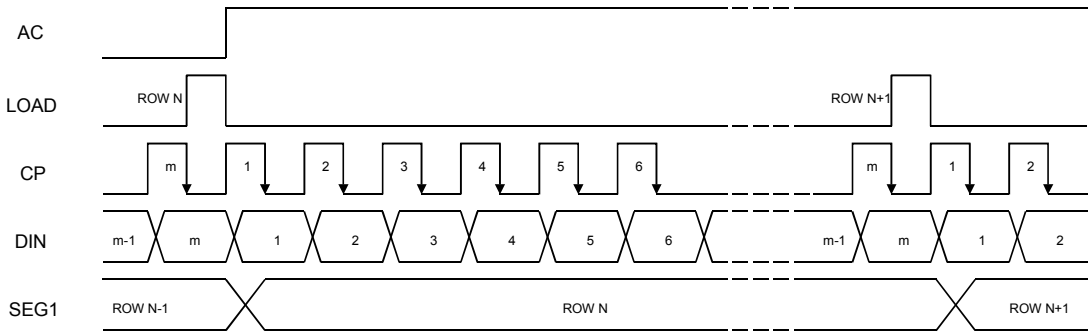


FIGURE 5-3 Driver Timing 2

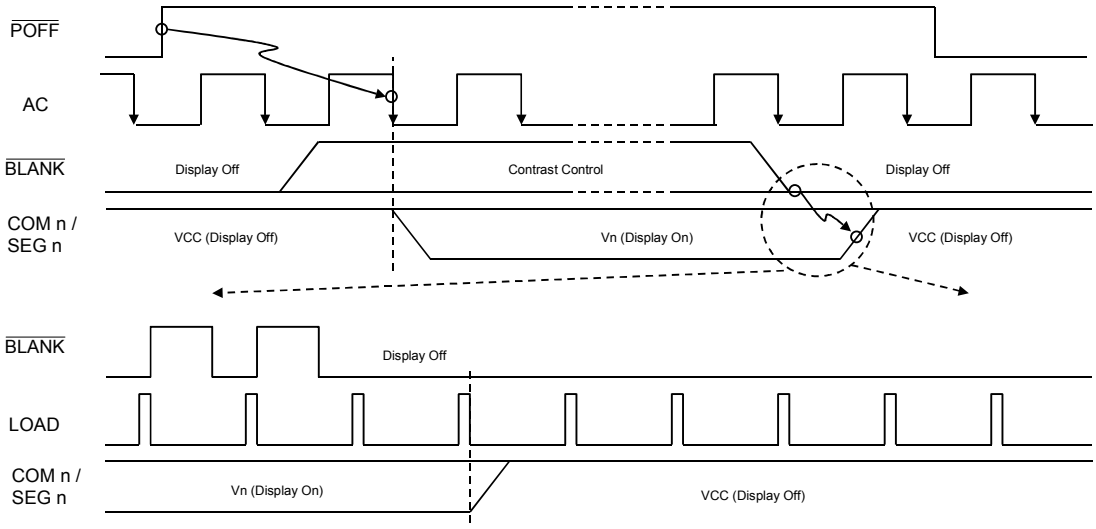


FIGURE 5-4 Driver Timing 3

6. Electrical Characteristics

6.1 Absolute Maximum Ratings*

Power supply voltage
- Double step-up ---------- -0.3V to +7.0V
- Triple step-up---------- -0.3V to +5.5V
- Quad step-up---------- -0.3V to +4.0V

Input Voltage---------- -0.3V to V_{DD}+0.3V
Operating Ambient Temperature --------- -10°C to +60°C
Storage Temperature ---------- -55°C to +125°C

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

6.2 DC Electrical Characteristics

Standard operation conditions: V_{DD} = 3.0V, GND = 0V, T_A = 25°C, unless otherwise specified

Parameter	Symbol	Min.	Max.	Unit	Condition
Operating Voltage	VCC	2.4	5.5	V	With double step-up
		2.4	4.5	V	With triple step-up
		2.4	3.3	V	With quad step-up
LCD voltage	VCC-V5		13.0	V	
Operating Current	I_{OP}		550	μA	F_{CP} = 500 KHz
Standby Current	I_{SB1}		1	μA	
Input pixel clock	F_{cp}		2M	Hz	Clock input to pin CP
Input High Voltage	V_{IH}	0.7VCC	VCC + 0.3	V	
Input Low Voltage	V_{IL}	GND -0.3	0.3VCC	V	
Output low voltage	V_{OL}		0.8	V	I_{OL} = 100 μA
Output high voltage	V_{OH}	2.8		V	I_{OH} = -100 μA

7. Application Circuits

7.1 1/48 duty, 112 segments, 3X set-up

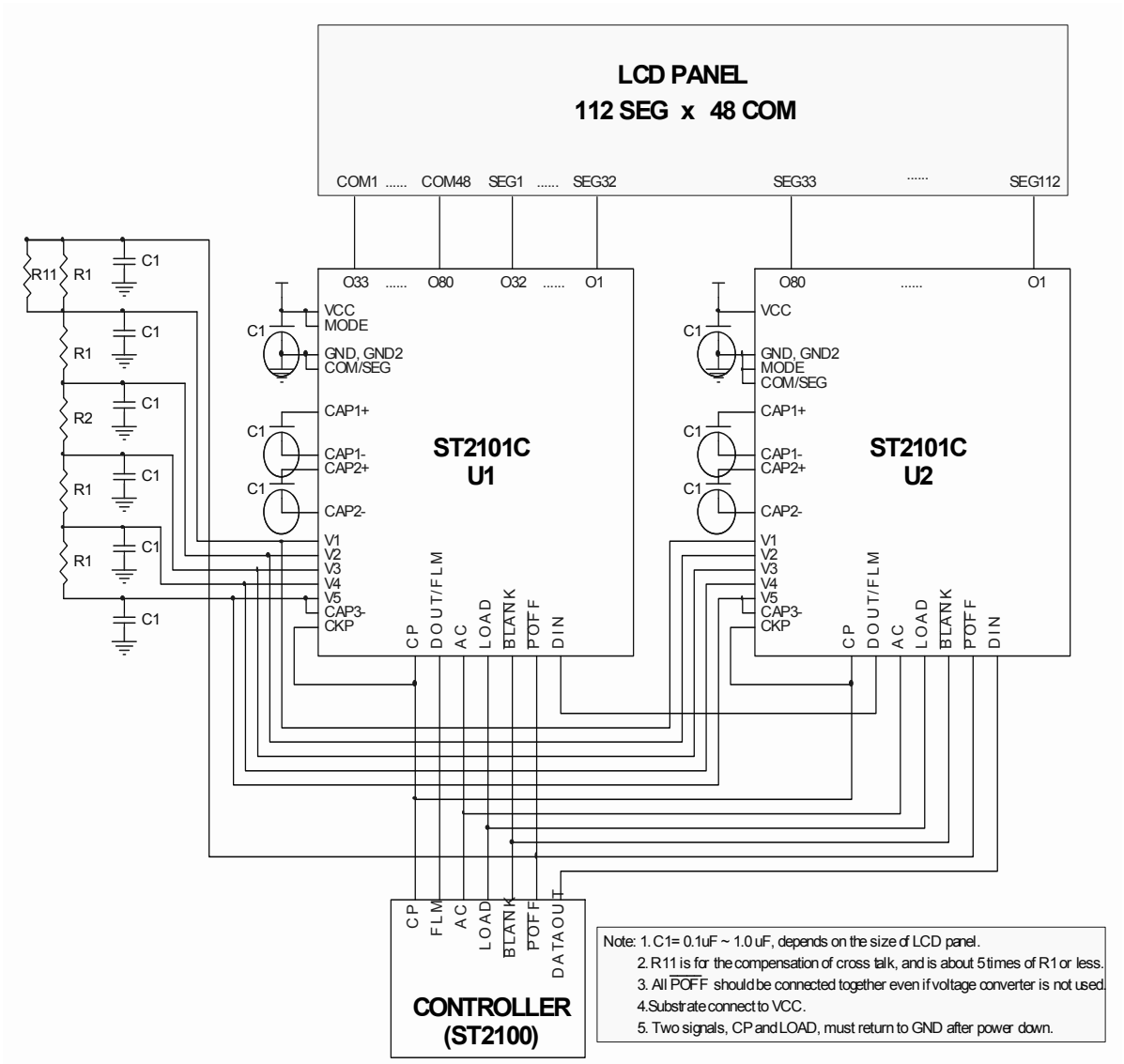


FIGURE 7-1 Application Circuit 1

7.2 1/32 duty, 128 segments, 3X set-up

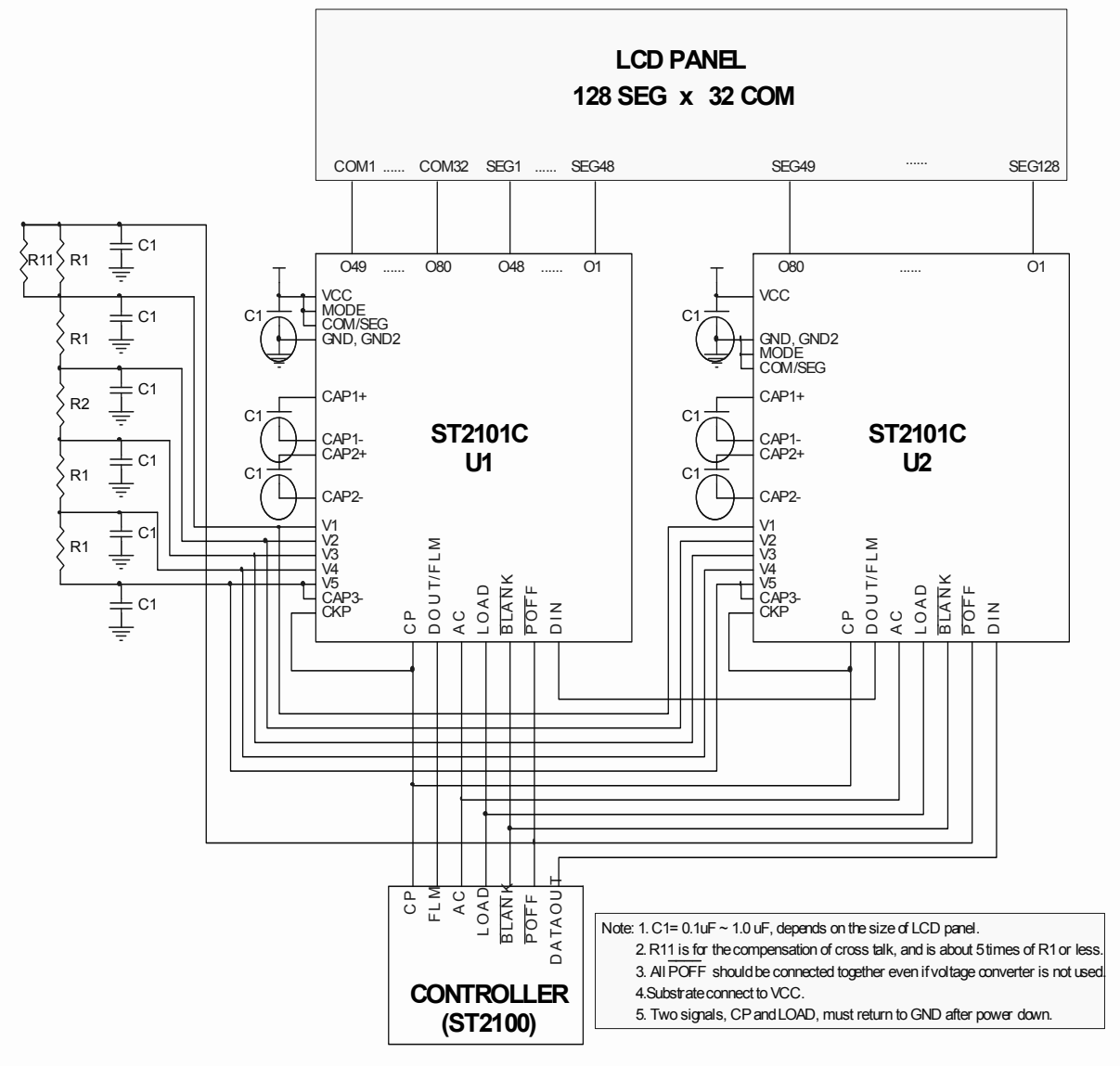


FIGURE 7-2 Application Circuit 2

7.3 1/32 duty, 48 segments, 3X set-up

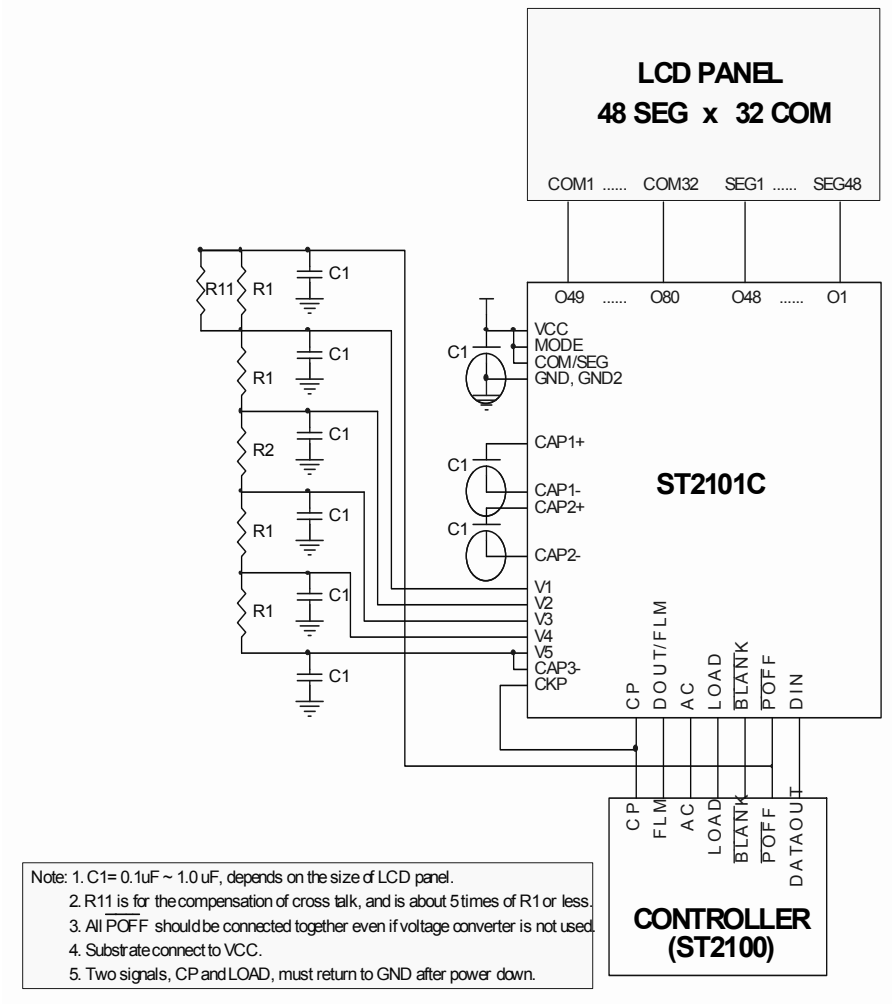


FIGURE 7-3 Application Circuit 3

7.4 1/80 duty, 160 segments, 4X set-up

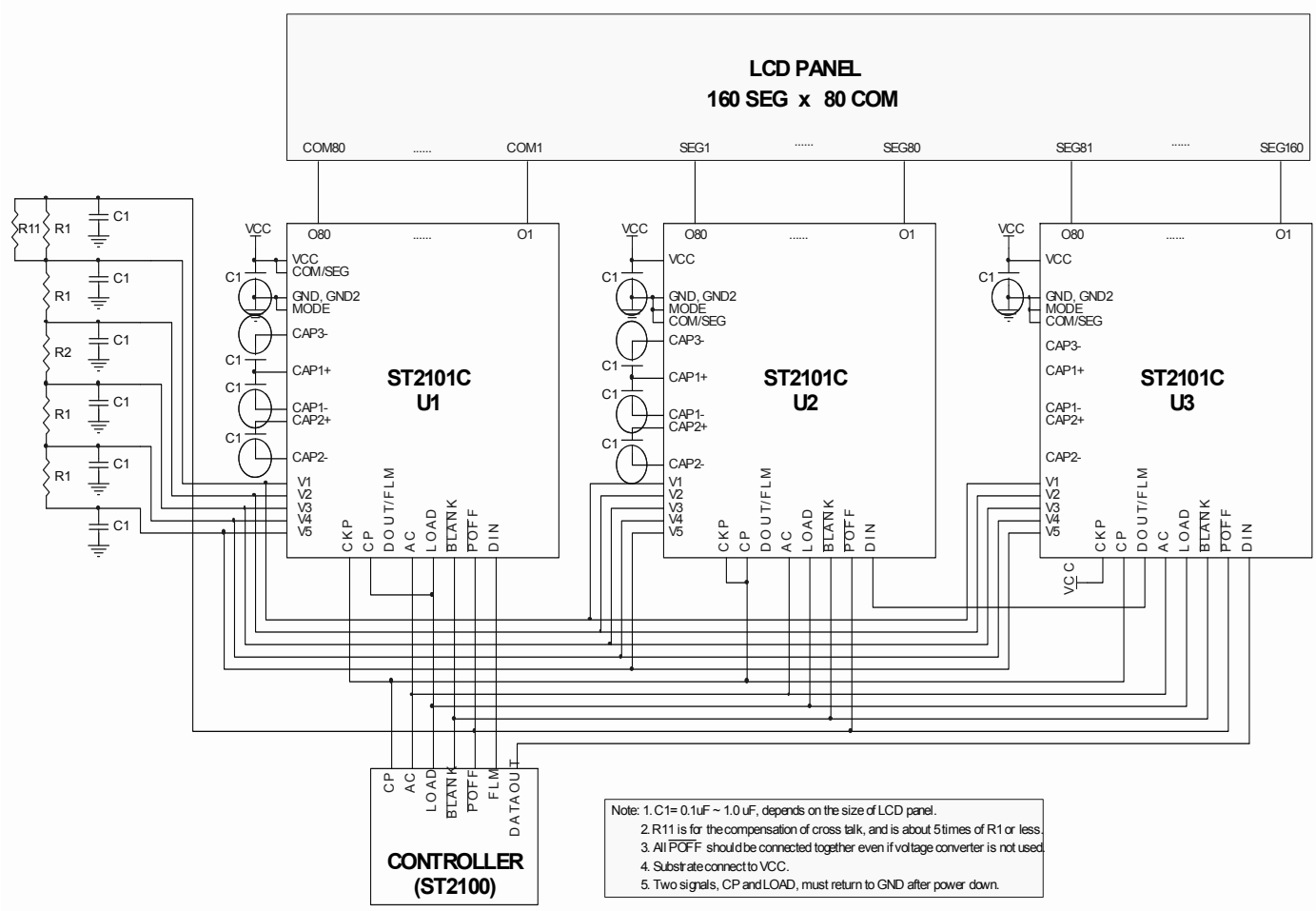


FIGURE 7-4 Application Circuit 4

8. Bonding Diagram

- Chip size: 4150μm x 2800μm
- Coordinate: Pad center (μm)
- Origin: Chip center
- Pad pitch: 110μm~130μm
- Substrate connection: VCC

Unit: μm

Pin No.	Name	X	Y	Pin No.	Name	X	Y
1	O[1]	-1327.7	1763.1	53	O[52]	1327.8	-1756.9
2	O[2]	-1327.7	1633.1	54	O[53]	1327.8	-1626.9
3	O[3]	-1327.7	1503.1	55	O[54]	1327.8	-1496.9
4	O[4]	-1327.7	1373.1	56	O[55]	1327.8	-1366.9
5	O[5]	-1327.7	1243.1	57	O[56]	1327.8	-1236.9
6	O[6]	-1327.7	1113.1	58	O[57]	1327.8	-1106.9
7	O[7]	-1327.7	993.1	59	O[58]	1327.8	-986.9
8	O[8]	-1327.7	883.1	60	O[59]	1327.8	-876.9
9	O[9]	-1327.7	773.1	61	O[60]	1327.8	-766.9
10	O[10]	-1327.7	663.1	62	O[61]	1327.8	-656.9
11	O[11]	-1327.7	553.1	63	O[62]	1327.8	-546.9
12	O[12]	-1327.7	443.1	64	O[63]	1327.8	-436.9
13	O[13]	-1327.7	333.1	65	O[64]	1327.8	-326.9
14	O[14]	-1327.7	223.1	66	O[65]	1327.8	-216.9
15	O[15]	-1327.7	113.1	67	O[66]	1327.8	-106.9
16	O[16]	-1327.7	3.1	68	O[67]	1327.8	3.1
17	O[17]	-1327.7	-106.9	69	O[68]	1327.8	113.1
18	O[18]	-1327.7	-216.9	70	O[69]	1327.8	223.1
19	O[19]	-1327.7	-326.9	71	O[70]	1327.8	333.1
20	O[20]	-1327.7	-436.9	72	O[71]	1327.8	443.1
21	O[21]	-1327.7	-546.9	73	O[72]	1327.8	553.1
22	O[22]	-1327.7	-656.9	74	O[73]	1327.8	663.1
23	O[23]	-1327.7	-766.9	75	O[74]	1327.8	773.1
24	O[24]	-1327.7	-876.9	76	O[75]	1327.8	883.1
25	O[25]	-1327.7	-986.9	77	O[76]	1327.8	993.1
26	O[26]	-1327.7	-1106.9	78	O[77]	1327.8	1113.1
27	O[27]	-1327.7	-1236.9	79	O[78]	1327.8	1233.1
28	O[28]	-1327.7	-1366.9	80	O[79]	1327.8	1363.1
29	O[29]	-1327.7	-1496.9	81	O[80]	1327.8	1503.1
30	O[30]	-1327.7	-1626.9	82	NC		
31	O[31]	-1327.7	-1756.9	83	DOUT/FLM	1327.8	1653.1
32	O[32]	-1174.2	-2003.5	84	AC	1287.8	2003.4
33	O[33]	-1064.2	-2003.5	85	$\overline{\text{BLANK}}$	1177.8	2003.4
34	O[34]	-954.2	-2003.5	86	CP	1067.8	2003.4
35	O[35]	-844.2	-2003.5	87	CKP	957.8	2003.4
36	O[36]	-734.2	-2003.5	88	DIN	847.8	2003.4
37	O[37]	-624.2	-2003.5	89	GND2	737.8	2003.4
38	O[38]	-514.2	-2003.5	90	$\overline{\text{POFF}}$	627.8	2003.4
39	O[39]	-404.2	-2003.5	91	LOAD	517.8	2003.4
40	O[40]	-294.2	-2003.5	92	MODE	407.8	2003.4
41	O[41]	-184.2	-2003.5	93	COM/SEG	297.8	2003.4
42	GND	-0.2	-1911.9	94	VCC	187.8	2003.4
43	O[42]	183.8	-2003.5	95	CAP1+	77.8	2003.4
44	O[43]	293.8	-2003.5	96	CAP1-	-32.2	2003.4
45	O[44]	403.8	-2003.5	97	V5	-142.2	2003.4

Pin No.	Name	X	Y	Pin No.	Name	X	Y
46	O[45]	513.8	-2003.5	98	CAP2+	-252.2	2003.4
47	O[46]	623.8	-2003.5	99	CAP2-	-362.2	2003.4
48	O[47]	733.8	-2003.5	100	CAP3-	-570.2	1908.1
49	O[48]	843.8	-2003.5	101	V1	-778.2	2003.4
50	O[49]	953.8	-2003.5	102	V2	-888.2	2003.4
51	O[50]	1063.8	-2003.5	103	V3	-998.2	2003.4
52	O[51]	1173.8	-2003.5	104	V4	-1108.2	2003.4

9. Revisions

Version 0.2
First release

Version 0.3
Page11,12 Add bonding diagram

Version 0.4
Page1 Remove NC pin in pad diagram

Version 0.5
Page All Change name of pin 83 from DOUT to DOUT/FLM
Page7~10 (section 7)
Change resistance of R11 from 10 times of R1 to 5 times of R1 or less

Version 0.6
Page6 Change maximum operation current from 100uA to 550uA in section 6.2.

Version 0.7a
Page10 Change 160x80 application circuit. Enable both ST2101C voltage converters for better display quality.

Version 0.8
Page 2,3,8~11
Add notes of two signals, CP and LOAD, that these two signals must return to GND level after power down