CMOS LSI

No. 4348

LC79430D

Dot Matrix LCD Driver

Overview

The LC79430D is a large-scale dot matrix LCD common driver LSI. The LC79430D contains an 80-bit bidirectional shift register and is equipped with a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the IC's number of bits. The LC79430D can be used in conjunction with segment driver LC79400D, LC79401D (QIP100D) to drive a wide-screen LCD panel.

Features

- On-chip LCD drive circuit (80 bits)
- Display duty selection ranging from 1/64 to 1/256
- On-chip input/output pins support further increases in bit number
- Supports externally supplied bias voltage
- On-chip 80-bit bidirectional shift register (supports 40-bit x 2 division)
- Supports single mode (80-bit shift register) and dual mode (40-bit x 2 shift register) applications
  - (1) O1 → O80
  - (2) O80 → O1

  } Single mode
  - (3) O1 → O40 and O41 → O80
  - (4) O80 → O41 and O40 → O1

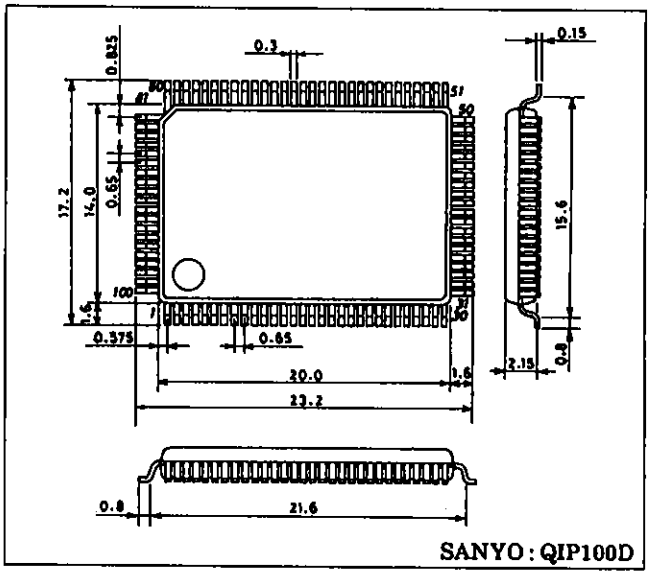
  } Dual mode

  All four of the shift direction selections listed above all supported.
- Operating power supply voltage/operating temperature include
  - V_{DD} (logic section) : 5 V ±10 % / –20 to +75 °C
  - V_{DD}-V_{EE} (LCD section) : 12 V to 32 V / –20 to +75°C
- CMOS process

Package Dimensions

unit : mm

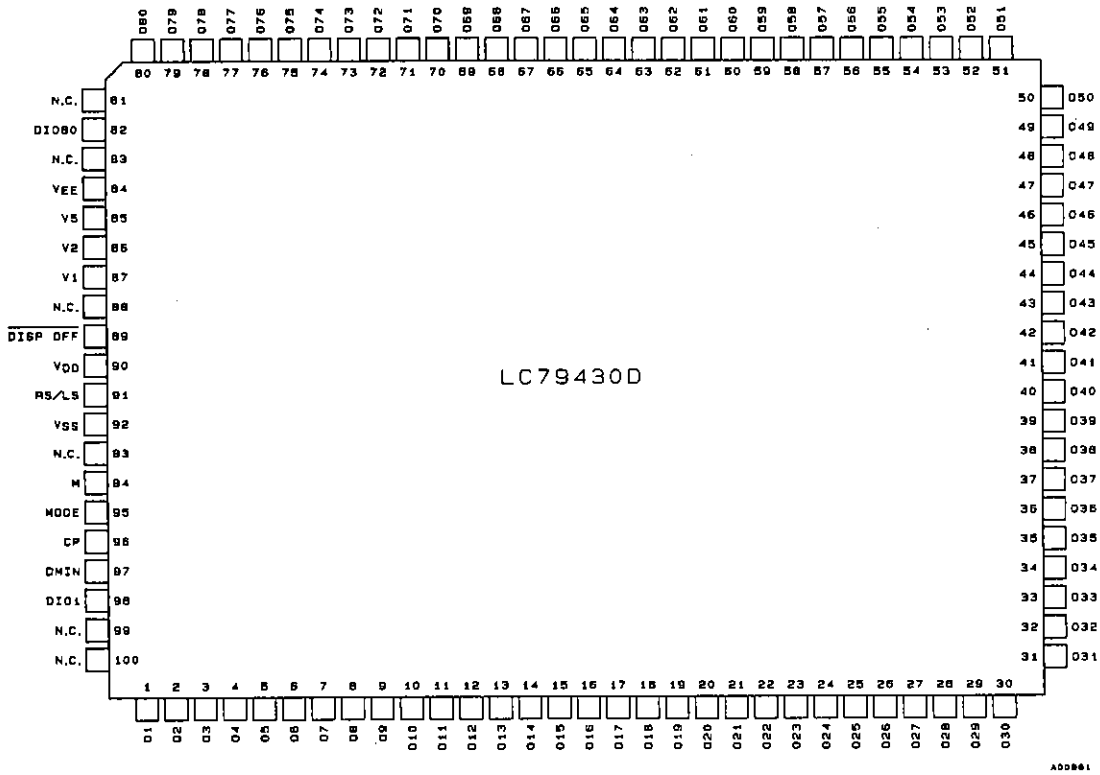
3180-QIP100D



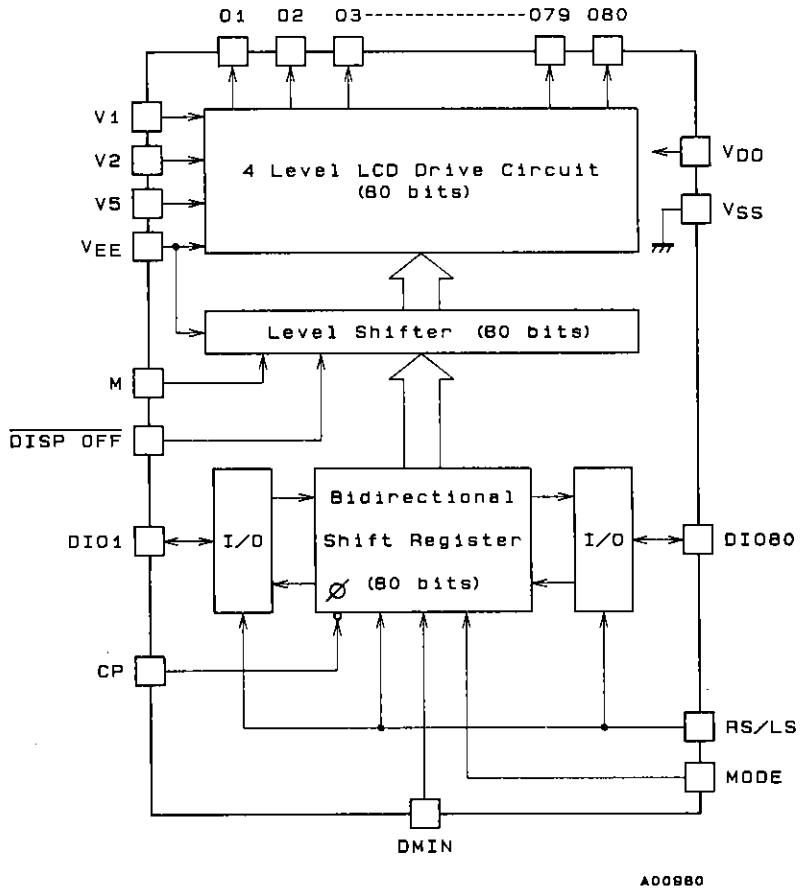
SANYO : QIP100D

SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Pin Assignment



Equivalent Circuit Block Diagram



Pin Descriptions

<table>
<tr><th>Pin No</th><th>Pin name</th><th>Input/Output</th><th>Functions</th></tr>
<tr><td>90
92
84</td><td>V_{DD}
V_{SS}
V_{EE}</td><td>Power supply</td><td>V_{DD} and V_{SS}: Power supply for logic section

V_{DD} and V_{EE}: Power supply for LCD drive circuit</td></tr>
<tr><td>87
86
85</td><td>V1
V2
V5</td><td>Power supply</td><td>Power supply for LCD drive level
V1 and V_{EE} : Select level
V2 and V5 : Non-select level</td></tr>
<tr><td>96</td><td>CP</td><td>Input</td><td>Bidirectional shift register shift clock (triggering on the trailing edge)</td></tr>
<tr><td>98
82

91
95
97</td><td>DIO1
DIO80

RS/LS
MODE
DMIN</td><td>Input/Output
Input/Output

Input
Input
Input</td><td>
<table>
<tr><th>MODE</th><th>RS/LS</th><th>Data Transfer Direction</th><th>DIO1</th><th>DIO80</th><th>DMIN</th></tr>
<tr><td rowspan="2">L
(Single)</td><td>L (Shift right)</td><td>O1 → O80</td><td>IN</td><td>OUT</td><td>*</td></tr>
<tr><td>H (Shift left)</td><td>O80 → O1</td><td>OUT</td><td>IN</td><td>*</td></tr>
<tr><td rowspan="2">H
(Dual)</td><td>L (Shift right)</td><td>O1 → O40
O41 → O80</td><td>IN</td><td>OUT</td><td>IN</td></tr>
<tr><td>H (Shift left)</td><td>O80 → O41
O40 → O1</td><td>OUT</td><td>IN</td><td>IN</td></tr>
</table>
* Don't care (May be set to either "H" or "L")
</td></tr>
<tr><td>94</td><td>M</td><td>Input</td><td>LCD drive output alternating current (AC) signal</td></tr>
<tr><td>89</td><td>$\overline{\text{DISP OFF}}$</td><td>Input</td><td>O1 to O80 output controlling input pins</td></tr>
<tr><td>1
:
80</td><td>O1
:
O80</td><td>Output</td><td>LCD drive output

As shown in the following table, output levels switch in response to the particular combination of scan data, M and $\overline{\text{DISP OFF}}$ signals.
<table>
<tr><th>M</th><th>Data</th><th>$\overline{\text{DISP OFF}}$</th><th>Output</th></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V_{EE}</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V5</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V1</td></tr>
<tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr>
</table>
* Don't care (May be set to either "H" or "L")
</td></tr>
</table>

Common Driver Multi-Unit Connection Circuits.

* Using single mode DMIN input pins are fixed to either "H" or "L".

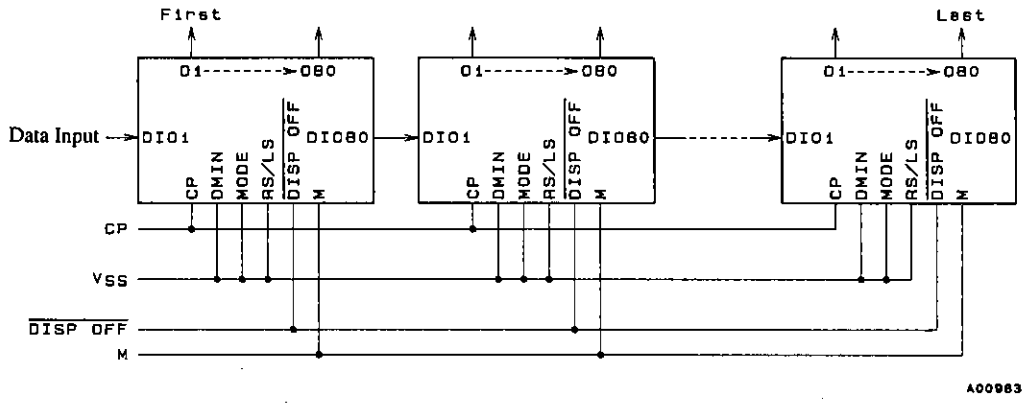


Figure 1 Single Mode (Right Directional Shift)

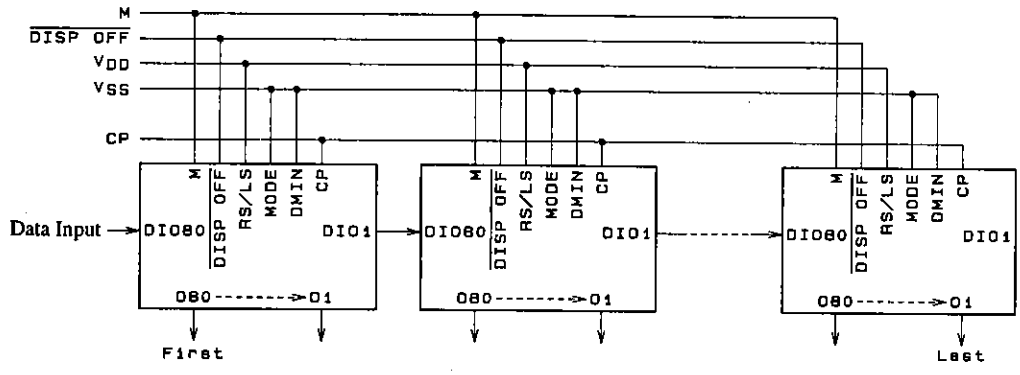


Figure 2 Single Mode (Left Directional Shift)

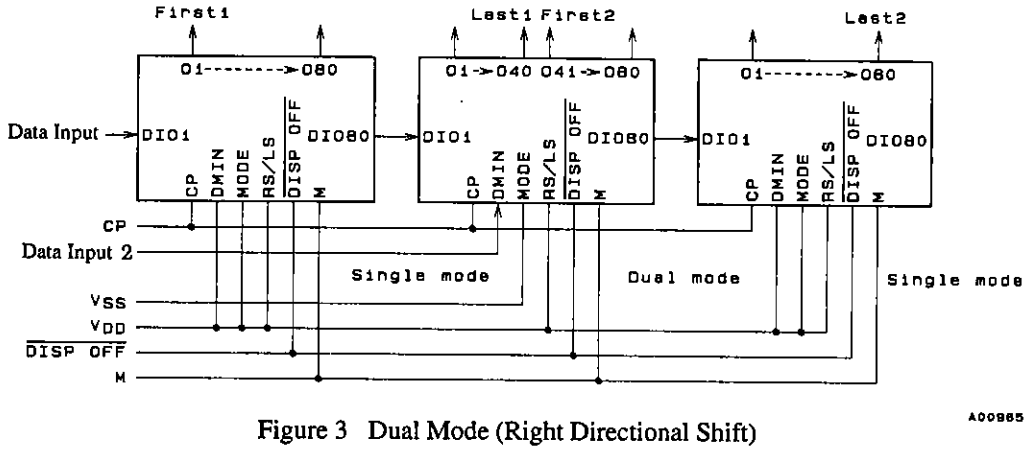


Figure 3 Dual Mode (Right Directional Shift)

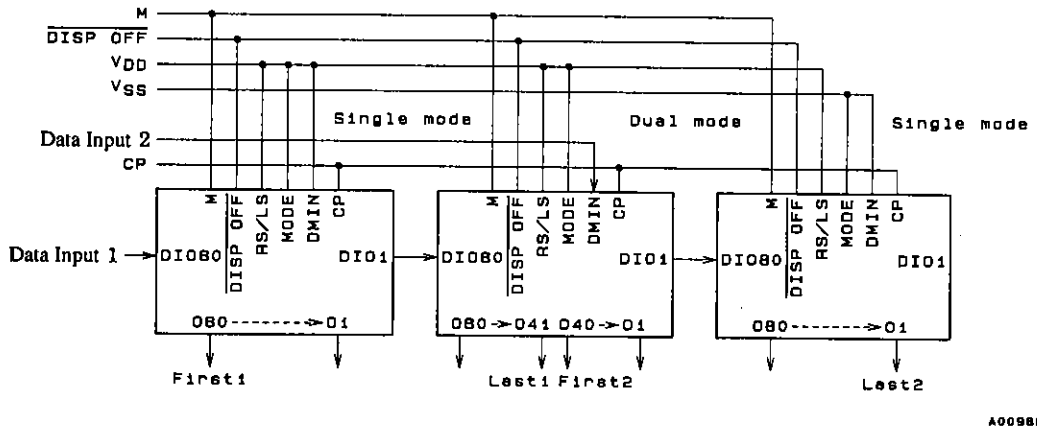


Figure 4 Dual Mode (Left Directional Shift)

Specifications

Absolute Maximum Ratings at Ta = 25±2°C, V_{SS} = 0V

			unit
Maximum supply voltage (LOGIC)	V_{DD} max	−0.3 to +7.0	V
Maximum supply voltage (LCD)	V_{DD}-V_{EE} max *1	0 to 35	V
Maximum input voltage	V_I max	−0.3 to V_{DD} +0.3	V
Storage temperature range	Tstg	−40 to +125	°C

* 1: The following relations between elements should be maintained: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, $V_{DD} - V2 \leq 7V$, $V5 - V_{EE} \leq 7V$.

Allowable Operating Ranges at Ta = –20 to +75°C, V_{SS} = 0V

			min	typ	max	unit
Supply voltage (LOGIC)	V_{DD}		4.5		5.5	V
Supply voltage (LCD)	V_{DD}-V_{EE}	*2, *3	12		32	V
Input "H" level voltage	V_{IH}	DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{\text{DISP OFF}}$	0.8V_{DD}			V
Input "L" level voltage	V_{IL}	DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{\text{DISP OFF}}$			0.2V_{DD}	V
CP (Shift Clock)	f_{CP}	CP			1	MHz
CP (Pulse width)	t_{WC}	CP	63			ns
Setup time	t_{SETUP}	DIO1 → CP, DIO80 → CP, DMIN → CP	100			ns
Hold time	t_{HOLD}	DIO1 → CP, DIO80 → CP, DMIN → CP	100			ns
CP Rise-Fall Time	t_R	CP			50	ns
	t_F	CP			50	ns

*2 The following relations between elements should be maintained: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, $V_{DD} - V2 \leq 7V$, $V5 - V_{EE} \leq 7V$.

*3 When the power supply is turned on, power to the LCD drive is turned on after or simultaneously with the turning on of the logic section's power supply. When the power supply is turned off, the logic power supply is turned off after or at the same time the LCD driver power supply is turned off.

Electrical Characteristics at Ta = 25±2°C, V_{SS} = 0V, V_{DD} = 5V±10%

			min	typ	max	unit
Input "H" level current	I_{IH}	$V_{IN} = V_{DD}$, V_{DD} = 5.5V; DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{\text{DISP OFF}}$			1	μA
Input "L" level current	I_{IL}	$V_{IN} = V_{SS}$, V_{DD} = 5.5V; DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{\text{DISP OFF}}$	–1			μA
Output "H" level voltage	V_{OH}	I_{OH} = –0.4mA, V_{DD} = 4.5V; DIO1, DIO80	V_{DD}–0.4			V
Output "L" level voltage	V_{OL}	I_{OL} = 0.4mA, V_{DD} = 4.5V; DIO1, DIO80			0.4	V
Driver On Resistor	R_{ON} (1)	V_{DD}-V_{EE} = 30V, | V_{DE}-Vo | = 0.5V, V_{DD} = 4.5V *4; O1 to O80			1.0	kΩ
	R_{ON} (2)	V_{DD}-V_{EE} = 20V, | V_{DE}-Vo | = 0.5V, V_{DD} = 4.5V *4; O1 to O80			1.0	kΩ
Consumable current (1)	I_{SS}	V_{DD}-V_{EE} = 30V, CP = 14kHz, no-load, V_{DD} = 5.5V; V_{SS}			100	μA
Consumable current (2)	I_{EE}	V_{DD}-V_{EE} = 30V, CP = 14kHz, no-load, V_{DD} = 5.5V; V_{EE}			100	μA
Input Capacity	C_I	f = 1MHz; CP		5		pF

*4 V_{DE} = V1 or V2 or V5 or V_{EE}, V1 = V_{DD}, V2 = 16/17 (V_{DD}-V_{EE}), V5 = 1/17 (V_{DD}-V_{EE})

Switching Characteristics at Ta = 25±2°C, V_{SS} = 0V, V_{DD} = 5V±10%

			min	typ	max	unit
Output Delay Time	t_{PLH}	C_L = 15pF; CP → DIO1, CP → DIO80			250	ns
	t_{PHL}	C_L = 15pF; CP → DIO1, CP → DIO80			250	ns

Switching Characteristics