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Princeton Technology Corp.
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DESCRIPTION

PT6880 is an OLED Driver/Controller IC utilizing CMOS Technology specially designed to display alphanumeric and Japanese kana characters as well as symbols and graphics. It can interface with either 4-bit or 8-bit Microprocessor and display up to one 8-character line or two 8-character lines.

Display RAM, Character Generator, OLED Driver as well as a wide range of instruction functions such as Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, Display Shift are all incorporated into a single chip having the highest performance and reliability. Pin assignments and application circuit are optimized for easy PCB layout and cost saving advantages.

FEATURES

- CMOS technology
- Low power consumption
- 4-bit or 8-bit MPU interface
- High speed MPU interface: 2MHz (VDD=5V)
- 80 x 8-bit display RAM (80 characters max.)
- Auto reset function
- 5 x 8 and 5 x 10 dot matrix
- Built-in oscillator with external resistors
- Programmable duty cycle:
  - 1/8 duty: (1 display line, 5 x 8 dots with cursor)
  - 1/11 duty: (1 display line, 5 x 10 dots with cursor)
  - 1/16 duty: (2 display lines, 5 x 8 dots with cursor)
- 9920-bit character generator ROM (CGROM)
  - 208 character fonts (5 x 8 dot matrix)
  - 32 character fonts (5 x 10 dot matrix)
- 64 x 8-bit character generator RAM (CGRAM)
  - 8 character fonts (5 x 8 dot matrix)
  - 4 character fonts (5 x 10 dot matrix)
- 16 common x 40 segment OLED drivers
- Available in C.O.B. or 100 Pins LQFP package

APPLICATIONS

- Cellular phone
- Data bank/Organizer
- Electronic dictionary/Translator
- Information appliance
- P.D.A.
- P.O.S.
- Car audio
- Electronic equipment with OLED display

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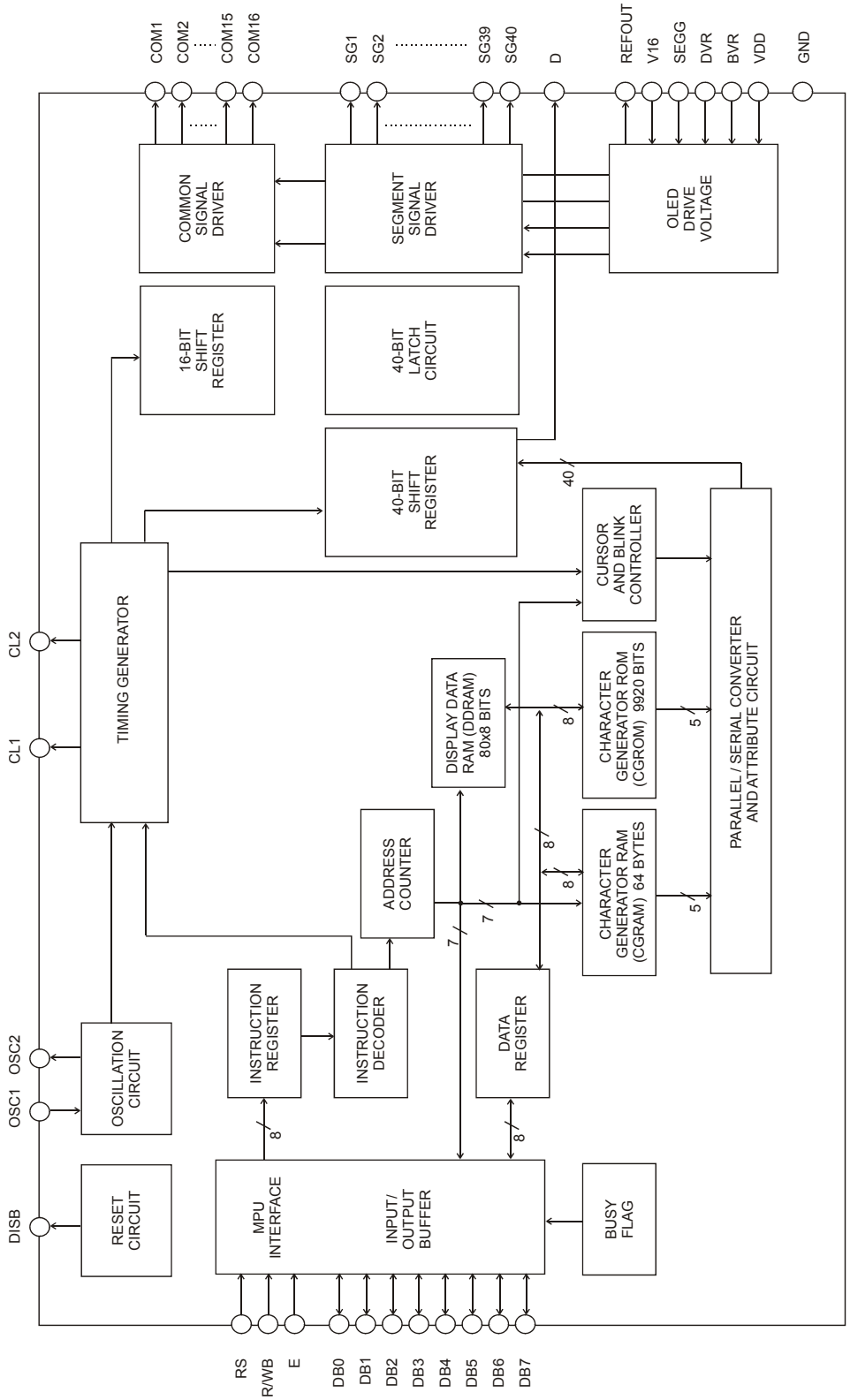
BLOCK DIAGRAM



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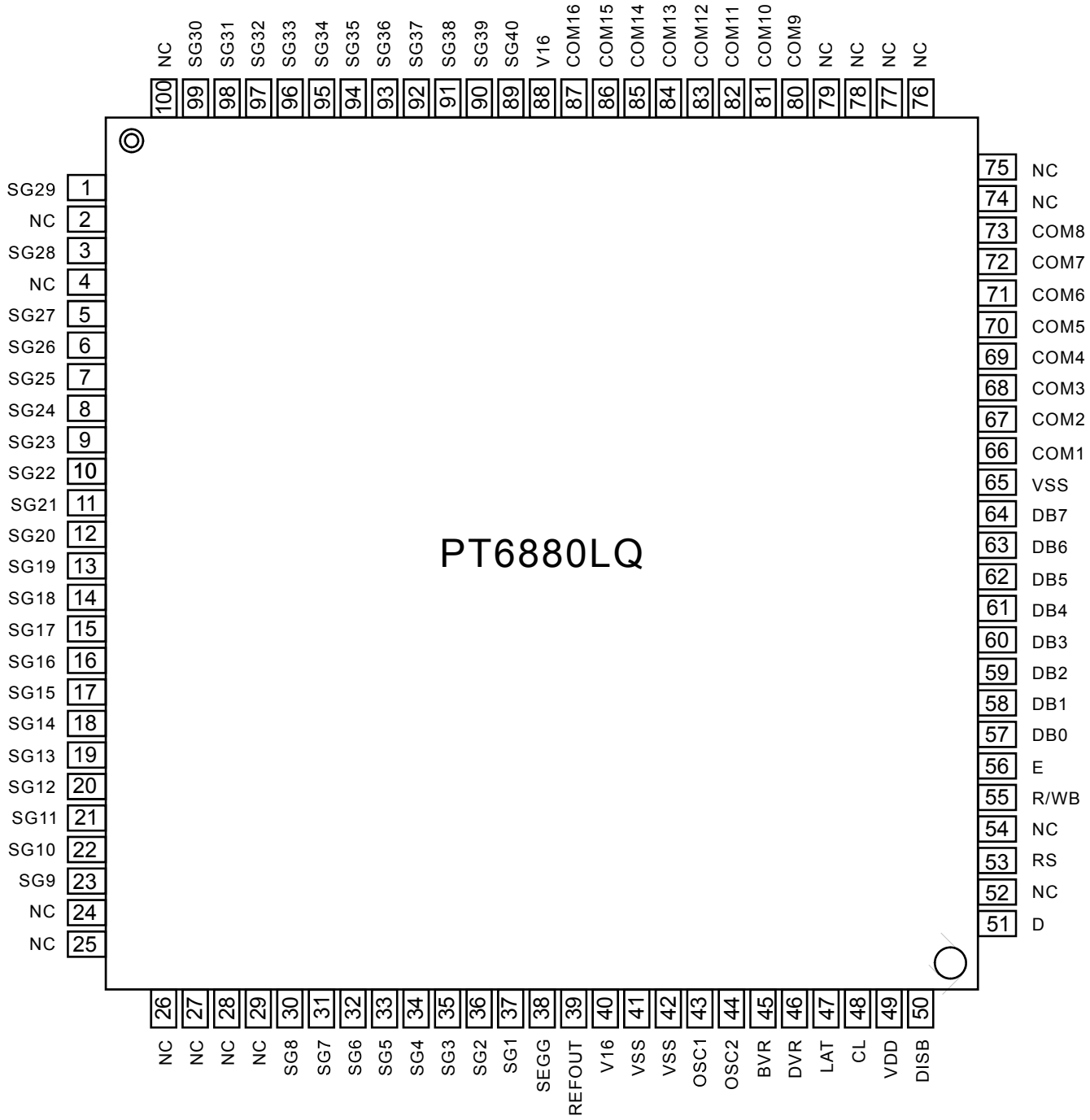
PIN CONFIGURATION

100 PINS, LQFP



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PIN/PAD DESCRIPTION

Pin Name	I/O	Description	Pad/Pin No.
SG40 ~ SG30 SG29, SG28 SG27 ~ SG9 SG8 ~ SG1	O	Segment Driver Output Pins	89 ~ 99 1, 3 5 ~ 23 30 ~ 37
SEGG	-	OLED Drive Power Supply (0V)	38
REFOUT	O	Reference Current Output Pin	39
V16	-	OLED Drive Power Supply (16V)	40, 88
VSS	-	Ground Pin (0V)	41, 42, 65
OSC1	I	Oscillator Input Pin	43
OSC2	O	Oscillator Output Pin	44
BVR	I	Brightness Control Input Pin	45
DVR	I	Precharge Time Control Input Pin	46
LAT	O	Latch Clock Output Pin	47
CL	O	Shift Clock Output Pin	48
VDD	-	Power Supply (2.7V to 5.5V)	49
DISB	O	Reset Signal Output Pin	50
D	O	Character Pattern Data Output Pin	51
RS	I	Register Select Input Pin When this pin is set to "0", it is used as an Instruction Register. When this pin is set to "1", it is used for as the Data Register.	53
R/WB	I	Read/Write Control Input Pin This pin is used to select either the Write or the Read Operation. If this pin is set to "0", then the Write Function is enabled. If this pin is set to "1", then the Read function is enabled.	55
E	I	Data Read/Write Start Control Pin	56
DB0 ~ DB3	I/O	Low Order Bidirectional Data I/O Pins These pins are used for data transfer and reception between the MPU and PT6880. These pins are not used during a 4-bit operation.	57 ~ 60
DB4 ~ DB7	I/O	High Order Bidirectional Data I/O Pins These pins are used for data transfer and reception between the MPU and PT6880. D7 can be used as a Busy Flag.	61 ~ 64
COM1 ~ COM8 COM9 ~ COM16	O	Common Driver Output Pins (see Note)	66 ~ 73 80 ~ 87
NC	-	No Connection	2, 4, 24 ~ 29, 52, 54, 74 ~ 79, 100

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Note:
COM1 to COM16 are used as the Common Output Driver Pins. However, when the pins are not in used, the respective common signals are transformed into non-selection waveforms. For example, under a 1/8 Duty Factors, the Common Driver Output Pins -- COM9 to COM16 are not used. Common Driver Output Pins -- COM12 to COM16 are not used during a 1/11 duty factor. Therefore, the common signals represented by aforementioned Unused Common Driver Output Pins are transformed into non-selection waveforms.

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FUNCTION DESCRIPTION

REGISTERS

PT6880 provides two types of 8-bit registers, namely: Instruction Register (IR) and Data Register (DR). The register is selected using the RS Pin. When the RS pin is set to "0", the Instruction Register Type is selected. When RS pin is set to "1", the Data Register Type is selected. Please refer to the table below.

RS	R/WB	Operation
0	0	Instruction register write as an internal operation.
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	Data register write as an internal operation (DR to DDRAM or CGRAM)
1	1	Data register read as an internal operation (DDRAM or CGRAM to DR)

INSTRUCTION REGISTER (IR)

The Instruction Register is used to store the instruction code (i.e. Display Clear, Cursor Home and others), Display Data RAM (DDRAM) Address, and the Character Generator RAM (CGRAM) Address. Instruction register can only be written from the MPU.

DATA REGISTER (DR)

The Data Register is used as a temporary storage for data that are going to be written into the DDRAM or CGRAM as well as those data that are going to be read from the DDRAM or CGRAM.

BUSY FLAG (BF)

The Busy Flag is used to determine whether PT6880 is idle or internally operating. When PT6880 is performing some internal operations, the Busy Flag is set to "1". Under this condition, the no other instruction will not be accepted. When RS Pin is set to "0" and R/WB Pin is set to "1", the Busy Flag will be outputted to the DB7 pin.

When PT6880 is idle or has completed its previous internal operation, the Busy Flag is set to "0". The next instruction can now be processed or executed.

ADDRESS COUNTER (AC)

The address counter is used to assign the Display Data RAM (DDRAM) Address and the Character Generator RAM (CGRAM) Address. When Address information is written into the Instruction Register (IR), this Address information is sent from the Instruction Register to the Address Counter. At the same time, the nature of the Address (either CGRAM or DDRAM) is determined by the instruction.
After writing into or reading from the DDRAM or CGRAM, the Address Counter is automatically increased or decreased by 1 (for Write or Read Function). It must be noted that when the RS pin is set to "0" and R/WB is set to "1", the contents of the Address Counter are outputted to the pins -- DB0 to DB6.

DISPLAY DATA RAM (DDRAM)

The Display Data RAM (DDRAM) is used to store the Display Data which is represented as 8-bit character code. The Display Data RAM supports an extended capacity of 80 x 8-bit or 80 characters. The area in the DDRAM which are not used for display can be used as General Data RAM. For more details, please refer to the sections below.

The Display Data RAM Address (ADD) is set in the Address Counter as a hexadecimal.

	High Order Bits			Low Order Bits			
Address Counter (hexadecimal)	AC6	AC5	AC4	AC3	AC2	AC1	AC0

An example of a DDRAM Address=4E is given below.

DDRAM Address: 4E						
AC6	AC5	AC4	AC3	AC2	AC1	AC0
1	0	0	1	1	1	0

1-LINE DISPLAY (N=0)

When the number of characters displayed is less than 80, the first character is displayed at the head position. The relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position (digit)	1	2	3	4	.....	78	79	80
DDRAM address (hexadecimal)	00	01	02	03	.....	4D	4E	4F

For example, when only 8 characters are displayed in one Display Line, the relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position	1	2	3	4	5	6	7	8
DDRAM address	00	01	02	03	04	05	06	07
Shift left	01	02	03	04	05	06	07	08
Shift right	4F	00	01	02	03	04	05	06

2-LINE DISPLAY (N=1)

Case 1: The Number of Characters displayed is less than 40 x 2 lines

When the number of characters displayed is less than 40 x 2 lines, then the first character of the first and second lines are displayed starting from the head. It is important to note that the first line end address and the second line start address are not consecutive. Please refer the figure below.

Display Position	1	2	3	4	…….	37	38	39	40
DDRAM Address (hexadecimal)	00	01	02	03	…….	24	25	26	27
	40	41	42	43	…….	64	65	66	67

To illustrate, for 2-line x 8 characters display, the relationship between the DDRAM address and position of the OLED panel is shown below.

Display Position	1	2	3	4	5	6	7	8
DDRAM address	00	01	02	03	04	05	06	07
	40	41	42	43	44	45	46	47
Shift left	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48
Shift right	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

Case 2: 16-Character x 2 Lines Display

PT6880 can be extended to display 16 characters x 2 lines by using the 40-output extension driver. When there is a Display Shift operation, the DDRAM Address is also shifted. Please refer to the example below.

Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
	PT6880 display								Extension driver display							
Shift left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
Shift right	27	00	01	02	03	04	05	06	07	08	09	0a	0b	0c	0d	0e
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

CHARACTER GENERATOR ROM (CGROM)

The Character Generator ROM (CGROM) is used to generate either 5 x 8 dots or 5 x 10 dots character patterns from 8-bit character codes. It can generate up to two hundred eight (208) 5 x 8 dot character patterns and thirty two (32) 5 x 10 dot character patterns. For user-defined character patterns, please contact PTC.

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WESTERN EUROPEAN CHARACTER FONT TABLE (PT6880-001)

Upper 4 bit / Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	CG RAM (2)															
LLHL	CG RAM (3)															
LLHH	CG RAM (4)															
LHLL	CG RAM (5)															
LHLH	CG RAM (6)															
LHHL	CG RAM (7)															
LHHH	CG RAM (8)															
HLLL	CG RAM (1)															
HLLH	CG RAM (2)															
HLHL	CG RAM (3)															
HLHH	CG RAM (4)															
HHLL	CG RAM (5)															
HHLH	CG RAM (6)															
HHHL	CG RAM (7)															
HHHH	CG RAM (8)															

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ENGLISH_JAPANESE CHARACTER FONT TABLE (PT6880-003)

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ENGLISH_RUSSIAN CHARACTER FONT TABLE (PT6880-004)

Upper 4 bit / Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	CG RAM (2)															
LLHL	CG RAM (3)															
LLHH	CG RAM (4)															
LHLL	CG RAM (5)															
LHLH	CG RAM (6)															
LHHL	CG RAM (7)															
LHHH	CG RAM (8)															
HLLL	CG RAM (1)															
HLLH	CG RAM (2)															
HLHL	CG RAM (3)															
HLHH	CG RAM (4)															
HHLL	CG RAM (5)															
HHLH	CG RAM (6)															
HHHL	CG RAM (7)															
HHHH	CG RAM (8)															

CHARACTER GENERATOR RAM (CGRAM)

The Character Generator RAM (CGRAM) is used to generate either 5 x 8 dot or 5 x 10 dot character patterns. It can generate eight 5 x 8 dot character patterns and four 5 x 10 dot character patterns. The character patterns generated by the CGRAM can be rewritten. User-defined character patterns for the CGRAM are supported. Areas in the CGRAM that are not used for display may be used as the General Data RAM.

RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR 5 X 8 DOT CHARACTER PATTERN)

Character Codes (DDRAM Data)									CGRAM Address							Character Patterns (CGRAM Data)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0		7	6	5	4	3	2	1	0	
High						Low			High							High						Low		
0	0	0	0	*	0	0	0		0	0	0	0	0	0		*	*	*	1	1	1	1	0	Character pattern 1
												0	0	1		*	*	*	1	0	0	0	1	
												0	1	0		*	*	*	1	0	0	0	1	
												0	1	1		*	*	*	1	1	1	1	0	
												1	0	0		*	*	*	1	0	1	0	0	
												1	0	1		*	*	*	1	0	0	1	0	
												1	1	0		*	*	*	1	0	0	0	1	
												1	1	1		*	*	*	0	0	0	0	0	Cursor Position
0	0	0	0	*	0	0	1		0	0	1	0	0	0		*	*	*	1	0	0	0	1	Character pattern 2
												0	0	1		*	*	*	0	1	0	1	0	
												0	1	0		*	*	*	1	1	1	1	1	
												0	1	1		*	*	*	0	0	1	0	0	
												1	0	0		*	*	*	1	1	1	1	1	
												1	0	1		*	*	*	0	0	1	0	0	
												1	1	0		*	*	*	0	0	1	0	0	
												1	1	1		*	*	*	0	0	0	0	0	Cursor position
												0	0	0		*	*	*						
												0	0	1		*	*	*						
0	0	0	0	*	1	1	1		1	1	1	1	0	0		*	*	*						
												1	0	1		*	*	*						
												1	1	0		*	*	*						
												1	1	1		*	*	*						

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Notes:

1. * = Not Relevant
2. The character pattern row positions correspond to the CGRAM data bits -- 0 to 4, where bit 4 is in the left position.
3. Character Code Bits 0 to 2 correspond to the CGRAM Address Bits 3 to 5 (3-bit: 8 types)
4. If the CGRAM Data is set to "1", then the selection is displayed. If the CGRAM is set to "0", there no selection is made.
5. The CGRAM Address Bits 0 to 2 are used to define the character pattern line position. The 8th line is the cursor position and its display is formed by the logical OR with the cursor. The 8th line CGRAM data bits 0 to 4 must be set to "0". If any of the 8th line CGRAM data bits 0 to 4 is set to "1", the corresponding display location will light up regardless of the cursor position.
6. When the Character Code Bits 4 to 7 are set to "0", then the CGRAM Character Pattern is selected. It must be noted that Character Code Bit 3 is not relevant and will not have any effect on the character display. Because of this, the first Character Pattern shown above (R) can be displayed when the Character Code is 00H or 08H.

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RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR 5 X10 DOT CHARACTER PATTERN)

Character Codes (DDRAM Data)									CGRAM Address							Character Patterns (CGRAM Data)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0		7	6	5	4	3	2	1	0	
High						Low			High				Low			High						Low		
0	0	0	0	*	0	0	*		0	0	0	0	0	0		*	*	*	0	0	0	0	0	Character pattern
											0	0	0	1		*	*	*	0	0	0	0	0	
											0	0	1	0		*	*	*	1	0	1	1	0	
											0	0	1	1		*	*	*	1	1	0	0	1	
											0	1	0	0		*	*	*	1	0	0	0	1	
											0	1	0	1		*	*	*	1	0	0	0	1	
											0	1	1	0		*	*	*	1	1	1	1	0	
											0	1	1	1		*	*	*	1	0	0	0	0	
											1	0	0	0		*	*	*	1	0	0	0	0	
											1	0	0	1		*	*	*	1	0	0	0	0	
											1	0	1	0		*	*	*	0	0	0	0	0	Cursor position
											1	0	1	1		*	*	*	*	*	*	*	*	
											1	1	0	0		*	*	*	*	*	*	*	*	
											1	1	0	1		*	*	*	*	*	*	*	*	
											1	1	1	0		*	*	*	*	*	*	*	*	
											1	1	1	1		*	*	*	*	*	*	*	*	
											0	0	0	0		*	*	*	*	*	*	*	*	
											0	0	0	1		*	*	*	*	*	*	*	*	
0	0	0	0	*	1	1	*		1	1	1	0	0	1		*	*	*	*	*	*	*	*	
											1	0	1	0		*	*	*	*	*	*	*	*	
											1	0	1	1		*	*	*	*	*	*	*	*	
											1	1	0	0		*	*	*	*	*	*	*	*	
											1	1	0	1		*	*	*	*	*	*	*	*	
											1	1	1	0		*	*	*	*	*	*	*	*	
											1	1	1	1		*	*	*	*	*	*	*	*	

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Notes:
1. * = Not Relevant
2. The character pattern row positions correspond to the CGRAM data bits -- 0 to 4, where bit 4 is in the left position.
3. Character Code Bits 1 and 2 correspond to the CGRAM Address Bits -- 4 and 5 respectively (2-bit : 4 types)
4. If the CGRAM Data is set to "1", then the selection is displayed. If the CGRAM is set to "0", there no selection is made.
5. The CGRAM Address Bits 0 to 3 are used to define the character pattern line position. The 11th line is the cursor position and its display is formed by the logical OR with the cursor. The 11th line CGRAM data bits 0 to 4 must be set to "0". If any of the 11th line CGRAM data bits 0 to 4 is set to "1", the corresponding display location will light up regardless of the cursor position.
6. When the Character Code Bits 4 to 7 are set to "0", then the CGRAM Character Pattern is selected. It must be noted that Character Code Bit -- 0 and 3 are not relevant and will not have any effect on the character display. Because of this, the Character Pattern shown above (P) can be displayed when the Character Code is 00H, 01H, 08H or 09H.

TIMING GENERATION CIRCUIT

The timing signals for the internal circuit operations (i.e. DDRAM, CGRAM, and CGROM) are generated by the Timing Generation Circuit. The timing signals for the MPU internal operation and the RAM Read for Display are generated separately in order to prevent one from interfering with the other. This means that, for example, when the data is being written into the DDRAM, there will be no unwanted interference such as flickering in areas other than the display area.

OLED DRIVER CIRCUIT

PT6880 provides 16 Common Drivers and 40 Segment Driver Outputs. When a character font and the number of lines to be displayed have been selected, the corresponding Common Drivers output the drive waveform automatically. A non-selection waveform will be outputted by the rest of the Common Drivers.

Serial data transmission always begins with the display data character pattern corresponding to the last Display Data RAM (DDRAM) Address. The serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register. Thus, PT6880 drives from the head display.

CURSOR/BLINK CONTROL CIRCUIT

The cursor or character blinking is generated by the Cursor / Blink Control Circuit. The cursor or the blinking will appear with the digit located at the Display Data RAM (DDRAM) Address Set in the Address Counter (AC).

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Address counter	0	0	0	1	0	0	0

CASE 1: FOR 1-LINE DISPLAY

Example: When the Address Counter (AC) is set to 08H, the cursor position is displayed at DDRAM Address 08H.

Display position	1	2	3	4	5	6	7	8	9	10	11	.....
DDRAM address (hexadecimal)	00	01	02	03	04	05	06	07	**08**	09	0A	.....

Cursor Position

Note: The cursor or blinking appears when the Address Counter (AC) selects the Character Generator RAM (CGRAM). When the AC selects CGRAM Address, then the cursor or the blinking is displayed in a irrelevant and meaningless position.

CASE 2: FOR 2-LINE DISPLAY

Example: When the Address Counter (AC) is set to 08H, the cursor position is displayed at DDRAM Address 08H.

Display position	1	2	3	4	5	6	7	8	9	10	11	.....
DDRAM address	00	01	02	03	04	05	06	07	**08**	09	0A	.....
(hexadecimal)	40	41	42	43	44	45	46	47	48	49	4A	.....

Cursor Position

Note:
The cursor or blinking appears when the Address Counter (AC) selects the Character Generator RAM (CGRAM). When the AC selects CGRAM Address, then the cursor or the blinking is displayed in an irrelevant and meaningless position.

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RESET FUNCTION

INTERNAL RESET CIRCUIT INITIALIZATION

When power is turned ON, PT6880 is initialized automatically by an internal reset circuit. The following instructions are executed during the initialization.

1. Display clear
2. Function set:
   DL="1": 8-bit interface data
   N="0": 1-line display
   F="0": 5 x 8 dot character font
3. Display on/off control:
   D="0": Display off
   C="0": Cursor off
   B="0": Blinking off
4. Entry mode set:
   I/D="1": Increment by 1
   S="0": No shift

The Busy Flag (BF) is in a busy state until the initialization is completed (BF="1"). The busy state will be in effect 10ms after the VDD rises to 4.5V.

Please note that in order for the initialization by internal reset circuit to be successful, the electrical characteristic conditions listed in the Electrical Characteristics Section must be complied with. Otherwise, such initialization must be performed by instruction from the MPU.

INSTRUCTIONS

PT6880's Instruction Register (IR) and Data Register (DR) are the only registers that can be controlled by the MPU. Prior to the commencement of it internal operation, PT6880 temporarily stores the control information to its Instruction Register (IR) and Data Register (DR) in order to easily facilitate interface with various types of MPU. The internal operations of the PT6880 are determined by the signals (RS, R/WB, DB0 to DB7) that are sent from the MPU. These signals are categorized into 4 instructions types, namely:

1. Function Setting Instructions (i.e. Display, Format, Data Length etc.)
2. Internal RAM Address Setting Instructions
3. Data Transfer with Internal RAM Instructions
4. Miscellaneous Function Instructions

The generally used instructions are those that execute data transfers with the internal RAM. However, when the internal RAM addresses are auto incremented/decremented by 1 after each Data Write, the program load of the MPU is lightened. The Display Shift Instruction can be executed at the same time as the Display Data Write, thereby minimizing system development time with maximum programming efficiency.

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When an instruction is being executed for an internal operation, only the Busy Flag/Address Read Instruction can be performed. The other instructions are not valid. It should be noted that during the execution of an instruction, the Busy Flag is set to "1". The Busy Flag is set to "0" when the instructions are can be accepted and executed. Therefore, the Busy Flag should be checked to make certain that BF="0" before sending another instruction from the MPU. If not, the time between the first instruction and the next instruction is longer than the time it takes to execute the instruction itself.

Instruction	Code										Description	Max. Execution Time when fsp or fosc = 250KHz
	RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display. Sets DDRAM Address 0 into the Address Counter	
Return Home	0	0	0	0	0	0	0	0	1	x	Sets DDRAM Address 0 into the Address Counter. Returns shifted display to original position. DDRAM contents remain unchanged.	1.52ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. (These operations are performed during data write and read.)	37µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets entire Display (D) ON/OFF. Sets Cursor (C) ON/OFF. Sets Blinking (B) of Cursor Position Character.	37µs
Cursor/ Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Moves cursor & shifts display without changing DDRAM contents.	37µs
Function Set	0	0	0	0	1	DL	N	F	x	x	Sets interface data length (DL). Sets number of display lines (N). Sets Character Font (F).	37µs
Set CGRAM Address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM Address. CGRAM data is sent and received after this setting.	37µs
Set DDRAM Address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM Address. The DDRAM data Is sent and received after this setting.	37µs
Read Busy Flag & Address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads Busy Flag (BF) indicating that internal operation is being performed. Reads Address Counter contents.	0µs
Write data into the CGRAM or DDRAM	1	0	Write Data								Writes data into the CGRAM or DDRAM	37µs tADD=4µs*
Read Data from the CGRAM or DDRAM	1	1	Read Data								Read data from the CGRAM or DDRAM	37µs tADD=4µs*

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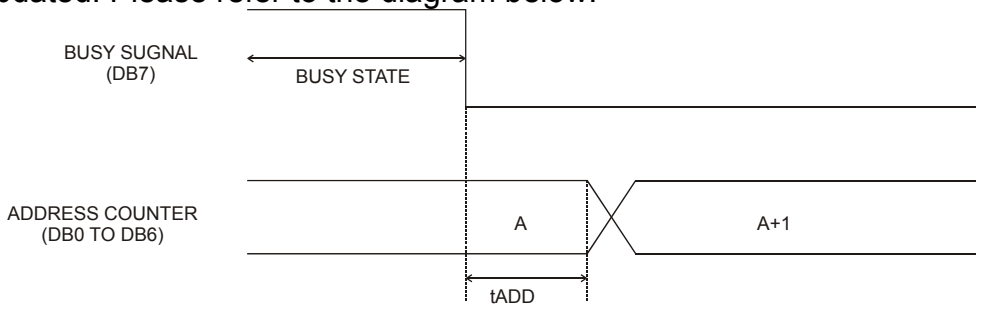
Notes:
1. x = Not Relevant
2. * = After the CGRAM/DDRAM Read or Write Instruction has been executed, the RAM Address Counter is incremented or decremented by 1. After the Busy Flag is turned OFF, the RAM Address is updated.
3. I/D=Increment/Decrement Bit
   - I/D="1": Increment
   - I/D="0": Decrement
4. S=Shift Entire Display Control Bit
5. BF=Busy Flag
   - BF="1": Internal Operating in Progress
   - BF="0": No Internal Operation is being executed, next instruction can be accepted.
6. R/L=Shift Right/Left
   - R/L="1": Shift to the Right
   - R/L="0": Shift to the Left
7. S/C=Display Shift/Cursor Move
   - S/C="1": Display Shift
   - S/C="0": Cursor Move
8. DDRAM=Display Data RAM
9. CGRAM=Character Generator RAM
10. ACG=CGRAM Address
11. ADD=Address Counter Address (corresponds to cursor address)
12. AC=Address Counter (used for DDRAM and CGRAM Addresses)
13. F=Character Pattern Mode
   - F="1": 5 x 10 dots
   - F="0": 5 x 8 dots
14. N=Number of Lines Displayed
   - N="1": 2 -Line Display
   - N="0": 1-Line Display
15. *=The time it takes to execute an instruction changes when the frequency changes. To illustrate an example: When fcp of fosc=250KHz, thenthe execution time = 37μs x 270/250=40μs
16. tADD is the time period starting when the Busy Flag is turned OFF up to the time the Address Counter is updated. Please refer to the diagram below.



where:
tADD depends on the operation frequency and may be calculated using the following equation
tADD=1.5/(fcp) seconds or
tADD=1.5/(fosc) seconds

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INSTRUCTION DESCRIPTION

CLEAR DISPLAY INSTRUCTION

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This instruction is used to clear the Display Write Space 20H in all DDRAM Addresses. That is, the character pattern for the Character Code 20H must be a BLANK pattern. It then sets the DDRAM Address 0 into the Address Counter and reverts the display to its original state (if the display has been shifted). The display will be cleared and the cursor or blinking will go to the left edge of the display. If there are 2 lines displayed, the cursor or blinking will go to the first line 's left edge of the display. Under the Entry Mode, this instruction also sets the I/D to 1 (Increment Mode). The S Bit of the Entry Mode does not change.

RETURN HOME INSTRUCTION

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	*

Note: * = Not Relevant

This instruction is used to set the DDRAM Address 0 into the Address Counter and revert the display to its original status (if the display has been shifted). The DDRAM contents do not change.
The cursor or blinking will go to the left edge of the display. If there are 2 lines displayed, the cursor or blinking will go to the first line's left edge of the display.

ENTRY MODE SET INSTRUCTION

The Entry Mode Set Instruction has two controlling bits: I/D and S. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

I/D IS THE INCREMENT/DECREMENT BIT.

When I/D is set to "1", the DDRAM Address is incremented by "1" when a character code is written into or read from the DDRAM. An increment of 1 will move the cursor or blinking one step to the right.

When I/D is set to "0", the DDRAM is decremented by 1 when a character code is written into or read from the DDRAM. A decrement of 1 will move the cursor or blinking one step to the left.

S: SHIFT ENTIRE DISPLAY CONTROL BIT

This bit is used to shift the entire display. When S is set to "1", the entire display is shifted to the right (when I/D ="0") or left (when I/D ="1"). The display does not shift when reading from the DDRAM, writing into or reading from the CGRAM. When S is set to "0", the display is not shifted.

DISPLAY ON/OFF CONTROL INSTRUCTION

The Display On / OFF Instruction is used to turn the display ON or OFF. The controlling bits are D, C and B.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

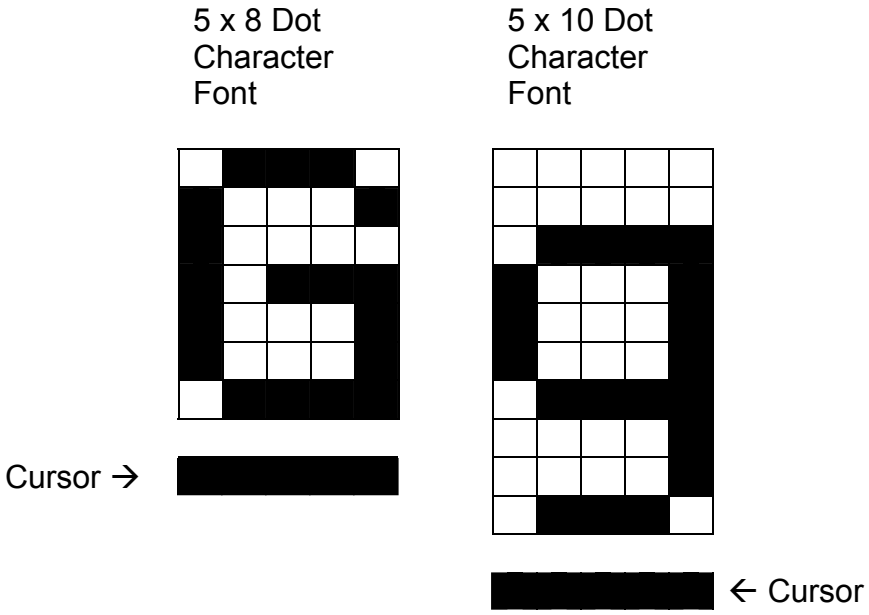
D: DISPLAY ON/OFF BIT

When D is set to "1", the display is turned ON. When D is set to "0", the display is turned OFF and the display data is stored in the DDRAM. The display data can be instantly displayed by setting D to "1".

C: CURSOR DISPLAY CONTROL BIT

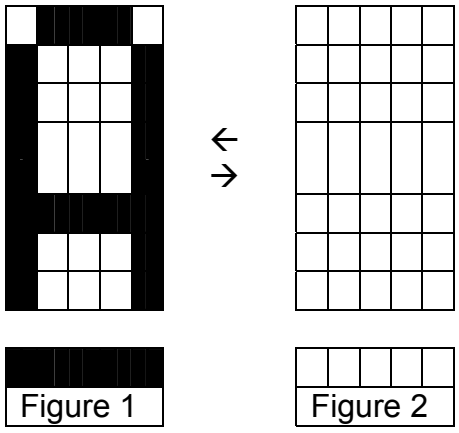
When C is set to "1", the cursor is displayed. In a 5 x 8 dot character font, the cursor is displayed via the 5 dots in the 8th line. In a 5 x 10 dot character font, it is displayed via 5 dots in the 11th line.

When C is set to "0", the cursor display is disabled.
During a Display Data Write, the function of the I/D and others will not be altered even if the cursor is not present. Please refer to the figure below.



B: BLINKING CONTROL BIT

When B is set to '1", the character specified by the cursor blinks. The blinking feature is displayed by switching between the blank dots and the displayed character at a speed of 409.6ms intervals when the fcp or fosc is 250KHz. Please refer to the figure below.



Note: Figures 1 and 2 are alternately displayed

The cursor and the blinking can be set to display at the same time. The blinking frequency depends on the fosc or the reciprocal of fcp.

To illustrate, when fcp=270KHz, then, the blinking frequency=409.6 x 250/270=379.2ms

CURSOR/DISPLAY SHIFT INSTRUCTION

This instruction is used to shift the cursor or display position to the left or right without writing or reading the Display Data. This function is used to correct or search the display. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	*	*

S/C	R/L	Shift Function
0	0	Shifts the cursor position to the left. (AC is decremented by 1).
0	1	Shifts cursor position to the right. (AC incremented by 1).
1	0	Shifts entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

In a 2-line Display, the cursor moves to the second line when it passes the 40th digit of the first line. The first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly, each line moves only horizontally. The second line display does not shift into the first line position.

The Address Counter (AC) contents will not change if the only action performed is a Display Shift.

FUNCTION SET INSTRUCTION

The Function Set Instruction has three controlling 3-bit, namely: DL, N and F. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	*	*

DL: INTERFACE DATA LENGTH CONTROL BIT

This is used to set the interface data length. When DL is set to "1", the data is sent or received in 8-bit length via the DB0 to DB7 (for an 8-Bit Data Transfer). When DL is set to "0", the data is sent or received in 4-bit length via DB4 to DB7 (for a 4-Bit Data Transfer). When the 4-bit data length is selected, the data must be sent or received twice.

N: NUMBER OF DISPLAY LINE

This is used to set the number of display lines. When N="1", the 2-line display is selected. When N is set to "0", the 1-line display is selected.

F: CHARACTER FONT SET

This is used to set the character font set. When F is set to "0", the 5 x 8 dot character font is selected. When F is set to "1", the 5 x 10 dot character font is selected.

It must be noted that the character font setting must be performed at the head of the program before executing any instructions other than the Busy Flag and Address Instruction. Otherwise, the Function Set Instruction cannot be executed unless the interface data length is changed.

SET CGRAM ADDRESS INSTRUCTION

This instruction is used to set the CGRAM Address binary AAAAAA into the Address Counter. Data is then written to or read from the MPU for CGRAM.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	ACG	ACG	ACG	ACG	ACG	ACG

Note: ACG is the CGRAM Address

SET DDRAM ADDRESS INSTRUCTION

This instruction is used to set the DDRAM Address binary AAAAAAA into the Address Counter. The data is written to or read from the MPU for the DDRAM. If 1-line display is selected (N="0"), then AAAAAAA can be 00H to 4FH. When the 2-line display is selected, then AAAAAAA can be 00H to 27H for the first line and 40H to 67H for the second line.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD
			←Higher Order Bits				Lower Order Bits →		

Note: ADD = DDRAM Address

READ BUSY FLAG AND ADDRESS INSTRUCTION

This instruction is used to read the Busy Flag (BF) to indicate if PT6880 is internally operating on a previously received instruction. If BF is set to "1", then the internal operation is in progress and the next instruction will not be accepted. If the BF is set to "0", then the previously received instruction has been executed and the next instruction can be accepted and processed. It is important to check the BF status before proceeding to the next write operation. The value of the Address Counter in binary AAAAAAA is simultaneously read out. This Address Counter is used by both the CGRAM and the DDRAM and its value is determined by the previous instruction. The contents of the address are the same as for the instructions -- Set CGRAM Address and Set DDRAM Address.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC	AC	AC	AC	AC	AC	AC
			←Higher Order Bits				Lower Order Bits →		

Notes:
1. BF=Busy Flag
2. AC=Address Counter

WRITE DATA TO CGRAM / DDRAM INSTRUCTION

This instruction writes 8-bit binary data -- DDDDDDDD to the CGRAM or the DDRAM. The previous CGRAM or DDRAM Address setting determines whether a data is to be written into the CGRAM or the DDRAM. After the write process is completed, the address is automatically incremented or decremented by 1 in accordance with the Entry Mode instruction. It must be noted that the Entry Mode instruction also determines the Display Shift.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D	D	D	D	D	D	D	D
		←Higher Order Bits					Lower Order Bits →		

READ DATA FROM THE CGRAM OR DDRAM INSTRUCTION

This instruction reads the 8-bit binary data -- DDDDDDDD from the CGRAM or the DDRAM. The Set CGRAM Address or Set DDRAM Address Set Instruction must be executed before this instruction can be performed, otherwise, the first Read Data will not be valid.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D	D	D	D	D	D	D	D
		←Higher Order Bits					Lower Order Bits →		

When the Read Instruction is executed in series, the next address data is normally read from the Second Read. There is no need for the Address Set Instruction to be performed before this Read instruction when using the Cursor Shift Instruction to shift the cursor (Reading the DDRAM). The Cursor Shift Instruction has the same operation as that of the Set the DDRAM Address Instruction.

After a Read instruction has been executed, the Entry Mode is automatically incremented or decremented by 1. It must be noted that regardless of the Entry Mode, the Display Shift is not executed.

After the Write instruction to either the CGRAM or DDRAM has been performed, the Address Counter is automatically increased or decreased by 1. The RAM data selected by the Address Counter cannot be read out at this time even if the Read Instructions are executed. Therefore, in order to correctly read the data, the following procedure has suggested:

1. Execute the Address Set or Cursor Shift (only with DDRAM) Instruction
2. Just before reading the desired data, execute the Read Instruction from the second time the Read Instruction has been sent.

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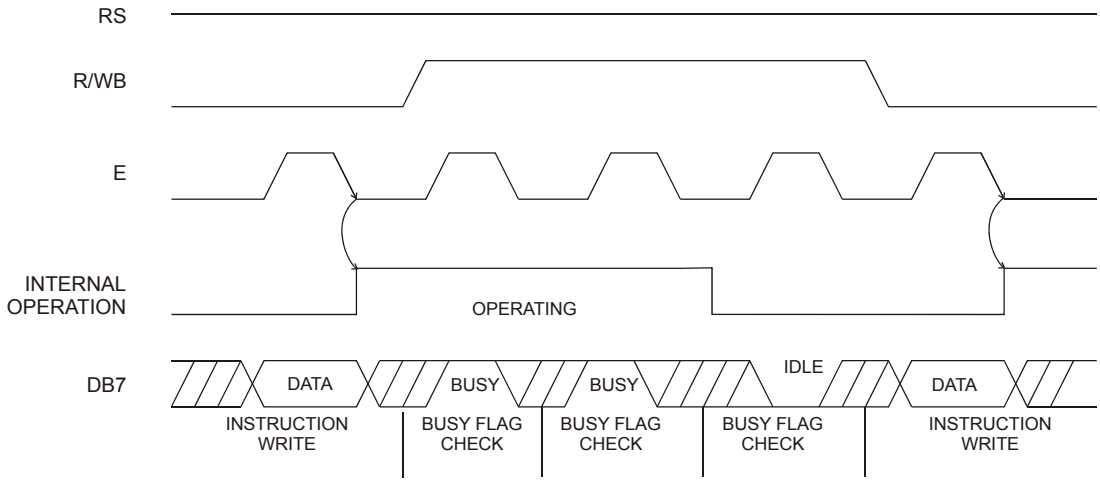
MPU INTERFACE

PT6880 can be configured to interface with either the 4-bit or 8-bit MPU via the DB0 to DB7 pins.

8-BIT MPU INTERFACE

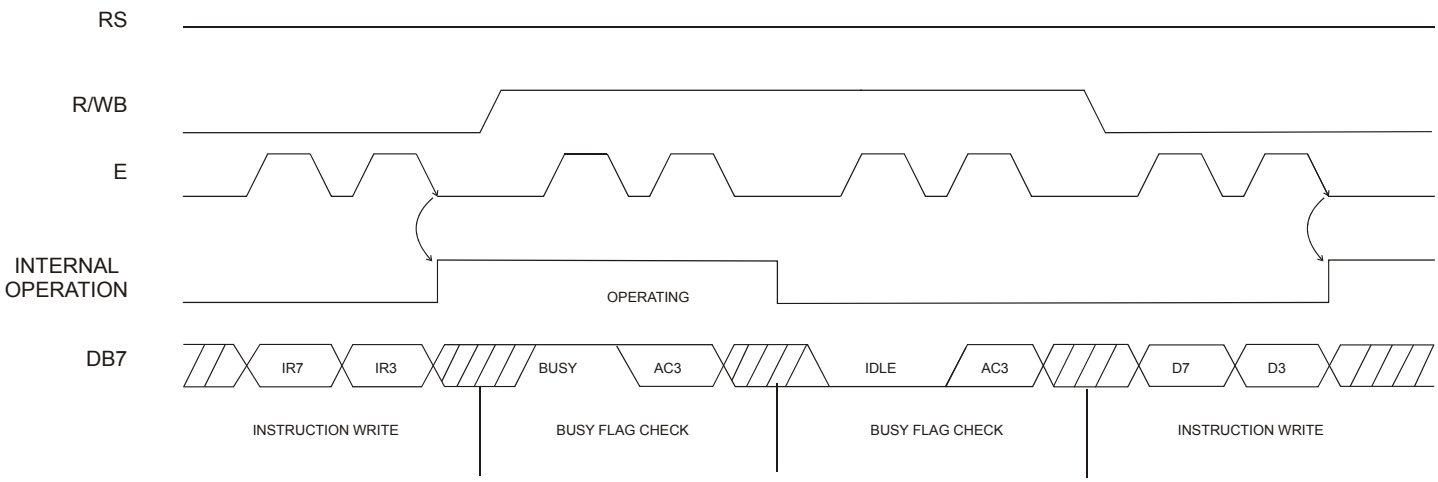
When PT6880 interfaces with an 8-bit MPU, DB0 to DB7 are used. The 8-bit data transfer starts from the four high order bits --DB4 to DB7 followed by the four low order bits -- DB0 to DB3.
An example of a Busy Flag Check Timing in an 8-Bit MPU Interface is given in the diagram below.



4-BIT MPU INTERFACE

PT6880 can be configured to interface with a 4-bit MPU and is selected via a program. If the I/O port of the 4-Bit MPU from which PT6880 is connected to, is capable of transferring 8-bit, then an 8-bit data transfer operation is executed. Otherwise, two 4-bit data transfer operations are needed to satisfy one complete data transfer.

Under the 4-bit data transfer, DB4 to DB7 are used as bus lines. DB0 to DB3 are disabled. The data transfer between PT6880 and MPU is completed after two 4-bit data have been transferred. The Busy Flag must be checked (one instruction) after completion of the data transfer (that is, 4-bit data has been transferred twice.). The Busy Flag must be checked after two 4-bit data transfer has been completed. Please refer to the diagram below for a 4-bit data transfer timing sequence.



where:
1. IR7=Instruction Bit 7
2. IR3=Instruction Bit 3
3. AC3=Address Counter 3

From the above timing diagram, it is important to note that the Busy Flag Check and the data transfer are both executed twice.

OLED INTERFACE

PT6880 supports two display types, namely: 5 x 8 dots and 5 x 10 dots character fonts. Each of these types includes a cursor display. Up to 2 lines may be displayed in a 5x 8 dot character font type and 1 line for a 5 x 10 dots character font type. The number of lines that can be displayed as well as the type of font can be selected by using the software program. Please refer to the table below

Number of Display Line	Character Font Type	Number of Common Signals	Duty Factor
1	5 x 8 dots + cursor	8	1/8
1	5 x 10 dots + cursor	11	1/11
2	5 x 8 dots + cursor	16	1/16

As shown in the table above, three types of common signals are available. An example of each configuration is shown in the examples below. It should be noted that every 5 segment signal lines can display one digit, therefore, PT6880 can display up to 8 digits in a 1-line display and 16 digits in a 2-line display.

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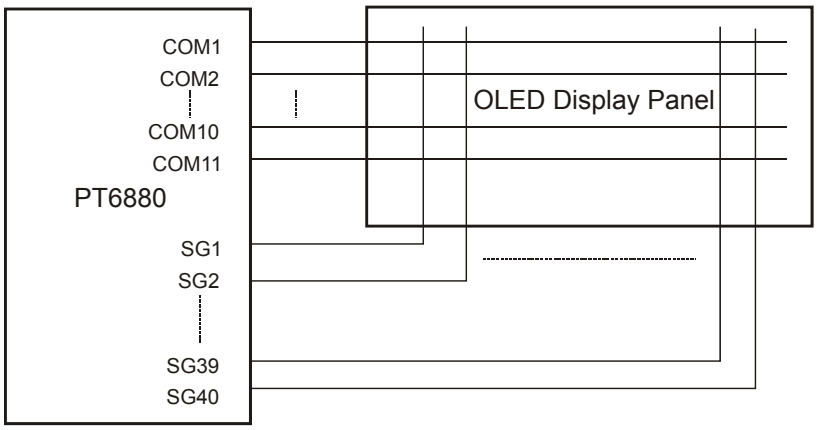
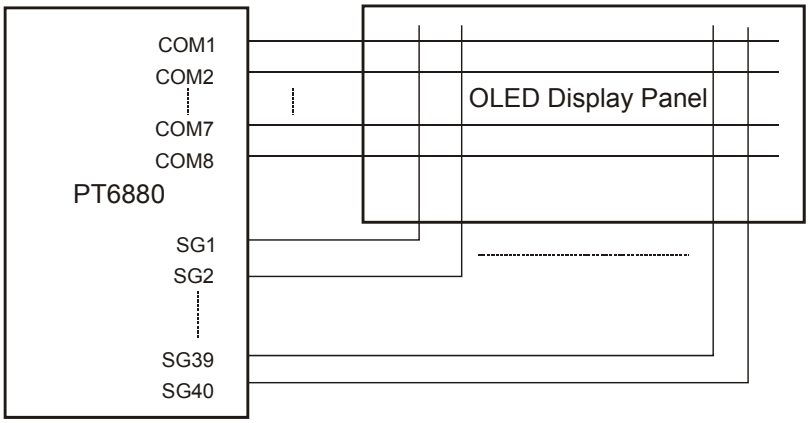
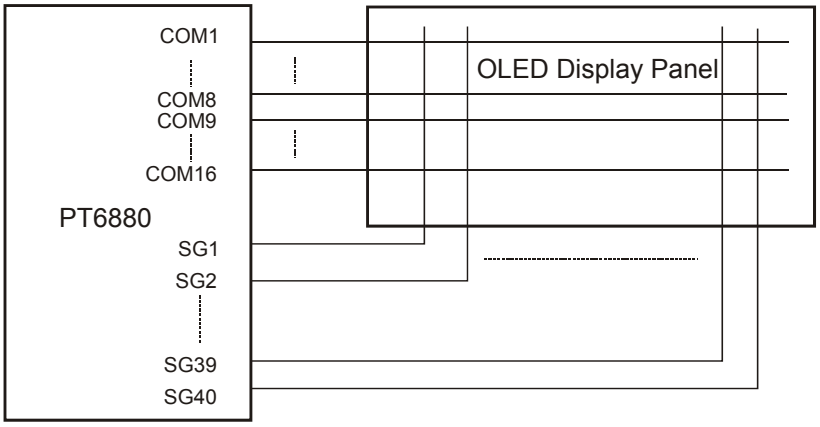
Example 1: An OLED and PT6880 interface with a 5 x 10 dot, 8-character x 1-line display at 1/11 duty cycle is given below.



Example 2: OLED and PT6880 connection with 5 x 8 dots, 8-character x 1-line display, at 1/8 duty cycle.



Example 3: OLED and PT6880 Connection when 5 x 8 dots, 8-character x 2-line display at 1/16 duty cycle.



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ABSOLUTE MAXIMUM RATING

(Unless otherwise specified, Ta=25℃)

Parameter	Symbol	Rating	Unit
Power supply voltage 1	VDD-GND	-0.3 to +5.5	V
Power supply voltage 2	V16 -SEGG	-0.3 to +18.0	V
Input voltage	Vt	-0.3 to VDD+0.3	V
Operating temperature	Topr	-40 to +85	℃
Storage temperature	Tstg	-65 to +150	℃

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃, V16=16V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage 1	VIH1	All input pins and I/O pins except OSC1 VDD=3V	0.7VDD	-	VDD VDD	V
		All input pins and I/O pins except OSC1 VDD=5V	2.2	-	VDD VDD	V
Low level input voltage 1	VIL1	All input pins and I/O pins except OSC1 VDD=3V	-0.3	-	0.55	V
		All input pins and I/O pins except OSC1 VDD=5V	-0.3	-	0.60	V
High level input voltage 2	VIH2	OSC1 VDD=3V	0.7VDD	-	VDD	V
		OSC1 VDD=5V	VDD -1.0	-	VDD	V
Low level input voltage 2	VIL2	OSC1 VDD=3V	-	-	0.2 VDD	V
		OSC1 VDD=5V	-	-	1.0	V
High level output voltage 1	VOH1	Applies to I/O Pins, DB0 to DB7, VDD=3V, IOH=-0.1mA	0.75VDD	-	-	V
		Applies to I/O Pins, DB0 to DB7, VDD=5V, IOH=-0.205mA	2.4	-	-	V
Low level output voltage 1	VOL1	Applies to I/O Pins, DB0 to DB7 VDD=3V, IOL=0.1mA	-	-	0.2VDD	V
		Applies to I/O Pins, DB0 to DB7 VDD=5V, IOL=1.2mA	-	-	0.1VDD	V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level output voltage 2	VOH2	All Output Pins except DB0 to DB7. VDD=3V, IOH=0.04mA	0.8VDD	-	-	V
		All Output Pins except DB0 to DB7. VDD=5V, IOH=0.04mA	0.9VDD	-	-	V
Low level output voltage 2	VOL2	All Output Pins except DB0 to DB7. VDD=3V, IOL=0.04mA	-	-	0.2VDD	V
		All Output Pins except DB0 to DB7. VDD=5V, IOL=0.04mA	-	-	0.1VDD	V
Input leakage current (see Note 1)	ILI	VDD=3V, VIN=0 to VDD	-1	-	1	μA
		VDD=5V, VIN=0 to VDD	-1	-	1	μA
Pull-up MOS current	Iup	DB0 to DB7, RS, R/WB VDD=3.0V	10	50	120	μA
		DB0 to DB7, RS, R/WB VDD=5.0V	50	125	250	μA
Operating current (see Notes 2)	Icc	Rf Oscillation, External Clock VDD=3V, fosc=270KHz	-	-	1	mA
		Rf Oscillation, External Clock VDD=5V, fosc=270KHz	-	-	2	mA
High level segment output current	ISEGOH	VSEGOH=14V	-30	-	-300	μA
High level segment output current tolerance	ITOL1	BVR=VDD, DVR=VDD VSEGOH=14V	-	-	±6	%
High level segment output current tolerance	ITOL2	BVR=VDD, DVR=VDD VSEGOH=14V	-	-	±6	%
Low level common sink current	ICOMOL	VCOMOL=0.4V	15	-	-	mA

Notes:
1. Current flowing through pull-up MOSs, excluding output drive MOS.
2. Input/Output current is not included. When the input is at an intermediate level with the CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.

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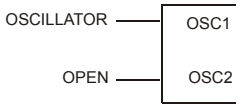
AC ELECTRICAL CHARACTERISTICS

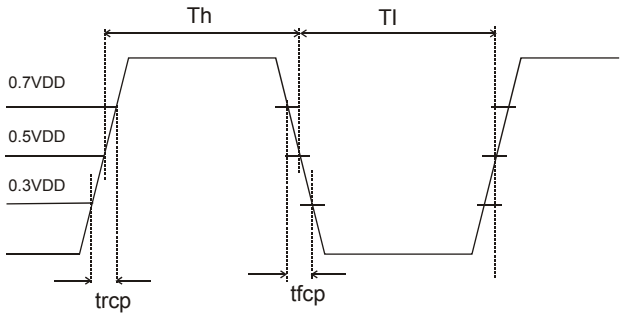
(Unless otherwise specified, Ta = 25℃, V16=16V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
External clock frequency	fcp	Applies only to external clock operation. (see Note 1), VDD=3V	370	460	670	KHz
		Applies only to external clock operation. (see Note 1), VDD=5V	370	460	670	KHz
External clock rise time	trcp	Applies only to external clock operation. (see Note 1), VDD=3V	-	-	0.2	μs
		Applies only to external clock operation. (see Note 1), VDD=5V	-	-	0.2	μs
External clock fall time	tfcp	Applies only to external clock operation. (see Note 1), VDD=3V	-	-	0.2	μs
		Applies only to external clock operation. (see Note 1), VDD=5V	-	-	0.2	μs
Clock oscillation frequency	fosc	Rf=75KΩ (see Note 2) VDD=3V	450	560	670	KHz
		Rf=91KΩ (see Note 2) VDD=5V	370	460	550	KHz

Notes:

1. These parameters apply only to external clock operation. Please refer to the diagram below.





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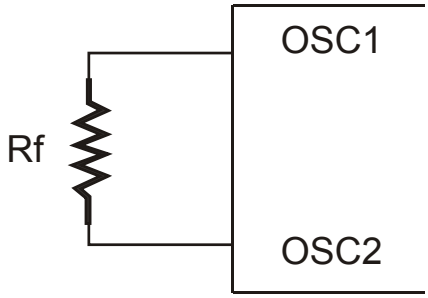
2. This parameter applies only to the internal oscillation operation using an oscillation resistor Rf. Please refer to the diagram below.



When VDD=5V, Rf=91KΩ ±2%
VDD=3V, Rf=75KΩ ±2%

The values of the Oscillation Frequency depend on the capacitance of the pins-OSC1 and OSC2-therefore, the wiring length of these puns must be minimized.

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BUS TIMING CHARACTERISTICS

(Unless otherwise specified, Ta=-20 to +75℃, VDD=5V or 3V, V16=16V)

WRITE OPERATION TIMING CHARACTERISTICS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Enable cycle time	tcycE	VDD=3V	1000	-	-	ns
		VDD=5V	500	-	-	ns
Enable pulse width (High level)	PWEH	VDD=3V	450	-	-	ns
		VDD=5V	230	-	-	ns
Enable rise/fall time	tEf, tEr	VDD=3V	-	-	25	ns
		VDD=5V	-	-	20	ns
Address set-up time (RS, R/WB to E)	tAS	VDD=3V	60	-	-	ns
		VDD=5V	40	-	-	ns
Address hold time	tAH	VDD=3V	20	-	-	ns
		VDD=5V	10	-	-	ns
Data set-up time	tDSW	VDD=3V	195	-	-	ns
		VDD=5V	80	-	-	ns
Data hold time	tH	VDD=3V	20	-	-	ns
		VDD=5V	20	-	-	ns

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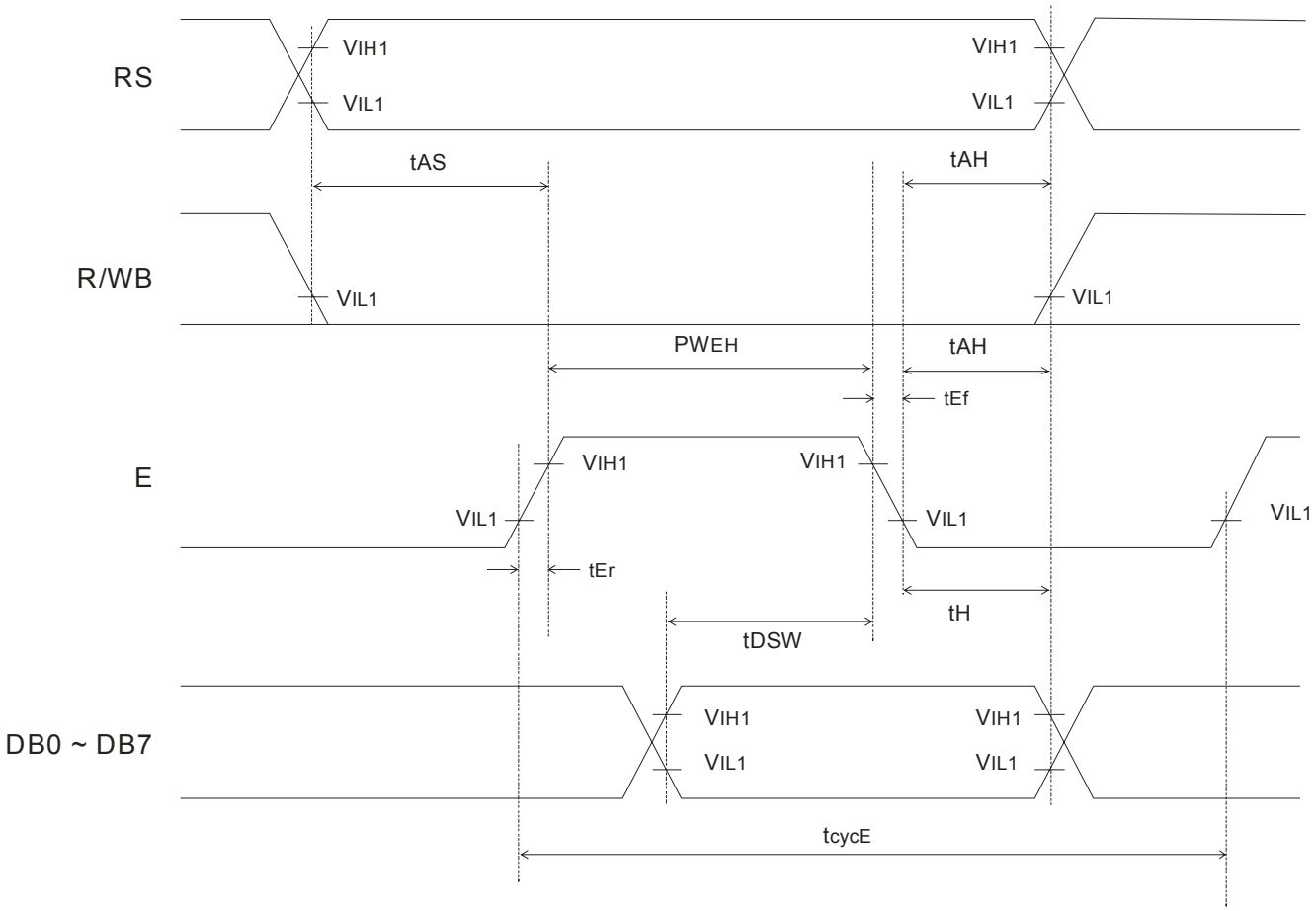
WRITE OPERATION TIMING DIAGRAM



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READ OPERATION TIMING CHARACTERISTICS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Enable cycle time	tcycE	VDD=3V	1000	-	-	ns
		VDD=5V	500	-	-	ns
Enable pulse width (High level)	PWEH	VDD=3V	450	-	-	ns
		VDD=5V	230	-	-	ns
Enable rise/fall time	tEf, tEr	VDD=3V	-	-	25	ns
		VDD=5V	-	-	20	ns
Address set-up time (RS, R/WB to E)	tAS	VDD=3V	60	-	-	ns
		VDD=5V	40	-	-	ns
Address hold time	tAH	VDD=3V	20	-	-	ns
		VDD=5V	10	-	-	ns
Data delay time	tDDR	VDD=3V	-	-	360	ns
		VDD=5V	-	-	160	ns
Data hold time	tDHR	VDD=3V	5	-	-	ns
		VDD=5V	5	-	-	ns

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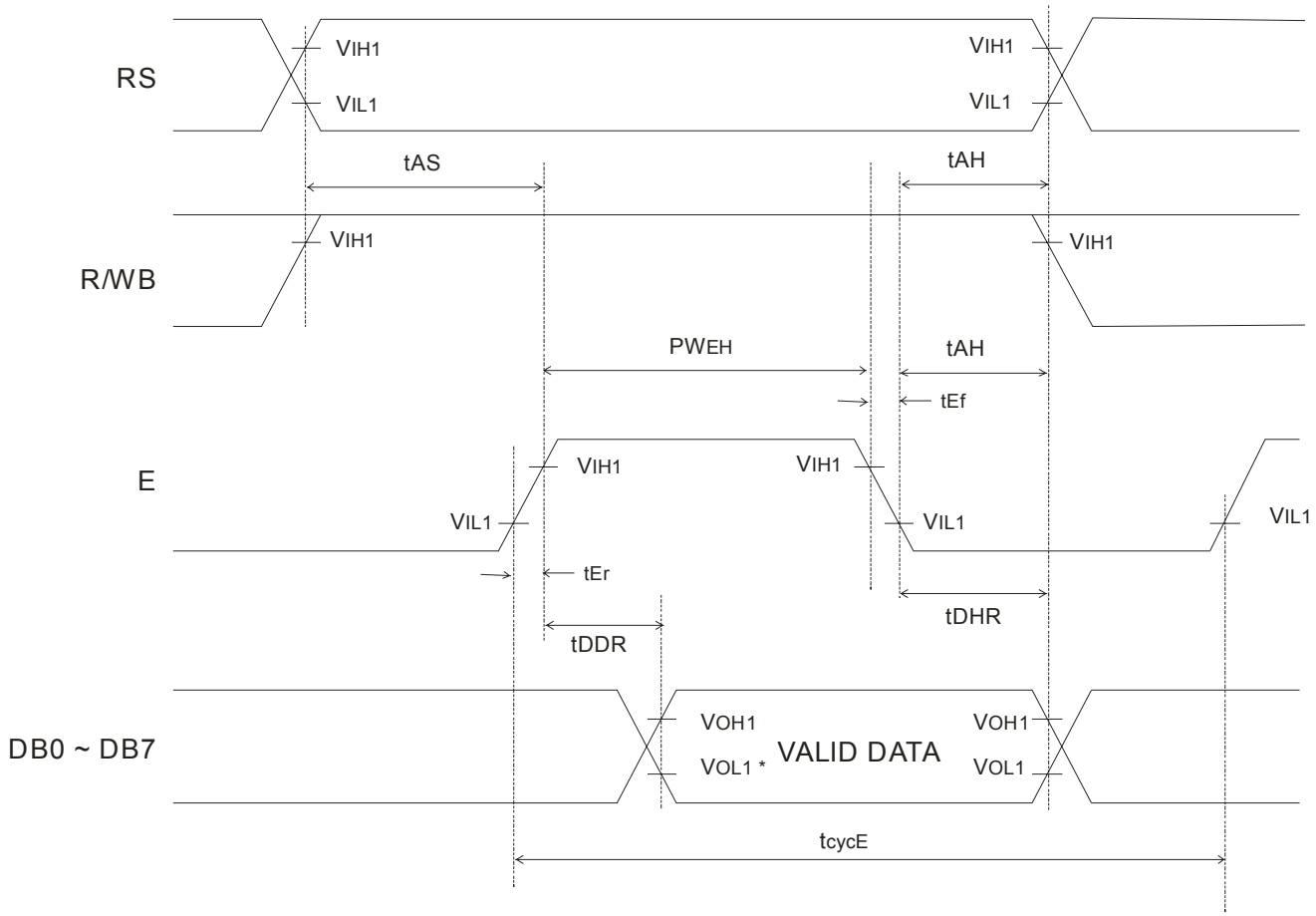
READ OPERATION TIMING DIAGRAM



Note: *=VOL1 is assumed to be 0.8V at 2MHz Operation.

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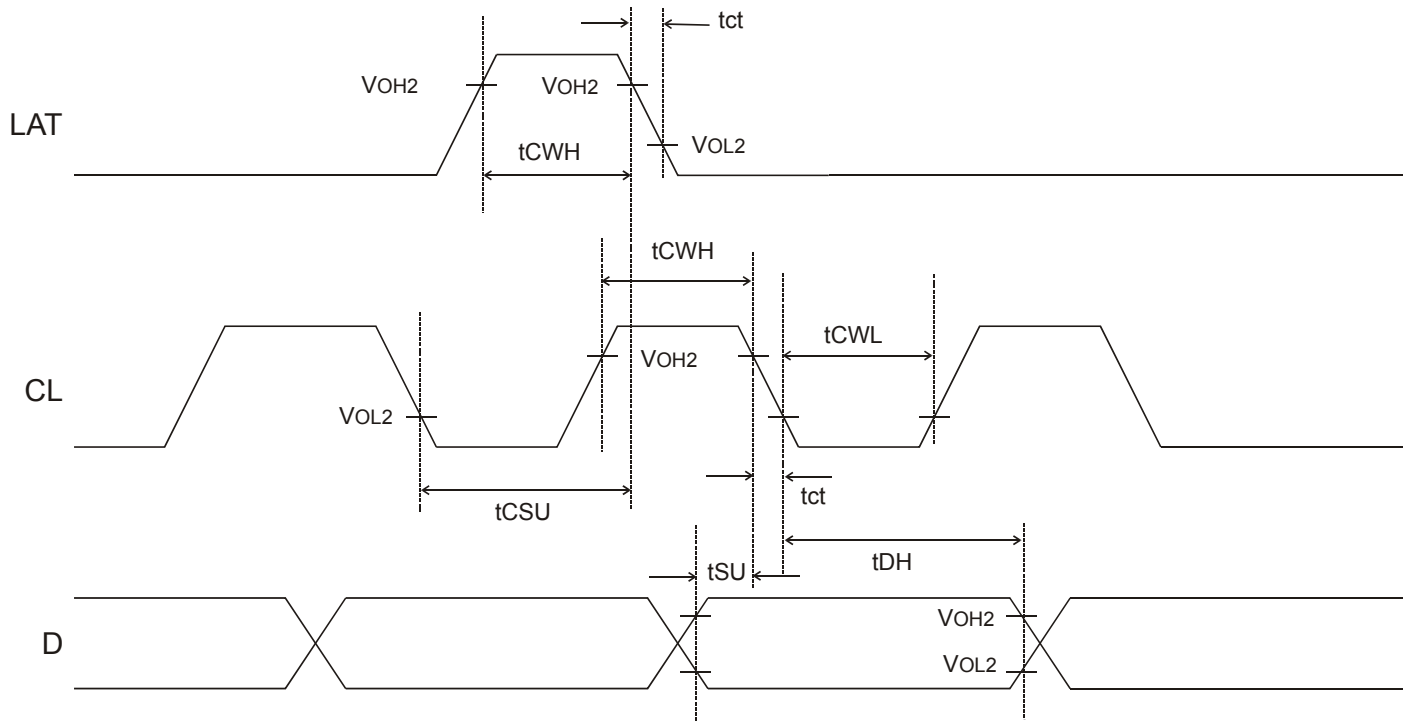
INTERFACE TIMING CHARACTERISTICS WITH EXTERNAL DRIVER

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level clock pulse width	tCWH	VDD=3V	800	-	-	ns
		VDD=5V	800	-	-	ns
Low level clock pulse width	tCWL	VDD=3V	800	-	-	ns
		VDD=5V	800	-	-	ns
Clock set-up time	tCSU	VDD=3V	500	-	-	ns
		VDD=5V	500	-	-	ns
Data set-up time	tSU	VDD=3V	300	-	-	ns
		VDD=5V	300	-	-	ns
Data hold time	tDH	VDD=3V	300	-	-	ns
		VDD=5V	300	-	-	ns
Clock rise/fall time	tct	VDD=3V	-	-	200	ns
		VDD=5V	-	-	100	ns

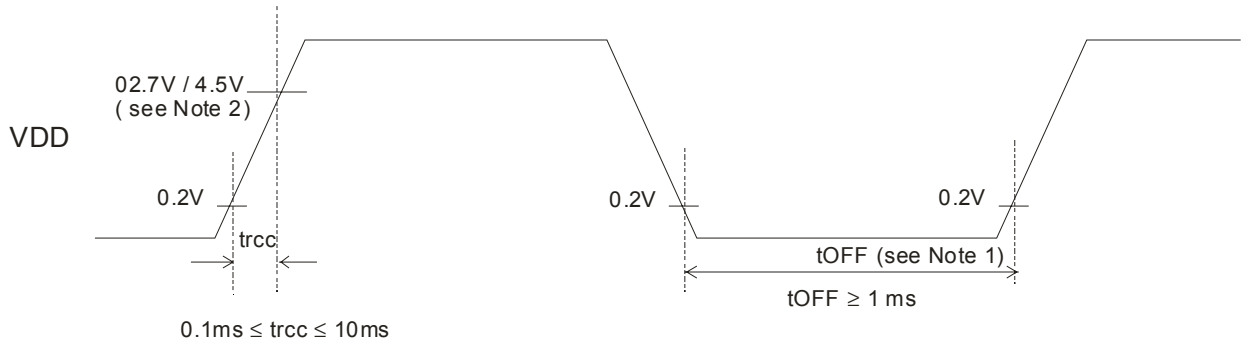
INTERFACE TIMING WITH EXTERNAL DRIVER DIAGRAM



POWER SUPPLY CONDITION FOR INTERNAL RESET CIRCUIT

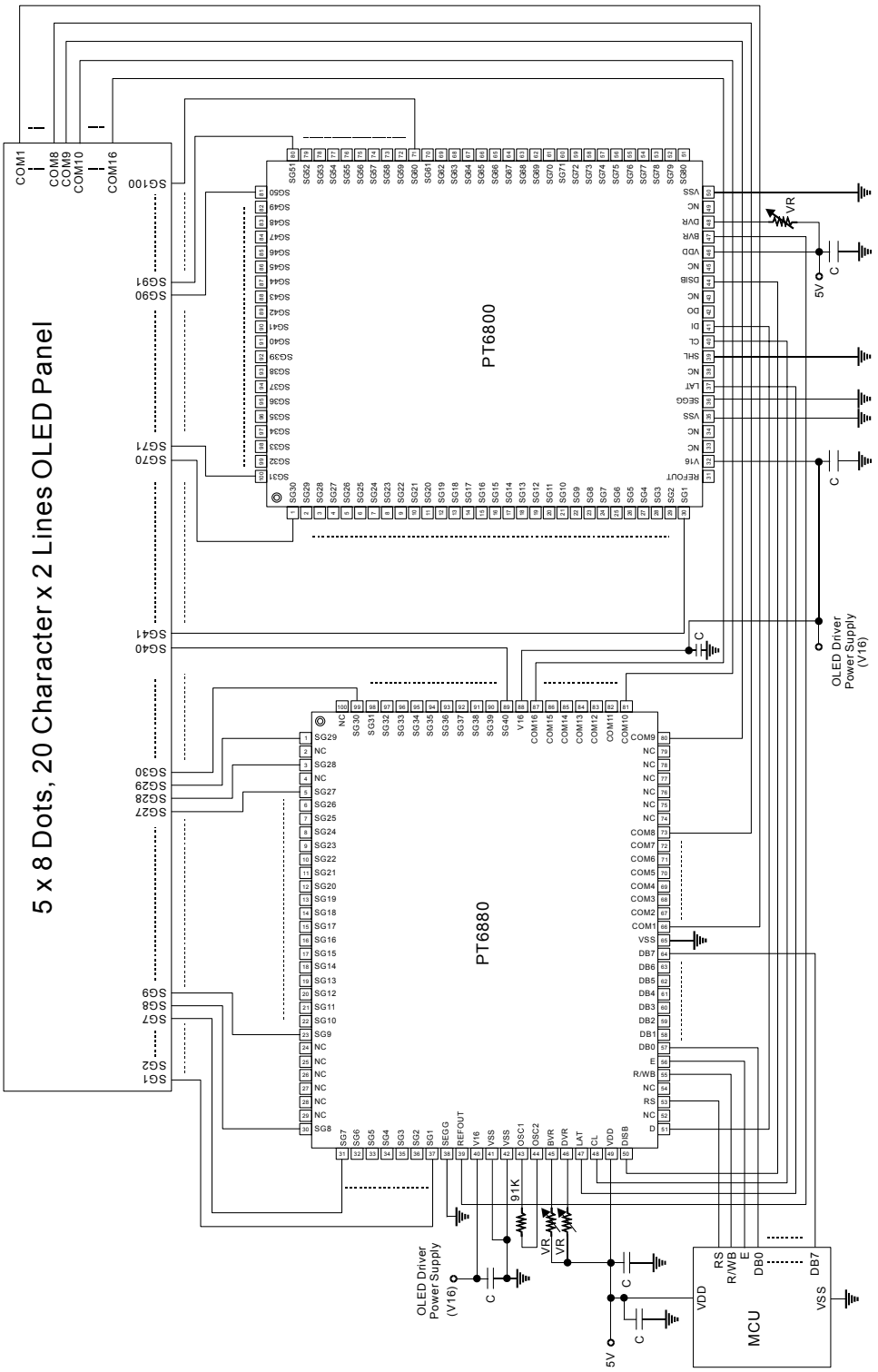
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply rise time	trCC	VDD=3V	0.1	-	10	ms
		VDD=5V	0.1	-	10	ms
Power supply off time	tOFF	VDD=3V	1	-	-	ms
		VDD=5V	1	-	-	ms

INTERNAL POWER SUPPLY RESET TIMING DIAGRAM



Notes:
1. tOFF compensates for the power oscillation period caused by the momentary power supply oscillations.
2. Specified at 4.5V for a 5-Volt operation and at 2.7 for a 3-Volt operation.
3. If 4.5V is not reached during the 5-Volt operation, the internal reset circuit will not operate normally. Under this condition, PT6880 must be initialized using the instructions.

APPLICATION CIRCUIT



Note: VR= 100KΩ, C=0.1μF

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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6880-001-H	COB	-
PT6880-003-H	COB	-
PT6880-004-H	COB	-
PT6880-LQ-001	100 Pins, LQFP	PT6880-LQ-001
PT6880-LQ-003	100 Pins, LQFP	PT6880-LQ-003
PT6880-LQ-004	100 Pins, LQFP	PT6880-LQ-004

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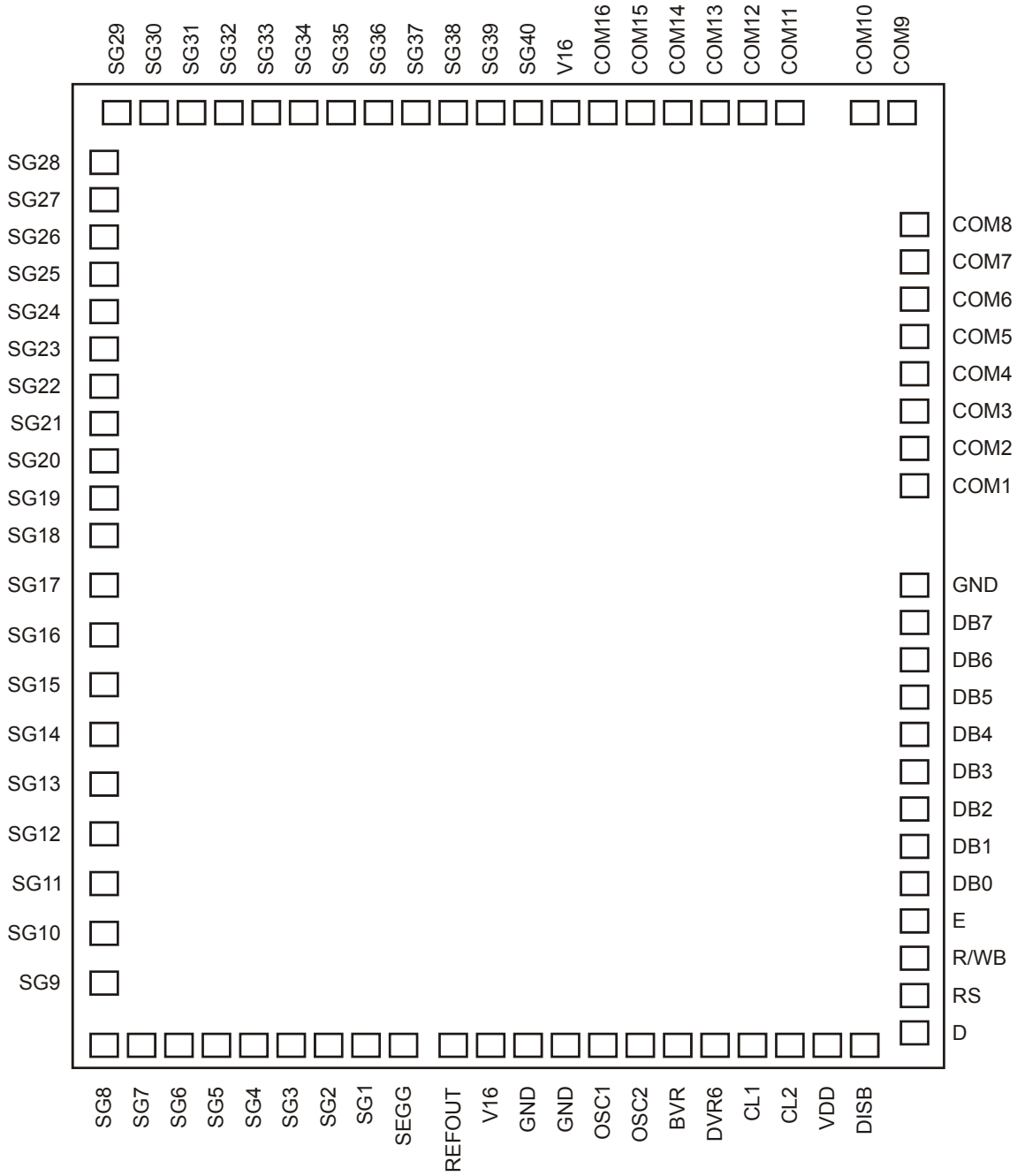
PAD CONFIGURATION



chip size: 2778*3128
pad size: 90*90
pitch size: 120
P-Substrate: VSS
unit: μm

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PAD LOCATION

PAD #	NAME	Location
1	SG(29)	[105.900, 3049.400]
2	NC	
3	SG(28)	[50.000, 2821.300]
4	NC	
5	SG(27)	[50.000, 2701.300]
6	SG(26)	[50.000, 2581.300]
7	SG(25)	[50.000, 2461.300]
8	SG(24)	[50.000, 2341.300]
9	SG(23)	[50.000, 2221.300]
10	SG(22)	[50.000, 2101.300]
11	SG(21)	[50.000, 1981.300]
12	SG(20)	[50.000, 1861.300]
13	SG(19)	[50.000, 1741.300]
14	SG(18)	[50.000, 1625.600]
15	SG(17)	[50.000, 1475.600]
16	SG(16)	[50.000, 1325.600]
17	SG(15)	[50.000, 1175.600]
18	SG(14)	[50.000, 1025.600]
19	SG(13)	[50.000, 875.600]
20	SG(12)	[50.000, 725.600]
21	SG(11)	[50.000, 575.600]
22	SG(10)	[50.000, 425.600]
23	SG(9)	[50.000, 275.600]
24	NC	
25	NC	
26	NC	
27	NC	
28	NC	
29	NC	
30	SG(8)	[50.000, 50.000]
31	SG(7)	[171.300, 50.000]
32	SG(6)	[292.000, 50.000]
33	SG(5)	[412.000, 50.000]

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PAD #	NAME	Location
34	SG(4)	[532.000, 50.000]
35	SG(3)	[652.000, 50.000]
36	SG(2)	[772.000, 50.000]
37	SG(1)	[892.000, 50.000]
38	SEGG	[1012.014, 50.000]
39	REFOUT	[1153.128, 50.000]
40	V16	[1282.214, 50.000]
41	VSS	[1402.200, 50.000]
42	VSS	[1522.200, 50.000]
43	OSC1	[1642.200, 50.000]
44	OSC2	[1762.200, 50.000]
45	BVR	[1882.200, 50.000]
46	DVR	[2002.200, 50.000]
47	LAT	[2122.200, 50.000]
48	CL	[2242.200, 50.000]
49	VDD	[2362.200, 50.000]
50	DISB	[2482.200, 50.000]
51	D	[2699.200, 90.500]
52	NC	
53	RS	[2699.200, 210.500]
54	NC	
55	R/WB	[2699.200, 330.500]
56	E	[2699.200, 450.500]
57	DB(0)	[2699.200, 570.500]
58	DB(1)	[2699.200, 690.500]
59	DB(2)	[2699.200, 810.500]
60	DB(3)	[2699.200, 930.500]
61	DB(4)	[2699.200, 1050.500]
62	DB(5)	[2699.200, 1170.500]
63	DB(6)	[2699.200, 1290.500]
64	DB(7)	[2699.200, 1410.500]
65	VSS	[2699.200, 1537.900]
66	COM(1)	[2699.200, 1921.000]
67	COM(2)	[2699.200, 2041.000]
68	COM(3)	[2699.200, 2161.000]

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PAD #	NAME	Location
69	COM(4)	[2699.200, 2281.000]
70	COM(5)	[2699.200, 2401.000]
71	COM(6)	[2699.200, 2521.000]
72	COM(7)	[2699.200, 2641.000]
73	COM(8)	[2699.200, 2761.000]
74	NC	
75	NC	
76	NC	
77	NC	
78	NC	
79	NC	
80	COM(9)	[2690.800, 3049.400]
81	COM(10)	[2570.800, 3049.400]
82	COM(11)	[2380.800, 3049.400]
83	COM(12)	[2240.800, 3049.400]
84	COM(13)	[2100.800, 3049.400]
85	COM(14)	[1960.800, 3049.400]
86	COM(15)	[1820.800, 3049.400]
87	COM(16)	[1680.800, 3049.400]
88	V16	[1560.800, 3049.400]
89	SG(40)	[1440.800, 3049.400]
90	SG(39)	[1320.800, 3049.400]
91	SG(38)	[1185.900, 3049.400]
92	SG(37)	[1065.900, 3049.400]
93	SG(36)	[945.900, 3049.400]
94	SG(35)	[825.900, 3049.400]
95	SG(34)	[705.900, 3049.400]
96	SG(33)	[585.900, 3049.400]
97	SG(32)	[465.900, 3049.400]
98	SG(31)	[345.900, 3049.400]
99	SG(30)	[225.900, 3049.400]
100	NC	

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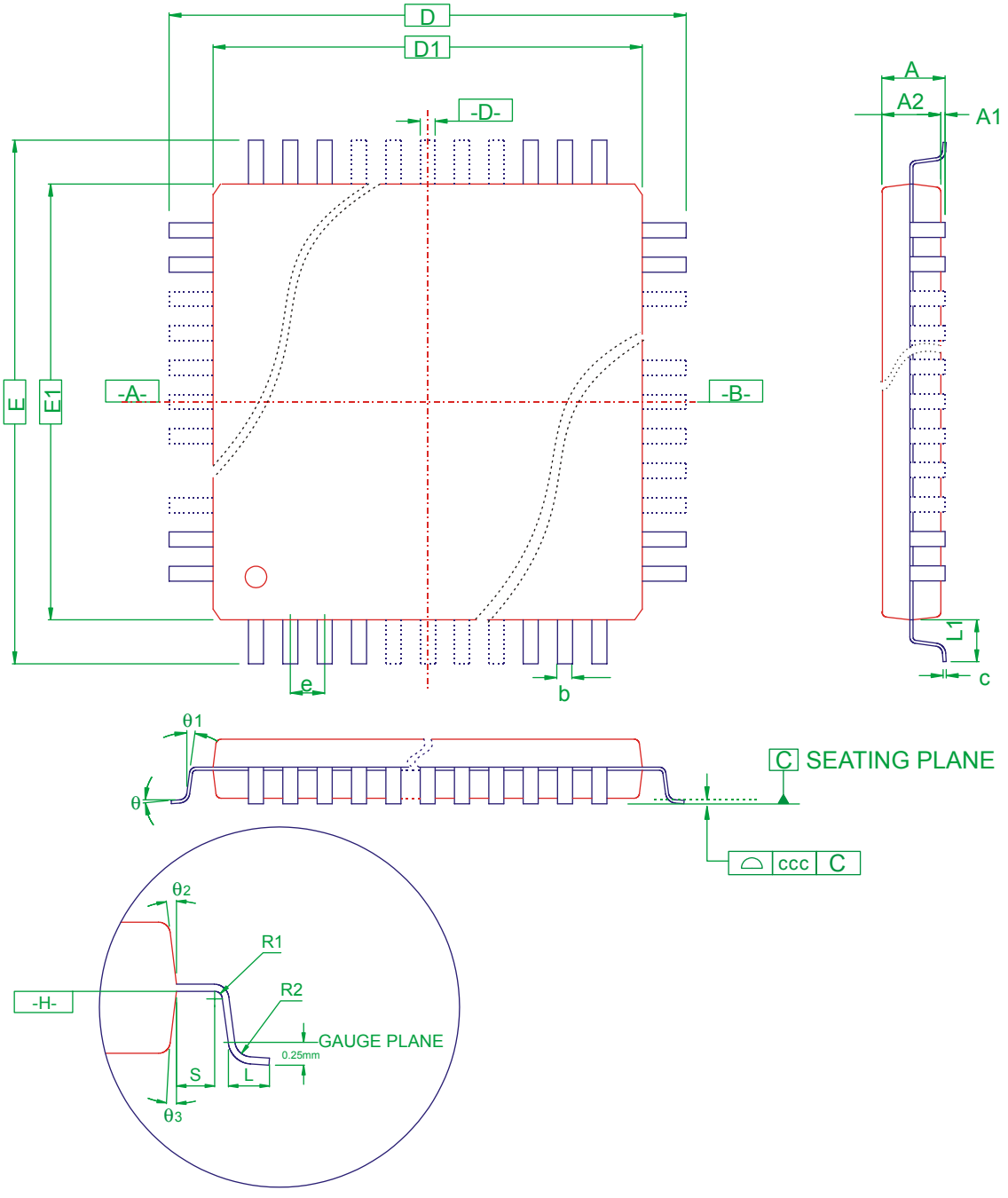
PACKAGE INFORMATION

100 PINS, LQFP PACKAGE (BODY SIZE: 14MM X 14MM, PITCH: 0.50MM, THK: 1.40MM)



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	.027
D		16.00 BSC.	
D1		14.00 BSC.	
E		0.50 BSC.	
E		16.00 BSC.	
E1		14.00 BSC.	
Θ	0^o	3.5^o	7^o
θ1	0^o	-	-
θ2	11^o	12^o	13^o
θ3	11^o	12^o	13^o
C	0.09	-	0.20
L	0.45	0.60	0.75
L1		1.00 REF.	
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
ccc		0.08	

Notes:
1. Dimensioning and tolerancing per ASMEY14.5-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at the datum plane H.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusions is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mismatch.
5. Details of Pin1 identifier are optional but must be located within the zone indicated.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
7. Exact shape of each corner is optional.
8. A1 is defined as the distance from the seating plane to the lowest point on the package body.
9. Controlling Dimension: Millimeters
10. Refer to JEDEC MS-026 Variation BED

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