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NT7705

160 Output LCD Segment/Common Driver

Features

(Segment mode)

- Shift Clock frequency :
  14 MHz (Max.) (V_{DD} = 5V ± 10%)
  8 MHz (Max.) (V_{DD} = 2.5V - 4.5V)
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function with an enable signal
- Automatic counting function when in the chip select mode, causes the internal clock to be stopped by automatically counting 160 bits of input data

(Common mode)

- Shift clock frequency:
  4.0MHz (Max.)
- Built-in 160-bits bidirectional shift register (divisible into 80-bits x 2)
- Available in a single mode (160-bits shift register) or in a dual mode (80-bits shift register x 2)
  1. Y1 → Y160 Single mode
  2. Y160 → Y1 Single mode
  3. Y1 → Y80, Y81 → Y160 Dual mode
  4. Y160 → Y81, Y80 → Y1 Dual mode

  The above 4 shift directions are pin-selectable
- Available in a 160 outputs mode or in a 120 outputs mode by pin option for easier the ITO layout

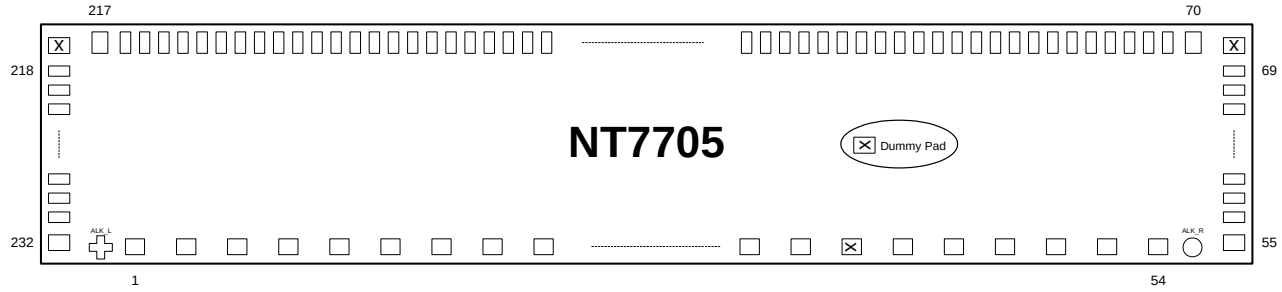
(Both segment mode and common mode)

- Supply voltage for LCD drive: 15.0 to 40.0V
- Number of LCD driver outputs: 160
- Low output impedance
- Low power consumption
- Supply voltage for the logic system: +2.5 to +5.5V
- CMOS process
- Package : Gold bump die
- Not designed or rated as radiation hardened

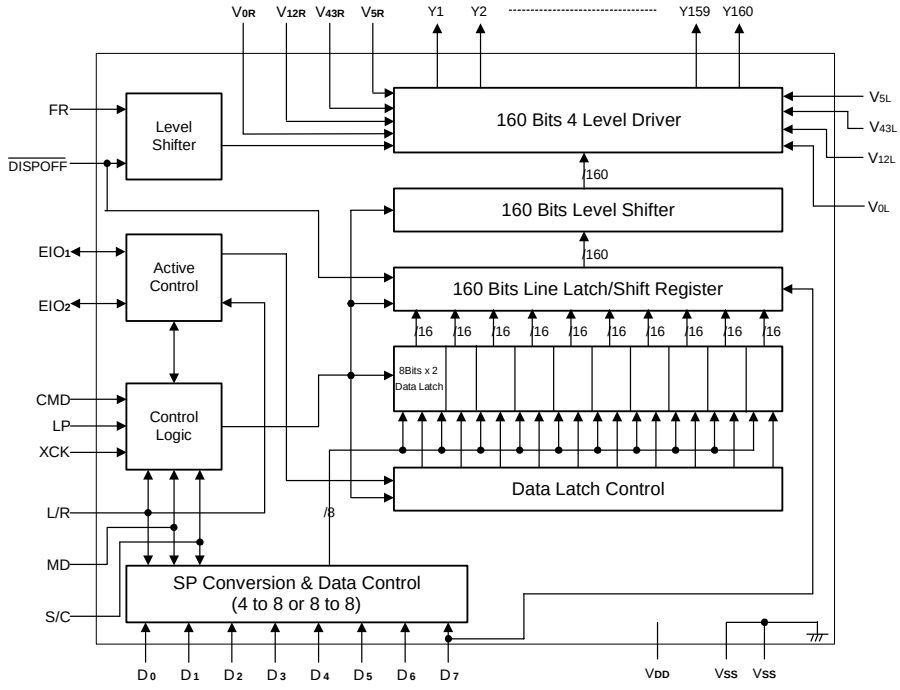
General Description

The NT7705 is a 160-bit output segment/common driver LSI suitable for driving the large-scale dot matrix LCD panels used by PDA's, personal computers and workstations for example. Through the use of COG technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The NT7705 is good as both a segment driver and a common driver, and a low power consuming, high-precision LCD panel display can be assembled using the NT7705. In the segment mode, the data input is selected 4bit parallel input mode or as 8bit parallel input mode by a mode (MD) pin. In common mode, the data input/output pins are bi-directional and the four data shift directions are pin-selectable.

Pad Configuration



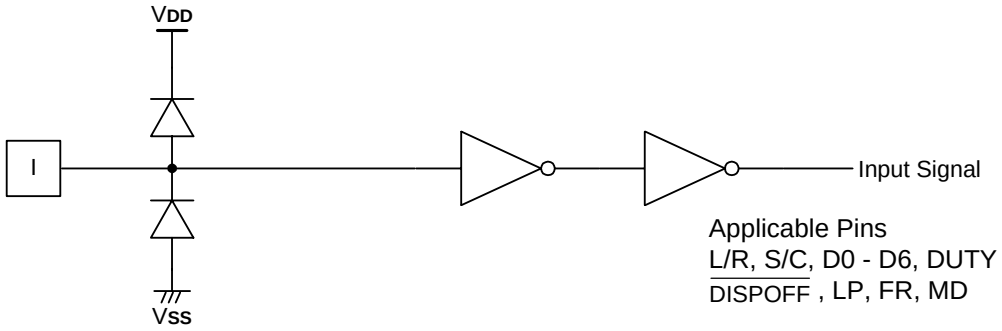
Block Diagram



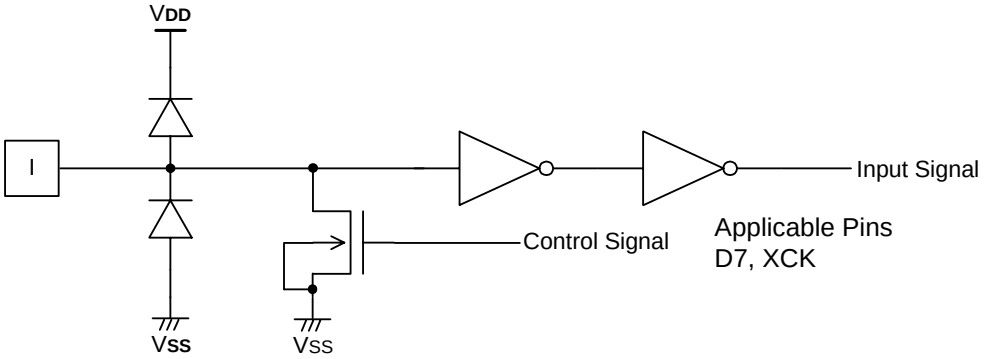
Pad Description

Pad No.	Designation	I/O	Description
224-226	V_{0L}	P	Power supply for LCD driver
227-229	V_{12L}	P	Power supply for LCD driver
230-232	V_{43L}	P	Power supply for LCD driver
1-2	V_{5L}	P	Power supply for LCD driver
3-6, 49-52	V_{SS}	P	Ground (0V), these pads must be connected to each other
7-8	CMD	I	Common mode output selection pin
9-10	L/R	I	Display data shift direction selection
11-16	V_{DD}	P	Power supply for the logic system (+2.5 to + 5.5V)
17-18	S/C	I	Segment mode/common mode selection
19-20	EIO_2	I/O	Input/output for chip select or data of shift register
21-34	D0 - D6	I	Display data input for segment mode
35-36	D7	I	Display data input for Segment mode / Dual mode data input
37-38	XCK	I	Display data shift clock input for segment mode
39-40	$\overline{DISPOFF}$	I	Control input for deselect output level
41-42	LP	I	Latch pulse input / shift clock input for the shift register
43-44	EIO_1	I/O	Input/output for chip select or data of the shift register
45-46	FR	I	AC-converting signal input for LCD driver waveform
47-48	MD	I	Mode selection input
53-54	V_{5R}	P	Power supply for LCD driver
55-57	V_{43R}	P	Power supply for LCD driver
58-60	V_{12R}	P	Power supply for LCD driver
61-63	V_{0R}	P	Power supply for LCD driver
64-223	Y1 - Y160	O	LCD driver output

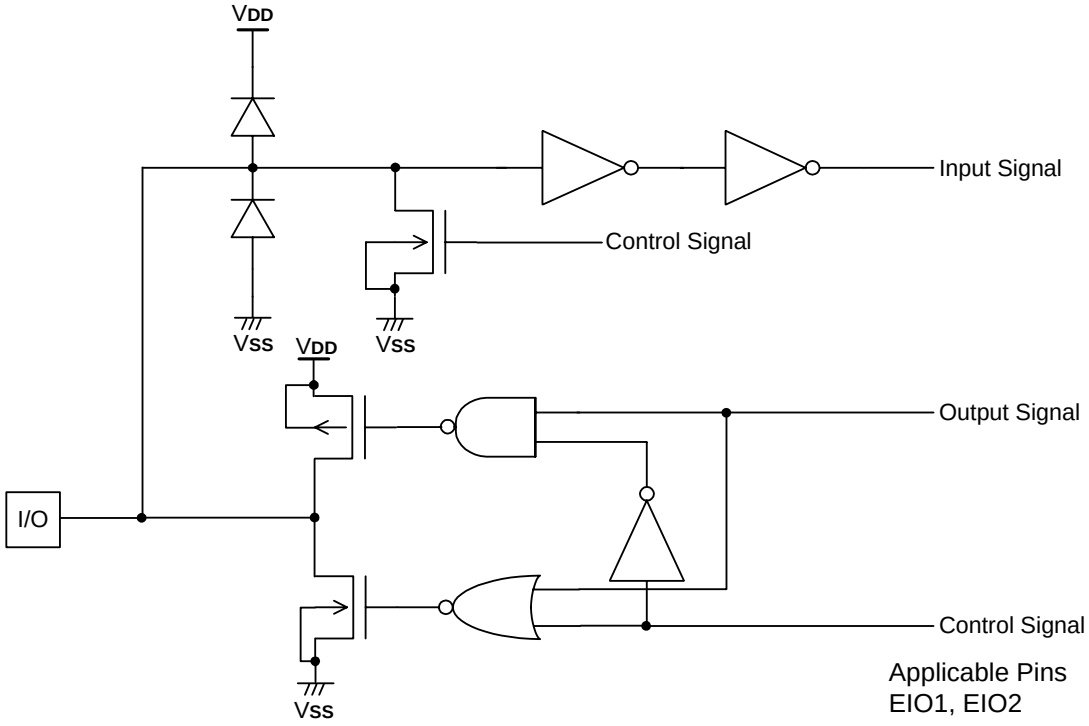
Input / Output Circuits



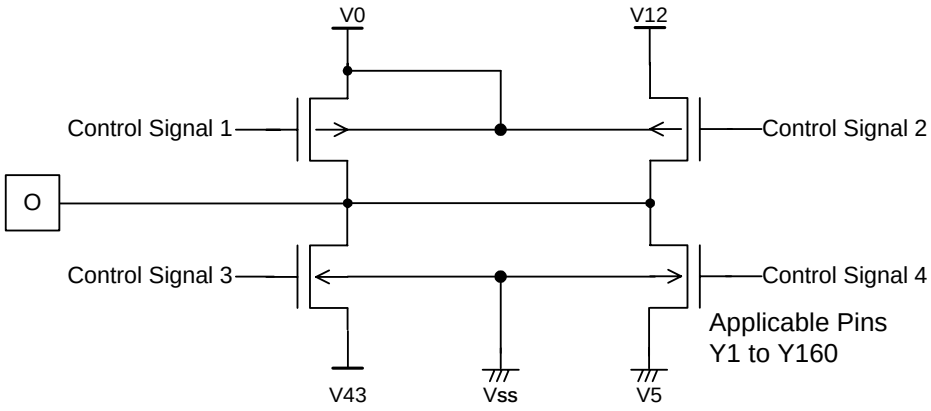
Input Circuit (1)



Input Circuit (2)



Input / Output Circuit



LCD Driver Output circuit

Pad Description

Segment mode

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5V
V_{SS}	Ground pin connects to 0V
V_{OR}, V_{OL} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply pin for LCD driver voltage bias ● Normally, the bias voltage used is set by a resistor divider ● Ensure that the voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$ ● To further reduce the differences between the output waveforms of the LCD driver output pins Y_1 and Y_{160}, externally connect V_{IR} and V_{IL} (I = 0, 12, 43)
D_0 - D_7	Input pin for display data ● In 4-bit parallel input mode, input data into the 4 pins D_0 - D_3. Connect D_4 - D_7 to V_{SS} or V_{DD} ● In 8-bit parallel input mode, input data into the 8 pins D_0 - D_7
XCK	Clock input pin for taking display data ● Data is read on the falling edge of the clock pulse
LP	Latch pulse input pin for display data ● Data is latched on the falling edge of the clock pulse
L/R	Direction selection pin for reading display data ● When set to V_{SS} level "L", data is read sequentially from Y160 to Y1 ● When set to V_{DD} level "H", data is read sequentially from Y1 to Y160
$\overline{\text{DISPOFF}}$	Control input pin for output deselect level ● The input signal is level-shifted from logic voltage level to LCD driver voltage level, and controls LCD driver circuit ● When set to V_{SS} level “L”, the LCD driver output pins (Y1 - Yl60) are set to level V_5 ● While $\overline{\text{DISPOFF}}$ is set to “L”, the contents of the line latch are reset, but the display data in the data latch are read regardless of the condition of $\overline{\text{DISPOFF}}$. When the $\overline{\text{DISPOFF}}$ function is canceled, the driver outputs deselect level (V_{12} or V_{43}), then outputs the contents of the date latch onto the next falling edge of the LP. That time, if $\overline{\text{DISPOFF}}$ removal time can not keep regulation what is shown AC characteristics, can not output the reading data correctly
FR	AC signal input for LCD driving waveform ● The input signal is level-shifted from the logic voltage level to the driver voltage level, and controls LCD driver circuit ● Normally inputs a frame inversion signal The LCD driver output pin’s output voltage level can be set to the line latch output signal and the FR signal
MD	Mode selection pin ● When set to V_{SS} level “L”, 4-bit parallel input mode is set ● When set to V_{DD} level “H", 8-bit parallel input mode is set
CMD	Not used ● Connect to V_{SS} or V_{DD}. Avoiding floating

Segment mode continued

Symbol	Function
S/C	Segment mode/common mode selection pin ● When set to V_{DD} level "H", segment mode is set. ● When set to V_{SS} level "L", common mode is set.
EIO_1, EIO_2	Input/output pin for chip selection ● When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. ● When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. ● During output, it is set to "H" while LP* $\overline{XCK}$ is "H" and after 160-bits of data have been read, it is set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H" ● During input, after the LP signal is input, the chip is selected while EI is set to "L". After 160-bits of data have been read, the chip is deselected
Y_1 - Y_{160}	LCD driver output pins These corresponding directly to each bit of the data latch, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output

Common mode

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5V
V_{SS}	Ground pin connects to 0V
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply pin for LCD driver voltage bias. ● Normally, the bias voltage used is set by a resistor divider ● Ensure that the voltages are set such that $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$ ● To further reduce the differences between the output waveforms of the LCD driver output pins Y_1 and Y_{160}, externally connect V_{IR} and V_{IL} (I = 0, 12, 43)
EIO_1	Bi-directional shift register shift data input/output pin ● Is an Output pin when L/R is at V_{SS} level "L" and an input pin when L/R is at V_{DD} level "H" ● When EIO_1 is used as an input pin, it will be pulled-down ● When EIO_1 is used as an output pin, it won't be pulled-down
EIO_2	Bi-directional shift register shift data input/output pin ● Is an Input pin when L/R is at V_{SS} level "L" and an output pin when L/R is at V_{DD} level "H" ● When EIO_2 is used as an input pin, it will be pulled-down ● When EIO_2 is used as an output pin, it won't be pulled-down
LP	Bi-directional shift register shift clock pulse input pin ● Data is shifted on the falling edge of the clock pulse
L/R	Bi-directional shift register shift direction selection pin ● Data is shifted from Y_{160} to Y_1 when it is set to V_{SS} level "L", and data is shifted from Y_1 to Y_{160} when it is set to V_{DD} level "H"

Common mode continued

Symbol	Function
$\overline{\text{DISPOFF}}$	Control input pin for output deselect level ● The input signal is level-shifted from the logic voltage level to the LCD driver voltage level and it controls the LCD driver circuit ● When set to V_{SS} level "L", the LCD driver output pins (Y_1 - Y_{160}) are set to level V_5 ● While set to "L", the contents of the shift resister are reset and not reading data. When the $\overline{\text{DISPOFF}}$ function is canceled, the driver outputs deselect level (V_{12} or V_{34}), and the shift data is read on the falling edge of the LP. That time, if $\overline{\text{DISPOFF}}$ removal time can not keep regulation what is shown AC characteristics, the shift data is not reading correctly
FR	AC signal input for LCD driving waveform ● The input signal is level-shifted from the logic voltage level to the LCD driver voltage level, and controls the LCD driver circuit ● Normally, inputs a frame inversion signal The LCD driver output pin's output voltage level can be set using the shift register output signal and the FR signal
MD	Mode selection pin ● When set to V_{SS} level "L", Single Mode operation is selected. When set to V_{DD} level "H", Dual Mode operation is selected
CMD	Common mode output selection pin ● When set to V_{SS} level "L", 160 outputs operation is selected. When set to V_{DD} level "H", 120 outputs operation is selected
D_7	Dual Mode data input pin ● According to the data shift direction of the data shift register, data can be input starting from the 81st bit When the chip is used as Dual Mode, D_7 will be pulled-down When the chip is used as Single Mode, D_7 won't be pulled-down
S/C	Segment mode/common mode selection pin ● When set to V_{SS} level "L", common mode is set
D_0 - D6	Not used ● Connect D_0-D_6 to V_{SS} or V_{DD}. Avoiding floating
XCK	Not used ● XCK is pulled-down in common mode, so connect to V_{SS} or open
Y_1 - Y_{160}	LCD driver output pins ● These corresponding directly Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output

Functional Description

1. Block description

1.1. Active Control

In the case of segment mode, controls the selection or deselection of the chip. Following a LP signal input, and after the select signal is input, a select signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the ship is deselected.

In the case of common mode, controls the input/output data of bidirectional pins.

1.2. SP Conversion & Data Control

In the case of segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bit parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

1.3. Data Latch Control

In the case of the segment mode, it selects the state of the data latch, which reads in the data bus signals. The shift direction is controlled by the control logic and for every 16 bits of data read in, the selection signal shifts one bit, based on the state of the control circuit.

1.4. Data Latch

In the case of the segment mode, it latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch control 160 bits of data are read in 20 sets of 8 bits.

1.5. Line Latch / Shift Register

In the case of the segment mode, all 160 bits which have been read into the data latch, are simultaneously latched on to the falling edge of the LP signal, and output to the level shift block.

In the case of the common mode, shifts data from the data input pin on to the falling edge of the LP signal.

1.6. Level Shifter

The logic voltage signal is level-shifted to the LCD driver voltage level, and output to the driver block.

1.7. 4-Level Driver

It drives the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V_0, V_{12}, V_{43}, V_5) based on the S/C, FR and $\overline{\text{DISPOFF}}$ signals.

1.8. Control Logic

It controls the operation of each block. In the case of the segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 160 bits of data are read in, and the chip is deselected.

In the case of the common mode, it controls the direction of the data shift.

2. LCD Driver Output Voltage Level

The relationship amongst the data bus signal, AC converted signal FR and LCD driver output voltage is as shown in the table below:

2.1. Segment Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y_1 - Y_{160})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

Here, $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, H: V_{DD} (+2.5 to +5.5V), L: V_{SS} (0V), X: Don't care

2.2. Common Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y_1 - Y_{160})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

Here, $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, H: V_{DD} (+2.5 to +5.5V), L: V_{SS} (0V), X: Don't care

Note: There are two kinds of power supply (logic level voltage, LCD driver voltage) for the LCD driver. Please supply regular voltage, which assigned by specification for each power pin.
That time "Don't care" should be fixed to "H" or "L", avoiding floating.

3. Relationship between the Display Data and Driver Output Pins

3.1. Segment Mode:

(a) 4-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					40clock	39clock	38clcok	~	3clock	2clock	1clock
L	L	Output	Input	D0	Y1	Y5	Y9	~	Y149	Y153	Y157
				D1	Y2	Y6	Y10	~	Y150	Y154	Y158
				D2	Y3	Y7	Y11	~	Y151	Y155	Y159
				D3	Y4	Y8	Y12	~	Y152	Y156	Y160
L	H	Input	Output	D0	Y160	Y156	Y152	~	Y12	Y8	Y4
				D1	Y159	Y155	Y151	~	Y11	Y7	Y3
				D2	Y158	Y154	Y150	~	Y10	Y6	Y2
				D3	Y157	Y153	Y149	~	Y9	Y5	Y1

(b) 8-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					20clock	19clock	18clcok	~	3clock	2clock	1clock
H	L	Output	Input	D0	Y1	Y9	Y17	~	Y137	Y145	Y153
				D1	Y2	Y10	Y18	~	Y138	Y146	Y154
				D2	Y3	Y11	Y19	~	Y139	Y147	Y155
				D3	Y4	Y12	Y20	~	Y140	Y148	Y156
				D4	Y5	Y13	Y21	~	Y141	Y149	Y157
				D5	Y6	Y14	Y22	~	Y142	Y150	Y158
				D6	Y7	Y15	Y23	~	Y143	Y151	Y159
				D7	Y8	Y16	Y24	~	Y144	Y152	Y160
H	H	Input	Output	D0	Y160	Y152	Y144	~	Y24	Y16	Y8
				D1	Y159	Y151	Y143	~	Y23	Y15	Y7
				D2	Y158	Y150	Y142	~	Y22	Y14	Y6
				D3	Y157	Y149	Y141	~	Y21	Y13	Y5
				D4	Y156	Y148	Y140	~	Y20	Y12	Y4
				D5	Y155	Y147	Y139	~	Y19	Y11	Y3
				D6	Y154	Y146	Y138	~	Y18	Y10	Y2
				D7	Y153	Y145	Y137	~	Y17	Y9	Y1

3.2. Common Mode

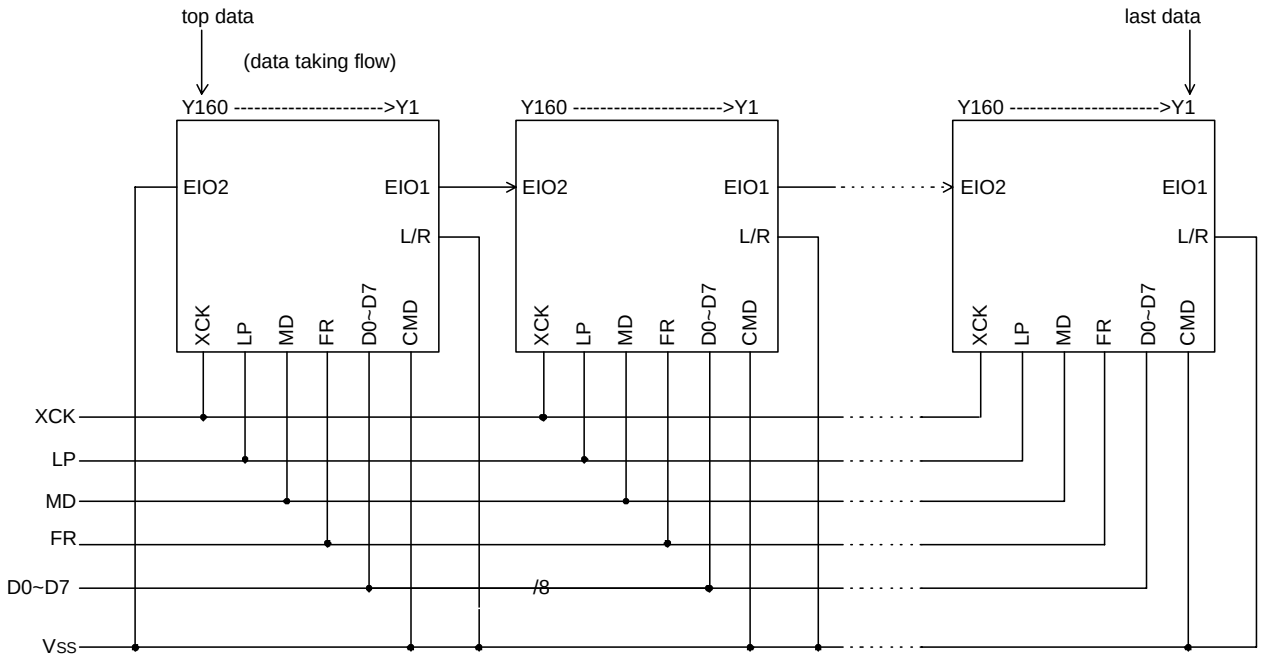
MD	CMD	L/R	Data Transfer Direction	Output pins			EIO1	EIO2	D7
				Y1~Y60	Y61~Y100	Y101~Y160			
L (Single)	L	L (shift to left)	Y160 to Y1	Output	Output	Output	Output	Input	X
		H (shift to right)	Y1 to Y160	Output	Output	Output	Input	Output	X
L (Single)	H	L (shift to left)	Y160 to Y101, Y60 to Y1	Output	NC	Output	Output	Input	X
		H (shift to right)	Y1 to Y60 , Y101 to Y160	Output	NC	Output	Input	Output	X
H (Dual)	X	L (shift to left)	Y160 to Y81 Y80 to Y1	Output	Output	Output	Output	Input	Input
		H (shift to right)	Y1 to Y80 Y81 to Y160	Output	Output	Output	Input	Output	Input

Here, L: V_{SS} (0V), H: V_{DD} (+2.5V to +5.5V), X: Don't care

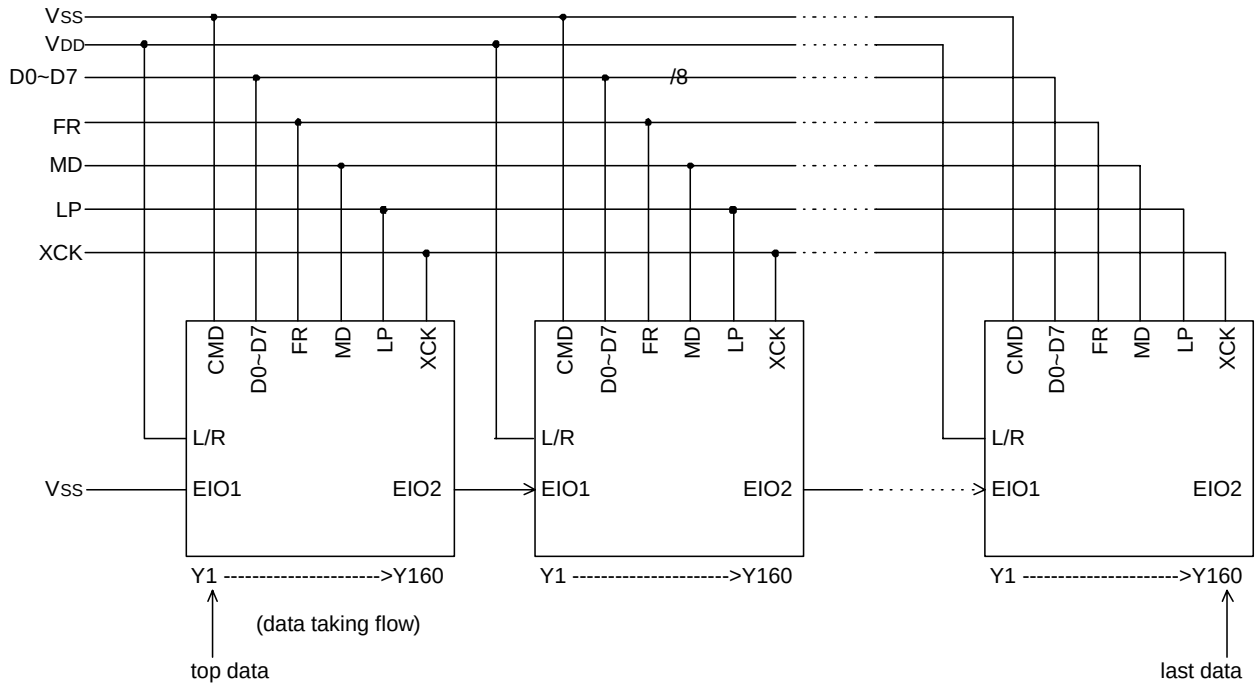
Note: "Don't care" should be fixed to "H" or "L", avoiding floating.

4. Connection Examples of Segment Drivers

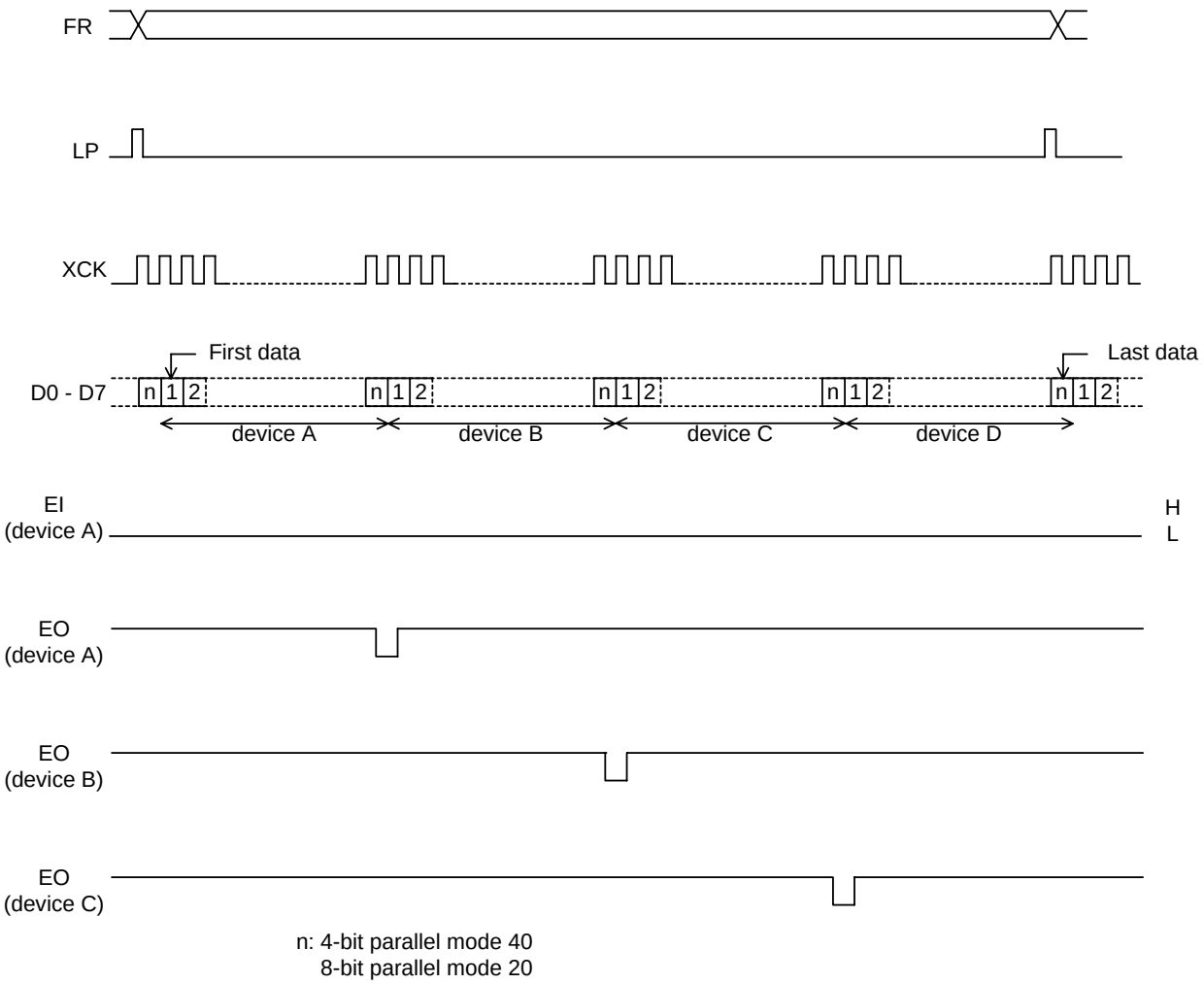
4.1. Case of L/R = "L"



4.2 Case of L/R = "H"

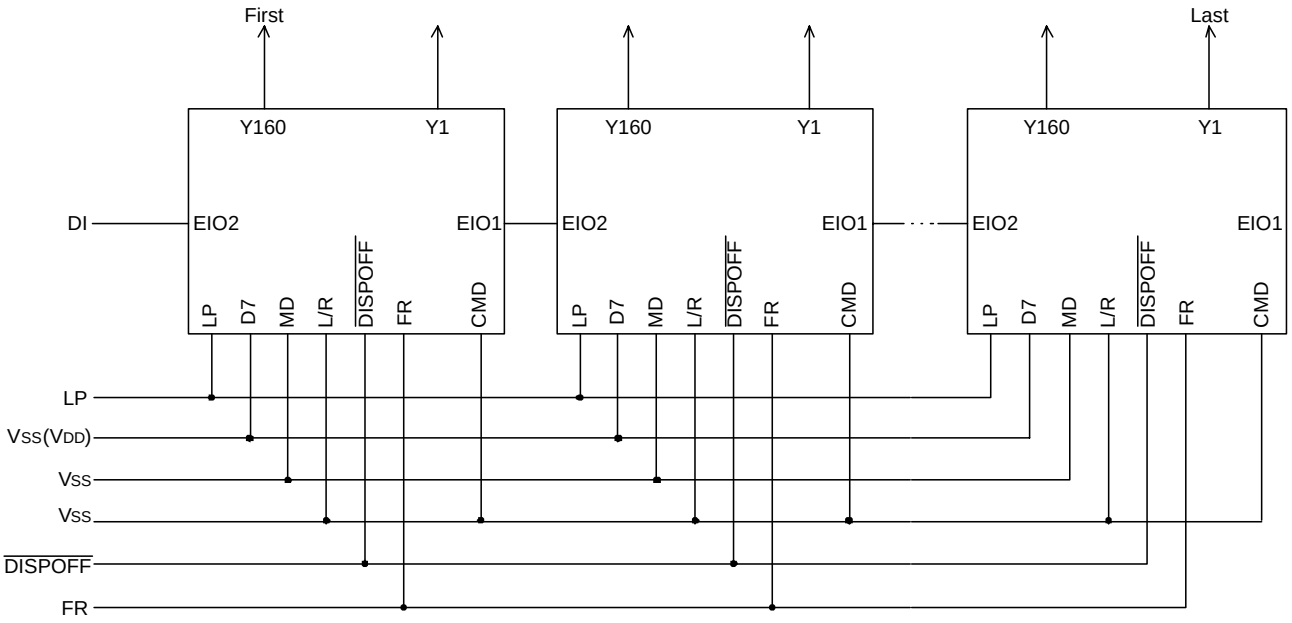


5. Timing Waveform of 4-Device Cascade Connection of Segment Drivers.

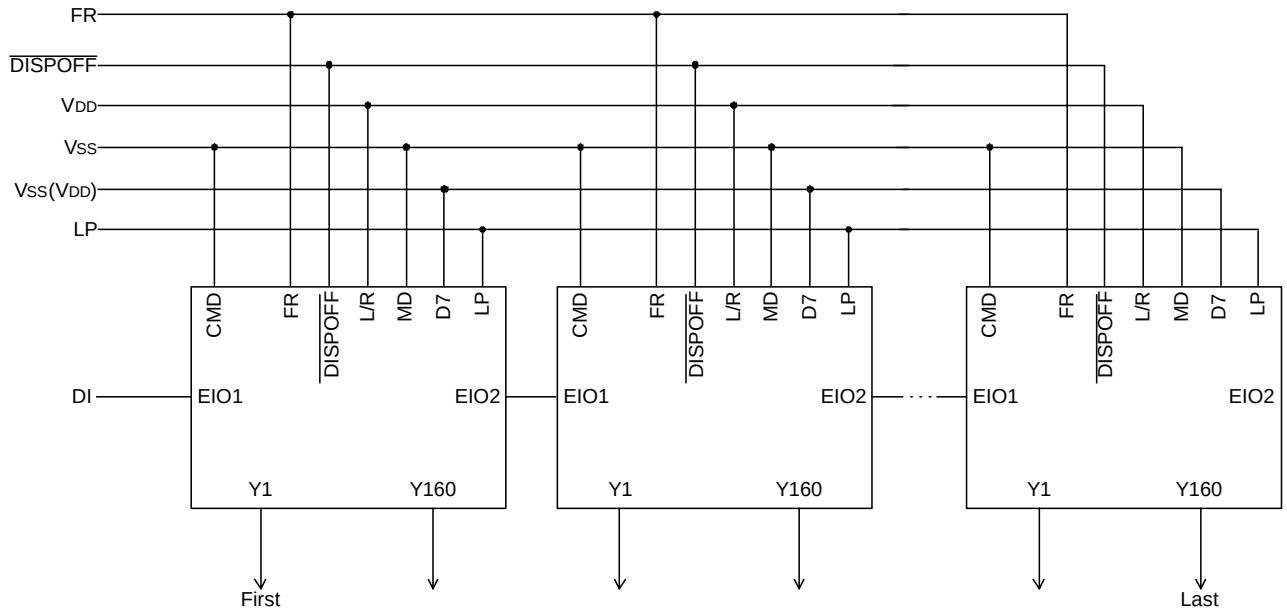


n: 4-bit parallel mode 40
8-bit parallel mode 20

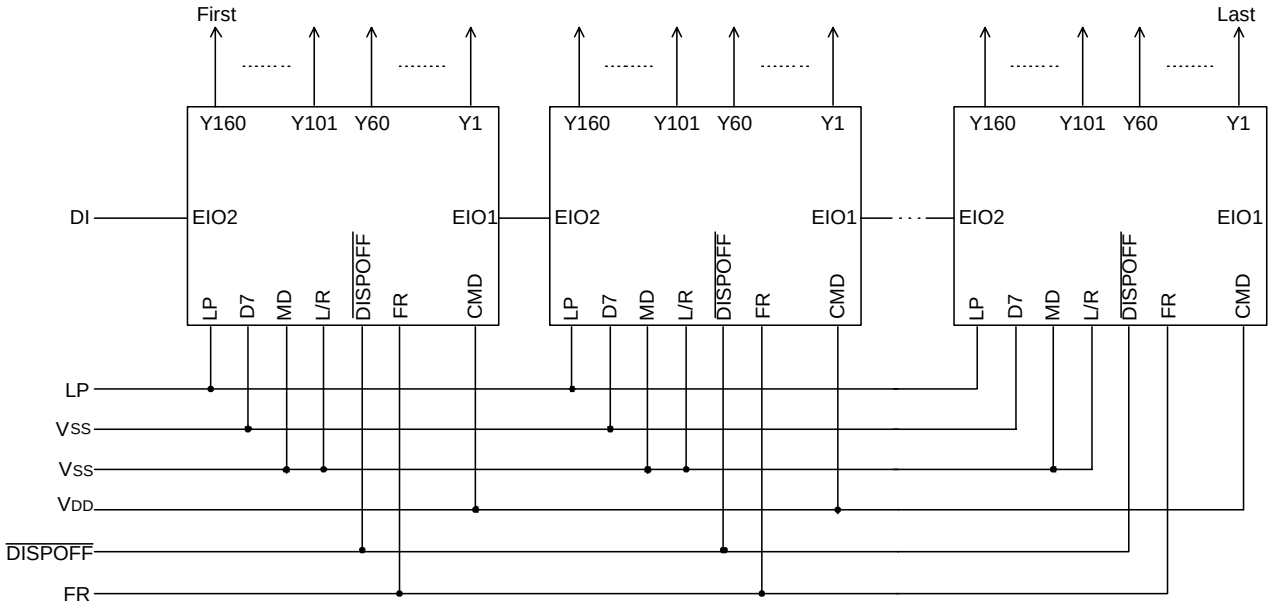
6. Connection Examples for Common Drivers



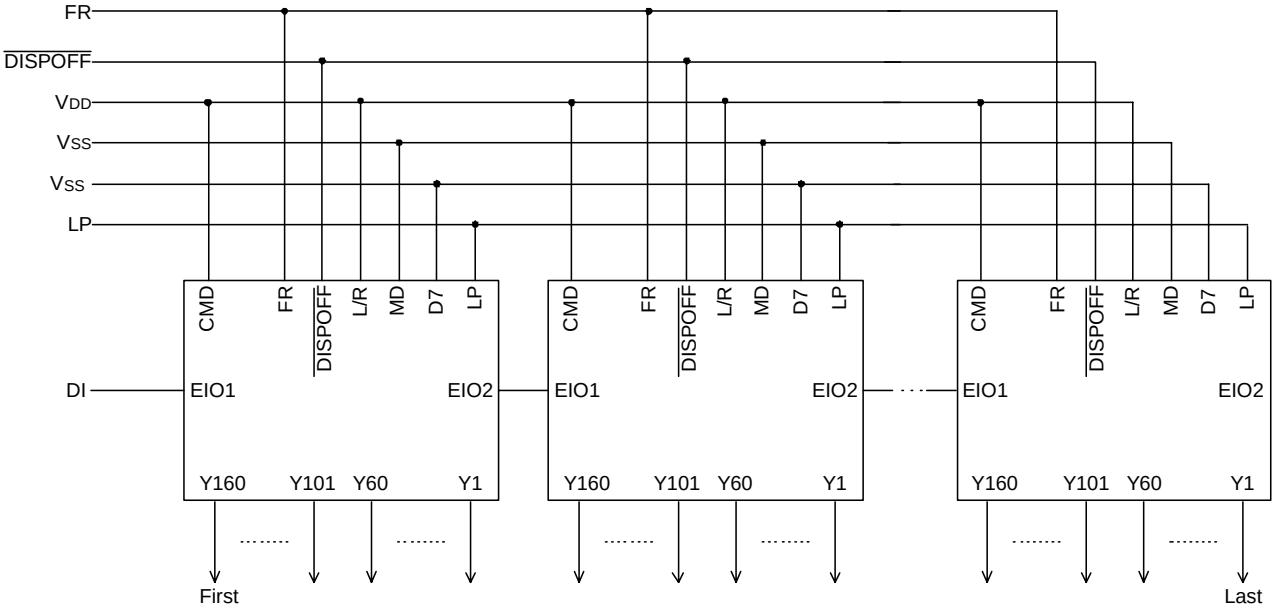
Single Mode (Shifting towards the left)



Single Mode (Sifting towards the right)



Dual Mode (Shifting towards the left)



Dual Mode (Sifting towards the right)

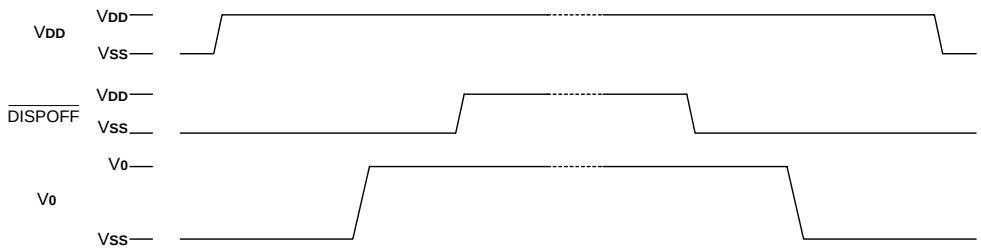
7. Precaution

Be careful when connecting or disconnecting the power

This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current, which may occur, if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating.
The details are as follows:

- When connecting the power supply, connect the LCD driver power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.
- We recommend that you connect a serial resistor (50-100Ω) or fuse to the LCD driver power V0 of the system as a current limiting device. Also, set a suitable value for the resistor in consideration of the LCD display grade.

In addition, when connecting the logic power supply, the logic condition of the LSI inside is insecure. Therefore connect the LCD driver power supply after resetting logic condition of this LSI inside on $\overline{\text{DISPOFF}}$ function. After that, the $\overline{\text{DISPOFF}}$ cancel the function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD driver output pins to level Vss on the $\overline{\text{DISPOFF}}$ function. After that, disconnect the logic system power after disconnecting the LCD driver power.
When connecting the power supply, follow the recommended sequence shown.



Absolute Maximum Rating*

DC Supply Voltage V_{DD} . . . . . -0.3V to +7.0V

DC Supply Voltage V_0 . . . . . -0.3V to +42.0V

Input Voltage . . . . . -0.3V to V_{DD} +0.3V

Operating Ambient Temperature . . . . -30°C to +85°C

Storage Temperature . . . . . .-45°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics

Segment Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 40 V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
Operating Voltage	V_{DD}	2.5	-	5.5	V		
Operating Voltage	V_0	15	-	40	V		
Input high voltage	V_{IH}	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, CMD and $\overline{DISPOFF}$ pins	
Input low voltage	V_{IL}	-	-	0.2 V_{DD}	V		
Output high voltage	V_{OH}	V_{DD} - 0.4	-	-	V	EIO_1, EIO_2 pins, I_{OH} = -0.4mA	
Output low voltage	V_{OL}	-	-	+0.4	V	EIO_1, EIO_2 pins, I_{OL} = +0.4mA	
Input leakage current 1	I_{IH}	-	-	+1	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2 and $\overline{DISPOFF}$ pins, V_I = V_{DD}	
Input leakage current 2	I_{IL}	-	-	-1	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2 and $\overline{DISPOFF}$ pins, V_I = V_{SS}	
Output resistance	R_{ON}	-	1.0	1.5	kΩ	V_0 = +40.0V	Y_1 - Y_{160} pins, $\lvert\Delta V_{ON}\rvert$ = 0.5V
		-	1.5	2.0		V_0 = +30.0V	
Stand-by current	I_{SB}	-	-	5	μA	V_{SS} pin, Note 1	
Consumed current (1) (Deselection)	I_{DD1}	-	-	2.0	mA	V_{DD} pin, Note 2	
Consumed current (2) (Selection)	I_{DD2}	-	-	8.0	mA	V_{DD} pin, Note 3	
Consumed current	I_0	-	-	1.0	mA	V_0 pin, Note 4	

Note:

1. V_{DD} = +5.0V, V_0 = +40V, V_I = V_{SS}
2. V_{DD} = +5.0V, V_0 = +40V, f_{XCK} = 14MHz, No-load, EI = V_{DD}
   The input data is turned over by the data taking clock (4-bit parallel input mode)
3. V_{DD} = +5.0V, V_0 = +40V, f_{XCK} = 14MHz, No-load. EI = V_{SS}
   The input data is turned over by the data taking clock (4-bit parallel input mode)
4. V_{DD} = +5.0V, V_0 = +40V, f_{XCK} = 14MHz, f_{LP} = 41.6kHz. f_{FR} = 80 Hz, No-load
   The input data is turned over by the data taking clock (4-bit parallel-input mode)

Common Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 40V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
Operating Voltage	V_{DD}	2.5	-	5.5	V		
Operating Voltage	V_0	15	-	40	V		
Input high voltage	V_{IH}	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, CMD and $\overline{DISPOFF}$ pins	
Input low voltage	V_{IL}	-	-	0.2 V_{DD}	V		
Output high voltage	V_{OH}	V_{DD} - 0.4	-	-	V	EIO_1, EIO_2 pins, I_{OH} = -0.4mA	
Output low voltage	V_{OL}	-	-	+0.4	V	EIO_1, EIO_2 pins, I_{OL} = +0.4mA	
Input leakage current 1	I_{IH}	-	-	+1.0	μA	D0 - 6, LP, L/R, FR, MD, S/C and $\overline{DISPOFF}$ pins, V_I = V_{DD}	
Input leakage current 2	I_{IL}	-	-	-1.0	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins, V_I = V_{SS}	
Output resistance	R_{ON}	-	1.0	1.5	kΩ	V_0 = +40.0V	Y_1 - Y_{160} pins, $\lvert\Delta V_{ON}\rvert$ = 0.5V
		-	1.5	2.0		V_0 = +30.0V	
Stand-by current	I_{SB}	-	-	5	μA	V_{SS} pin, Note 1	
Consumed current (1)	I_{DD}	-	-	80	μA	V_{DD} pin, Note 2	
Consumed current (2)	I_0	-	-	160	μA	V_0 pin, Note 2	

Note:

1. V_{DD} = +5.0V, V_0 = +40V, V_I = V_{SS}
2. V_{DD} = +5.0V, V_0 = +40V, f_{LP} = 41.6KHz, f_{FR} = 80Hz, case of 1/480 duty operation, No-load

AC Characteristics

Segment Mode 1 (V_{SS} = V_5 = 0V, V_{DD} = 4.5 - 5.5V, V_0 = 15 to 40, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	71	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	23	-		ns	
Shift clock "L" pulse width	t_{WCKL}	23	-		ns	
Data setup time	t_{DS}	10	-		ns	
Data hole time	t_{DH}	20	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	23	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	25	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	25	-		ns	
Latch pulse fall to Shift clock rise time	t_{LH}	25	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	21	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	40	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL = 15pF

Note

1. Take the cascade connection into consideration.
2. (T_{ck} - t_{WCKII} - t_{wckl})/2 is the maximum in the case of high speed operation.

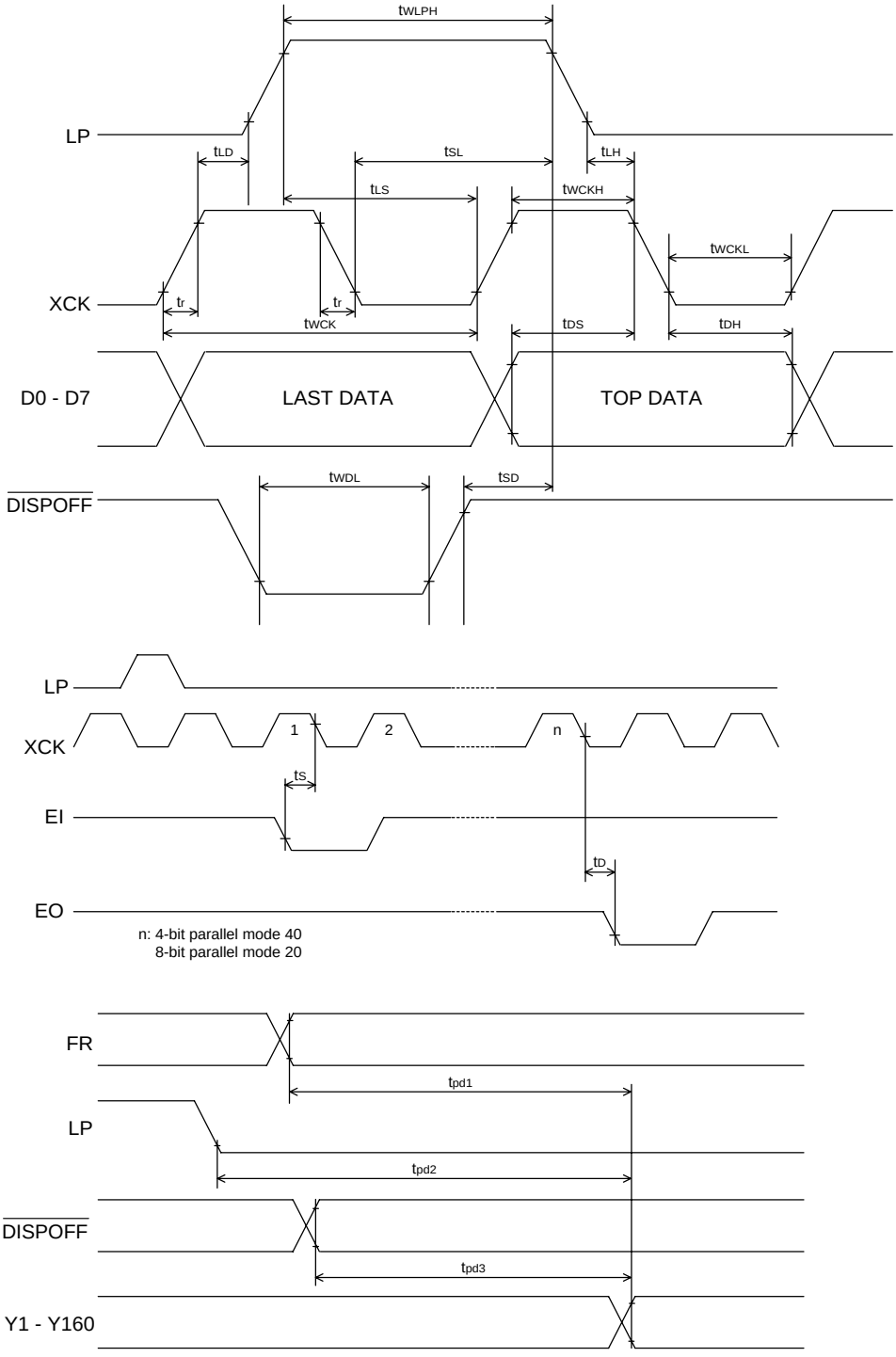
Segment Mode 2 (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 4.5V, V_0 = 15 to 40, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	125	-		ns	tr, tf ≦ 11ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	51	-		ns	
Shift clock "L" pulse width	t_{WCKL}	51	-		ns	
Data setup time	t_{DS}	30	-		ns	
Data hole time	t_{DH}	40	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	51	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	51	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	51	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	51	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	36	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	78	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL = 15pF

Note

1. Take the cascade connection into consideration.
2. (t_{CK} - t_{WCKII} - t_{WCKL})/2 is the maximum in the case of high speed operation.

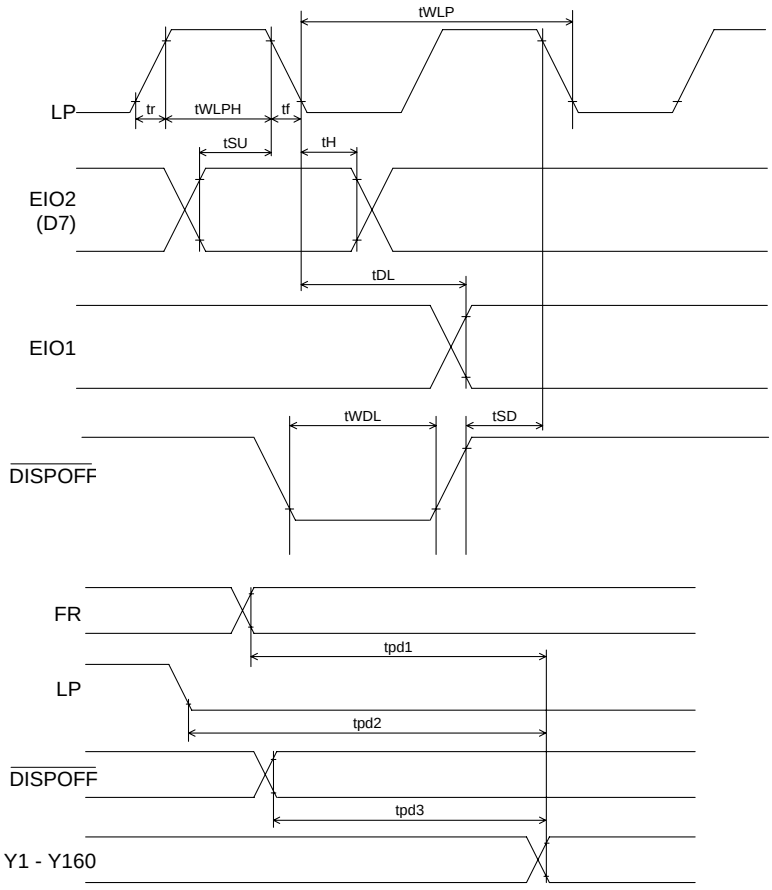
Timing waveform of the Segment Mode



Common Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 40V and T_A = -30 to +85°C, unless otherwise noted)

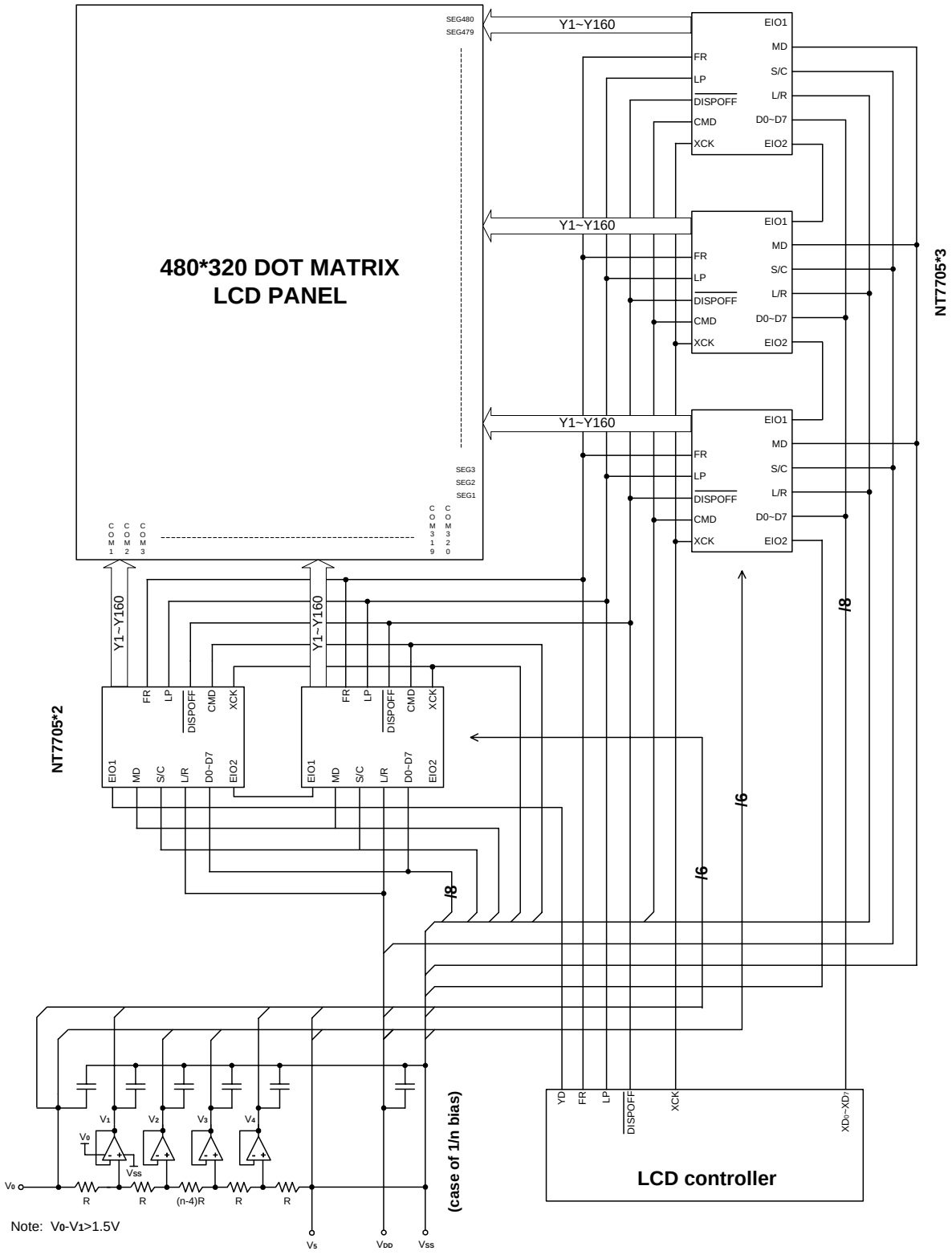
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WLP}	250	-	-	ns	t_r, t_f ≦ 20ns
Shift clock "H" pulse width	t_{WLPH}	15	-	-	ns	V_{DD} = +5.0V ± 10%
		30	-	-	ns	V_{DD} = +2.5 - +4.5V
Data setup time	t_{SU}	30	-	-	ns	
Data hole time	t_H	50	-	-	ns	
Input signal rise time	t_r		-	50	ns	
Input signal fall time	t_f		-	50	ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-	-	ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-	-	μs	
Output delay time (1)	t_{DL}	-	-	200	ns	C_L = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}	-	-	1.2	μs	C_L = 15pF
Output delay time (3)	t_{pd3}	-	-	1.2	μs	C_L = 15Pf

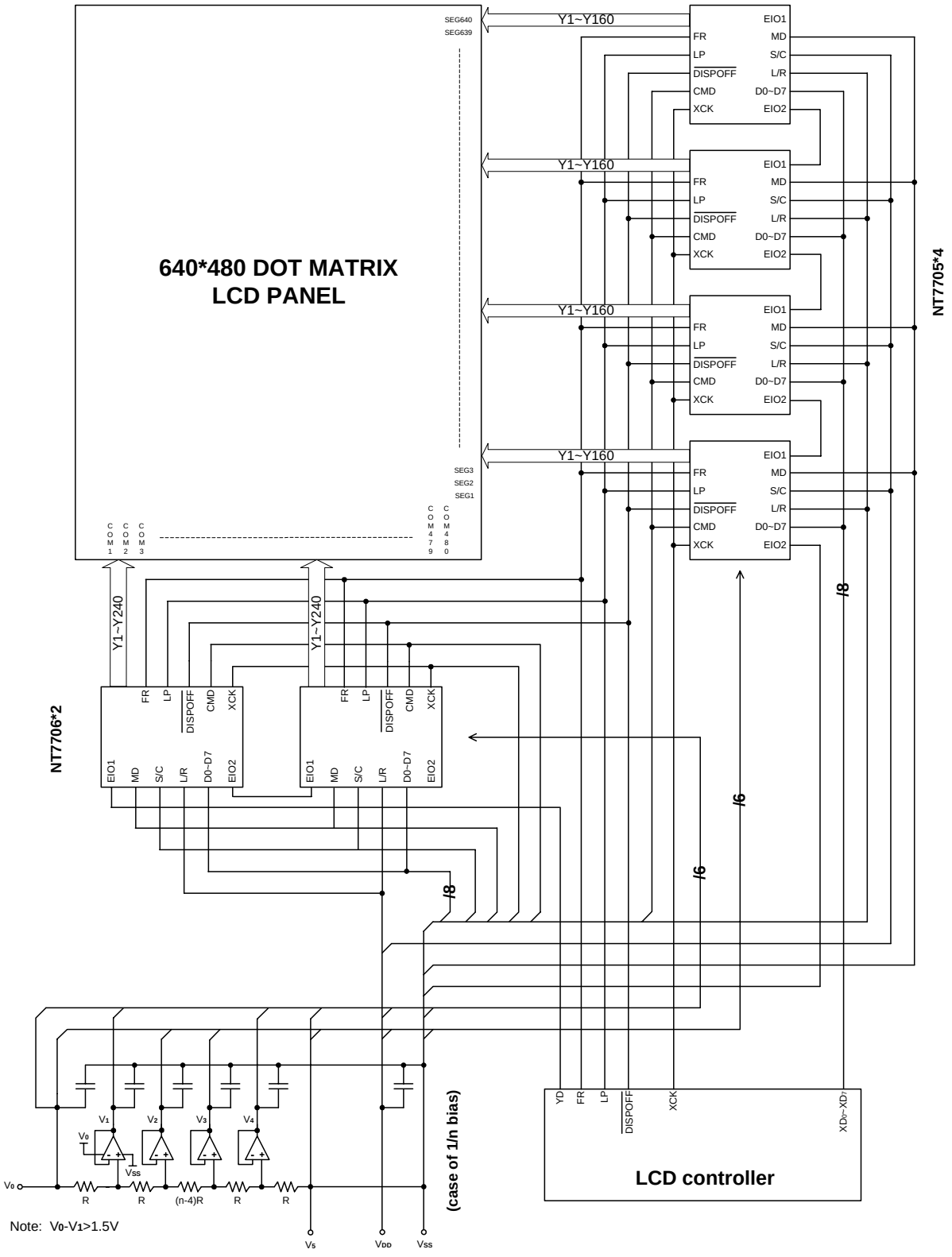
Timing Characteristics of Common Mode



L/R = "L"

Application Circuit (for reference only)




640*480 DOT MATRIX
LCD PANEL
SEG640
SEG639
SEG3
SEG2
SEG1
COM1
COM2
COM3
COM479
COM480
Y1~Y160
Y1~Y240
EIO1
FR
MD
LP
S/C
DISPOFF
L/R
CMD
D0~D7
XCK
EIO2
NT7705*4
NT7706*2
/8
/6
V0
V1
V2
V3
V4
VSS
R
(n-4)R
V5
VDD
(case of 1/n bias)
YD
XD0~XD7
LCD controller
Note: V0-V1>1.5V

Application and ITO Layout Notice(for reference only)

Application Notices

1. Adjust the voltage of V1and V4 you can amend the phenomena of ”cross talk” (V1& V4 range of adjusting is less than 100mV, Be sure V0-V1=V4-V_{SS} after adjusting;
2. When NT7705 is applied in COG type LCM, we recommend to use FPC of 0.5mm pitch
3. Add 0.1μf high frequency capacitors between V_{DD} & V0 ~ V4 and V_{SS};
4. When OP(LP324) is used as follow of bias voltage, be sure OP power voltage must be 1.5V (or more) higher than output voltage;
5. XCK,D0-D7,LP are high frequency (Max. 20MHZ) signals, pay attention to the distance between them and other signals nearby to avoid high frequency interference;
6. EIO1,EIO2 are enable signals for connecting chips, pay attention to the distance between them and other signals nearby to avoid interference. The distance of connection between two chips is as shorter as better.
7. CMD must be connected to V_{DD} or V_{SS}.

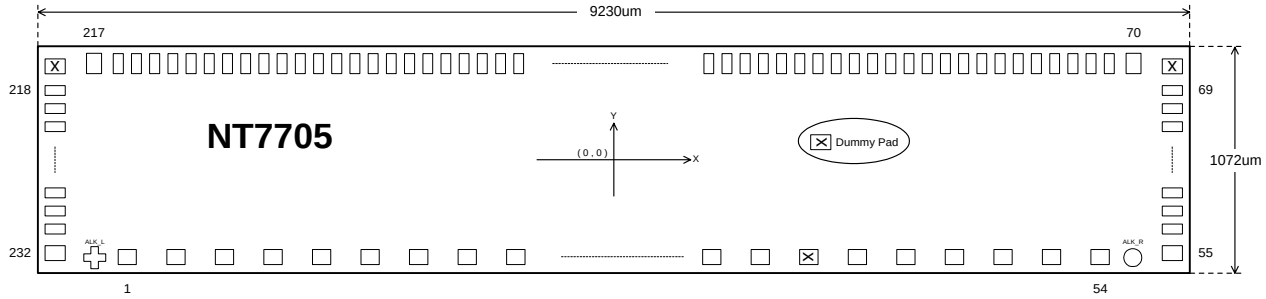
ITO Layout Notice（It is for application of COG type）

1. We suggest that LCD panel is made of glass whose ITO resistor is about 15 Ω / square , power ITO are better to be straight, its resistor value is as smaller as better.
2. Among interface Pins , first to be sure ITO resistors value of V_{DD},V_{SS},V0 ~ V4 are less than values we suggest. It is shown below:

Pin name	ITO resistors value
V_{SS} & V_{DD}	less than 75Ω(when V_{DD} < 2.7V) less than 130Ω (when V_{DD} ≥ 2.7V)
Other Power Pins (V0,V12,V43,V5 R/L)	less than 200Ω

3. Reference figure and characteristic of ITO Layout
   a). VDD/VSS of IC and VDD/VSS of FPC are almost at the same vertical level. ITO is very straight;
   b). Closer IC to FPC, shorter the length of ITO;

Bonding Diagram



Pad Location

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	V5L	-4320	-483	31	D5	480	-483
2	V5L	-4160	-483	32	D5	640	-483
3	VSS	-4000	-483	33	D6	800	-483
4	VSS	-3840	-483	34	D6	960	-483
5	VSS	-3680	-483	35	D7	1120	-483
6	VSS	-3520	-483	36	D7	1280	-483
7	CMD	-3360	-483	37	XCK	1440	-483
8	CMD	-3200	-483	38	XCK	1600	-483
9	L/R	-3040	-483	39	$\overline{\text{DISPOFF}}$	1760	-483
10	L/R	-2880	-483	40	$\overline{\text{DISPOFF}}$	1920	-483
11	VDD	-2720	-483	41	LP	2080	-483
12	VDD	-2560	-483	42	LP	2240	-483
13	VDD	-2400	-483	43	EIO1	2400	-483
14	VDD	-2240	-483	44	EIO1	2560	-483
15	VDD	-2080	-483	45	FR	2720	-483
16	VDD	-1920	-483	46	FR	2880	-483
17	S/C	-1760	-483	47	MD	3040	-483
18	S/C	-1600	-483	48	MD	3200	-483
19	EIO2	-1440	-483	49	VSS	3520	-483
20	EIO2	-1280	-483	50	VSS	3680	-483
21	D0	-1120	-483	51	VSS	3840	-483
22	D0	-960	-483	52	VSS	4000	-483
23	D1	-800	-483	53	V5R	4160	-483
24	D1	-640	-483	54	V5R	4320	-483
25	D2	-480	-483	55	V43R	4558	-470
26	D2	-320	-483	56	V43R	4558	-390
27	D3	-160	-483	57	V43R	4558	-330
28	D3	0	-483	58	V12R	4558	-270
29	D4	160	-483	59	V12R	4558	-210
30	D4	320	-483	60	V12R	4558	-150

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	V0R	4558	-90	101	Y38	2550	479
62	V0R	4558	-30	102	Y39	2490	479
63	V0R	4558	30	103	Y40	2430	479
64	Y1	4558	90	104	Y41	2370	479
65	Y2	4558	150	105	Y42	2310	479
66	Y3	4558	210	106	Y43	2250	479
67	Y4	4558	270	107	Y44	2190	479
68	Y5	4558	330	108	Y45	2130	479
69	Y6	4558	390	109	Y46	2070	479
70	Y7	4430	479	110	Y47	2010	479
71	Y8	4350	479	111	Y48	1950	479
72	Y9	4290	479	112	Y49	1890	479
73	Y10	4230	479	113	Y50	1830	479
74	Y11	4170	479	114	Y51	1770	479
75	Y12	4110	479	115	Y52	1710	479
76	Y13	4050	479	116	Y53	1650	479
77	Y14	3990	479	117	Y54	1590	479
78	Y15	3930	479	118	Y55	1530	479
79	Y16	3870	479	119	Y56	1470	479
80	Y17	3810	479	120	Y57	1410	479
81	Y18	3750	479	121	Y58	1350	479
82	Y19	3690	479	122	Y59	1290	479
83	Y20	3630	479	123	Y60	1230	479
84	Y21	3570	479	124	Y61	1170	479
85	Y22	3510	479	125	Y62	1110	479
86	Y23	3450	479	126	Y63	1050	479
87	Y24	3390	479	127	Y64	990	479
88	Y25	3330	479	128	Y65	930	479
89	Y26	3270	479	129	Y66	870	479
90	Y27	3210	479	130	Y67	810	479
91	Y28	3150	479	131	Y68	750	479
92	Y29	3090	479	132	Y69	690	479
93	Y30	3030	479	133	Y70	630	479
94	Y31	2970	479	134	Y71	570	479
95	Y32	2910	479	135	Y72	510	479
96	Y33	2850	479	136	Y73	450	479
97	Y34	2790	479	137	Y74	390	479
98	Y35	2730	479	139	Y75	330	479
99	Y36	2670	479	139	Y76	270	479
100	Y37	2610	479	140	Y77	210	479

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
141	Y78	150	479	181	Y118	-2250	479
142	Y79	90	479	182	Y119	-2310	479
143	Y80	30	479	183	Y120	-2370	479
144	Y81	-30	479	184	Y121	-2430	479
145	Y82	-90	479	185	Y122	-2490	479
146	Y83	-150	479	186	Y123	-2550	479
147	Y84	-210	479	187	Y124	-2610	479
148	Y85	-270	479	188	Y125	-2670	479
149	Y86	-330	479	189	Y126	-2730	479
150	Y87	-390	479	190	Y127	-2790	479
151	Y88	-450	479	191	Y128	-2850	479
152	Y89	-510	479	192	Y129	-2910	479
153	Y90	-570	479	193	Y130	-2970	479
154	Y91	-630	479	194	Y131	-3030	479
155	Y92	-690	479	195	Y132	-3090	479
156	Y93	-750	479	196	Y133	-3150	479
157	Y94	-810	479	197	Y134	-3210	479
158	Y95	-870	479	198	Y135	-3270	479
159	Y96	-930	479	199	Y136	-3330	479
160	Y97	-990	479	200	Y137	-3390	479
161	Y98	-1050	479	201	Y138	-3450	479
162	Y99	-1110	479	202	Y139	-3510	479
163	Y100	-1170	479	203	Y140	-3570	479
164	Y101	-1230	479	204	Y141	-3630	479
165	Y102	-1290	479	205	Y142	-3690	479
166	Y103	-1350	479	206	Y143	-3750	479
167	Y104	-1410	479	207	Y144	-3810	479
168	Y105	-1470	479	208	Y145	-3870	479
169	Y106	-1530	479	209	Y146	-3930	479
170	Y107	-1590	479	210	Y147	-3990	479
171	Y108	-1650	479	211	Y148	-4050	479
172	Y109	-1710	479	212	Y149	-4110	479
173	Y110	-1770	479	213	Y150	-4170	479
174	Y111	-1830	479	214	Y151	-4230	479
175	Y112	-1890	479	215	Y152	-4290	479
176	Y113	-1950	479	216	Y153	-4350	479
177	Y114	-2010	479	217	Y154	-4430	479
178	Y115	-2070	479	218	Y155	-4558	390
179	Y116	-2130	479	219	Y156	-4558	330
180	Y117	-2190	479	220	Y157	-4558	270

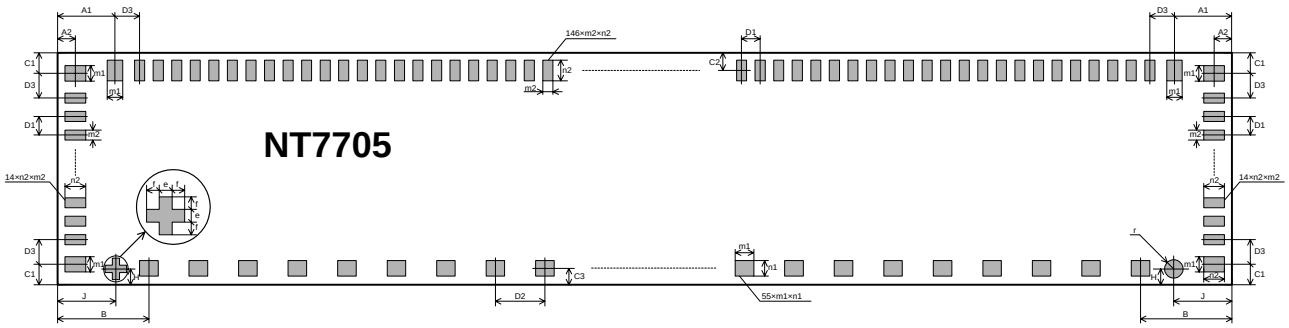
Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
221	Y158	-4558	210	228	V12L	-4558	-210
222	Y159	-4558	150	229	V12L	-4558	-270
223	Y160	-4558	90	230	V43L	-4558	-330
224	V0L	-4558	30	231	V43L	-4558	-390
225	V0L	-4558	-30	232	V43L	-4558	-470
226	V0L	-4558	-90		ALK_L	-4462	-485
227	V12L	-4558	-150		ALK_R	4462	-485

Dummy Pad Location (Total: 3 pad)

NO.	X	Y
1	3360	-483
2	4558	470
3	-4558	470

Package Information



Chip Outline Dimensions

unit: μm

Symbol	Dimensions in um	Symbol	Dimensions in um
A1	185	m1	58
A2	57	m2	38
B	295	n1	70
C1	66	n2	78
C2	57	r	35
C3	53	e	24
D1	60	f	23
D2	160	H	51
D3	80	J	153

Pad Dimensions

unit: μm

	Pad No.	Size	
		X	Y
Chip size	-	9230	1072
Pad pitch	1~54	160	
	56~69，71~216，218~231	60	
	55~56，70~71，216~217 231~232	80	
Bump size	1~54	58	70
	55，232	78	58
	56~69，218~231	78	38
	70，217	58	78
	71~216	38	78
Bump height	All pad	15±3	

Product Spec. Change Notice

NT7705 Specification Revision History		
Version	**Content**	**Date**
1.0	Formal version released	Apr. 2003
0.3	Operation Voltage V0 changed (30V to 40V) (Page 19, 20) Reference circuit modified (Page 26, 27)	Mar. 2002
0.2	Pad Location Addition	Jan. 2002
0.0	Original	Jun. 2001