NOVATEK
聯 詠 科 技

Data Sheet

NT39103

One-chip Driver IC with internal GRAM
for 262,144 colors 132 RGB x 162 dot TFT LCD

Version 0.0.8
2007/01/04

ABBREVIATIONS AND VOCABULARY

↑	Rising edge active
/CSX	Chip Select, active low
AM	Active Matrix
AGND	Analog ground
ASIC	Application Specific Integrated Circuit
AV	Audio-Visual Entities
AVDD	Source driver supply voltage (Driver internal analog supply voltage)
B/W	Black & White
COG	Chip On Glass
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
D/CX	Display Data/Command data select, Command data is active low
DE	Date Enable
DGND	Digital (Logic) ground
DIN	Data In, display side
DOUT	Data Out, display side
E	Read and Write Function in 6800 MCU I/F
EMR	Electro Magnetic Resonance
EMC	Electro Magnetic Compatibility
fps	Frame per second
FPWB	Flexible Printed Wiring Board
Hi-Z	High Impedance
HS	Horizontal Synchronization
H/W	Hardware
I/O	Input/Output pin
IC	Integrated Circuit
IBIS	Input/Output Buffer Information Specification
IDD	Analog power supply current
IDDI	Digital power supply current
I/F	Interface
Idle	8-colour mode
ISO	International Organization for Standardization
LC	Liquid Crystal
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LUT	Look Up table
MCU	Micro Controller Unit
MSB	Most Significant Bit
N/A	Not Applicable
PCLK	Pixel Clock
ppi	pixels per inch
pps	points per second
PT	Product Technologies
PWB(PCB)	Printed Wiring Board (Printed Circuit Board)
PWM	Pulse Width Modulation
RAM	Random Access Memory
RDX	Read function in 8080 MCU I/F, the display start to control data bus lines when there is a falling edge of the RDX and the host reads data bus lines when there is a rising edge of the RDX
RESX	Reset H/W Control pin, active Low
RGB	Red, Green, Blue
RH	Relative Humidity
RT	Room Temperature
S/W	Software
SoC	Statement of Conformance
Ta	Ambient Temperature
TBD	To Be Defined
TP	Technology Platforms
TR	Transflective LC type
TRC	Tone Rendering Curve (Gamma)
TM	Transmissive LC type

VCC	Digital power supply voltage (for Driver internal digital power supply)
VCOMAC	Command Amplitude voltage
VCOMH	Command High level voltage
VCOML	Command Low level voltage
VCI1	Booster input voltage (regulator from VDD)
VCL	VCOML supply voltage
VDD	Analog (Booster) power supply voltage
VDDI	Logic (I/O) power supply voltage
VS	Vertical Synchronization
VSS	System Ground
WRX	Write function in 8080 MCU I/F, the host start to control data bus lines when there is a falling edge of the WRX and the display reads data bus lines when there is a rising edge of the WRX

INDEX

Revision History

NT39103 Specification Revision History		
Version	**Content**	**Date**
0.0.0	Original	2006/10/17
0.0.1	Modified WRX description. (Page.16)	2006/10/19
0.0.2	Modified Power Consumption. (Page.23)	2006/10/26
	Added Maximum Series Resistance. (Page.25)	
	Modified Bump Location and Dimension. (Page.249)	
	Modified Pad Coordinate. (Page.250)	
0.0.3	Modified FRMCTR1~FRMCTR3. (Page.186~191)	2006/11/01
	Modified Bump Location and Dimension. (Page.249)	
0.0.4	Modified MTP Access Sequence. (Page.220)	2006/11/02
	Modified NVFCTR1(D9h). (Page.218)	
0.0.5	Modified External Components Connection. (Page.230)	2006/11/09
	Modified Deviation value of VCI1. (Page.199)	
0.0.6	Modified MTP Access Sequence. (Page.220)	2006/11/10
0.0.7	Modified Pin.110~114 Name. (Page.250)	2006/12/22
0.0.8	Modified Gamma Setting for MVA-Type. (Page.234)	2007/01/04
	Modified PWCTR1(C0h).(Page.199)	

1. Introduction

The NT39103 is one chip solution for TFT-LCD panel: source driver with built-in memory, gate driver, power IC are integrated on one chip. This IC can display to a maximum of 132-RGB x 162 -dot graphics on 262k-color TFT panel.

The NT39103 supports 18-/16-/9-/8-bit high-speed bus interface and serial peripheral interfaces (SPI). It also supplies 18-bit, 16-bit or 6-bit RGB interface for driving Video signal directly from controller. The moving picture area can be specified in internal GRAM by window function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

The NT39103 has various functions for reducing the power consumption of a LCD system: operating at low voltage (minimum 1.6V), register-controlled power-save mode, partial display mode and so on. The IC has internal GRAM to store 132-RGB x 162-dot 262k-color image and internal booster that generates the LCD driving voltage, breeder resistance and the voltage follower circuit for LCD driver.

This LSI is suitable for any medium-sized or small portable mobile solution requiring long-term driving capabilities, such as digital cellular phones supporting a web browser, bi-directional pagers, and small PDA.

2. Feature

◆ Chip size: 13.5mm * 0.7mm
◆ Single chip AM-TFT-LCD Controller/ driver with Display RAM.
◆ Display resolution: 132RGB (H) *162(V)
◆ Display data RAM (frame memory): 132 x 162 x 18-bits = 384912 bits
◆ Operation Frequency: ~10MHz
◆ Output:
- 396ch source outputs (132RGB)
- 162ch Gate outputs
- Common electrode output

◆ Display mode (Color mode)
- Full color mode (Idle mode off): 262K-colors
- Reduce color mode (Idle mode on): 8-colors (3-bits binary mode)

◆ Display resolution option
- 128 x 160 Display with 128 x 18-bits x 160 display RAM (when GM1, GM0 = ”00”)
- 120 x 160 Display with 120 x 18-bits x 160 display RAM (when GM1, GM0 = ”01”)
- 128 x 128 Display with 128 x 18-bits x 128 display RAM (when GM1, GM0 = ”10”)
- 132 x 162 Display with 132 x 18-bits x 162 display RAM (when GM1, GM0 = ”11”)

◆ Different LC type option
- Transflective LC type (When LCM1-0 = “00”)
- Transmission LC type (When LCM1-0 = “01”)
- Low Voltage LC type (When LCM1-0 = “10”)
- MVA LC type (When LCM1-0 = “11”)

◆ Interface mode (Color modes on the display host interface):
- 12-bits/Pixel: RGB= (444) using the 384k-bits frame memory and LUT.
- 16-bits/Pixel: RGB= (565) using the 384k-bits frame memory and LUT.
- 18-bits/Pixel: RGB= (666) using the 384k-bits frame memory and LUT.

◆ MCU Interface:
- 3-pin/4-pin serial interface
- 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-series MCU
- 8-bits, 9-bits, 16-bits, 18-bits interface with 6800-series MCU
- 12-bits, 16-bits, 18-bits RGB interface with graphic controller

◆ Display features
- Area scrolling
- Partial display mode
- Software programmable color depth mode

◆ On chip
- DC/DC converter
- Adjusted VCOM generation
- NV Memory to store initialization register setting
- Oscillator for display clock generation
- Timing generation
- 8 preset gamma curve selectable
- Factory default value (Contrast, Module ID, Module version, etc) are stored on the display module
- Line inversion, frame inversion

◆ NV Memory
- 7-bits for ID2
- 8-bits for ID3
- 7-bits for VCOM adjustment

◆ Supply voltage range
- Analog supply voltage range for VDD to AGND: 2.6V ~ 3.3V
- I/O supply voltage range for VDDI to DGND: 1.6V ~ 3.3V
- Internal Digital supply voltage range for VCC to DGND: **1.5V ~ 2.0V**

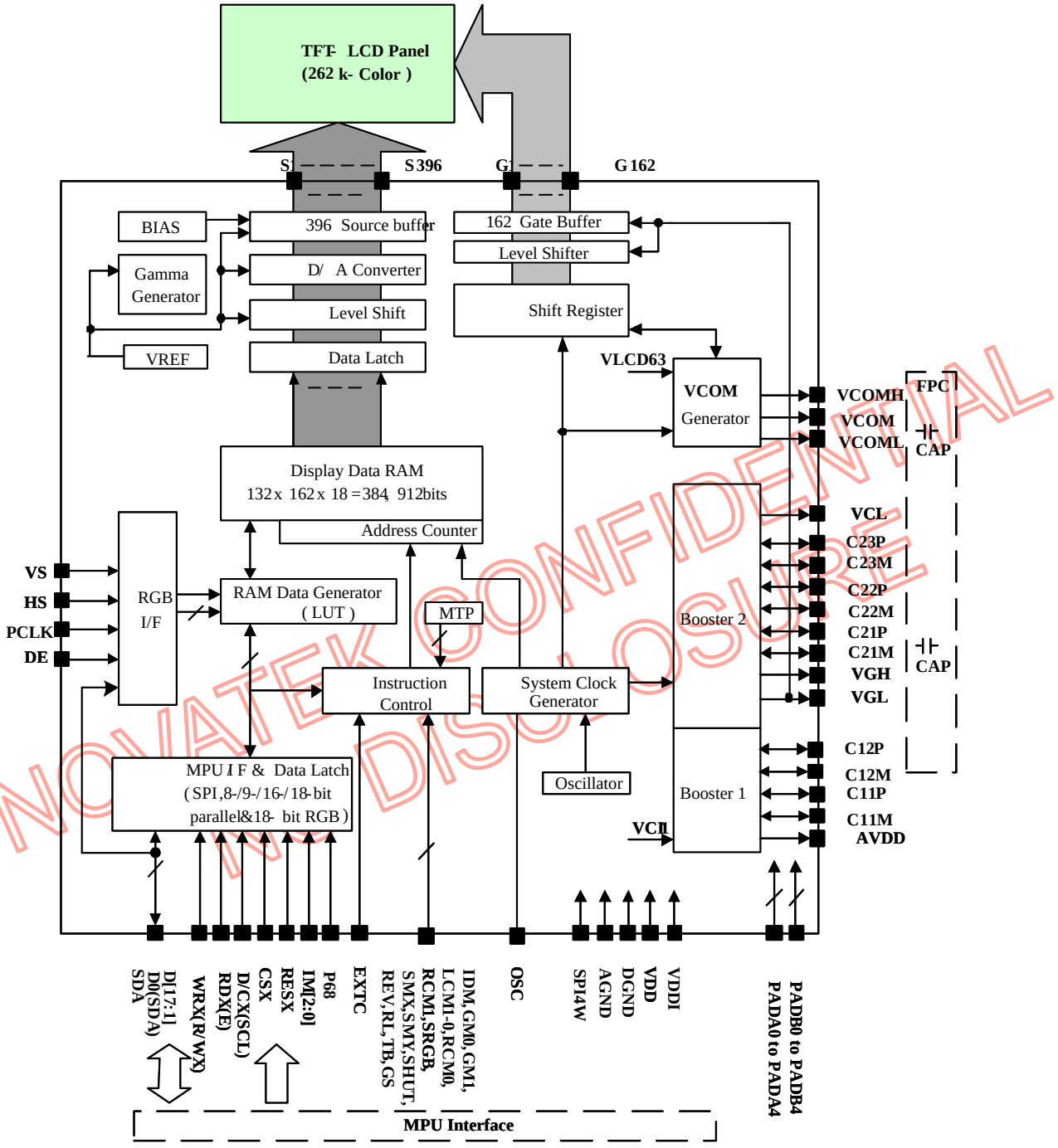
◆ Output voltage levels
- Source output voltage range for GVDD to AGND: 3.0V to 5.0V
- Power supply for driver circuit range for AVDD to AGND: 4.95V (VDD=VCI1=2.6V) to **5.5V**
- Common electrode output High voltage range for VCOMH to AGND: 2.5V to 5.0V
- Common electrode output Low voltage range for VCOML to AGND: -2.5V to 0.0V
- Positive Gate output voltage range for VGH to AGND: +10.0V to +16V
- Negative Gate output voltage range for VGL to AGND: –16V to –9.0V

◆ Lower power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Optimized layout for COG assembly
- Operate Temperature range: -40℃ to +85℃

Note 1: Blank display means: Normal White display = White display, Normal Black display = Black display

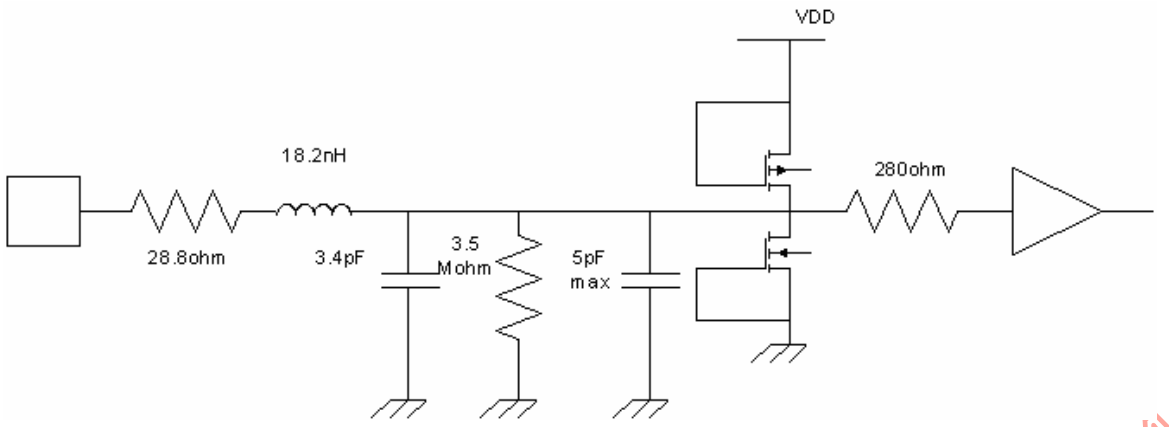
Note 2. The display interface does not support any noise recovery, external temperature or light sensing circuit. It needs a copy and detailed explanation of the implementation.

3. Display Module Block Diagram (for example)

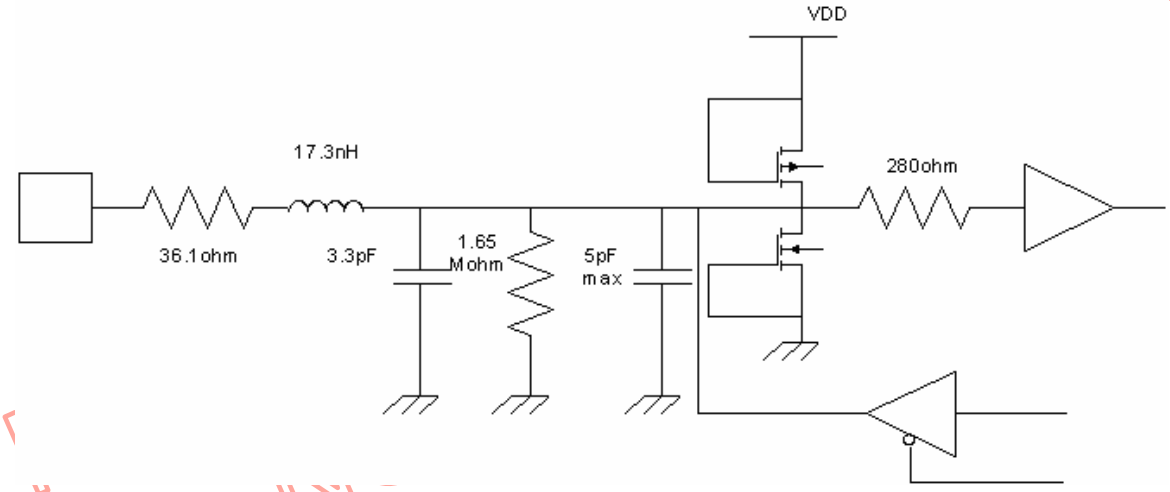


4. Display Module Pin Configuration (This is an example)

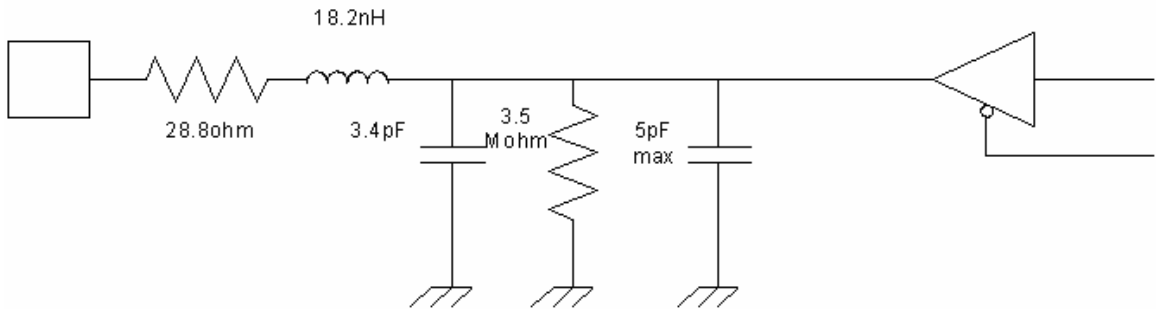
CSX, RESX, P68, D/CX _SCL, WRX,



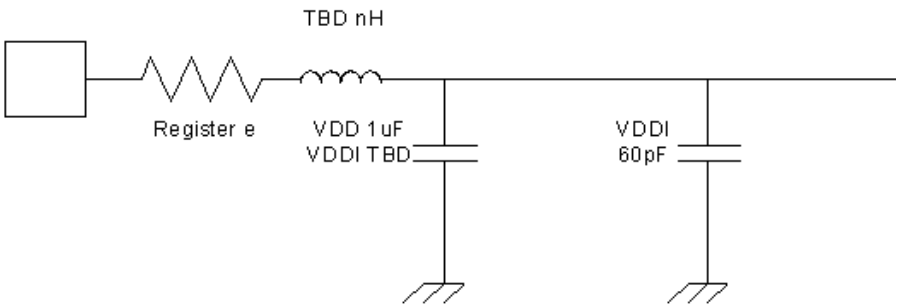
D7, D6, D6, D4, D3, D2, D1, D0_SDA



TE



VDDI, VDD



5. Driver IC Pin Description

The Abbreviation and vocabulary of pins need be fix at the further.

5.1 Power Supply Pins

Table 5.1.1: Power Supply Pins

Symbol	Name	Description
VDD	Analog voltage	Power supply for analog system and booster system
VDDI	Logic voltage	Power supply for I/O system
AGND	Analog GND	System ground for Analog and Booster system
DGND	Logic GND	System Ground for I/O system and internal digital system

5.2 Interface Logic pins

Table 5.2.1: Interface Logic Pins

Symbol	I/O	Description
P68	I	8080 /6800 MCU Interface mode select. If not used, please fix this pin at VDDI or DGND level. -P68='1', select 6800-MCU parallel interface -P68='0', select 8080-MCU parallel interface
IM2	I	MCU Parallel interface bus and Serial interface select -IM2='1', Parallel interface -IM2='0', Serial interface
IM1, IM0	I	-MCU Parallel interface type selection IM1 / IM0 / Parallel interface 0 / 0 / MCU 8-bit Parallel 0 / 1 / MCU 16-bit Parallel 1 / 0 / MCU 9-bit Parallel 1 / 1 / MCU 18-bit Parallel
SPI4W	I	-SPI4W='0', 3-wire SPI. (default) -SPI4W='1', 4-wire SPI. There is a pull-low resistor in the pin.
RESX	I	-This signal low, will reset the device and must be applied to properly initialize the chip. Signal is active
CSX	I	-Chip select input pin ("Low" enable). -This pin can be permanently fixed "Low" in MCU interface mode only.
D/CX (SCL)	I	-Display data / Command selection pin in parallel and SCL in 3-pin Serial I/F. -D/CX='1': Display data. D/CX='0': Command data. -If not used, please connect to ground or VDDI this pin interface
RDX (E)	I	-Read enable in 8080-parallel interface. -Read/ Write operation enable pin in 6800-parallel interface. -If not used, please connect to ground or VDDI this pin
WRX (R/WX)(D/CX)	I	-Write enable in parallel interface -If not used, please connect to ground or VDDI this pin -WRX-for 8080 MCU -R/WX-for 6800 MCU -D/CX-for 4-wire SPI
D[17:0]	I/O	-When RCM='1'(RGB I/F), D[17:0] are used to RGB interface data bus -when RCM='0' (MCU I/F), D[17:0] are used to MCU parallel interface data bus D0 is the Serial input/ output signal in serial I/F mode. -In serial interface, D[17:1] are not used and should be connected to ground or VDDI.
TE	O	-Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. -If not used, please open this pin.
SDA	I/O	-When RCM1, RCM0='1X' (RGB I/F), Serial input/output signal in serial I/F mode. The data is input on the rising edge of the SCL signal. The data is output on the falling edge of the SCL signal. -When RCM1, RCM1='0X' (MCU I/F), This pin is not used, and fix at VDDI or DGND level. -If not used, please fix this pin at VDDI or DGND level.
PCLK	I	-Pixel clock signal in RGB I/F mode. -If not used, please fix this pin at VDDI or DGND level.
VS	I	-Vertical sync. Signal in RGB I/F mode. -If not used, please fix this pin at VDDI or DGND level.

HS	I	-Horizontal sync. Signal in RGB I/F mode. -If not used, please fix this pin at VDDI or DGND level.
DE	I	-Data enable signal in RGB I/F mode. -If not used, please fix this pin at VDDI or DGND level.
OSC	O	-Oscillator output or test purpose

Note1. If CSX is connected to ground in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

Note2. When in 8 line parallel mode (IM1, IM0="0"") then id some data or signal appears on D[15:8] then it will have no influence to the system. (D[15:8] can be connected to '1' or '0')

Note3. When CSX='1', there is no influence to the parallel and serial interface.

Note4. '1' = VDDI level, '0' = DGND level.

5.3 Mode Selection pins

Table 5.3.1: Mode Selection Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>EXTC</td><td>I</td><td>-To use extended command set (like EEPROM program), please connect this pin to VDDI. During normal operation, please open this pin. (It has an internal pull low resistor.)
-EXTC='1', use extended command table (command value can be modify by external command table)
-EXTC='0', only use default command value</td></tr>
<tr><td>IDM</td><td>I</td><td>-Normal mode and Idle mode control pin
-Please refer RGB I/F for detail using.
<table>
<tr><th>IDM</th><th>Idle mode H/W controller</th></tr>
<tr><td>0</td><td>Normal display (can be changed to Idle mode by S/W)</td></tr>
<tr><td>1</td><td>Into Idle mode</td></tr>
</table></td></tr>
<tr><td>GM1, GM0</td><td>I</td><td>-Panel resolution selection pins.
<table>
<tr><th>GM1</th><th>GM0</th><th>Resolution selection</th></tr>
<tr><td>0</td><td>0</td><td>128RGB x 160(S7~S390 and G2~G161 output)</td></tr>
<tr><td>0</td><td>1</td><td>120RGB x 160(S7~S366 and G2~G161 output)</td></tr>
<tr><td>1</td><td>0</td><td>128RGB x 128(S7~S390 and G2~G129 output)</td></tr>
<tr><td>1</td><td>1</td><td>132RGB x 162(S1~S396 and G1~G162 output)</td></tr>
</table></td></tr>
<tr><td>RCM1, RCM0</td><td>I</td><td>- RGB and MCU interface mode selection pin.
<table>
<tr><th>RCM1</th><th>RCM0</th><th>Resolution selection</th></tr>
<tr><td>0</td><td>0</td><td>MCU interface mode</td></tr>
<tr><td>0</td><td>1</td><td>MCU interface mode</td></tr>
<tr><td>1</td><td>0</td><td>RGB Interface (1)</td></tr>
<tr><td>1</td><td>1</td><td>RGB Interface (2)</td></tr>
</table></td></tr>
<tr><td>SRGB</td><td>I</td><td>-RGB direction select H/W pin for Color filter default setting.
<table>
<tr><th>SRGB</th><th>RGB filter order for Color filter default setting</th></tr>
<tr><td>0</td><td>S1, S2, S3 filter order = 'R', 'G', 'B'</td></tr>
<tr><td>1</td><td>S1, S2, S3 filter order = 'B', 'G', 'R'</td></tr>
</table>-Please refer chapter 13 for detail using</td></tr>
<tr><td>SMX</td><td>I</td><td>-Module source output direction H/W select pin
<table>
<tr><th rowspan="2">SMX</th><th colspan="4">Module source output direction</th></tr>
<tr><th>GM='00'</th><th>GM= '01'</th><th>GM='10'</th><th>GM='11'</th></tr>
<tr><td>0</td><td>S7 -> S390</td><td>S7 -> S366</td><td>S7 -> S390</td><td>S1 -> S396</td></tr>
<tr><td>1</td><td>S390 -> S7</td><td>S366 -> S7</td><td>S390 -> S7</td><td>S396 -> S1</td></tr>
</table>-Please refer chapter 13 for detail using
-Please refer RL pin setting in RGB I/F Mode 2.</td></tr>
<tr><td>SMY</td><td>I</td><td>-Module Gate output direction H/W select pin
<table>
<tr><th rowspan="2">SMY</th><th colspan="3">Module Gate output direction</th></tr>
<tr><th>GM='00', '01'</th><th>GM='10'</th><th>GM='11'</th></tr>
<tr><td>0</td><td>G2 -> G161</td><td>G2 -> G129</td><td>G1 -> G162</td></tr>
<tr><td>1</td><td>G161 -> G2</td><td>G129 -> G2</td><td>G162 -> G1</td></tr>
</table>-Please refer chapter 13 for detail using
-Please refer TB pin setting in RGB I/F Mode 2.</td></tr>
</table>

<table>
<tr><td>SHUT</td><td>I</td><td>-Display On/ Off H/W control pin In RGB I/F
<table>
<tr><th>SHUT</th><th>Display On/Off in RGB I/F</th></tr>
<tr><td>0</td><td>Display On</td></tr>
<tr><td>1</td><td>Display Off</td></tr>
</table>
-Please refer RGB I/F for detail using.</td></tr>
<tr><td>REV</td><td>I</td><td>-Source output data polarity select H/W pin.
<table>
<tr><th>REV</th><th>Source output data polarity</th></tr>
<tr><td>0</td><td>Data not reverse</td></tr>
<tr><td>1</td><td>Data reverse</td></tr>
</table>
-Please refer RGB I/F for detail using.</td></tr>
<tr><td>LCM1-0</td><td>I</td><td>-Different Liquid Crystal (LC) type selection pins.
-There is a pull-low resistor only in LCM1 pin.
<table>
<tr><th>LCM1</th><th>LCM0</th><th>LC type selection</th></tr>
<tr><td>0</td><td>0</td><td>TR (Transflective) LC type</td></tr>
<tr><td>0</td><td>1</td><td>TM (Transmission) LC type</td></tr>
<tr><td>1</td><td>0</td><td>Low Voltage LC type</td></tr>
<tr><td>1</td><td>1</td><td>MVA LC type</td></tr>
</table></td></tr>
<tr><td>GS</td><td>I</td><td>Input pin to select the gamma curve order.
- Connect to VDDI for GC0(2.2), GC1(1.8), GC2(2.5), and GC3(1.0).
- Connect to DGND for GC0(1.0), GC1(2.5), GC2(2.2), and GC3(1.8).</td></tr>
<tr><td>TESEL</td><td>I</td><td>Input pin to select horizontal line number in TE signal.
- There is a pull-high resistor only in the pin.
- Connect to VDDI for 160 lines in TE signal.
- Connect to DGND for 162 lines in TE signal.</td></tr>
<tr><td>RL</td><td>I</td><td>-Source output direction H/W select pin in RGB I/F Mode 2.
When SMX=0
<table>
<tr><th rowspan="2">RL</th><th colspan="4">Module source output direction</th></tr>
<tr><th>GM=‘00’</th><th>GM= ‘01’</th><th>GM=’10’</th><th>GM=’11’</th></tr>
<tr><td>0</td><td>S7 -> S390</td><td>S7 -> S366</td><td>S7 -> S390</td><td>S1 -> S396</td></tr>
<tr><td>1</td><td>S390 -> S7</td><td>S366 -> S7</td><td>S390 -> S7</td><td>S396 -> S1</td></tr>
</table>
When SMX=1
<table>
<tr><th rowspan="2">RL</th><th colspan="4">Module source output direction</th></tr>
<tr><th>GM=’00’</th><th>GM= ‘01’</th><th>GM=’10’</th><th>GM=’11’</th></tr>
<tr><td>0</td><td>S390 -> S7</td><td>S366 -> S7</td><td>S390 -> S7</td><td>S396 -> S1</td></tr>
<tr><td>1</td><td>S7 -> S390</td><td>S7 -> S366</td><td>S7 -> S390</td><td>S1 -> S396</td></tr>
</table>
-Please refer RGB I/F for detail using.</td></tr>
<tr><td>TB</td><td>I</td><td>-Gate output direction H/W select pin on RGB I/F Mode 2.
When SMY=0
<table>
<tr><th rowspan="2">TB</th><th colspan="3">Module Gate output direction</th></tr>
<tr><th>GM=’00’, ‘01’</th><th>GM=’10’</th><th>GM=‘11’</th></tr>
<tr><td>0</td><td>G2 -> G161</td><td>G2 -> G129</td><td>G1 -> G162</td></tr>
<tr><td>1</td><td>G161 -> G2</td><td>G129 -> G2</td><td>G162 -> G1</td></tr>
</table>
When SMY=1
<table>
<tr><th rowspan="2">TB</th><th colspan="3">Module Gate output direction</th></tr>
<tr><th>GM=’00’, ‘01’</th><th>GM=’10’</th><th>GM=‘11’</th></tr>
<tr><td>0</td><td>G161 -> G2</td><td>G129 -> G2</td><td>G162 -> G1</td></tr>
<tr><td>1</td><td>G2 -> G161</td><td>G2 -> G129</td><td>G1 -> G162</td></tr>
</table>
-Please refer RGB I/F for detail using.</td></tr>
</table>

5.4 Driver Output Pins

Table 5.4.1: Driver output Pins

Symbol	I/O	Description
S1 to S396	O	-Source driver output pins.
G1 to G162	O	-Gate driver output pins.
VCI1	I/O	-A reference voltage in step-up circuit 1. -Connect a capacitor for stabilization.
AVDD	O	-A power output pin for source driver block that is generated from power block -Output of booster 1 circuit (output of 2-times output of VCI1 or VCI) -Connect a capacitor for stabilization.
VCL	O	-A power supply pin for generating VCOML. -Connect a capacitor for stabilization.
VGH	O	-Positive voltage of the Booster circuit 2 -Connect a capacitor for stabilization.
VGL	O	-Negative voltage of the Booster circuit 3 -Connect a capacitor for stabilization.
VREF	O	-Reference voltage for power block. -Connect a capacitor for stabilization.
GVDD	O	-A standard level for grayscale voltage generator -Connect a capacitor for stabilization.
VCOMH	O	-Positive voltage output of VCOM -Connect a capacitor for stabilization.
VCOML	O	-Negative voltage output of VCOM -Connect a capacitor for stabilization.
VCOM	O	-A power supply for the TFT common electrode.
C11P, C11M C12P, C12M	O	-Capacitor connecting pins for Booster circuit 1 (for AVDD)
C21P, C21M C22P, C22M C23P, C23M	O	-Capacitor connecting pins for Booster circuit 2 (for VGH, VGL, VCL)
VDDIO	O	-VDDI voltage output level for control pins using
DGNDO	O	-DGND voltage output level for control pins using
VCC	O	-Power supply for internal digital system

5.5 Test Pins

Table 5.5.1: Driver output Pins

Symbol	I/O	Description
PADA0	O	-These test pins for display glass break detection. -If not used, please open these pins.
PADB0	I	-These test pins for display glass break detection. -If not used, please open these pins **or fix to GND**.
PADA1, PADA2 PADA3, PADA4	O	-These test pins for chip attachment detection. -If not used, please open these pins.
PADB1, PADB2 PADB3, PADB4	I	-These test pins for chip attachment detection. -If not used, please open these pins **or fix to GND**.
DUMMY_TEST**, DUMMY_TESTOSC**	I	-These test pins for Driver vender test used. -If not used, please open these pins **or fix to GND**.
DUMMY_TESTDA[6:0], DUMMY_VPRER_OUT	O	-These test pins for Driver vender test used. -If not used, please open these pins.
DUMMY1~ DUMMY26	-	-These pins are dummy (not have any function inside) -Can have signal traces pass through on TFT glass under the PAD.

6. Driver Electrical Characteristics

6.1. Absolute Maximum Ratings

Table 6.1.1: Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	VDD	-0.3 ~ +4.6	V
Supply voltage (Logic)	VDDI	-0.3 ~ +4.6	V
Supply voltage (Digital)	VCC	-0.3 ~ +2.4	V
Driver supply Voltage	VGH-VGL	-0.3 ~ +33.0	V
Logic Input voltage range	V IN	-0.3 ~ VDDI + 0.3	V
Logic Output voltage range	VO	-0.3 ~ VDDI + 0.3	V
Operating temperature range	TOPR	-40 ~ +85	℃
Storage Temperature range	TSTG	-55 ~ +125	℃

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6.2 ESD Protection Level

Table 6.2.1: ESD Protection Level

Model	Test Condition	Protection Level	Unit
ESD Human Body Model	C = 100 pF, R = 1.5 kΩ 3 times zapping/ each pin, 1sec/ a zapping	±2500 for each pin ±3000 for connecter pin	V
ESD Machine Model	C = 200 pF, R = 0.0 Ω 3 times zapping/ each pin, 1sec/a zapping	±250 for each pin	V

Note: connecter pin is DATA BUS, Power, CSX, RDX, WRX, RESX, TE…

6.3 LATCH-UP PROTECTION LEVEL

The device will not latch up at trigger current levels less than ±100 mA.

6.4 Light Sensitivity

The operation of the IC will not be materially altered by incident light.

6.5 DC Characteristics

Table 6.5.1: Interface DC Characteristics

Parameter	Symbol	Conditions	Specification TYP			Unit	Related Pins
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VDD	Operating Voltage	2.6	2.78	3.3	V	Note 2
Logic Operating voltage	VDDI	I/O supply voltage	1.6	1.8/ 2.78	3.3	V	Note 2
Digital Operating voltage	VCC	Digital supply voltage	1.5	1.8	2.0	V	Note 2
Gate Driver High voltage	VGH		10.0		16.0	V	Note 3
Gate Driver Low voltage	VGL		-16.0		-9.0	V	Note 3
Driver Supply voltage		|VGH-VGL|	19		32	V	Note 3
Input /Output							
Logic High level input voltage	VIH		0.7VDDI	-	VDDI	V	Note 1, 2, 3
Logic Low level input voltage	VIL	-	VSS	-	0.3VDDI	V	Note 1, 2, 3
Logic High level output voltage	VOH	IOH = -1.0mA	0.8VDDI	-	VDDI	V	Note 1, 2, 3
Logic Low level output voltage	VOL	IOL = 1.0mA	VSS	-	0.2VDDI	V	Note 1, 2, 3
Logic High level input current	IIH				1	μA	Note 1, 2, 3
Logic Low level input current	IIL		-1			μA	Note 1, 2, 3
Logic Input leakage current	IIL	VIN = VDDI or VSS	-0.1	-	+0.1	μA	Note 1, 2, 3
VCOM Operation							
VCOM High voltage	VCOMH	Ccom=12nF	2.5		5.0	V	Note 3
VCOM Low voltage	VCOML	Ccom=12nF	-2.5		0.0	V	Note 3
VCOM Amplitude voltage	VCOMA	|VCOMH-VCOML|	4.0		5.5	V	Note 3
Source Driver							
Source output range	VSout		0.1		AVDD-0.1	V	Note 4
Gamma reference voltage	GVDD		3.0		5.0	V	Note 3
Source output settling time	Tr	Below with 99% precision		15	20	μs	Note 4, 5 Fig.6.5.2
Output deviation voltage (Source output channel)	V,dev	Sout >= 4.2V, Sout <= 0.8V			20	mV	Note 4 Fig.6.5.3
		4.2V>Sout>0.8V			15	mV	
Output offset voltage	VOFSET				35	mV	Note 8
Booster Operation							
1st Booster (VDDx2) voltage	AVDD		4.95 *6)		5.5 *7)	V	Note 3
1st Booster (VDDx2) Drop voltage	VDDx2,drop	I loading = 1mA			5	%	Note 3
Linear range	VLinear		0.2		AVDD-0.2	V	

Note 1: VDDI=1.6 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃ (to +85℃ no damage)

Note 2: Please supply digital VDDI voltage equal or less than analog VDD voltage. (VDDI ≤ VDD)

Note 2, 3, 4: When the measurements are performed with LCD module, Measurement Points are like below.

Note 3: CSX, RDX, WRX, D[23:0], D/CX, RESX, TE, PCLK, VS, HS, DE, SDA, SCL, GM1, GM0, LCM, RCM1, RCM0, P68, IM2, IM1, IM0, SRGB, REV, SMX, SMY, RL, TB, IDM, SHUT, PREG, GS and Test pins

Note 5, Source channel loading= 10pF/channel, Gate channel loading= 50pF/channel.

Note 6, VDD=2.6V or VCI1=2.6V

Note 7, VDD=3.3V or VCI1=3.3V

Note 8, The Max. value is between with Note 4 measure point and Gamma setting value.

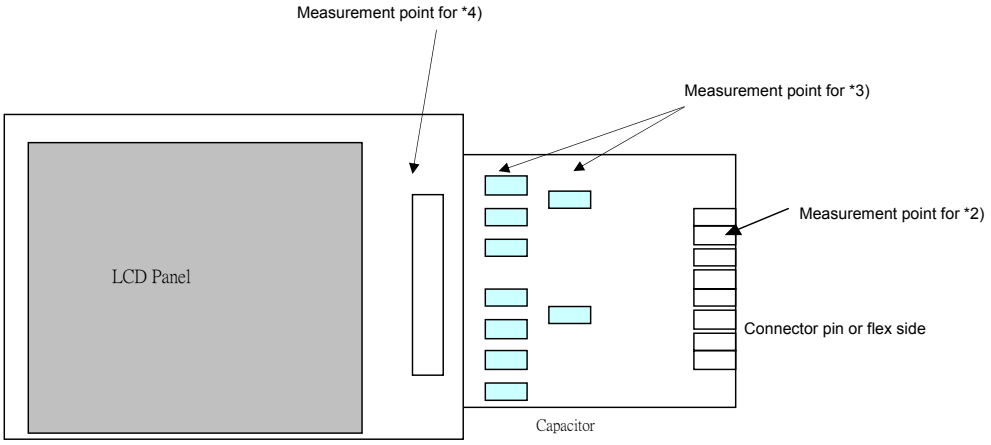


Fig 6.5.1 Measurement Points for All Characteristics.

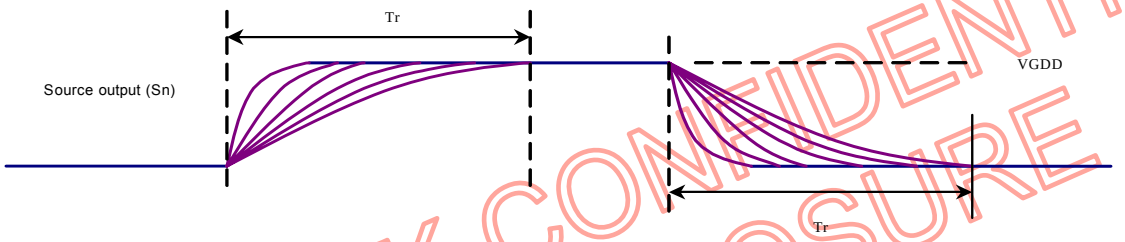


Fig. 6.5.2 Tr : Source output stable timing

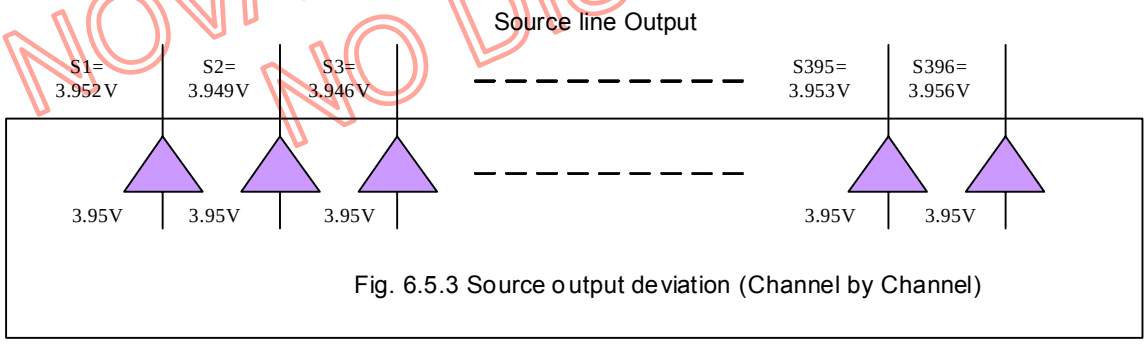


Fig. 6.5.3 Source output deviation (Channel by Channel)

-When Sout >=4.2V, Sout<=0.8V

Max (S1, S2, S3, …. , S396) – Min (S1, S2, S3, …. , S396) <= 20mV

-When 4.2V>Sout>0.8V

Max (S1, S2, S3, …. , S396) – Min (S1, S2, S3, …. , S396) <= 6mV

-Example

When Sout level is 3.95V (Gray scale voltage)

Max (S1, S2, S3, …. , S396) = 3.956V

Min (S1, S2, S3, …. , S396) = 3.946V

Sout deviation =

Max (S1, S2, S3, …. , S396) – Min (S1, S2, S3, …. , S396) = 10mV <- Out Spec

6.6 Power Consumption

Note: Power consumption table is included display module specification.

Mode of operation	Frame Frequency	Inversion Mode	Image	B5;B6;B7	Current consumption			
					Typical		Worst case	
					IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
-Normal Mode On -Partial Mode Off -Idle Mode Off -Sleep Out Mode (5)	60Hz	One Line	Note 1	X;X;X	0.002	1	0.002	1.1
		One Line	Note 2	X;X;X	0.002	1.7	0.002	1.8
		One Line	Note 3	X;X;X	0.002	1.4	0.002	1.5
		One Line	Note 4	X;X;X	0.002	1.4	0.002	1.5
		One Line	Note 6	X;X;X	0.002	1.7	0.002	1.8
-Normal Mode On -Partial Mode Off -Idle Mode On -Sleep Out Mode (5)	60Hz	Frame	Note 6	X;X;X	0.002	0.5	0.002	0.55
-Normal Mode Off -Partial Mode On (40 lines) -Idle Mode Off -Sleep Out Mode (5)	60Hz	Line	Note 6	X;X;X	0.002	0.65	0.002	0.7
-Normal Mode Off -Partial Mode On (40 lines) -Idle Mode On -Sleep Out Mode (5)	60Hz	Frame	Note 3	X;X;X	0.002	0.4	0.002	0.45
		Frame	Note 6	X;X;X	0.002	0.4	0.002	0.45
-Sleep In Mode (5)	N/A	N/A	N/A	X;X;X	0.002	0.014	0.002	0.015
-Normal Mode On -Partial Mode Off -Idle Mode Off -Sleep Out Mode	60Hz	One Line	Note 7-A CPU Access @ 30 fps	0;0;0	0.105	1.41	0.11	1.83
				0;0;1	0.105	1.41	0.11	1.83
				0;1;0	0.105	1.41	0.11	1.83
				0;1;1	0.105	1.41	0.11	1.83
				1;0;0	0.105	1.41	0.11	1.83
				1;0;1	0.105	1.41	0.11	1.83
				1;1;0	0.105	1.41	0.11	1.83
				1;1;1	0.105	1.41	0.11	1.83
			Note 7-B CPU Access @ 30 fps	0;0;0	0.105	1.63	0.11	2.12
				0;0;1	0.105	1.63	0.11	2.12
				0;1;0	0.105	1.63	0.11	2.12
				0;1;1	0.105	1.63	0.11	2.12
				1;0;0	0.105	1.63	0.11	2.12
				1;0;1	0.105	1.63	0.11	2.12
				1;1;0	0.105	1.63	0.11	2.12
				1;1;1	0.105	1.63	0.11	2.12

Table 6.6.1. Power consumption of display module, Architecture type I
Typical Case: T_A = 25 °C, VDD = 2.8 V, VDDI = 1.80 V
Worst Case: T_A = -30 to70 °C, VDD = 2.60 V to 2.9 V, VDDI = 1.65 V to 1.95 V
Includes Process Variance.

Notes:

1. All pixels black.

2. All pixels white.

3. Checker board 4 by 4.

4. Grayscale from top to bottom.

5. CPU access is inactive.

6. Absolute Worst Case Patterns: Vertical gray bar(involve 0-64 level)

7. A-Moving pattern: Frames 1,3,5,...=White/Black 1x1 pattern, Frames 2,4,6,...= Black /White 1x1 pattern.
B-Moving pattern: Vertical gray bar (involve 0-64 level)

8. Inrush currents are not included in current consumption values.

9. Now all values were evaluated for reference. Data will be updated after display modules come out.

6.7 Maximum Series Resistance

The driver will operate in 'Chip on Glass' applications with series resistances (due to ITO track resistance). Voltages are specified at module I/O assuming maximum values as in Table 6.7.

Pin No	Pin Name	Resistance	Pin No	Pin Name	Resistance	Pin No	Pin Name	Resistance
1	EXTC	<=100	31	D7	<=100	61	GVDD	<=10
2	IM0	<=100	32	D6	<=100	62	C11P	<=20
3	IM1	<=100	33	D5	<=100	63	C11M	<=20
4	IM2	<=100	34	D4	<=100	64	C12P	<=20
5	P68	<=100	35	D3	<=100	65	C12M	<=20
6	RCM0	<=100	36	D2	<=100	66	CGND	<=10
7	RCM1	<=100	37	D1	<=100	67	VCL	<=20
8	SRGB	<=100	38	D0 (SDA)	<=100	68	C21P	<=20
9	SMX	<=100	39	OSC	<=100	69	C21M	<=20
10	SMY	<=100	40	TE	<=100	70	C22P	<=20
11	IDM	<=100	41	CSX	<=100	71	C22M	<=20
12	REV	<=100	42	RDX (E)	<=100	72	C23P	<=20
13	RL	<=100	43	WRX (R/Wx)	<=100	73	C23M	<=20
14	TB	<=100	44	SDA	<=100	74	VGL	<=20
15	SHUT	<=100	45	GS	<=100	75	VGH	<=20
16	GM1	<=100	46	SPI4W	<=100	76	VCOMH	<=10
17	GM0	<=100	47	RESX	<=300	77	VCOML	<=10
18	LCM0	<=100	48	D/CX(SCL)	<=100			
19	LCM1	<=100	49	PCLK	<=100			
20	D17	<=100	50	DE	<=100			
21	D16	<=100	51	HS	<=100			
22	D15	<=100	52	VS	<=100			
23	D14	<=100	53	DGND	<=10			
24	D13	<=100	54	VDDI	<=10			
25	D12	<=100	55	VCC	<=10			
26	D11	<=100	56	VCI1	<=10			
27	D10	<=100	57	AGND	<=10			
28	D9	<=100	58	VDD	<=10			
29	D8	<=100	59	VREF	<=10			
30	TESEL	<=100	60	AVDD	<=10			

Table 6.7 Maximum series resistance on module.

7. Timing Charts

7.1 Parallel Interface Characteristics 18, 16, 9 or 8-bits bus (8080-series MCU)

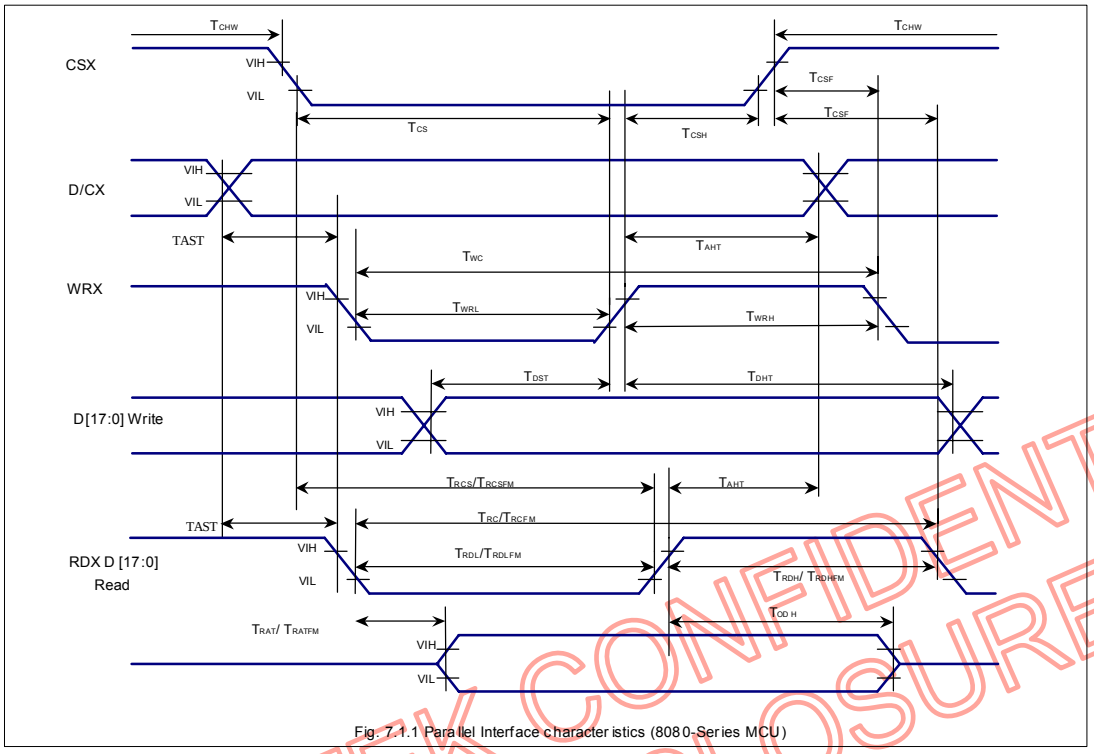


Fig. 7.1.1 Parallel Interface characteristics (8080-Series MCU)

Table .7.7.1: AC Characteristics for Parallel Interface 24, 16, 8-bits bus (8080-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	TAST	Address setup time	10		ns	-
	TAHT	Address hold time (Write/Read)	10		ns	
CSX	TCHW	Chip select “H”pulse width	0		ns	
	TCS	Chip select setup time (Write)	35		ns	
	TRCS	Chip select setup time (Read ID)	45		ns	
	TRCSFM	Chip select setup time (Read FM)	355		ns	
	TCSF	Chip select wait time (Write/Read)	10		ns	
	TCSH	Chip select hold time	10		ns	
WRX	TWC	Write cycle	100		ns	
	TWRH	Control pulse “H” duration	35		ns	
	TWRL	Control pulse “L” duration	35		ns	
RDX (ID)	TRC	Read cycle (ID)	160		ns	When read ID data
	TRDH	Control pulse “H” duration (ID)	90		ns	
	TRDL	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	TRCFM	Read cycle (FM)	450		ns	When read from frame memory
	TRDHFM	Control pulse “H” duration (FM)	90		ns	
	TRDLFM	Control pulse “L” duration (FM)	355		ns	
D[17:0]	TDST	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	TDHT	Data hold time	10		ns	
	TRAT	Read access time (ID)		40	ns	
	TRATFM	Read access time (FM)		340	ns	
	TODH	Output disable time	20	80	ns	

Note 1: VDD1=1.6 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

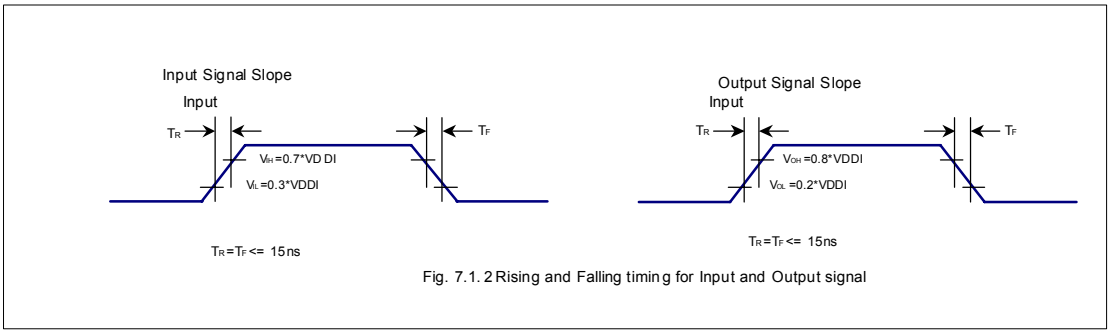


Fig. 7.1. 2 Rising and Falling timing for Input and Output signal

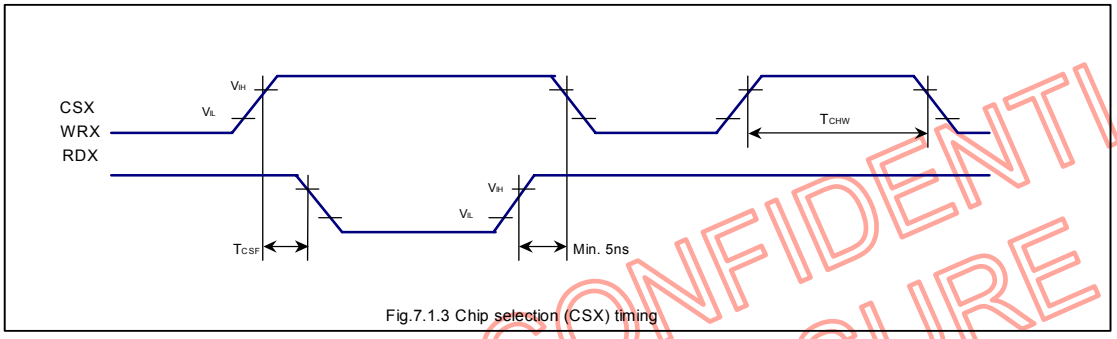


Fig.7.1.3 Chip selection (CSX) timing

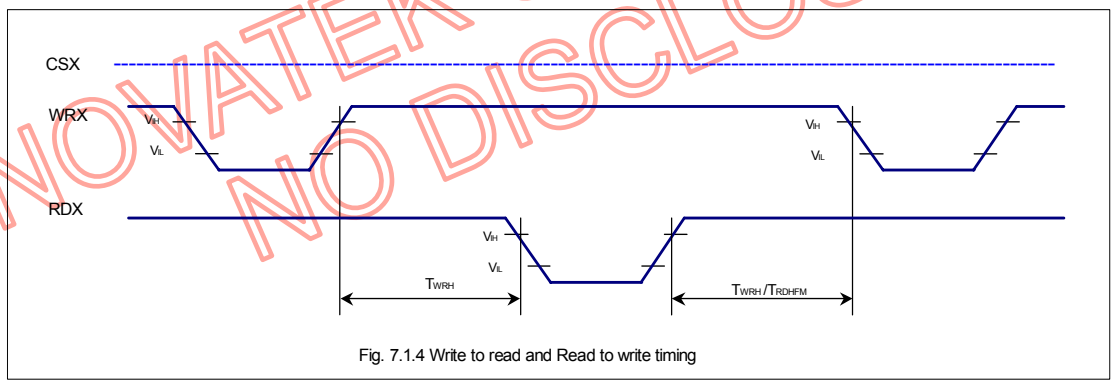


Fig. 7.1.4 Write to read and Read to write timing

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.2 Parallel Interface Characteristics 18, 16, 9 or 8-bits bus (6800-series MCU)

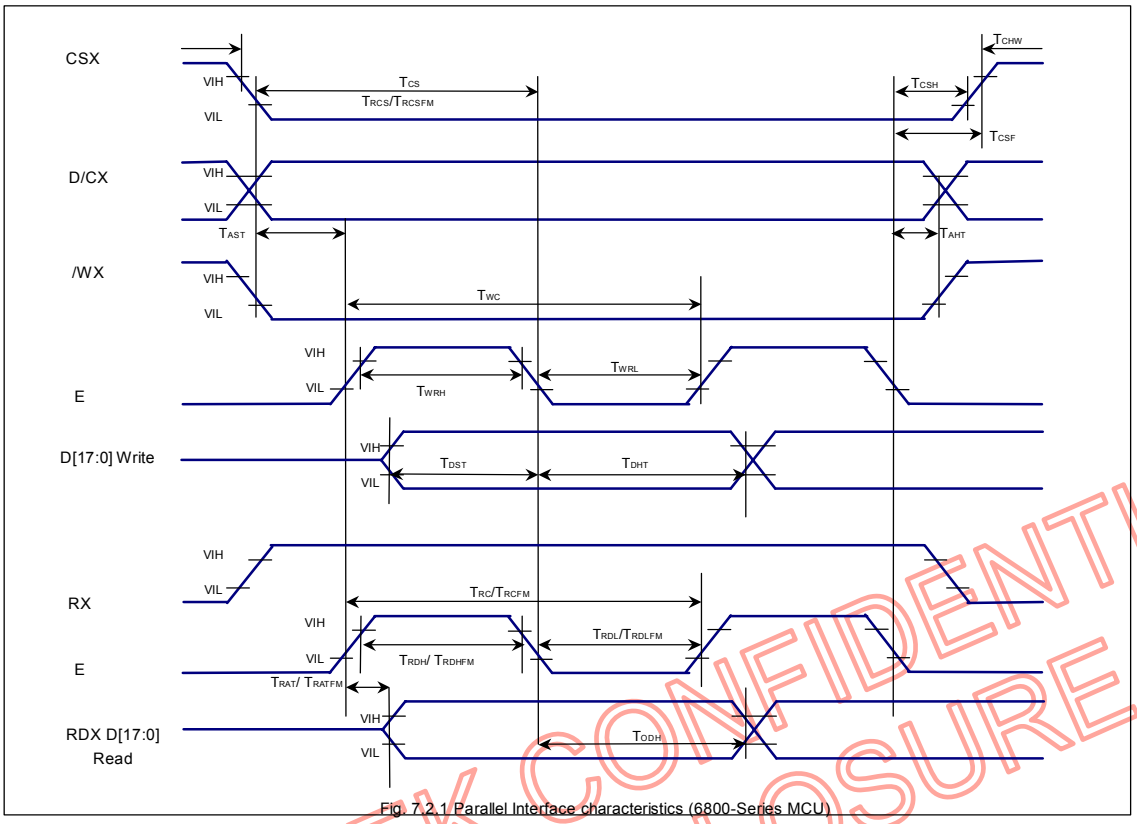


Fig. 7.2.1 Parallel Interface characteristics (6800-Series MCU)

Table 7.2.1: AC Characteristics for Parallel Interface 24, 16, 8-bits bus (6800-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	tAST	Address setup time	10		ns	-
	tAHT	Address hold time (Write/Read)	10		ns	
CSX	tCHW	Chip select "H" pulse width	0		ns	-
	tCS	Chip select setup time (Write)	35		ns	
	tRCS	Chip select setup time (Read ID)	45		ns	
	tRCSFM	Chip select setup time (Read FM)	355		ns	
	tCSF	Chip select wait time (Write/Read)	10		ns	
	tCSH	Chip select hold time	10		ns	
WRX	tWC	Write cycle	100		ns	
	tWRH	Control pulse "H" duration	35		ns	
	tWRL	Control pulse "L" duration	35		ns	
RDX (ID)	tRC	Read cycle (ID)	160		ns	When read ID data
	tRDH	Control pulse "H" duration (ID)	90		ns	
	tRDL	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	tRCFM	Read cycle (FM)	450		ns	When read from frame memory
	tRDHFM	Control pulse "H" duration (FM)	90		ns	
	tRDLFM	Control pulse "L" duration (FM)	355		ns	
D[17:0]	tDST	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	tDHT	Data hold time	10		ns	
	tRAT	Read access time (ID)		40	ns	
	tRATFM	Read access time (FM)		340	ns	
	tODH	Output disable time	20	80	ns	

Note 1: VDD1=1.6 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.3 Serial Interface Characteristics

7.3.1 3-pin Serial Interface

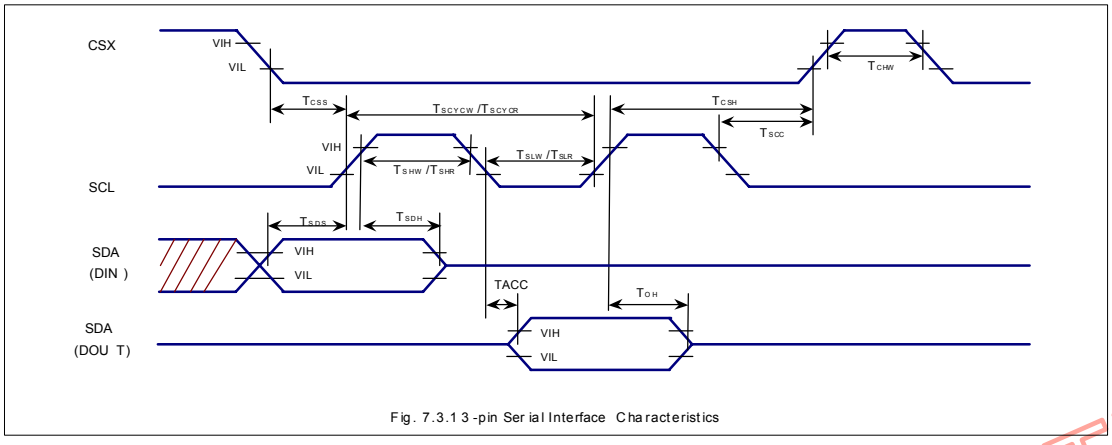


Fig. 7.3.1 3-pin Serial Interface Characteristics

Table 7.3.1: 3-pin Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time	60		ns	
	TCSH	Chip select hold time	54		ns	
	TSCC	Chip select setup time	20		ns	
	TCHW	Chip select setup time	34		ns	
SCL	TSCYCW	Serial clock cycle (Write)	65		ns	-
	TSHW	SCL “H” pulse width (Write)	14		ns	
	TSLW	SCL “L” pulse width (Write)	15		ns	
	TSCYCR	Serial clock cycle (Read)	150		ns	
	TSHR	SCL “H” pulse width (Read)	54		ns	
	TSLR	SCL “L” pulse width (Read)	54		ns	
SDA (DIN) (DOUT)	TSDS	Data setup time	7		ns	
	TSDH	Data hold time	7		ns	
	TACC	Access time	10	50	ns	For maximum CL=30pF
	TOH	Output disable time	15		ns	For minimum CL=8pF

Note 1: VDD1=1.6 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 10% and 90% of VDDI for Input signals.

7.3.2 4-pin Serial Interface

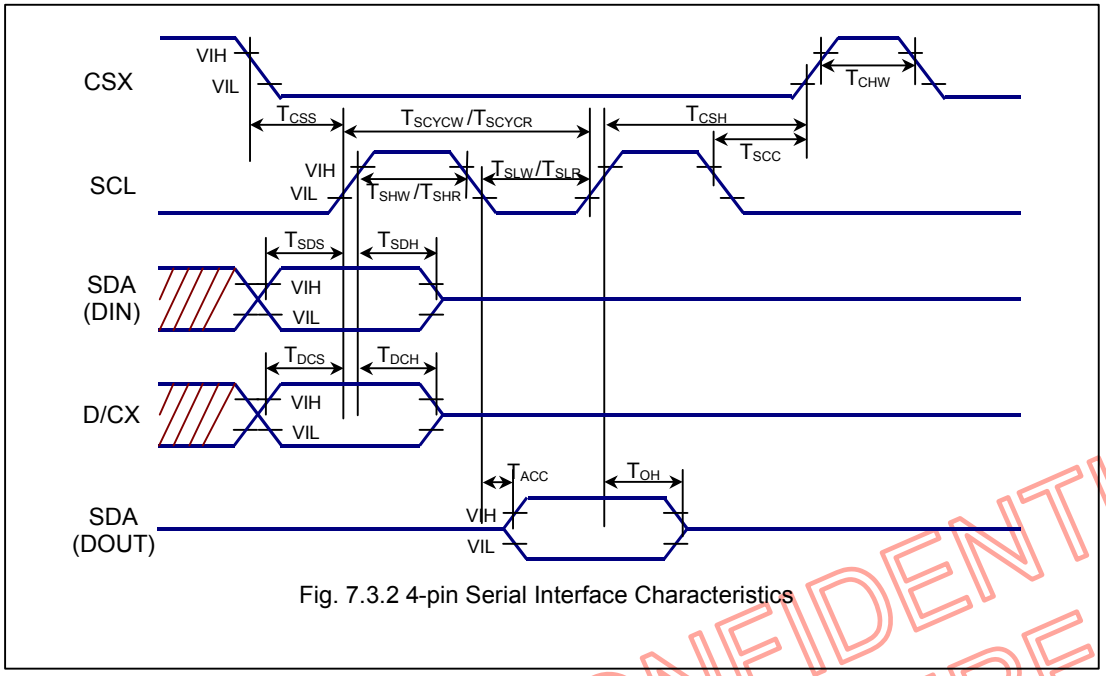


Fig. 7.3.2 4-pin Serial Interface Characteristics

Table 7.3.2: 4-pin Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time	60		ns	
	TCSH	Chip select hold time	54		ns	
	TSCC	Chip select setup time	20		ns	
	TCHW	Chip select setup time	34		ns	
SCL	TSCYCW	Serial clock cycle (Write)	65		ns	-
	TSHW	SCL “H” pulse width (Write)	14		ns	
	TSLW	SCL “L” pulse width (Write)	15		ns	
	TSCYCR	Serial clock cycle (Read)	150		ns	
	TSHR	SCL “H” pulse width (Read)	54		ns	
	TSLR	SCL “L” pulse width (Read)	54		ns	
D/CX	TDCS	D/CX setup time	7		ns	
	TDCH	D/CX hold time	7		ns	
SDA (DIN) (DOUT)	TSDS	Data setup time	7		ns	
	TSDH	Data hold time	7		ns	
	TACC	Access time	10	50	ns	For maximum CL=30pF
	TOH	Output disable time	15		ns	For minimum CL=8pF

Note 1: VDD1=1.6 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 10% and 90% of VDDI for Input signals.

7.4 RGB Interface Characteristics

7.4.1 General Timing Diagram

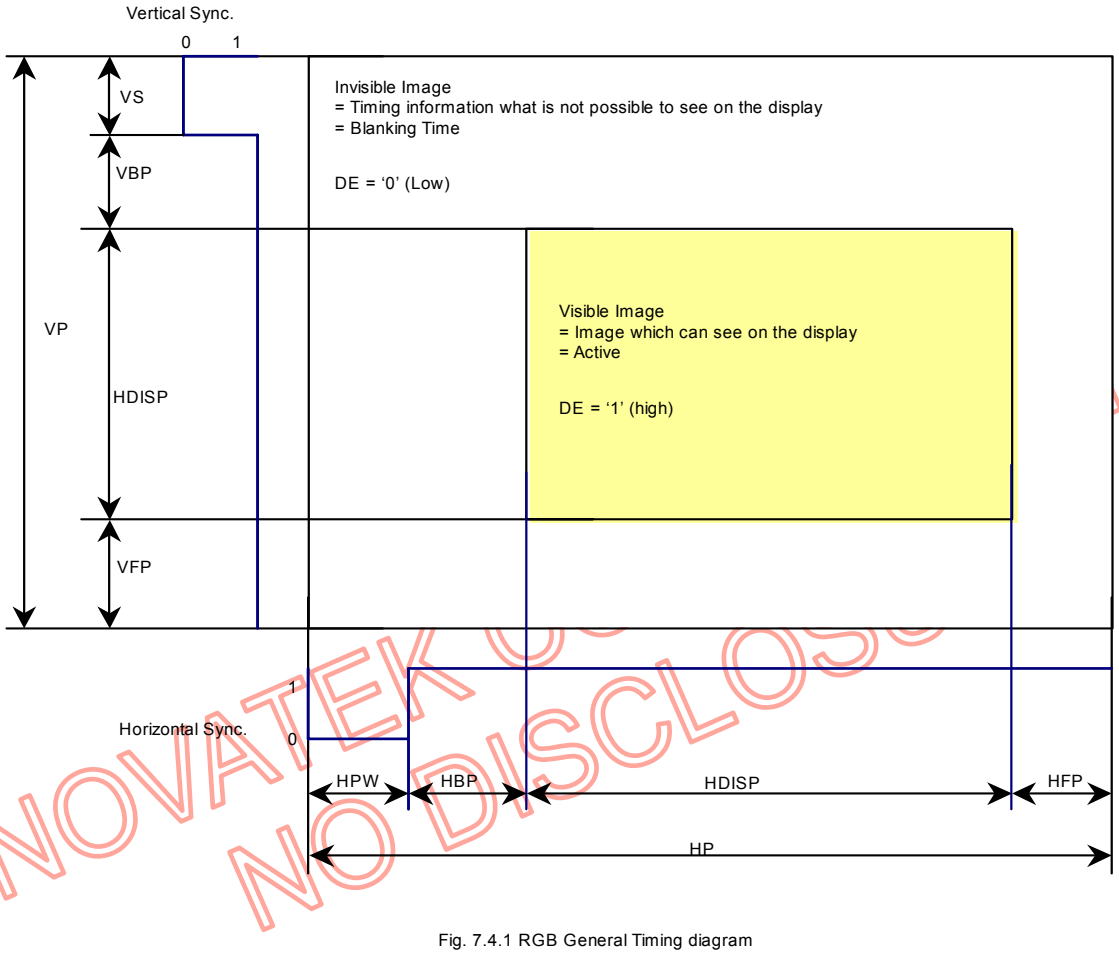


Fig. 7.4.1 RGB General Timing diagram

The image information must be correct on the display, when the timings are in range on the interface. However, the image information can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing

7.4.2 Updating Order on Display Active Area (Normal Display Mode On + Sleep Out)

There is defined different kind of updating orders for display. These updating orders are controlled by H/W (SMX, SMY) and S/W (MX, MY, MV) bits

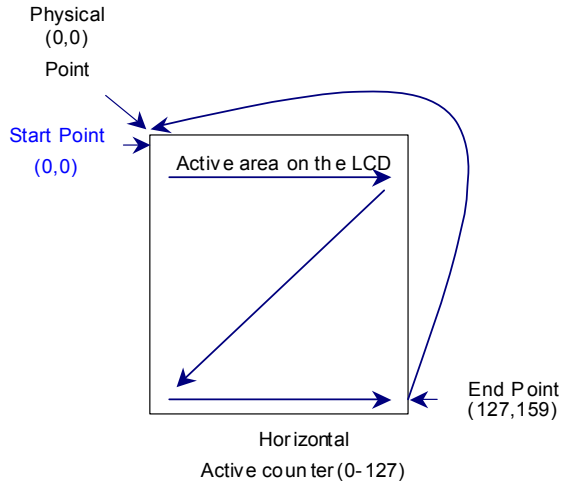


Fig. 7.4.2 Updating order when MADCTL's MX= '0' and MY= '0'

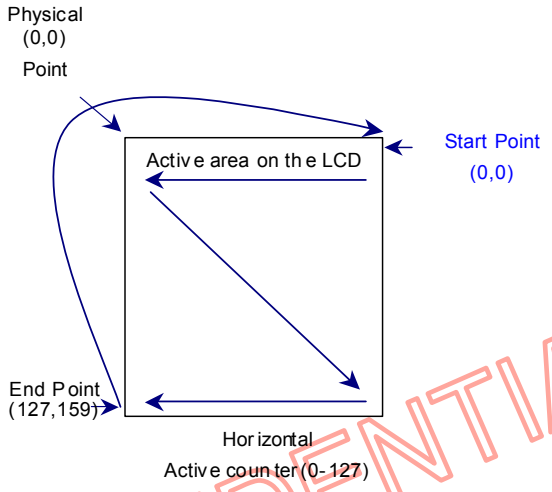


Fig. 7.4.3 Updating order when MADCTL's MX= '1' and MY= '0'

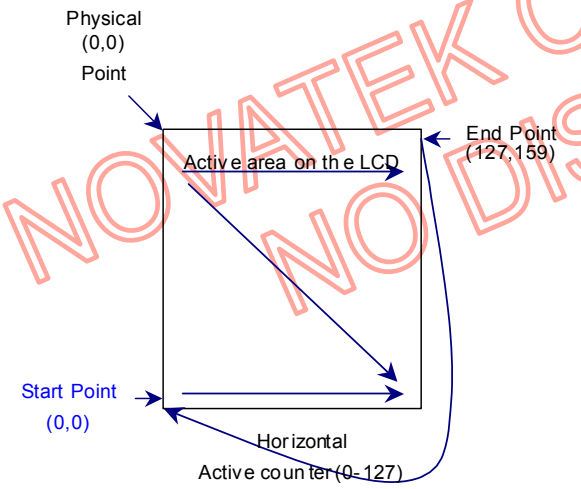


Fig. 7.4.4 Updating order when MADCTL's MX= '0' and MY= '1'

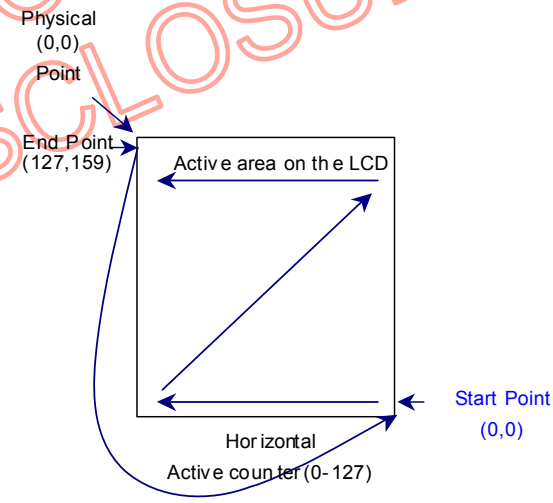
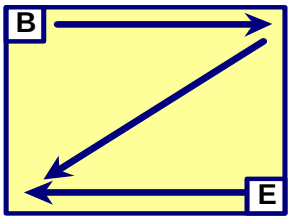


Fig. 7.4.5 Updating order when MADCTL's MX= '1' and MY= '1'

Table 7.4.1 Rules for Updating Order

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Signal Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter is larger than 127 and the Vertical counter is larger than 159	Return to 0	Return to 0

Note 1. Pixel order is RGB on the display.
Note 2. Data streaming direction from the host to the display is described in the following figure.
Note 3. In this case, GM="00" and 128RGB x 160.



Data Stream from RGB I/F is like in this figure

Fig. 7.4.6 Data streaming order from RGB I/F

7.4.3 General Timings for RGB I/F

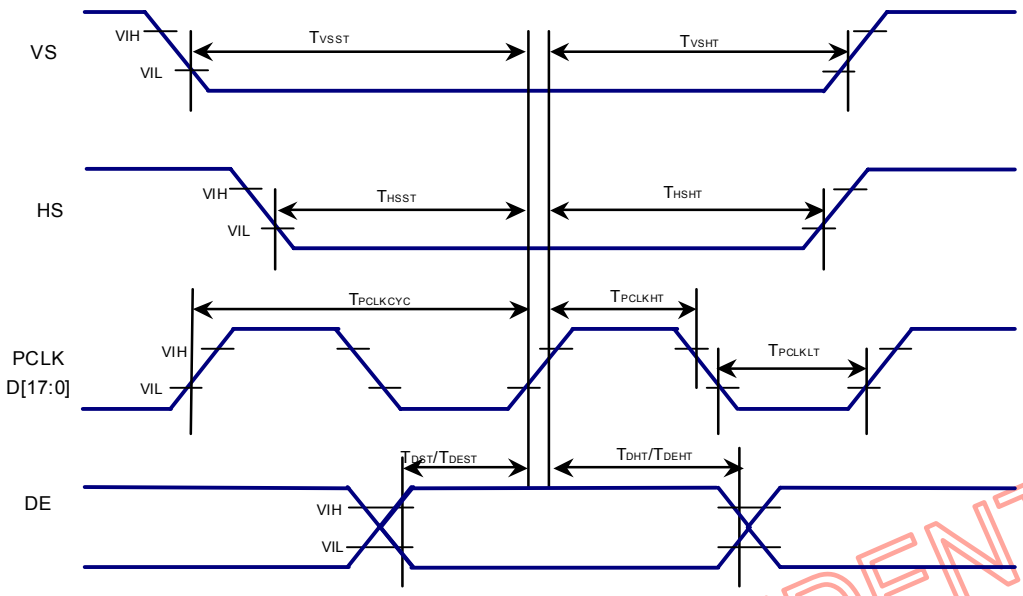


Fig. 7.4.3.1 General Timing for RGB I/F

Table 7.4.3 General Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Pixel low pulse width	TPCLKLT		15			ns
Pixel high pulse width	TPCLKHT		15			ns
Vertical Sync. set-up time	TVSST		15			ns
Vertical Sync. hold time	TVSSHT		15			ns
Horizontal Sync. set-up time	THSST		15			ns
Horizontal Sync. hold time	TVSSHT		15			ns
Data Enable set-up time	TDEST		15			ns
Data Enable hold time	TDEHT		15			ns
Data set-up time	TDST		15			ns
Data hold time	TDHT		15			ns

Note 1: VDDI=1.6 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Note 3. Data lines can be set to "High" or "Low" during blanking time – Don't care.

Note 4. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Note 5. HP is multiples of eight PCLK.

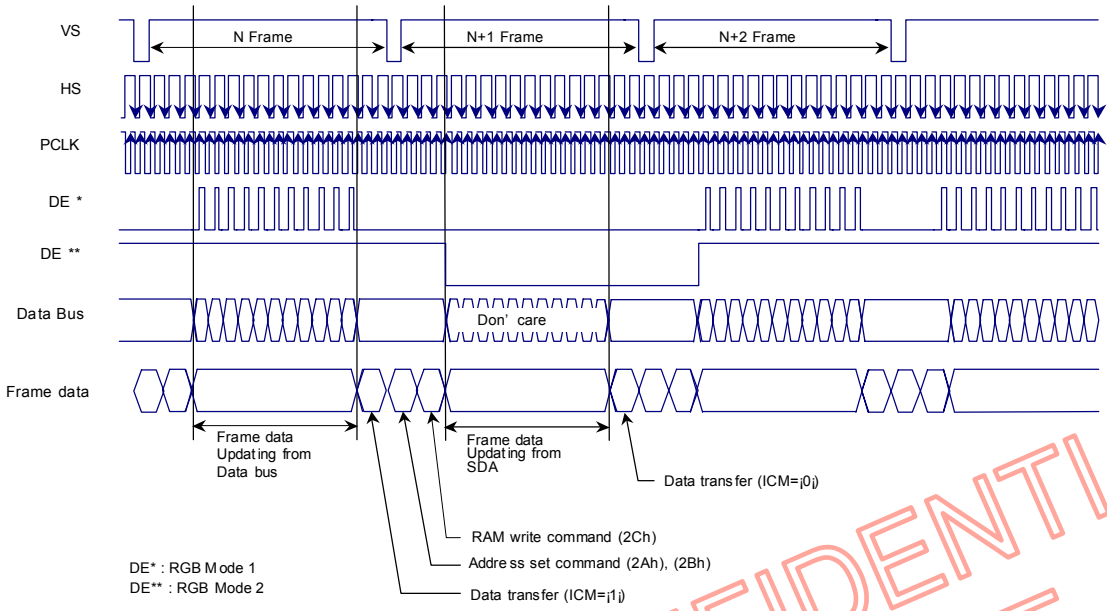


Fig. 7.4.3.2 RAM Access via SPI Interface in RGB Mode (V)

7.4.4 Vertical and Horizontal Timings for RGB I/F Mode 1

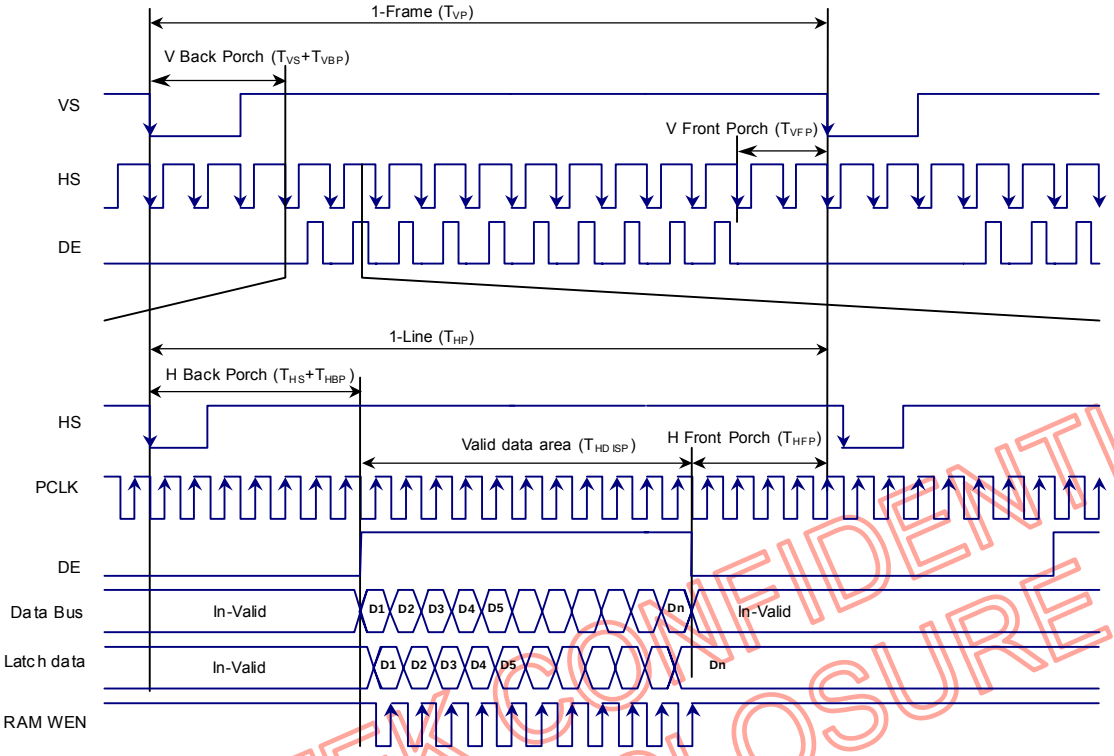
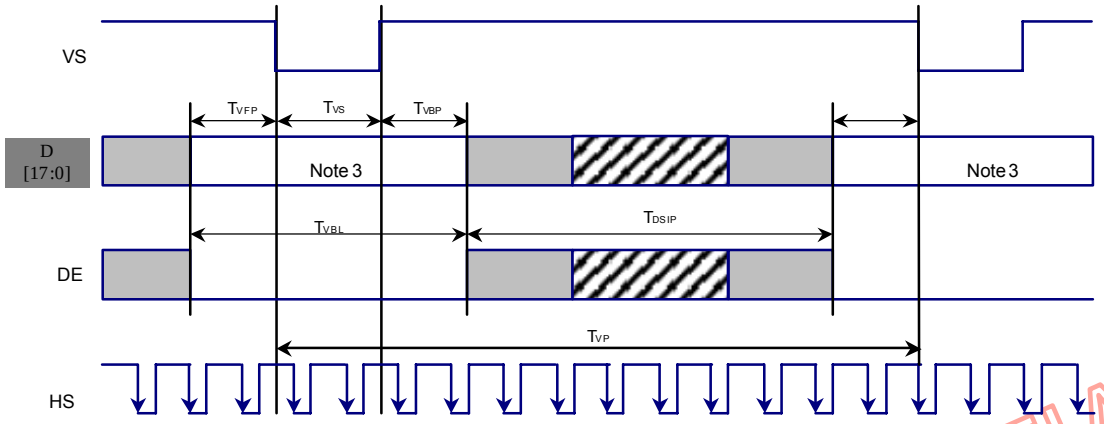


Fig. 7.4.4.1 RGB Mode 1 Timing Diagram

Note: DP=0, EP=0, HSP=0 and VSP=0 of RGBCTR (B0h) command.

Vertical Timing for RGB I /F



Horizontal Timing for RGB I/F

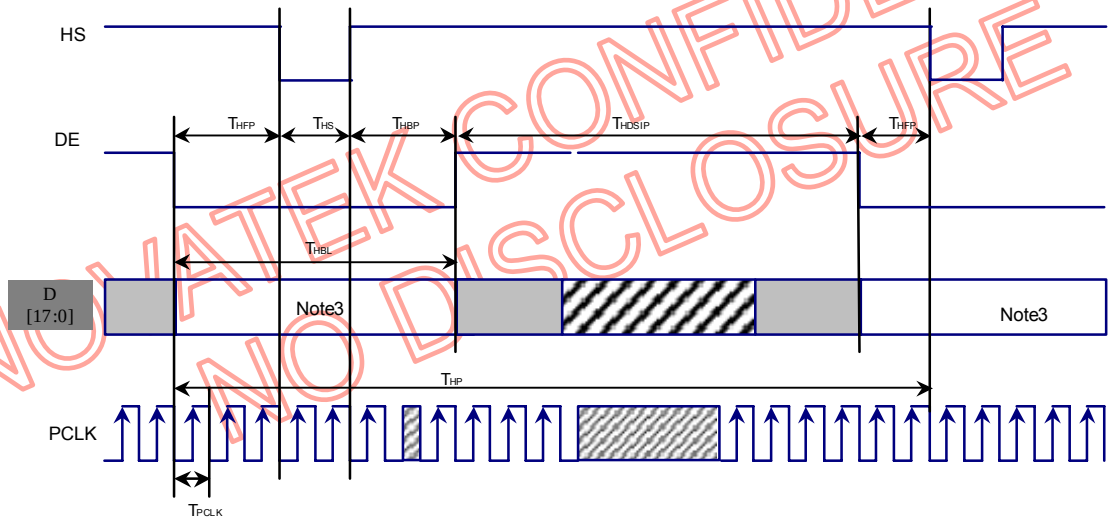


Fig. 7.4.4.2 Vertical and Horizontal timing for RGB I/F

Table 7.4.4 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	TVP	GM=”00”, “01”	166		172	HS
	TVP	GM=”10”	134		140	HS
	TVP	GM=”11”	168		174	HS
Vertical low pulse width	TVS		2		4	HS
Vertical front porch	TVFP		2		4	HS
Vertical back porch	TVBP		2		4	HS
Vertical data start line		TVS + TVBP	4		8	HS
Vertical blanking period	TVBL	TVS + TVBP + TVFP	6		12	HS
Vertical active area	TVDISP	GM=”00”, “01”		160		HS
	TVDISP	GM=”10”		128		HS
	TVDISP	GM=”11”		162		HS
Vertical refresh rate	TVRR	Frame rate	61.75	65	68.25	Hz
Horizontal Timing						
Horizontal cycle period	THP	GM=”00”, “10”	160		745	PCLK
	THP	GM=“01”	152		745	PCLK
	THP	GM=“11”	164		745	PCLK
Horizontal low pulse width	THS		2		255	PCLK
Horizontal front porch	THFP		2		255	PCLK
Horizontal back porch	THBP		2		255	PCLK
		THS + THBP	30		766	PCLK
Horizontal data start point		ff HS+ fHBP	1.0			μs
Horizontal blanking period	THBL		32		768	PCLK
Horizontal active area	THDISP	GM=”00”, “10”		128		PCLK
		GM=“01”		120		PCLK
		GM=“11”		132		PCLK
Pixel clock cycle	TPCLKCYC	GM=“00”	100		579	ns
	fPCLKCYC	TVRR=65Hz	1.7		10	MHz
	TPCLKCYC	GM=“01”	100		610	ns
	fPCLKCYC	TVRR=65Hz	1.6		10	MHz
	TPCLKCYC	GM=“10”	100		718	ns
	fPCLKCYC	TVRR=65Hz	1.4		10	MHz
	TPCLKCYC	GM=“11”	100		559	ns
	fPCLKCYC	TVRR=65Hz	1.8		10	MHz

Note 1. VDD1=1.6 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃ (to +85 ℃ no damage)

Note 2. Data lines can be set to “High” or “Low” during blanking time – Don’t care.

Note 3. HP is multiples of eight PCLK.

7.4.5 Vertical and Horizontal Timings for RGB I/F Mode 2

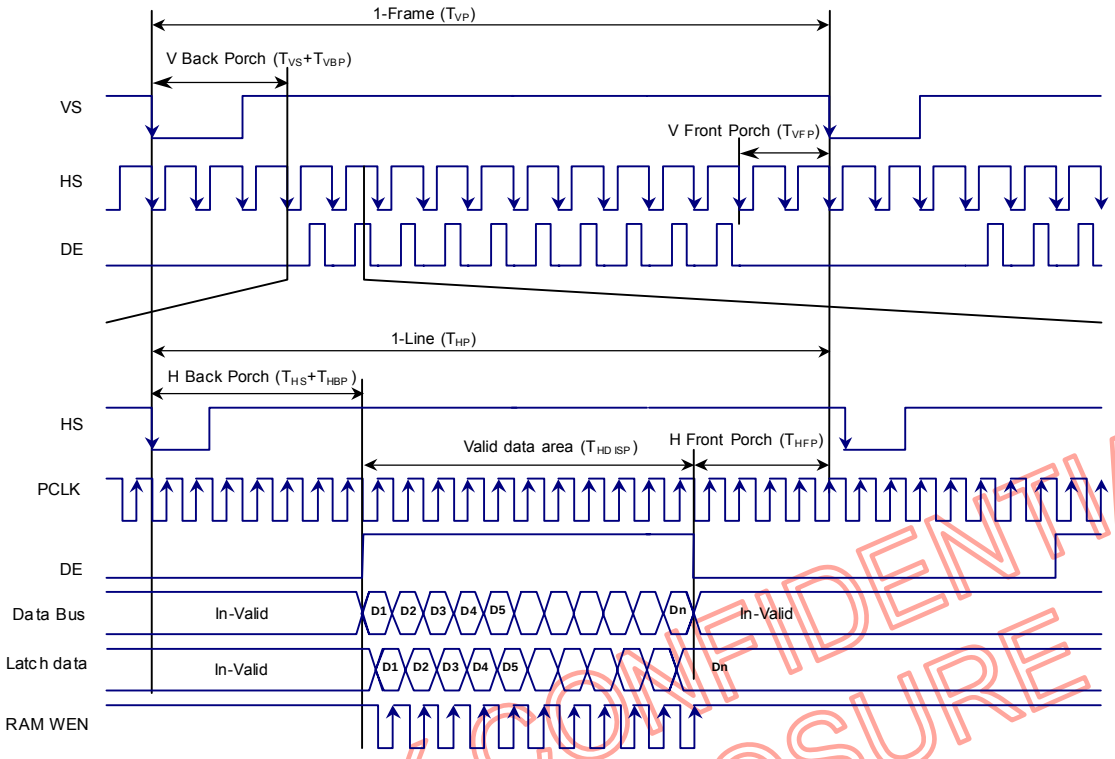


Fig. 7.4.5.1 RGB Mode 2 Timing Diagram

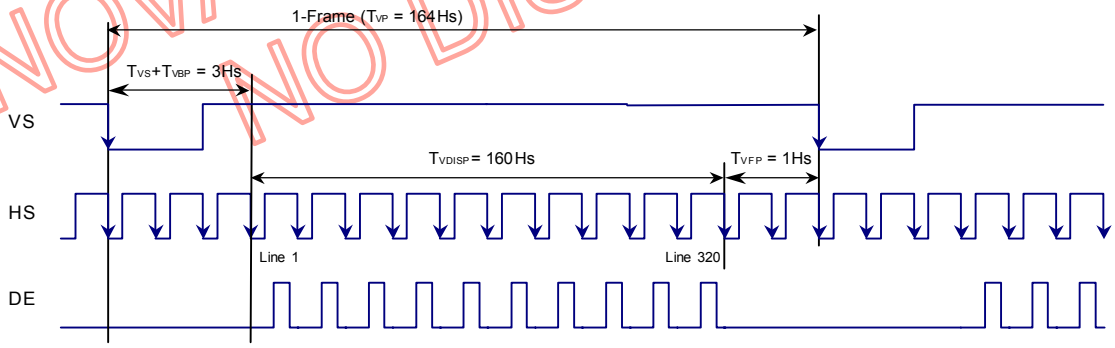


Fig. 7.4.5.2 RGB Mode 2 Vertical Timing Diagram

Note: DP=0, EP=0, HSP=0 and VSP=0 of RGBCTR (B0h) command.

-128xRGB x160

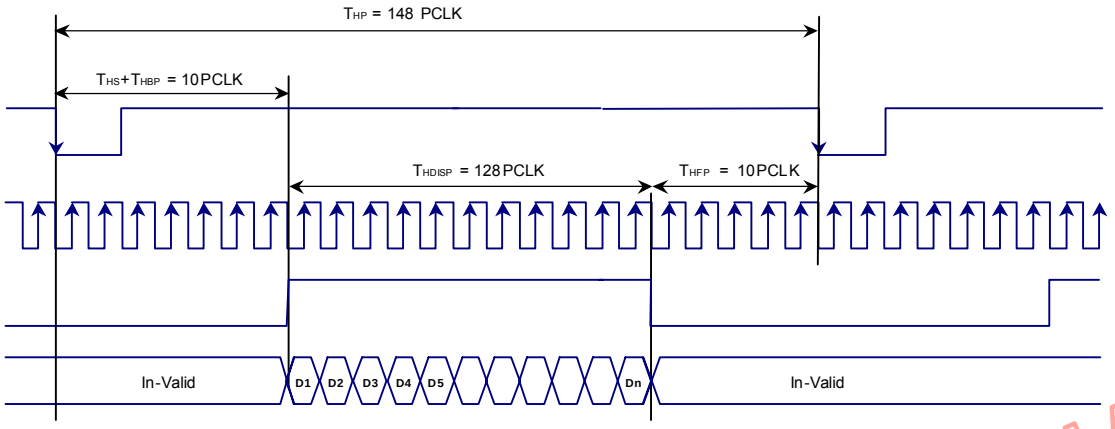


Fig. 7.4.5.3 RGB Mode 2 Horizontal Timing Diagram

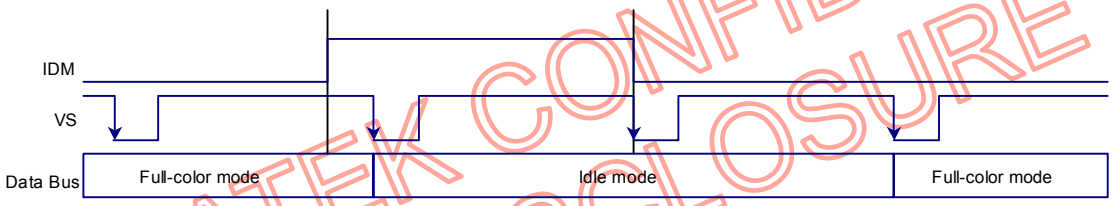


Fig. 7.4.5.4 RGB Mode 2 Idle mode Timing Diagram

Table 7.4.5 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	TVP	GM="00", "01"	163	164		HS
	TVP	GM="10"	131	132		HS
	TVP	GM="11"	165	166		HS
Vertical low pulse width	TVS		1		4	HS
Vertical front porch	TVFP		1	1	1023	HS
Vertical back porch	TVBP		1		1022	HS
Vertical data start line		TVS + TVBP	2	3	1023	HS
Vertical blanking period	TVBL	TVS + TVBP + TVFP	3	4	1023	HS
Vertical active area	TVDISP	GM="00", "01"		160		HS
	TVDISP	GM="10"		128		
	TVDISP	GM="11"		162		
Vertical refresh rate	TVRR	Frame rate	61.75	65	68.25	Hz
Horizontal Timing						
Horizontal cycle period	THP	GM="00", "10"	131	148	511	PCLK
	THP	GM="01"	123	140	511	PCLK
	THP	GM="11"	135	152	511	PCLK
Horizontal low pulse width	THS		1		63	PCLK
Horizontal front porch	THFP		1		63	PCLK
Horizontal back porch	THBP		1		62	PCLK
		THS + THBP	1	10	63	PCLK
Horizontal data start point		ff HS+ fHBP	TBD			μs
Horizontal blanking period	THBL		3	20	256	PCLK
Horizontal active area	THDISP	GM="00", "10"		128		PCLK
		GM="01"		120		PCLK
		GM="11"		132		PCLK
Pixel clock cycle	TPCLKCYC	GM="00"	100	634	720	ns
	fPCLKCYC	TVRR=65Hz	1.39	1.58	10	MHz
	TPCLKCYC	GM="01"	100	670	767	ns
	fPCLKCYC	TVRR=65Hz	1.30	1.49	10	MHz
	TPCLKCYC	GM="10"	100	788	896	ns
	fPCLKCYC	TVRR=65Hz	1.12	1.27	10	MHz
	TPCLKCYC	GM="11"	100	610	691	ns
	fPCLKCYC	TVRR=65Hz	1.45	1.64	10	MHz

Note 1. VDD1=1.6 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃ (to +85 ℃ no damage)

Note 2. Data lines can be set to "High" or "Low" during blanking time – Don't care.

Note 3. HP is multiples of eight PCLK.

7.4.5.1 Power ON Sequence on RGB I/F Mode 2

The Driver operates power up and display ON by VDD, VDDI, SHUT, VS, HS, DE, PCLK on RGB mode 2 as show as following figure.

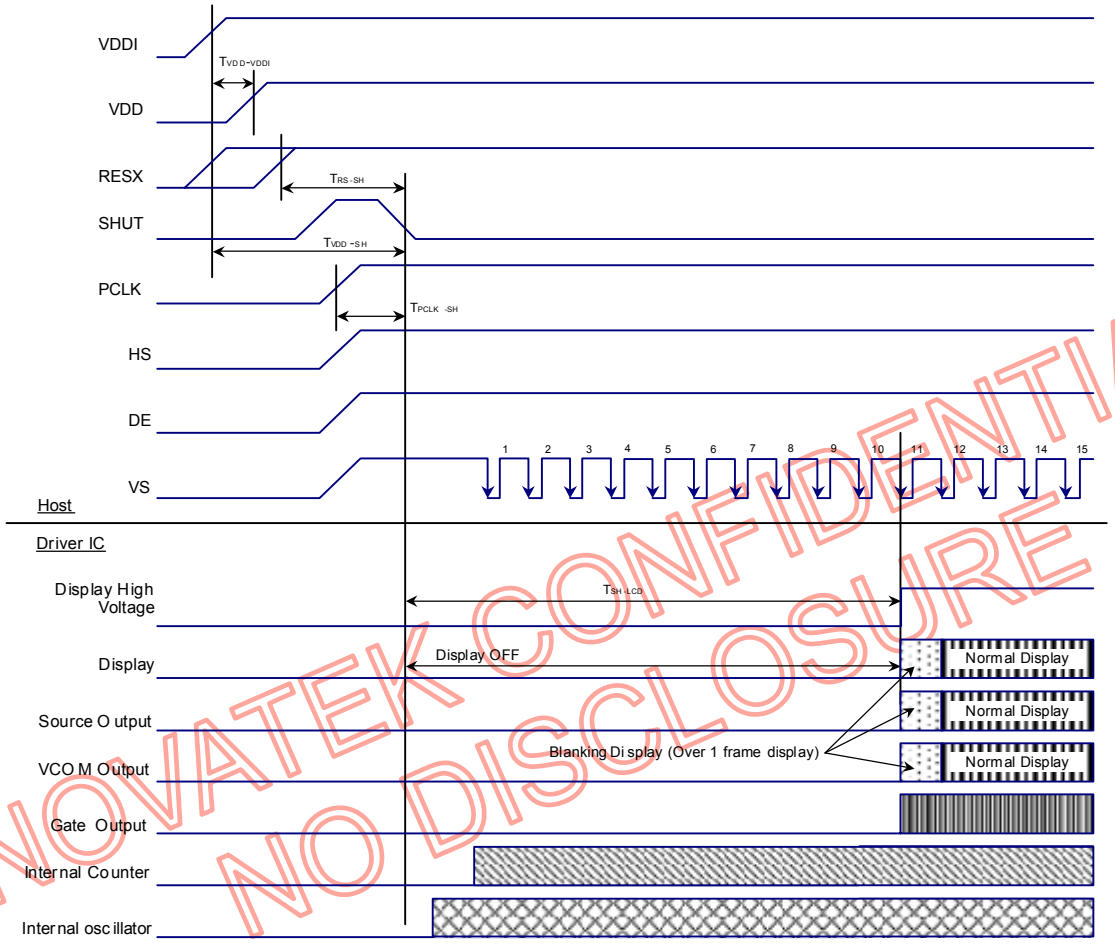


Fig. 7.4.5. 5 Power On Sequence on RGB Mode 2

Table 7.4.5.1 Power ON AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDDI On to VDD On	$T_{VDDI-VDD}$	0			ns	Note1
VDDI/VDD on to falling edge of SHUT	T_{VDD-SH}	1			ms	
RESX to falling of SHUT	T_{RS-SH}	10			us	
Signals input to falling edge of SHUT *	T_{CLK-SH}	1			PCLK	Note2
Falling edge of SHUT to LCD power ON	T_{SH-LCD}			120	ms	
Falling edge of SHUT to Display start	T_{SH-ON}		10		VS	

Note 1: TVDDI-VDD can be <=0ns, >0ns. In any case, VDDI and VDD power up sequence should not have any impact on the driver / display functionalities / performance.
Note 2: Signals mean VS, HS, DE and PCLK signal.
Note 3: DP=’0’, EP=’0’, HSP=’0’ and VSP=’0’ of RGBCTR (B0h) command.

7.4.5.2 Power OFF Sequence on RGB I/F Mode 2

The Driver operates power off and display OFF by VDD, VDDI, SHUT, VS, HS and DE on RGB mode 2 as show as following figure.

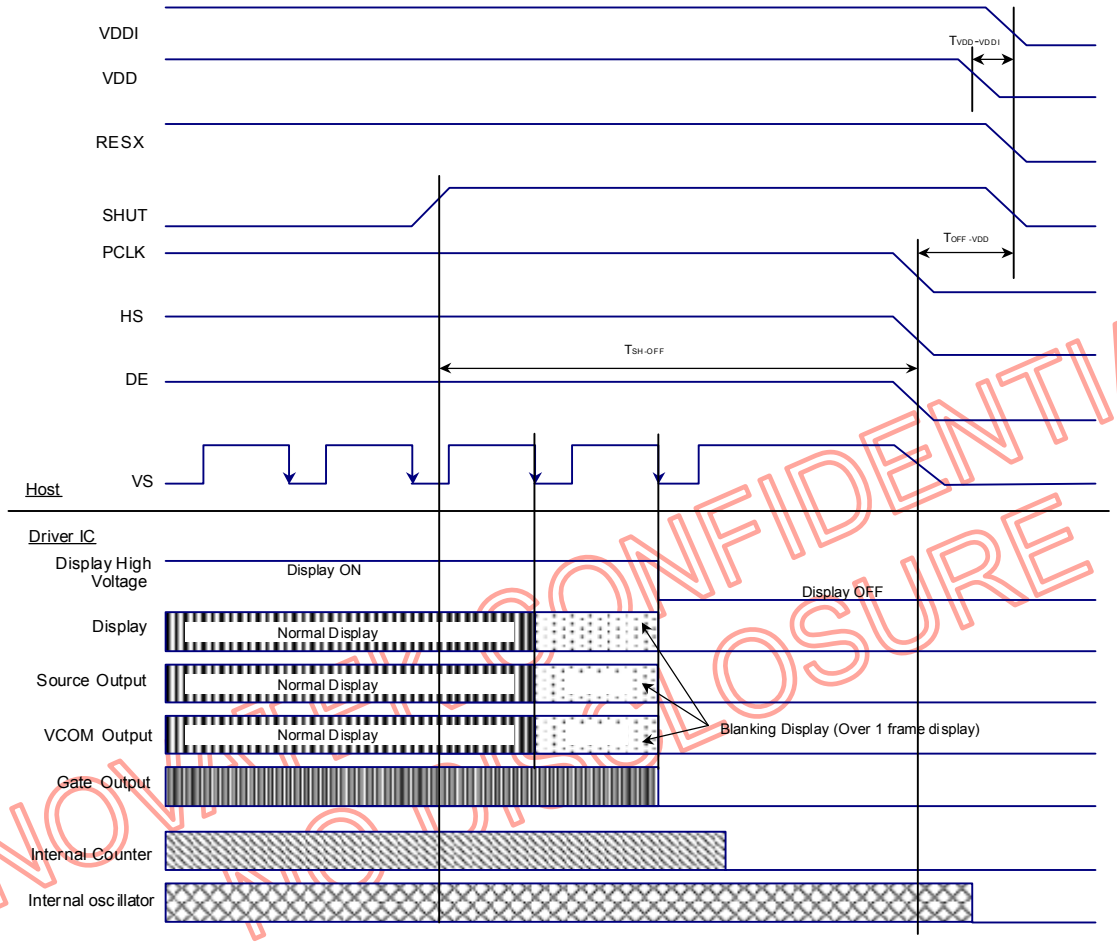


Fig. 7.4.5.6 Power OFF Seq uence on RGB M ode 2

Table 7.4.5.2 Power OFF AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDDI On to VDD On	$T_{VDDI-VDD}$	0			ns	Note1
Signals input to VDDI/VDD off	T_{SH-OFF}	1			us	Note2
Rising edge of SHUT to Display off	T_{SH-OFF}	2			VS	

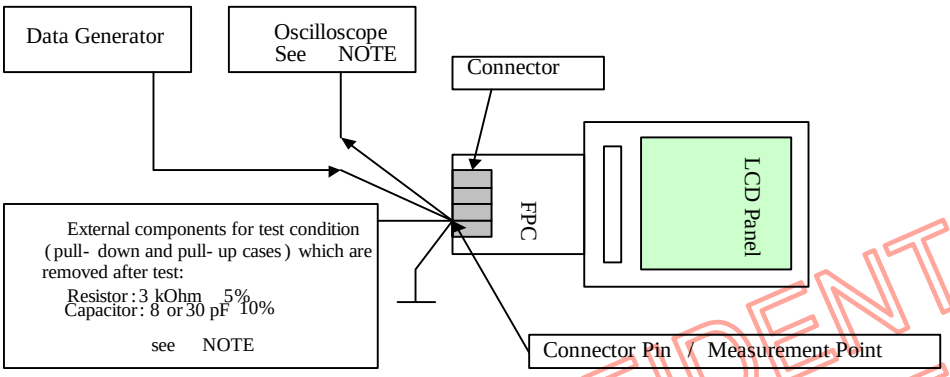
Note 1: TVDDI-VDD can be <=0ns, >0ns. In any case, VDDI and VDD power up sequence should not have any impact on the driver / display functionalities / performance.
Note 2: Signals mean VS, HS, DE and PCLK signal.
Note 3: DP=’0’, EP=’0’, HSP=’0’ and VSP=’0’ of RGBCTR (B0h) command.

7.5 Measurement Conditions

7.5.1 Parallel Interface Characteristics 24, 18, 16 or 8-bits bus (8080 & 6800-series MCU)

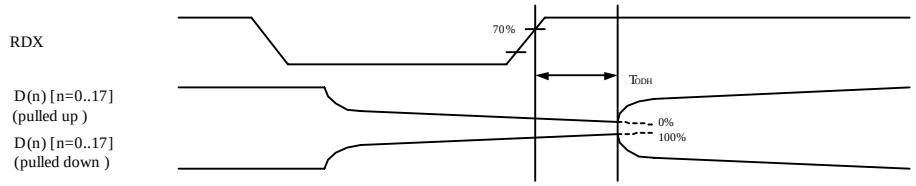
7.5.1.1 TRAT, TRATFM, TODH Measurement Condition:

7.5.1.1.1 Measurement Condition Set-up

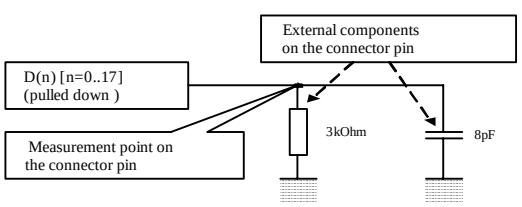


Note: Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements.

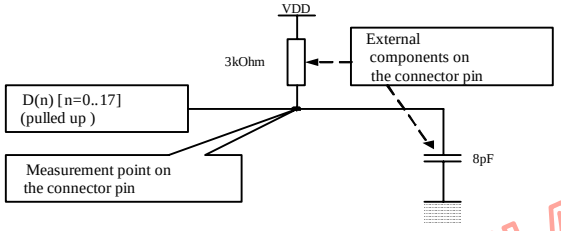
7.5.1.1.2 Minimum Value Measurement



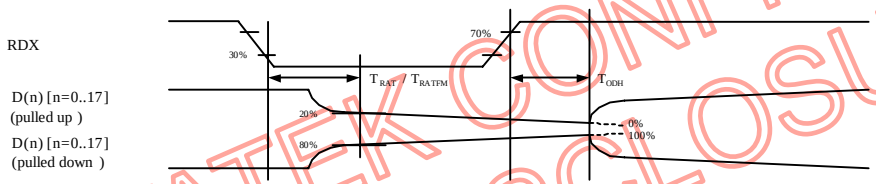
Measurement circuit pulled down



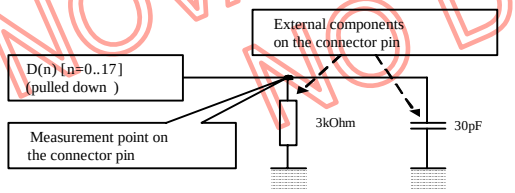
Measurement circuit pulled up



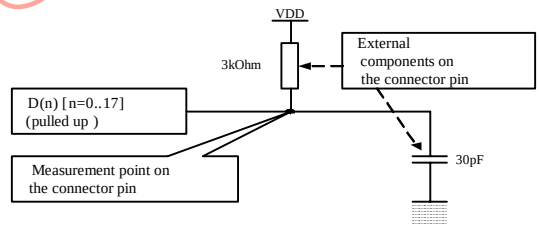
7.5.1.1.3 Maximum Value Measurement



Measurement circuit pulled down



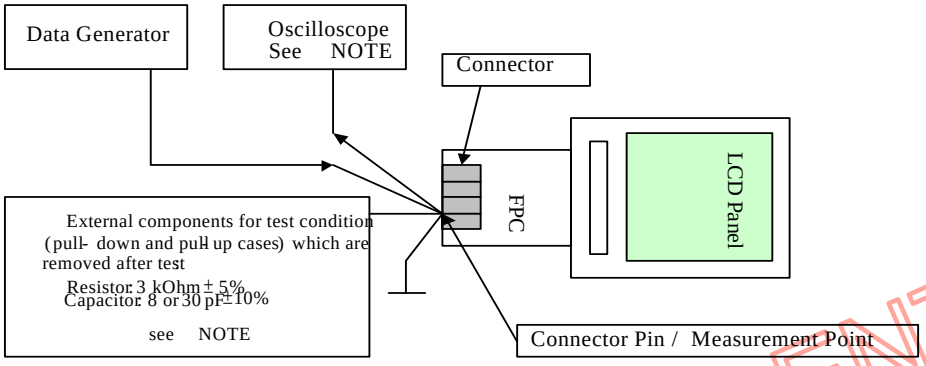
Measurement circuit pulled up



7.5.2 Serial Interface Characteristics

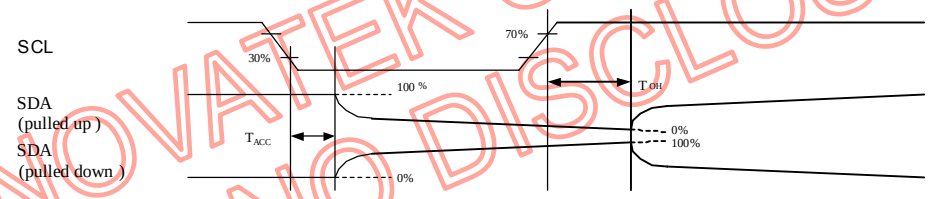
7.5.2.1 TACC, TOH Measurement Condition

7.5.2.1.1 Measurement Condition Set-up

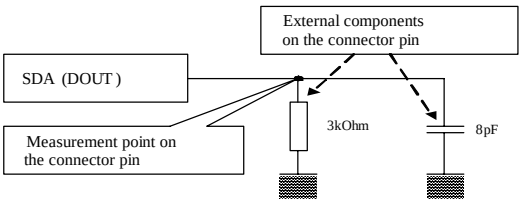


Note: Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements.

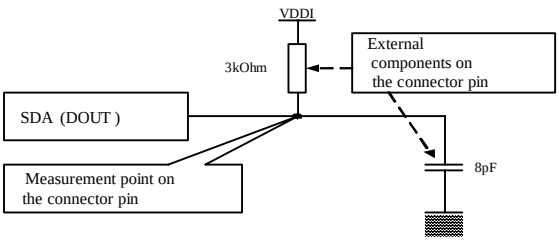
7.5.2.1.2 Minimum Value Measurement



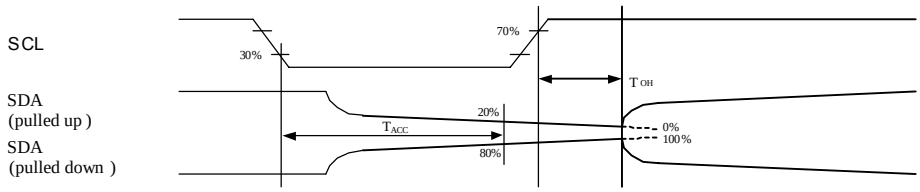
Measurement circuit pulled down



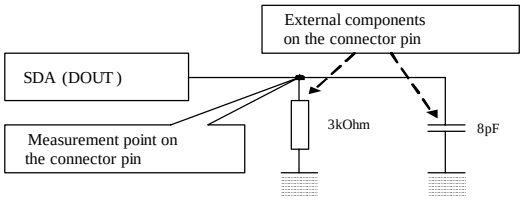
Measurement circuit pulled up



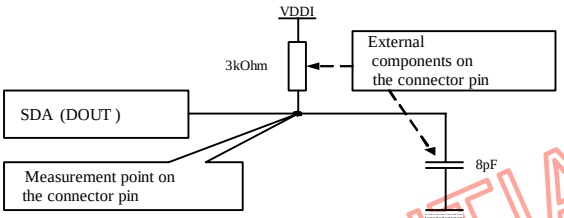
7.5.2.1.3 Maximum Value Measurement



Measurement circuit pulled down



Measurement circuit pulled up



8. Function Description

8.1 Interface Type Selection

The selection of a given interfaces are done by setting P68, IM2, IM1, and IM0 pins as show in Table 8.1.1 and Table 8.1.2.

Table 8.1.1 MCU Interface Type Selection

P68	IM2	IM1	IM0	Interface	Read back selection
-	0	-	-	Serial interface	Via the read instruction (12-bit, 16-bit and 18-bit read parameter
0	1	0	0	8080 MCU 8-bit Parallel	RDX strobe (8-bit read data and 8-bit read parameter)
0	1	0	1	8080 MCU 16-bit Parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	1	1	0	8080 MCU 9-bit Parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	1	1	1	8080 MCU 18-bit Parallel	RDX strobe (18-bit read data and 8-bit read parameter)
-	0	-	-	Serial interface	Via the read instruction (12-bit, 16-bit and 18-bit read parameter
1	1	0	0	6800 MCU 8-bit Parallel	E strobe (8-bit read data and 8-bit read parameter)
1	1	0	1	6800 MCU 16-bit Parallel	E strobe (9-bit read data and 8-bit read parameter)
1	1	1	0	6800 MCU 9-bit Parallel	E strobe (16-bit read data and 8-bit read parameter)
1	1	1	1	6800 MCU 18-bit Parallel	E strobe (18-bit read data and 8-bit read parameter)

Table 8.1.2 Pin connection According to MCU Interface Type Selection

P68	IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Read back selection
-	0	-	-	Serial interface	Note1	Note 1	SCL	D[17:1]: Unused, D0: SDA
0	1	0	0	8080 MCU 8-bit Parallel	RDX	WRX	D/CX	D[17:8]: Unused, D7-D0: 8-bit Data
0	1	0	1	8080 MCU 16-bit Parallel	RDX	WRX	D/CX	D[17:16]: Unused, D15-D0: 16-bit Data
0	1	1	0	8080 MCU 9-bit Parallel	RDX	WRX	D/CX	D[17:9]: Unused, D8-D0: 9-bit Data
0	1	1	1	8080 MCU 18-bit Parallel	RDX	WRX	D/CX	D17-D0: 18-bit Data
-	0	-	-	Serial interface	Note1	D/CX	SCL	D[17:1]: Unused,D0:SDA
1	1	0	0	6800 MCU 8-bit Parallel	E	WRX	RS	D[17:8]: Unused,D7-D0:8-bit Data
1	1	0	1	6800 MCU 16-bit Parallel	E	WRX	RS	D[17:16]: Unused, D15-D0: 16-bit Data
1	1	1	0	6800 MCU 9-bit Parallel	E	WRX	RS	D[17:9]: Unused,D8-D0:9-bit Data
1	1	1	1	6800 MCU 18-bit Parallel	E	WRX	RS	D17-D0: 18-bit Data

Note 1. Unused pins connect to DGND or VDDI level.

8.2 8080-Series Parallel Interface (P68='0')

The MCU uses a 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.
The Graphics Controller Chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.
The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is low state (DGND). Interface bus width can be selected with IM2, IM1 and IM0. The interface function of 8080-series parallel interface are given in Table 8.2.1

Table 8.2.1 The function of 8080-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
0	1	0	0	8-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	↑	1	Read 8-bit Display data (D7 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	0	1	16-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 16-bit display data or 8-bit parameter (D15 to D0)
					1	↑	1	Read 16-bit Display data (D15 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	1	0	9-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 9-bit display data or 8-bit parameter (D8 to D0)
					1	↑	1	Read 9-bit Display data (D8 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	1	1	18-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 18-bit display data or 8-bit parameter (D17 to D0)
					1	↑	1	Read 18-bit Display data (D17 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh.

8.2.1 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=’0’) and vice versa it is data (=’1’)

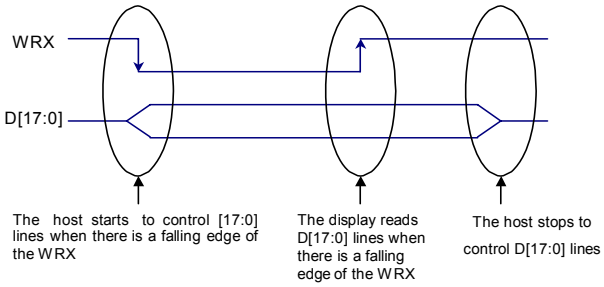


Fig. 8.2.1 8080-Series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped)

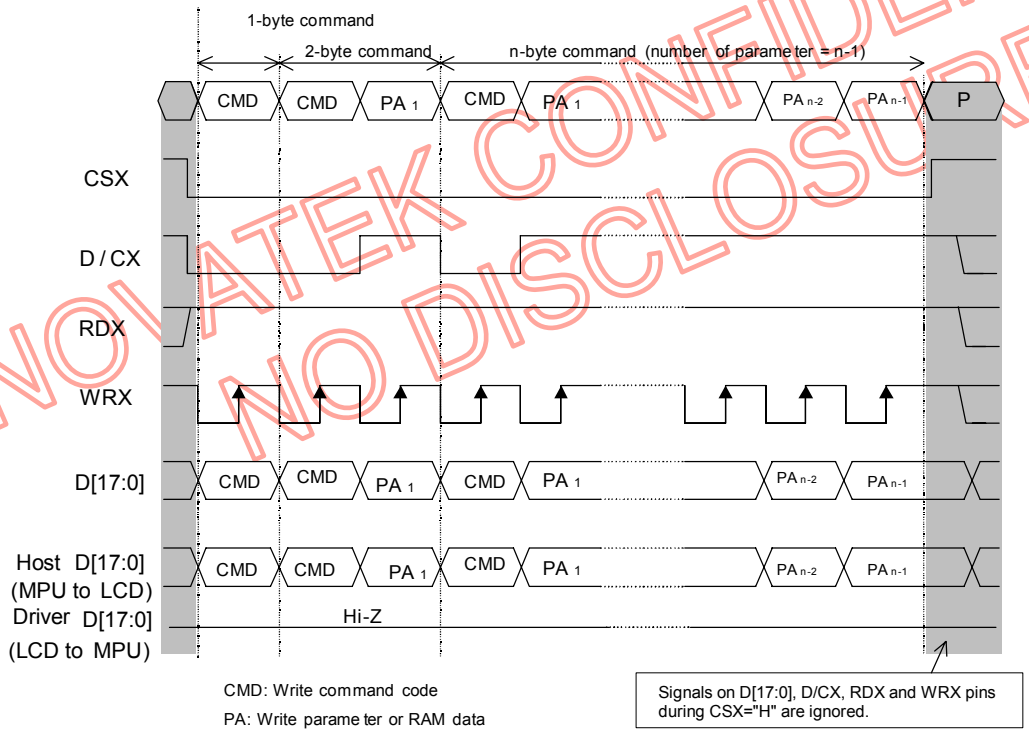


Fig. 8.2.2 8080-Series Parallel bus protocol (write to register or display RAM)

8.2.2 Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

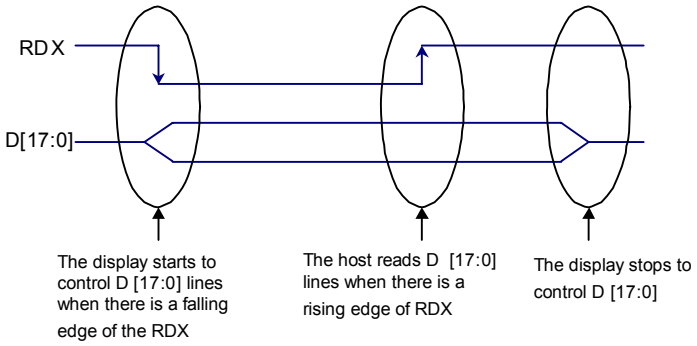


Fig. 8.2.3 8080-Series RDX Protocol

Note: RDX is an unsynchronized signal (It can be stopped)

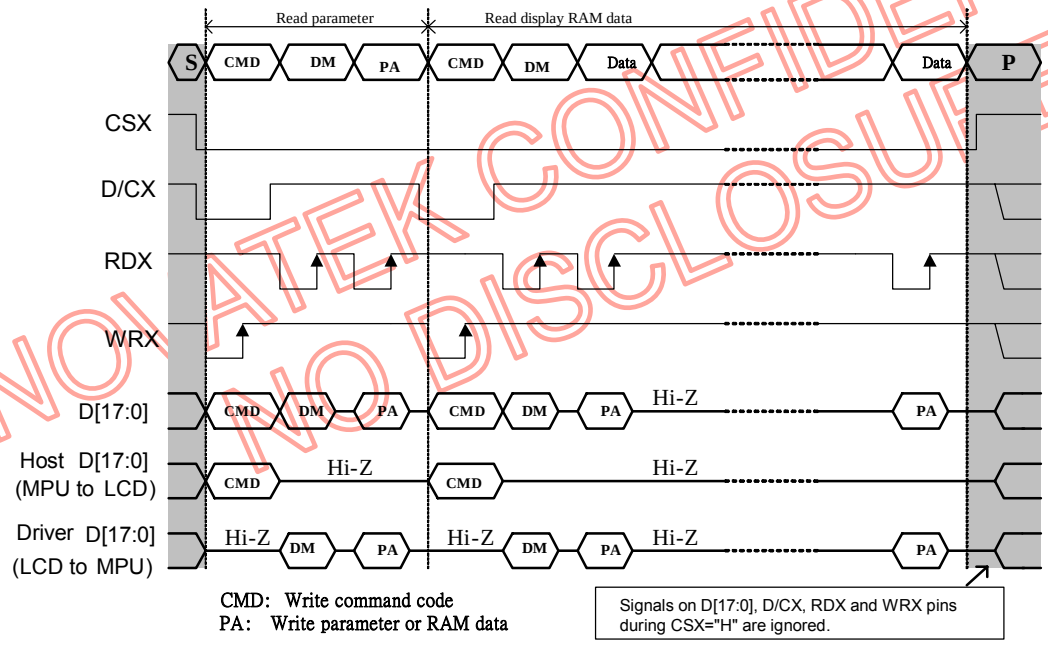


Fig. 8.2.4 8080-Series Parallel bus protocol (Read from register or display RAM)

8.3 6800-Series Parallel Interface (P68='1')

The MCU uses a 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data.
The Graphics Controller Chip reads the data at the falling edge of E signal when R/WX= '1' and Writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C= '0', D[17:0] bits are commands.
The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is high state (VDDI). Interface bus width can be selected with IM2, IM1 and IM0. The interface functions of 6800-series parallel interface are given in Table 8.3.1.

Table 8.3.1 The function of 6800-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	R/WX	E	Function
1	1	0	0	8-bit interface	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	1	↓	Read 8-bit display data (D7 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	0	1	16-bit interface	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 16-bit display data or 8-bit parameter (D15 to D0)
					1	1	↓	Read 16-bit display data (D15 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	1	0	9-bit interface	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 9-bit display data or 8-bit parameter (D8 to D0)
					1	1	↓	Read 9-bit display data (D8 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	1	1	18-bit interface	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 18-bit display data or 8-bit parameter (D17 to D0)
					1	1	↓	Read 18-bit display data (D17 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh.

8.3.1 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

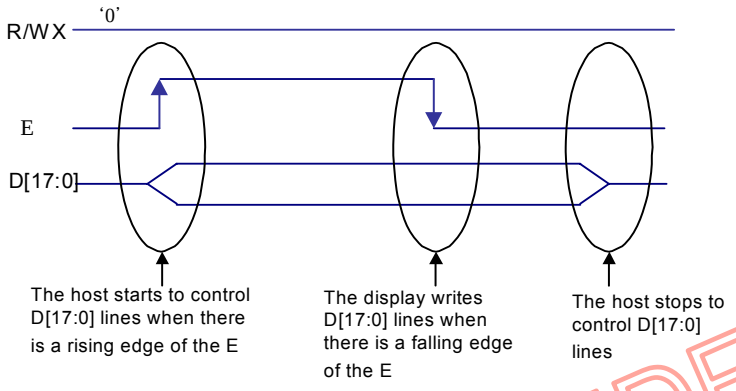


Fig. 8.3.1 6800-Series Write Protocol

Note: E is an unsynchronized signal (It can be stopped)

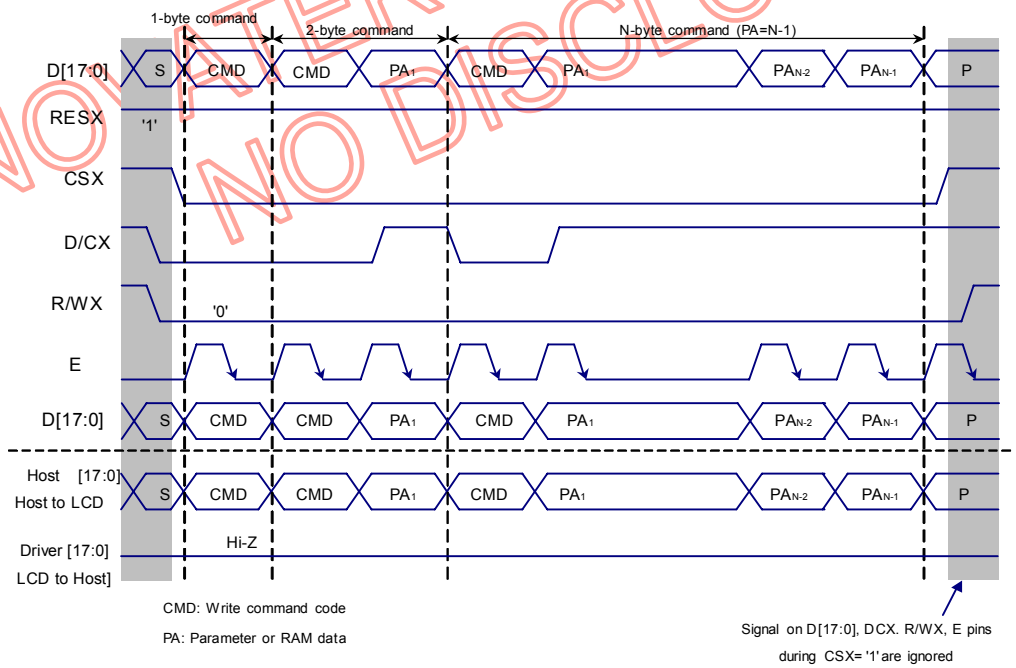


Fig. 8.3.2 6800-Series parallel bus protocol, Write to register or display RAM

8.3.2 Read cycle sequence

The write cycle means that the host reads information (command or/and data) to the display via the interface. Each read cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data ('1').

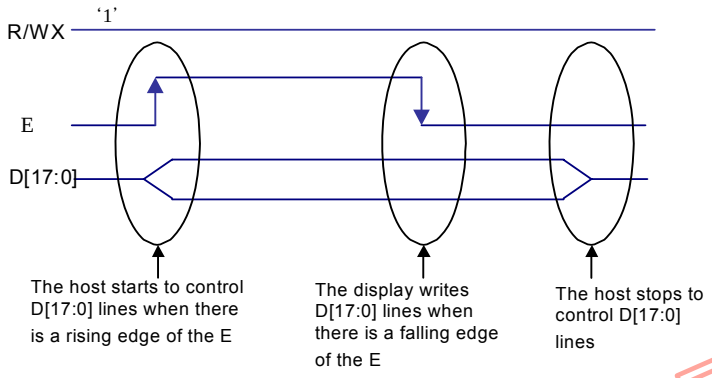


Fig. 8.3.3 6800-Series Read Protocol

Note: E is an unsynchronized signal (It can be stopped)

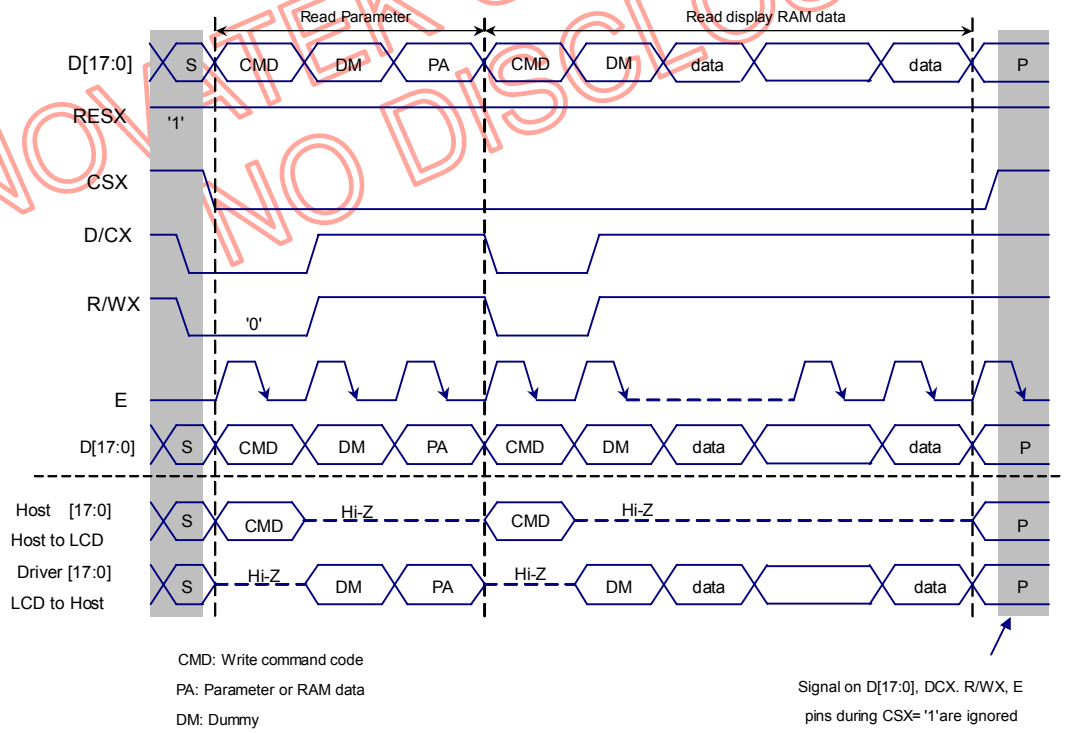


Fig. 8.3.4 6800-Series parallel bus protocol, Read data from register or display RAM

8.4 Serial Interface

The selection of this interface is done by IM2. See the Table 8.4.1.

Table 8.4.1 Serial Interface Type Selection

IM2 (IF_SELECT)	4WSPI	Interface	Read back selection
0	0	3-Pins Serial interface	Via the read instruction (8-bits, 24-bits and 32-bits read parameter
0	1	4-Pins Serial interface	Via the read instruction (8-bits, 24-bits and 32-bits read parameter

The serial interface is a 3-pins/ 9-bits or 4-pins/ 8-bts bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pins serial use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output) and the 4-pins serial use: CSX (chip enable), D/CX (data/ command select), SCL (serial clock) and SDA (serial data input/output) Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

8.4.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-Pins serial data packet contains a control bit D/CX and a transmission byte and in 4-pins serial case, data packet contains just transmission byte and control bit D/CX is transfrerred by the D/CX pin.. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the DRIVER. The MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

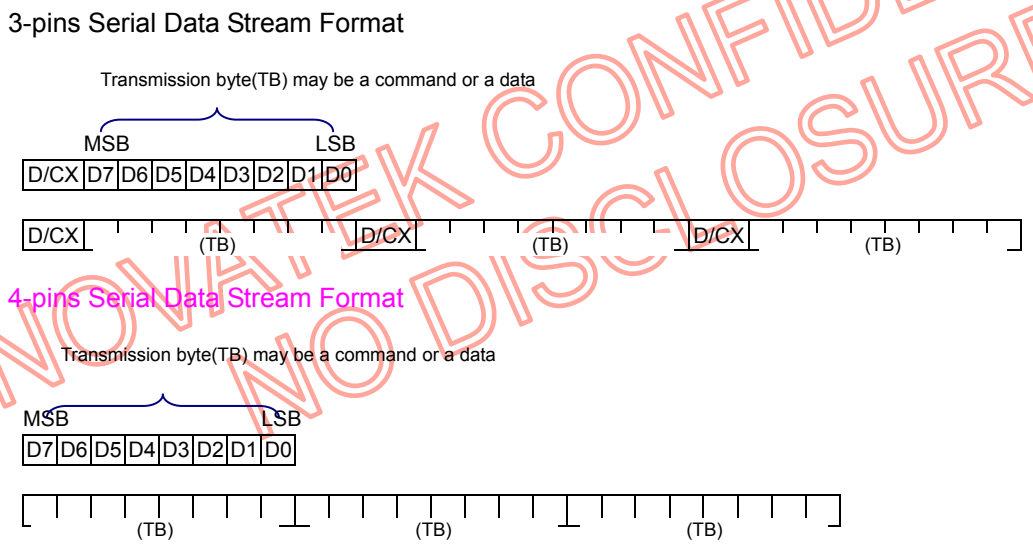


Fig. 8.4.1.1 Serial interface data Stream format

When CSX is “high”, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low (see *Fig 6.1.1.2*). SDA is sampled at the rising edge of CSX. D/CX indicates, whether the byte is command code (D/CX=’0’) or parameter/RAM data (D/CX=’1’). It is sampled when first rising edge of SCL (3-pin serial interface) or 8th rising edge of SCL (4-pins serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-pin serial interface) or D7 (4-pins serial interface) of the next byte at the next rising edge of SCL.

3-pins Serial Interface Protocol

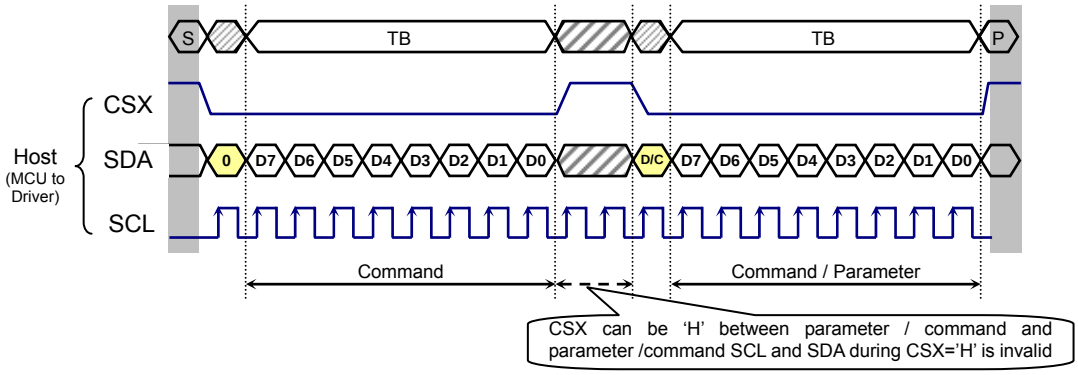


Fig. 8.4.1.2 3-pins Serial interface Write protocol (Write to register with control bit in

4-pins Serial Interface Protocol

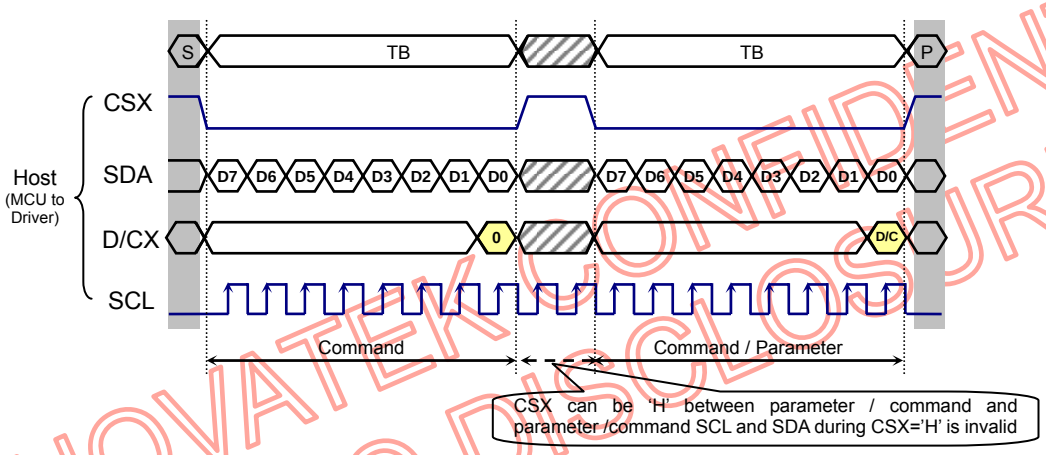
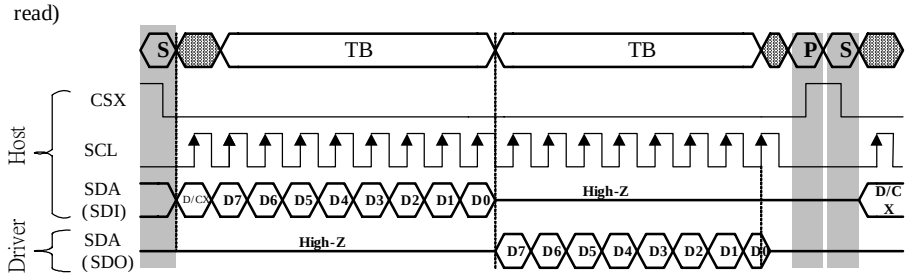


Fig. 8.4.1.3 4-pins Serial interface Write protocol (Write to register with control bit in

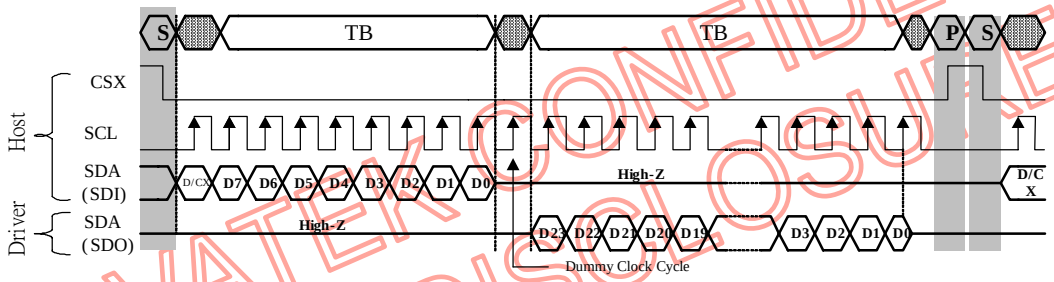
8.4.2 Read Functions

The read mode of the interface means that the micro controller reads register value from the Driver. To do the micro controller first has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

3- Pin Serial Protocol(for RDID1/ RDID2/ RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0 Fh command: 8- bit read)



3- Pin Serial Protocol(for RDDID command: 24- bit read)



3- Pin Serial Protocol(for RDDST command : 32- bit read)

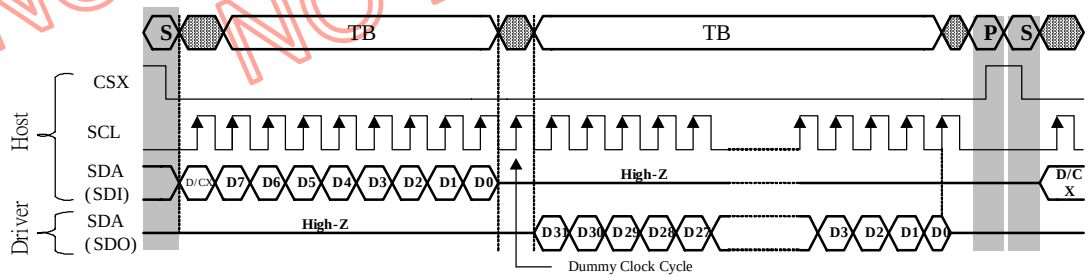
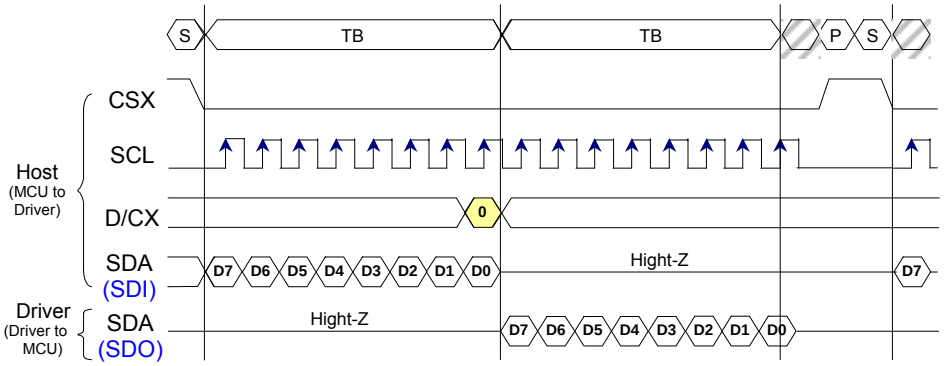
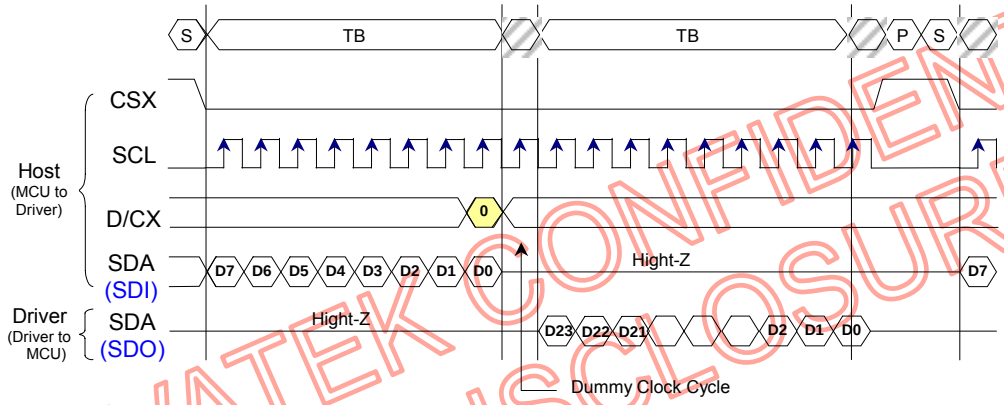


Fig. 8.4.2.1 3-pin Serial interface Read protocol

4-pins Serial Protocol (for RDID1/ RDID2/ RDID3/ 0AH/ 0BH/ 0CH/ 0DH/ 0EH/ 0FH command: 8-bits read)



4-pins Serial Protocol (for RDID command: 24 -bits read)



4-pins Serial Protocol (for RDST command: 32 -bits read)

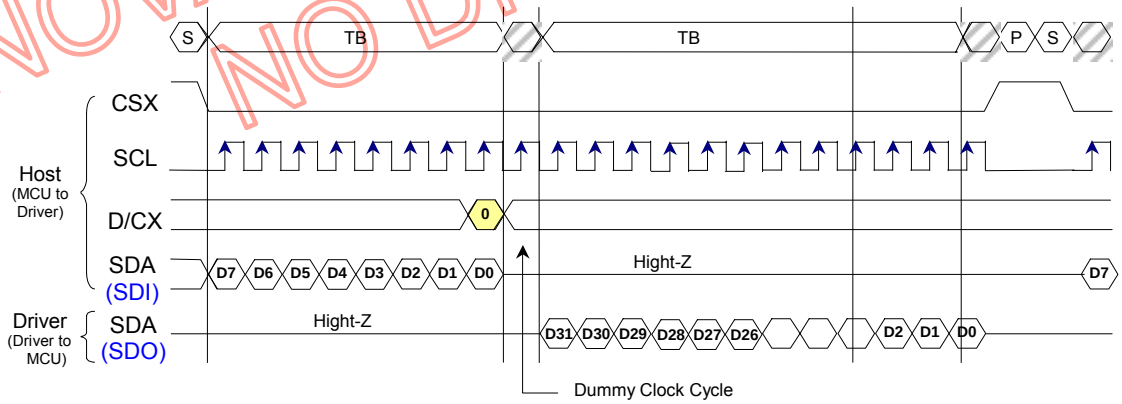


Fig. 8.4.2.2 4-pin Serial interface Read protocol

8.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example

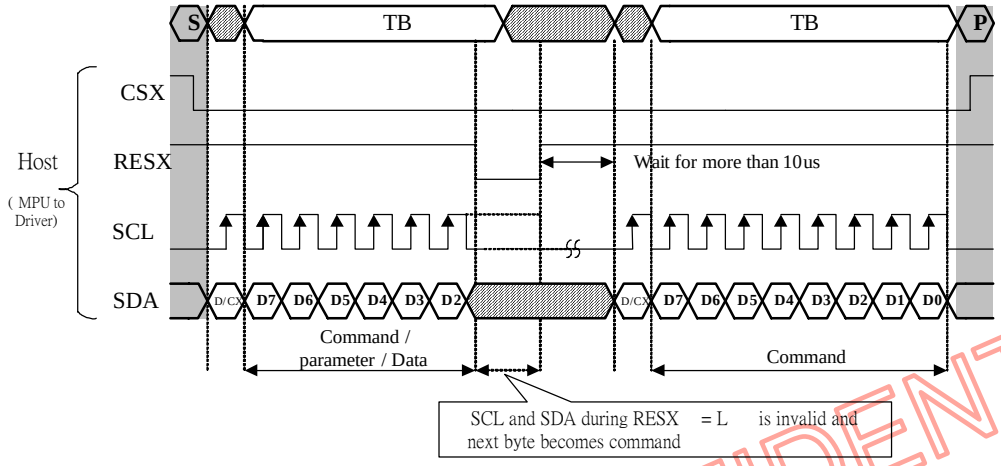


Fig. 8.5.1 Serial bus protocol, write mode – interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

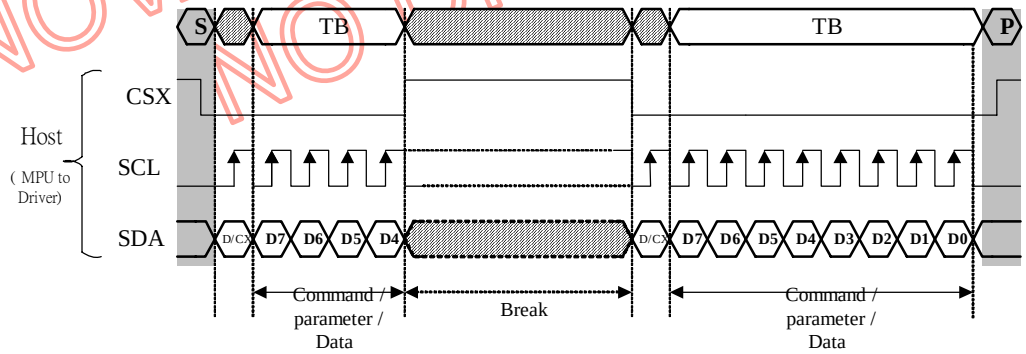


Fig. 8.5.2 Serial bus protocol, write mode – interrupted by CSX

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

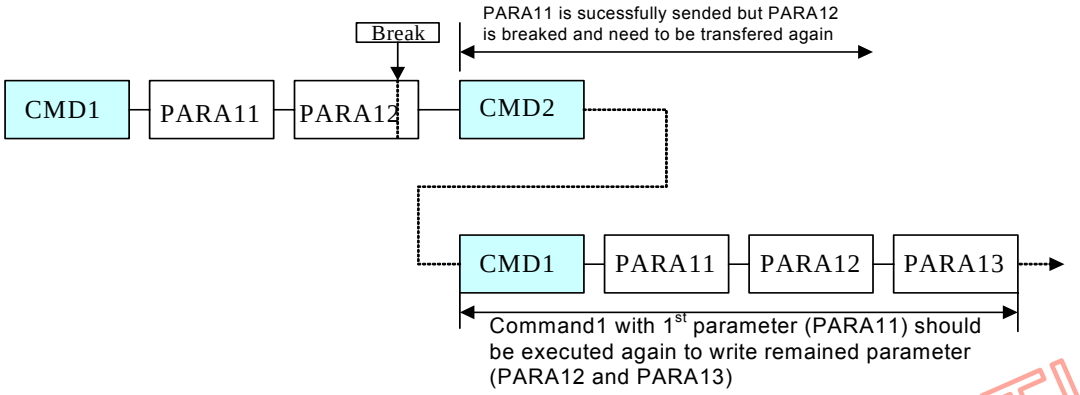


Fig.8.5.3 Write interrupts recovery (serial interface)

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

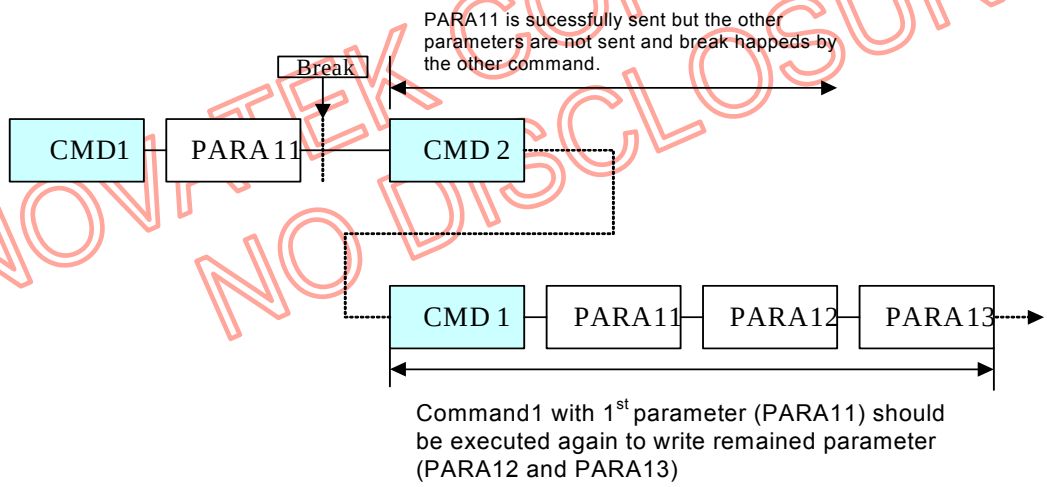


Fig. 8.5.4 Write interrupts recovery (both serial and parallel interface)

8.6 Data Transfer Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then DRIVER will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command 's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

8.6.1 Serial Interface Pause

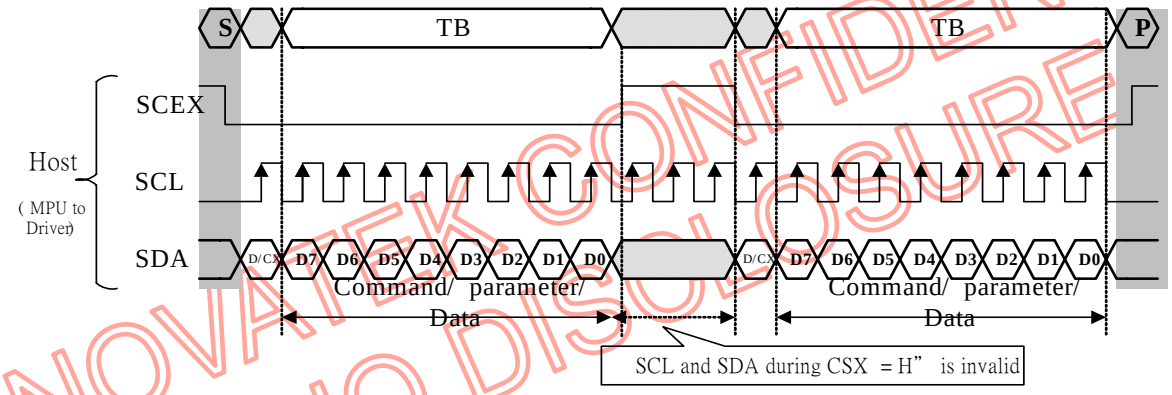


Fig. 8.5.5 Serial interface Pause Protocol (pause by CSX)

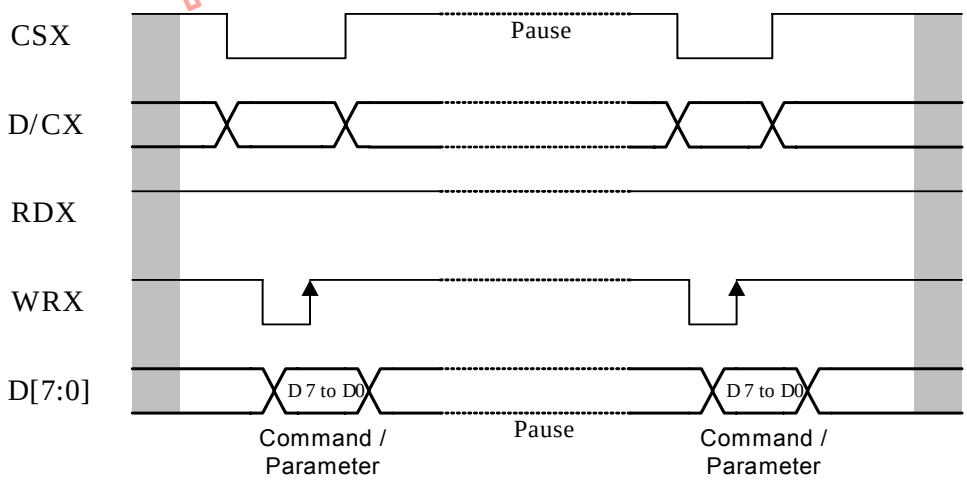


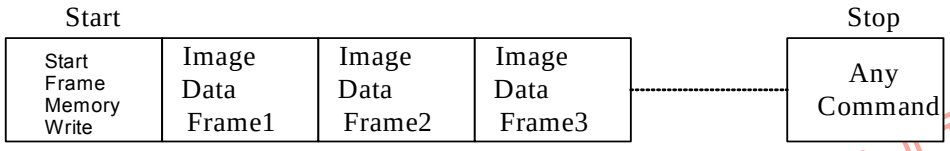
Fig. 8.5.6 Parallel bus Pause Protocol (paused by CSX)

8.7 Data Transfer Modes

The Module has three kinds colour modes for transferring data to the display RAM. These are 12-bit colour per pixel, 16-bit colour per pixel and 18-bit colour per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

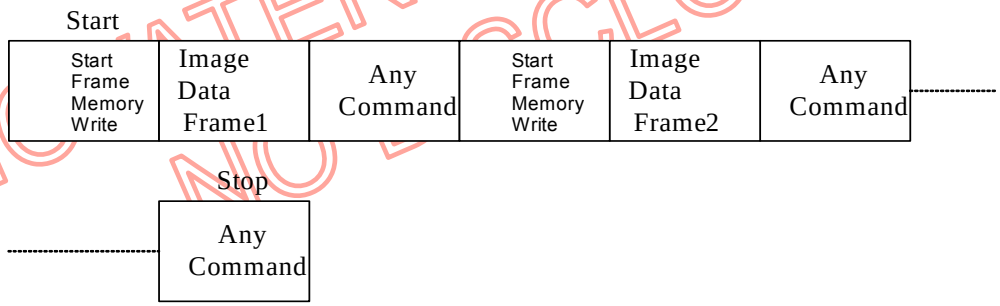
8.7.1 Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written



8.7.2 Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note:

1) These apply to all Data Transfer Color modes on both Serial and Parallel interfaces.

2) The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

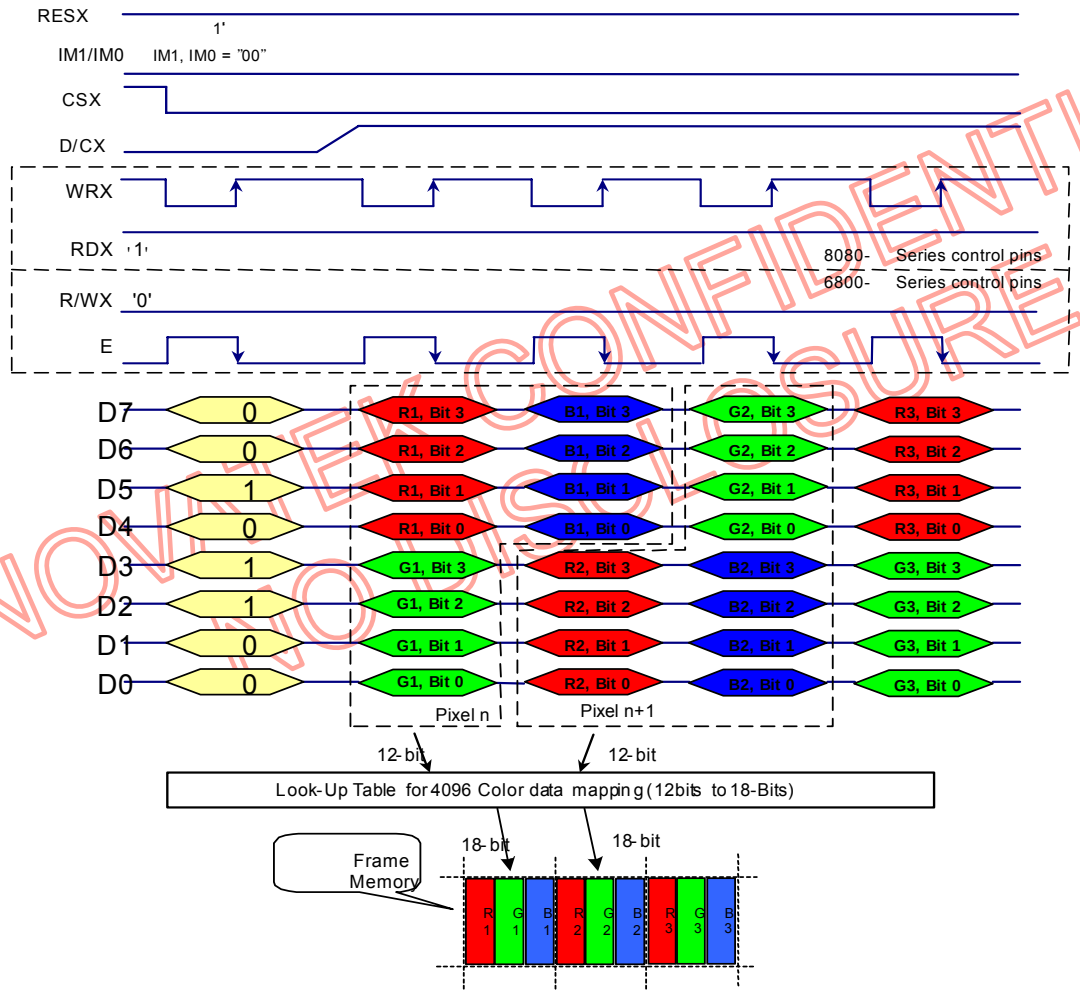
8.8 Data Colour Coding

8.8.1 8-Bits Parallel Interface (IM2='1', IM1, IM0= "00")

Different display data formats are available for three Colours depth supported by listed below.
- 4k Colours, RGB 4,4,4-bits input,
- 65k Colours, RGB 5,6,5-bits input, .
- 262k Colours, RGB 6,6,6-bits input,

8.8.1.2 Write 8-bit data for RGB 4-4-4-bits input

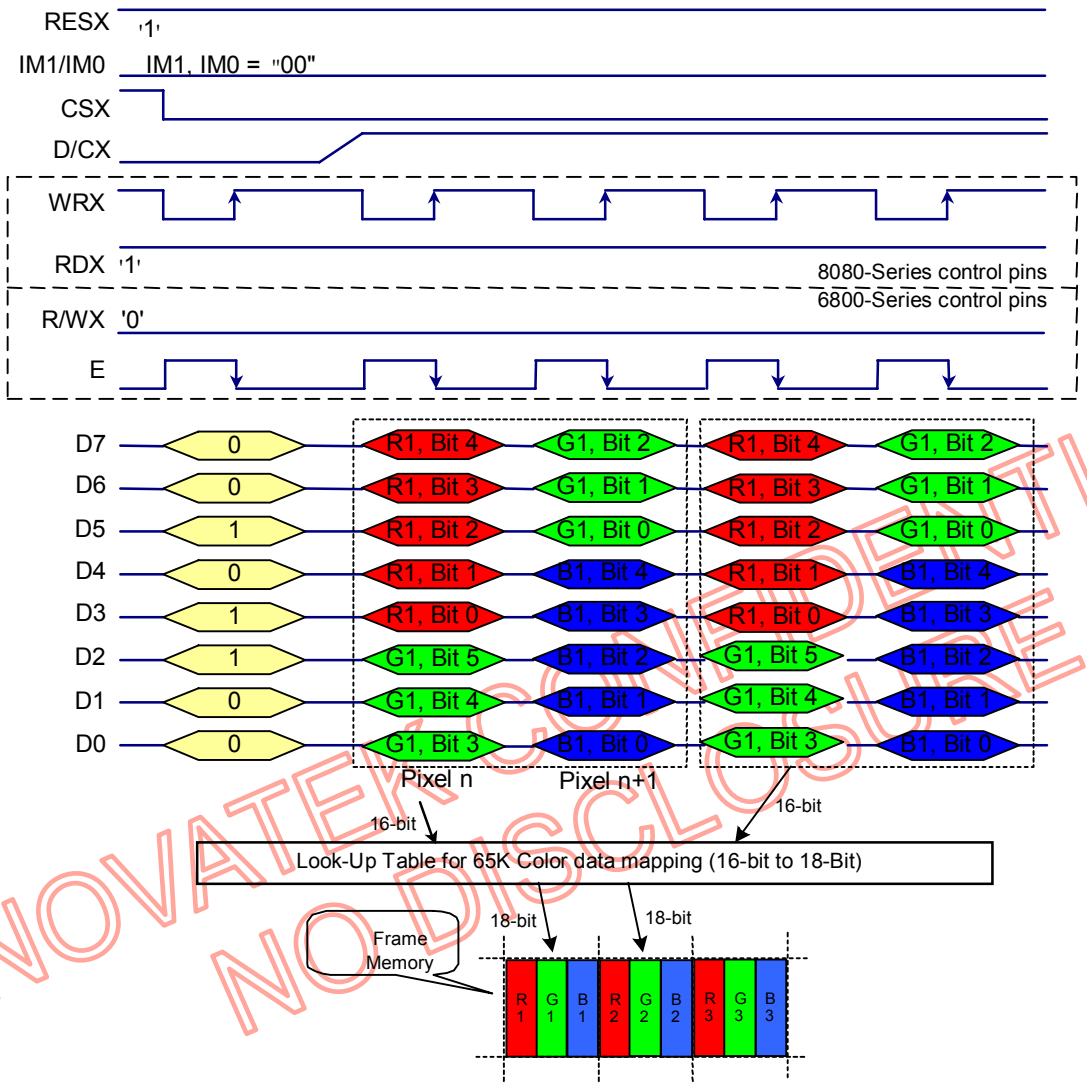
There are 2 pixels (6 sub-pixels) per 3-transfer.



Note 1. The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2. 3-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.
Note 3. '-' = Don't care - Can be set to '0' or '1'

8.8.1.3 Write 8-bits data for RGB 5-6-5-bits input

There is 1 pixel (3 sub-pixels) per 2- transfer.



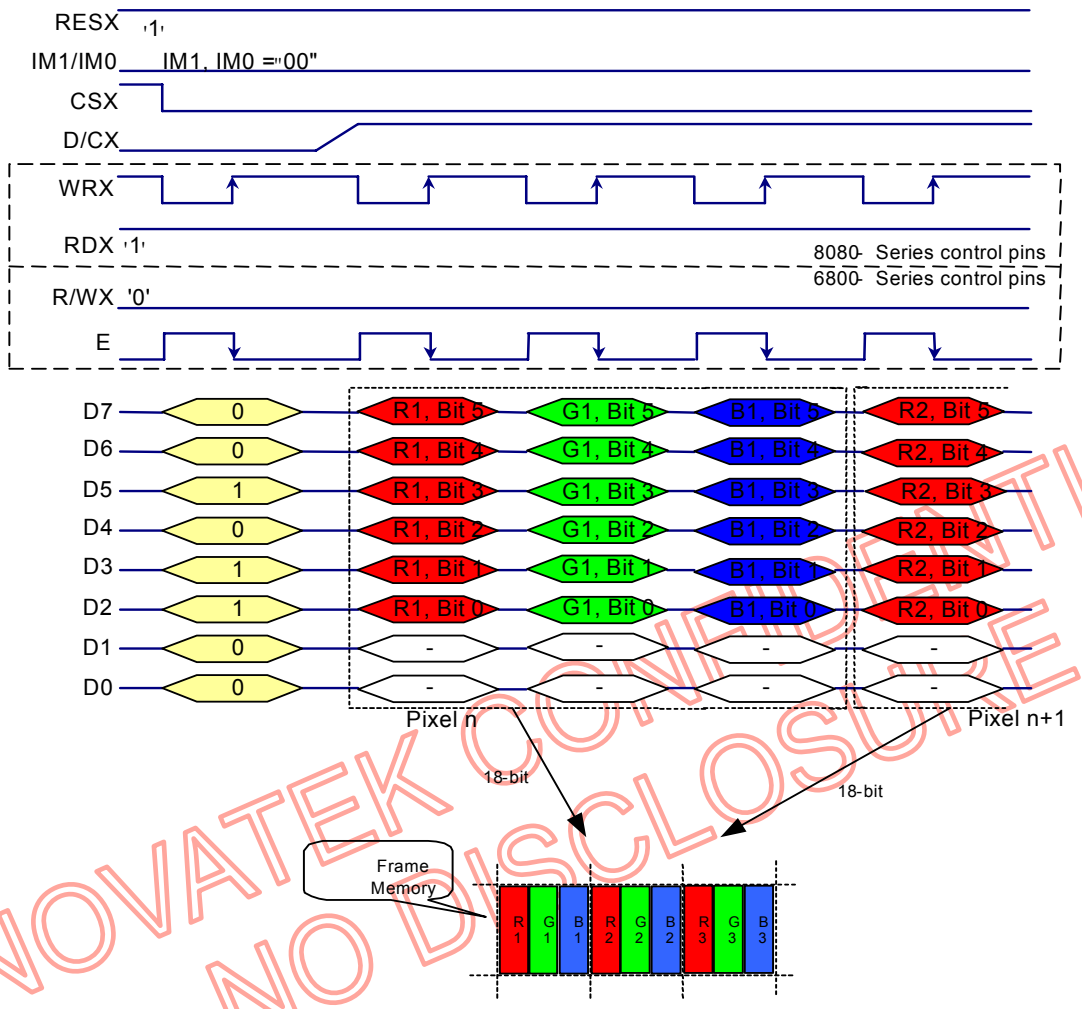
Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

8.8.1.4 Write 8-bit data for RGB 6-6-6-bits input

There is 1 pixel (3 sub-pixels) per 3- transfer.



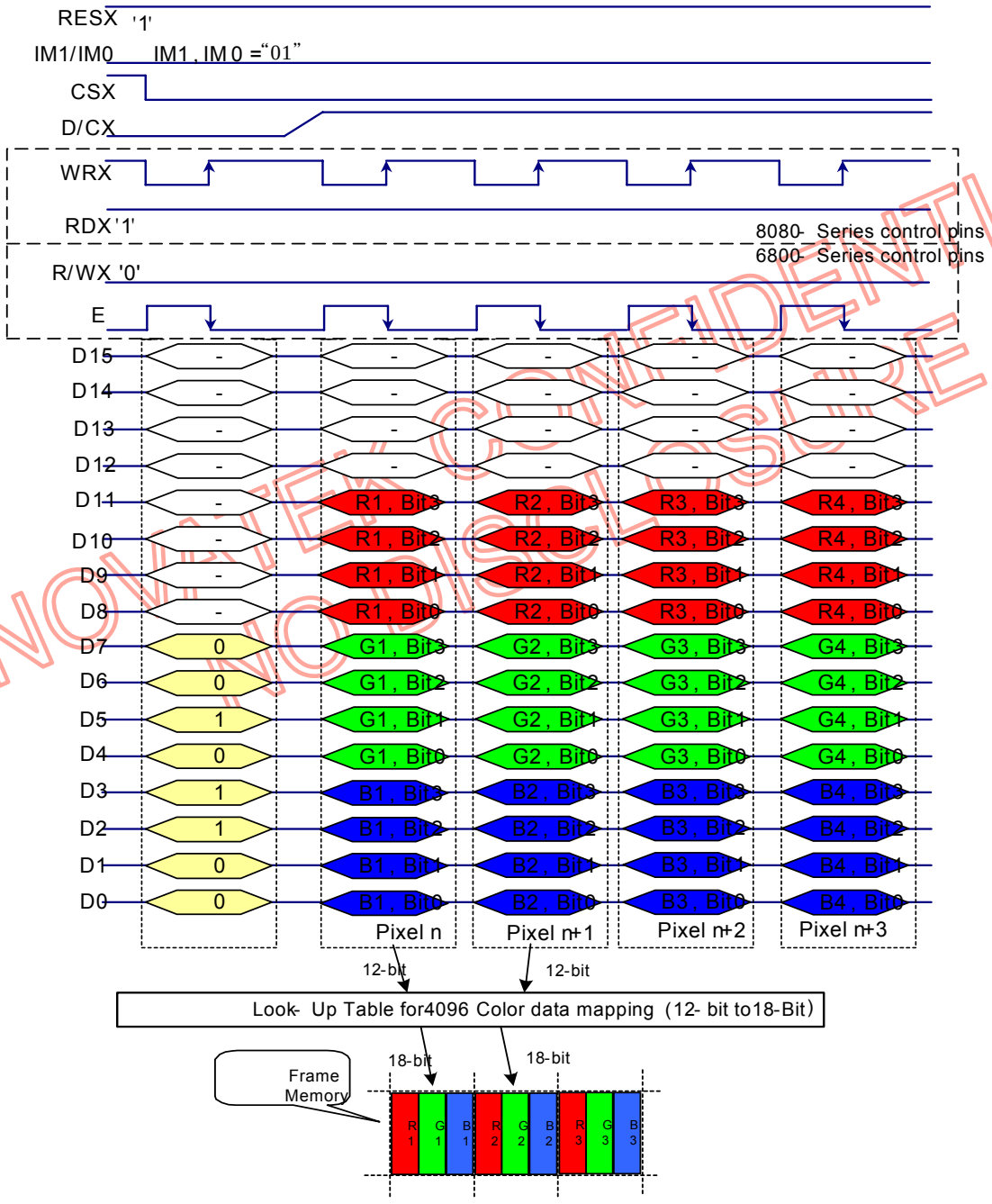
Note 1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2. 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3. '-' = Don't care - Can be set to '0' or '1'

8.8.2 16-Bit Parallel Interface (IM2='1', IM1, IM0="01")

Different display data formats are available for three colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bits input
- 65k colors, RGB 5,6,5-bits input
- 262k colors, RGB 6,6,6-bits input

8.8.2.2 Write 16-bit data for RGB 4-4-4-bits input (4k-color)

There is 1 pixel (3 sub-pixels) per 1-transfer, 12-bits/pixel.



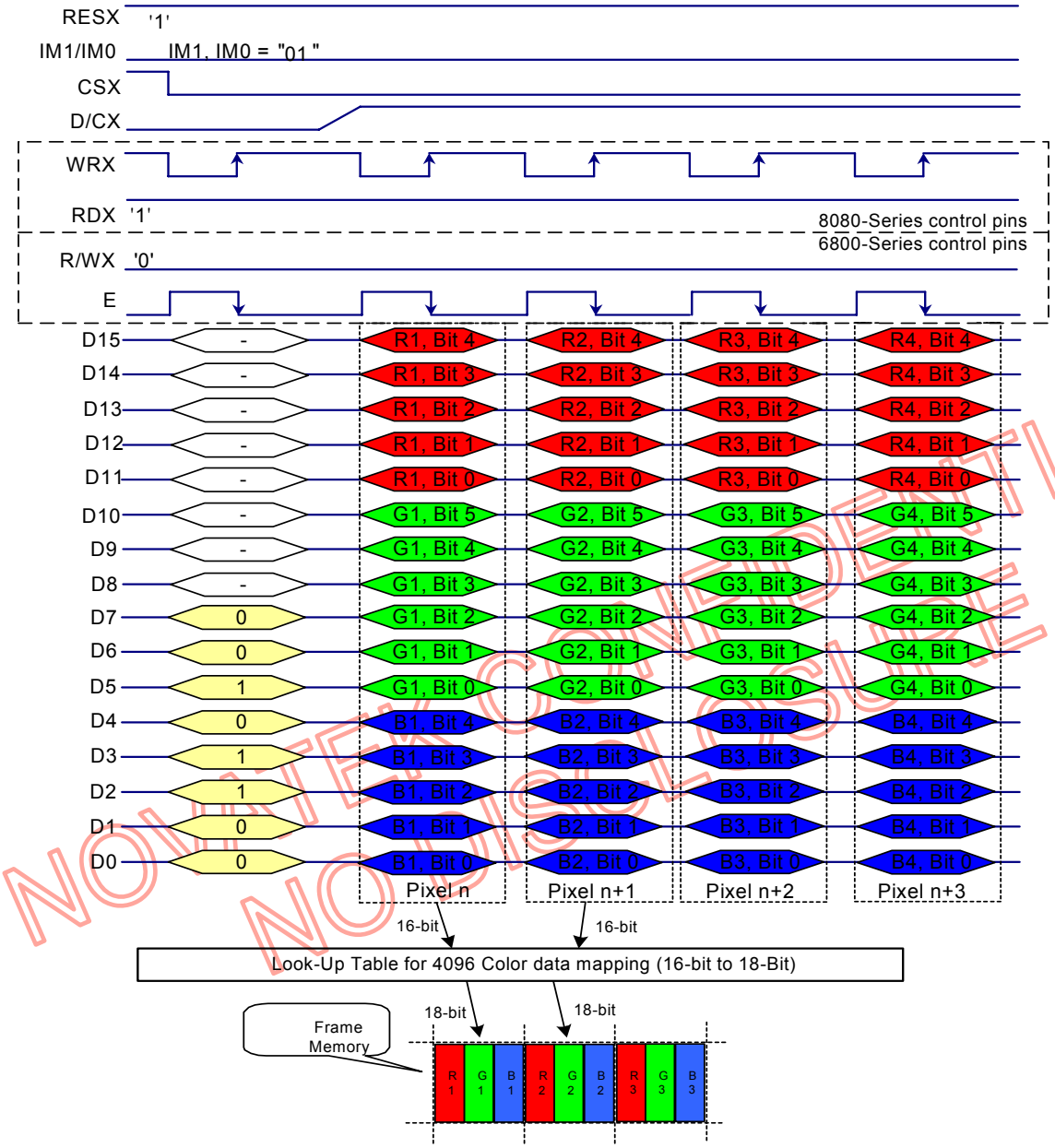
Note 1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red and Green and MSB=Bit 3, LSB=Bit 0 for Blue data.

Note 2. 1-times transfer (D7 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

8.8.2.3 Write 16-bit data for RGB 5-6-5-bits input (65k-color)

There is 1 pixel (3 sub-pixels) per 1-transfer, 16-bits/pixel.



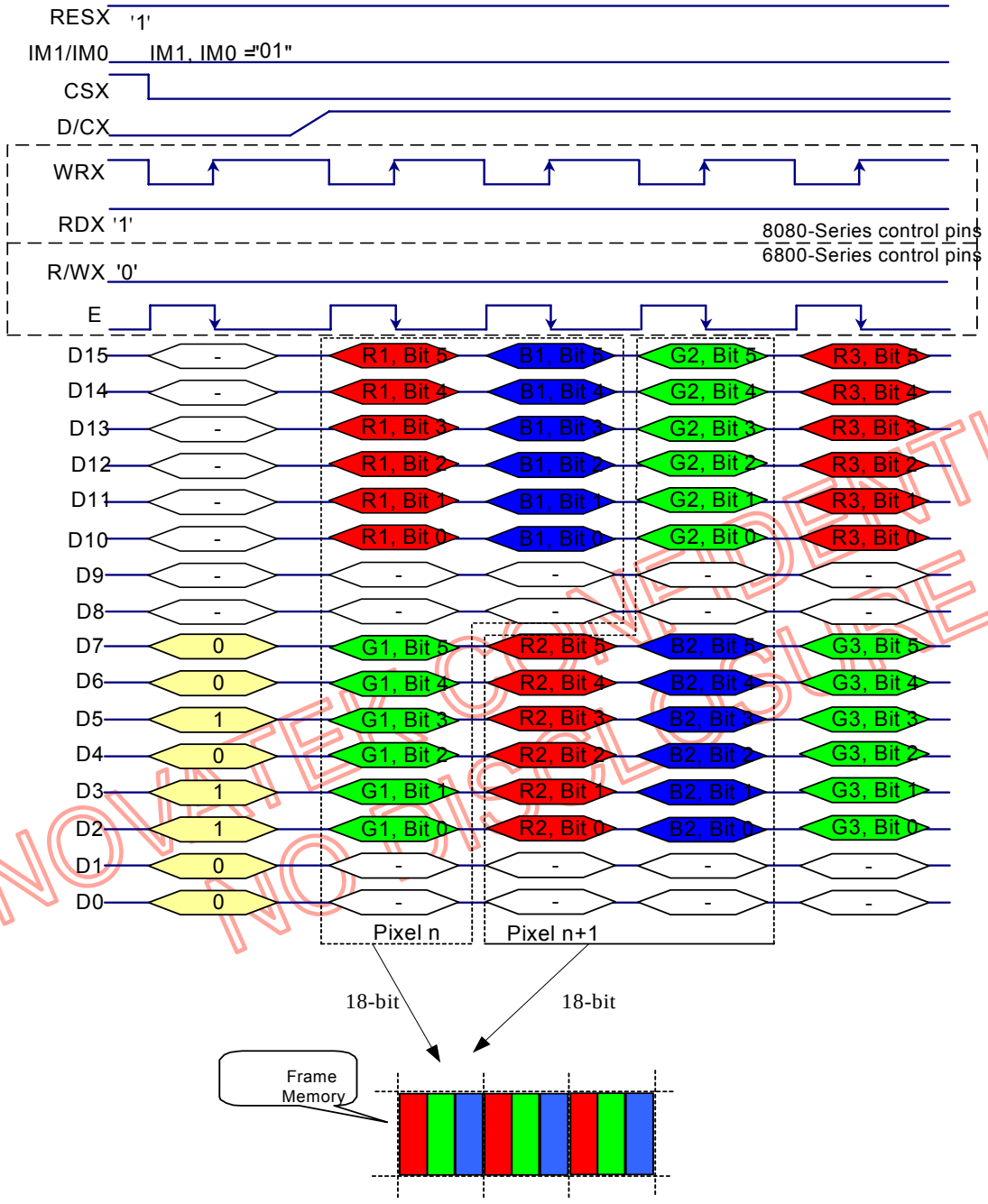
Note 1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red and Blue and MSB=Bit 5, LSB=Bit 0 for Green data.

Note 2. 1-times transfer (D7 to D0) is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

8.8.2.4 Write 16-bit data for RGB 6-6-6-bits input (262k-color)

There are 2 pixels (6 sub-pixels) per 3-transfer, 18-bit/pixel



Note 1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 2, LSB=Bit 0 for Read and Green and MSB=Bit 1, LSB=Bit 0 for Blue data.

Note 2. 1-times transfer (D7 to D0) is used to transmit 1 pixel data with the 8-bit color depth information.

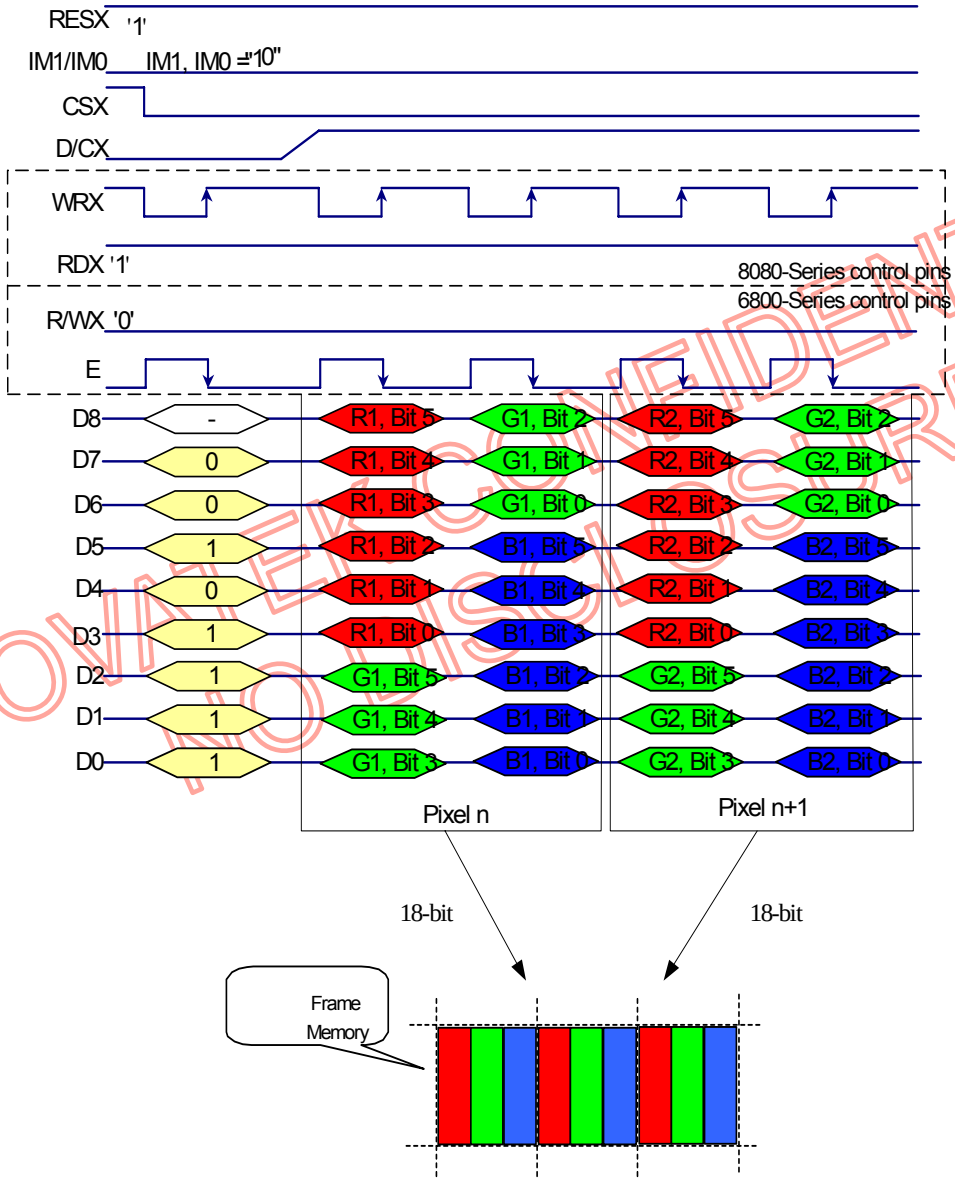
Note 3. '-' = Don't care - Can be set to '0' or '1'

8.8.3 9-Bit Parallel Interface (IM2='1', IM1, IM0="10")

Different display data formats are available for three colors depth supported by listed below.
- 262k colors, RGB 6,6,6-bits input

8.8.3.1 Write 9-bit data for RGB 6-6-6-bits input (262k-color)

There are 2 pixels (6 sub-pixels) per 4-transfer, 18-bits/pixel.



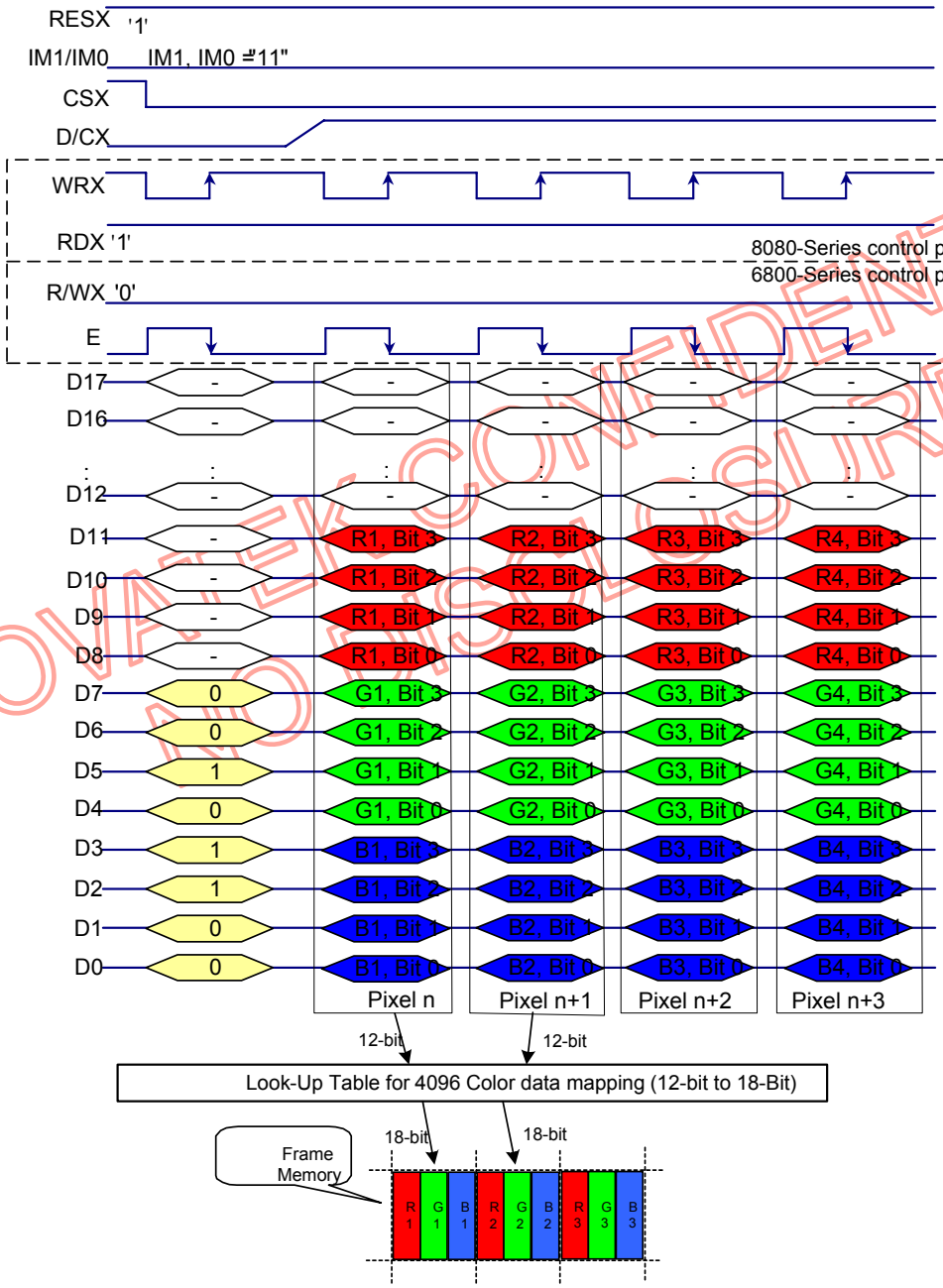
Note 1. The data order is ad follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2. 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3. '-' = Don't care - Can be set to '0' or '1'

8.8.4 18-Bit Parallel Interface (IM2='1', IM1, IM0="11")

Different display data formats are available for three colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bits input
- 65k colors, RGB 5,6,5-bits input
- 262k colors, RGB 6,6,6-bits input.

8.8.4.1 Write 18-bits data for RGB 4-4-4-bits input (4k-color)

There is 1 pixel (3 sub-pixels) per 1-transfer, 12-bits/pixel.



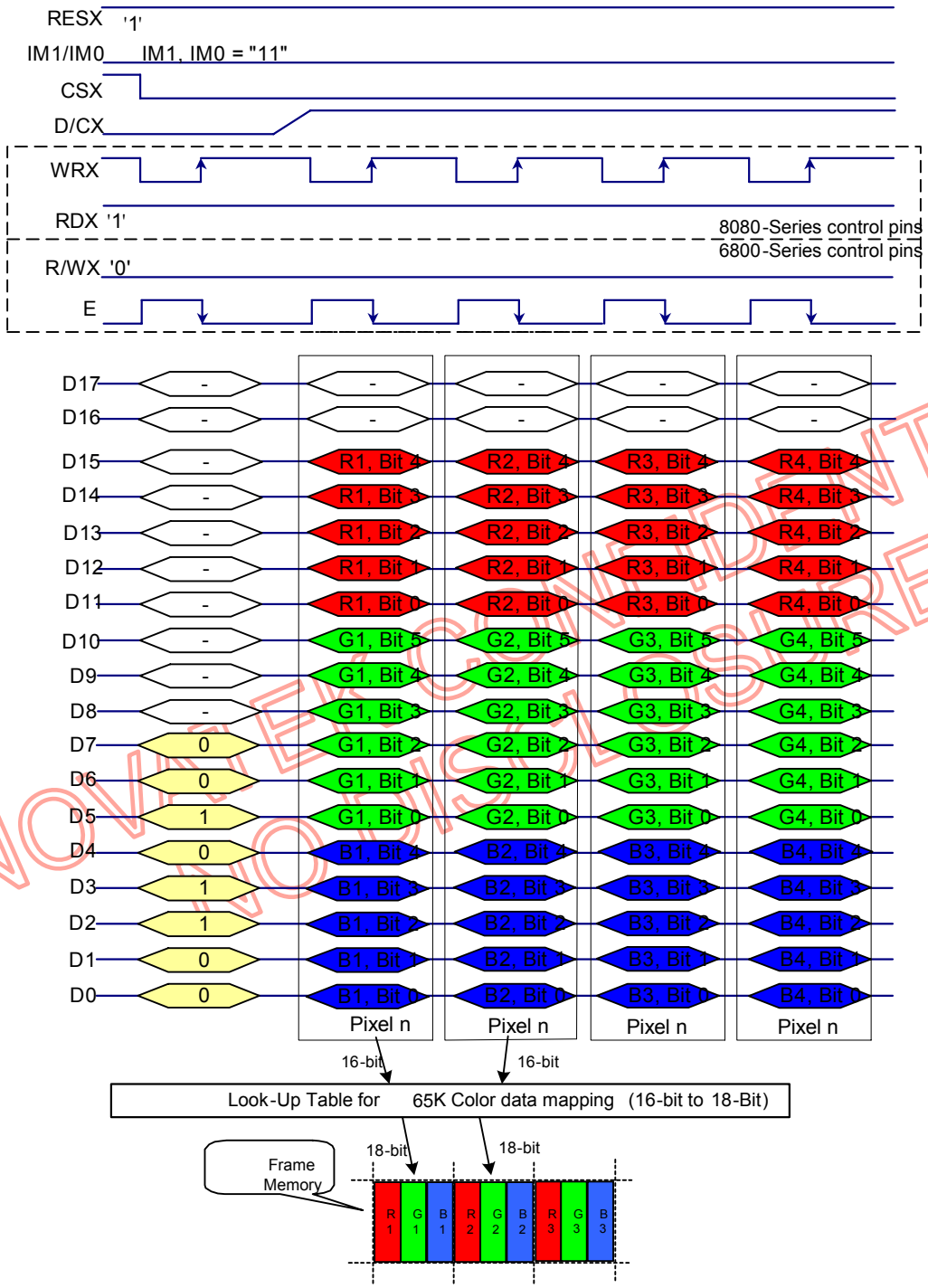
Note 1. The data order is ad follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 1-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

8.8.4.2 Write 18-bits data for RGB 5-6-5-bits input (65k-color)

There is 1 pixel (3 sub-pixels) per 1-transfer, 16-bits/pixel.



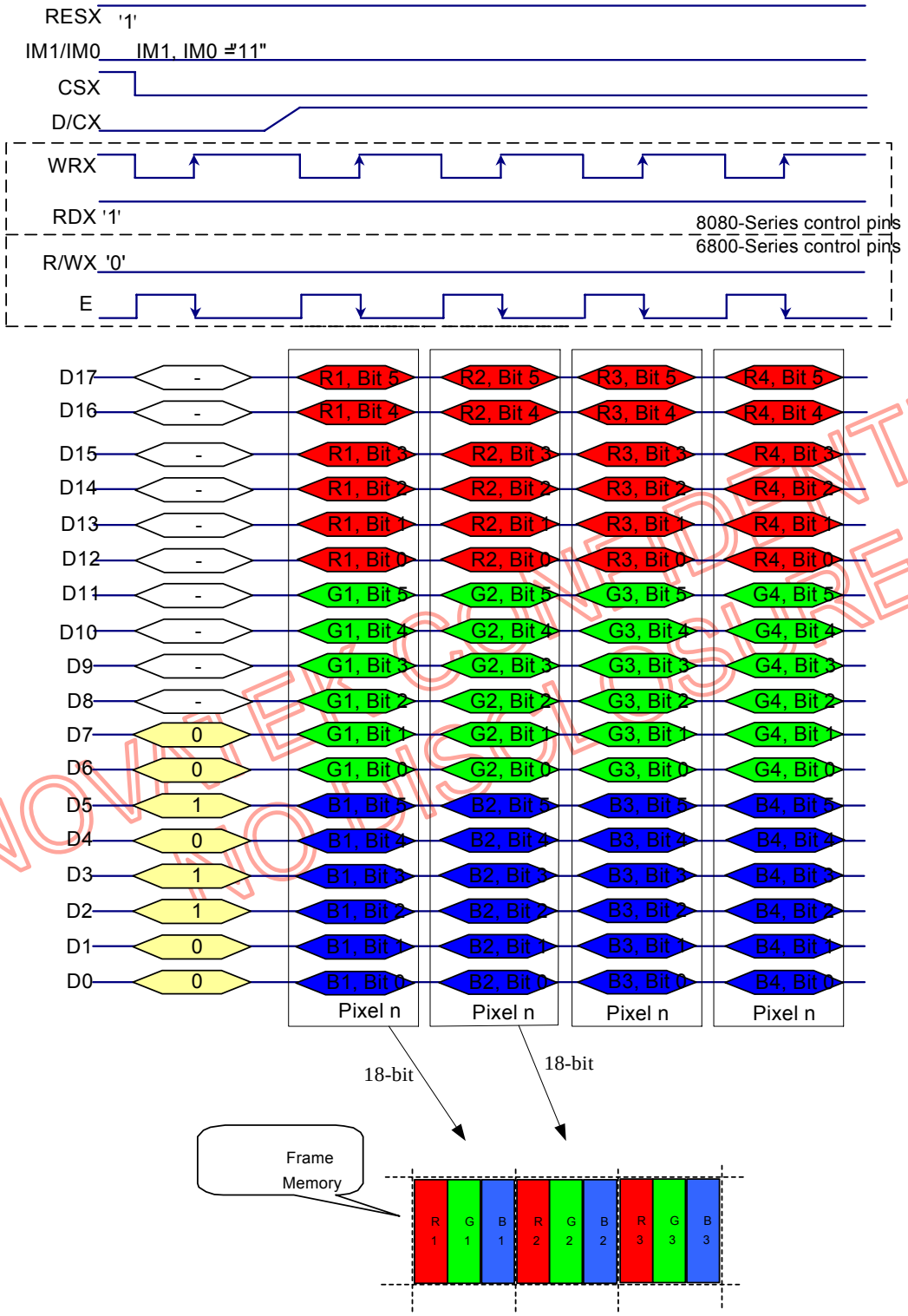
Note 1. The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2. 1-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

8.8.4.3 Write 18-bit data for RGB 6-6-6-bits input (262k-color)

There is 1 pixel (3 sub-pixels) per 1-transfer, 18-bit/pixel.



Note 1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2. 1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

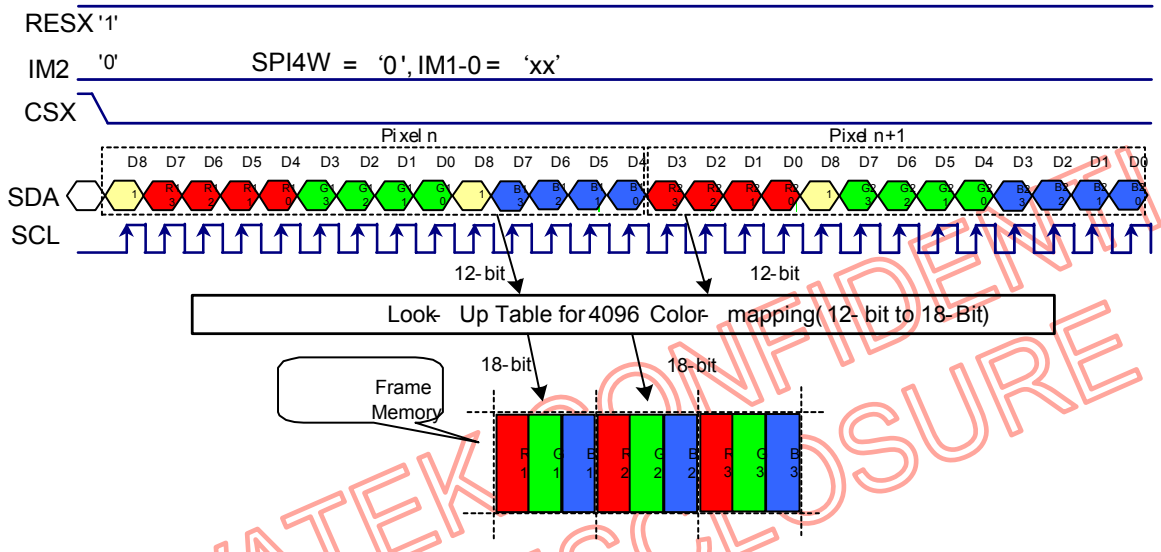
Note 3. '-' = Don't care - Can be set to '0' or '1'

8.8.5 Serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.
- 4k colors, RGB 4-4-4-bits input
- 65k colors, RGB 5-6-5-bits input
- 262k colors, RGB 6-6-6-bits input

8.8.5.1 Write data for RGB 4-4-4-bits input

3-pin 9-bit Series data protocol



Note 1. pixel data with the 12-bits color depth information

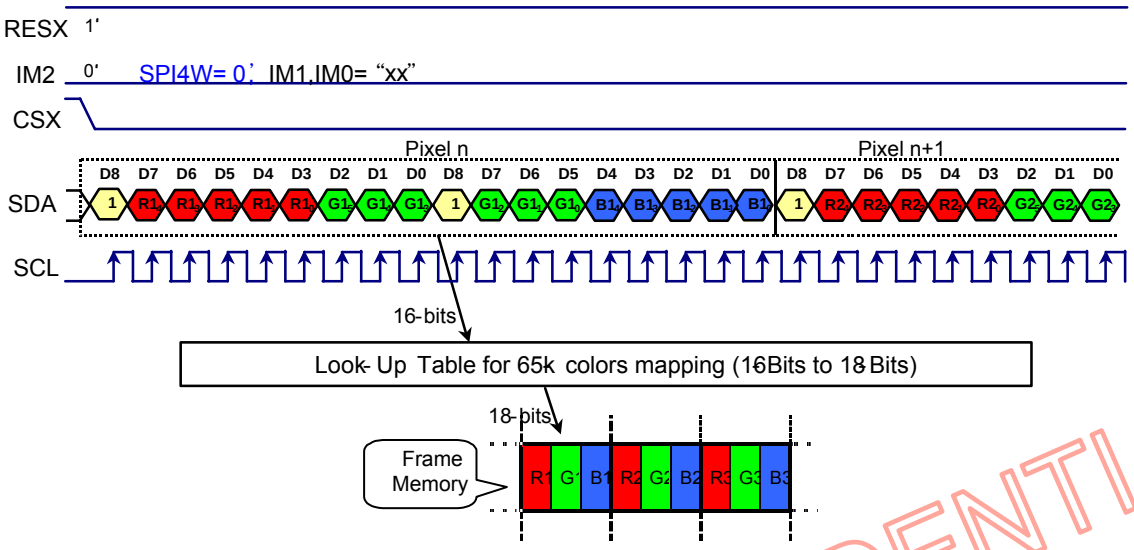
Note 2. The most significant bits are: Rx3, Gx3 and Bx3

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

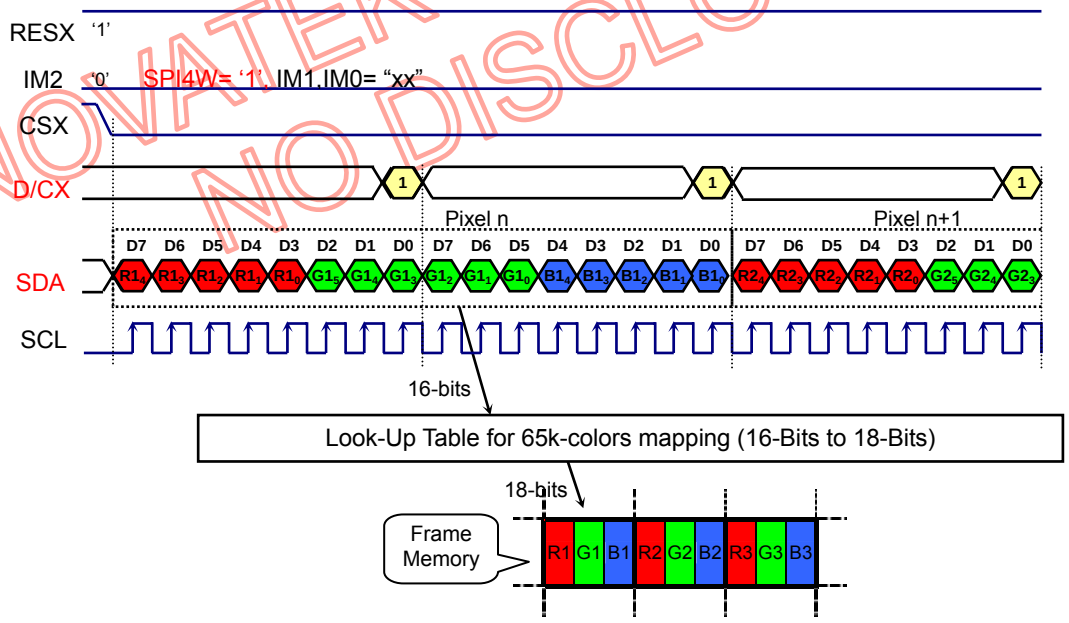
Note 4. X = Don't care - Can be set to '0' or '1'

8.8.5.2 Write data for RGB 5-6-5-bits input

3-pin 9-bit Series data protocol



4-pin 8-bit Series data protocol



Note 1. pixel data with the 16-bit color depth information

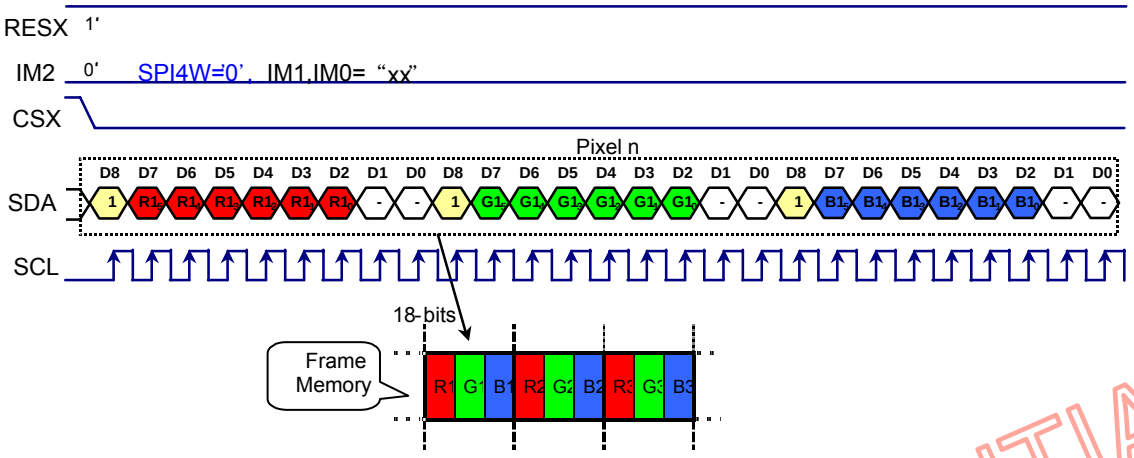
Note 2. The most significant bits are: Rx4, Gx5 and Bx4

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

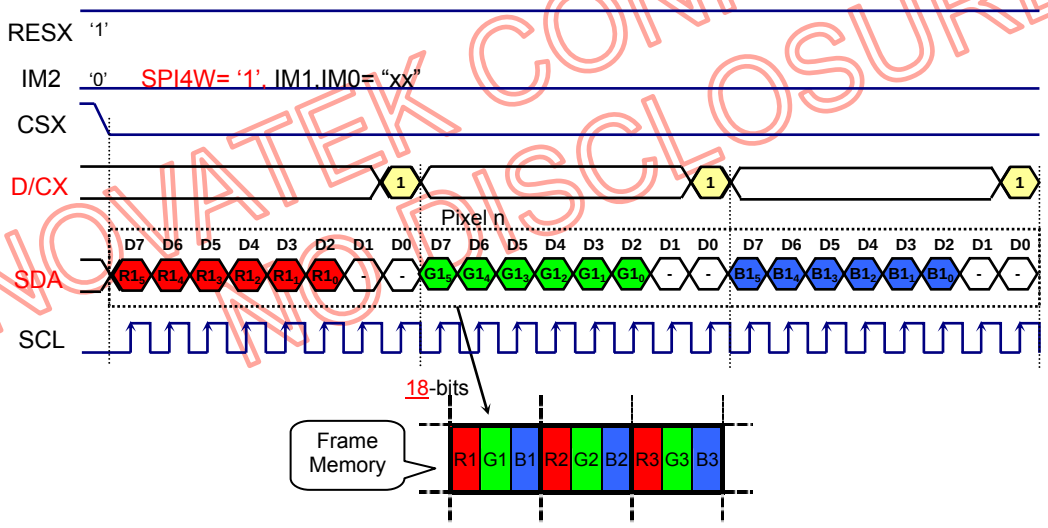
Note 4. X = Don't care - Can be set to '0' or '1'

8.8.5.3 Write data for RGB 6-6-6-bits input

3-pin 9-bit Series data protocol



4-pin 8-bit Series data protocol



Note 1. pixel data with the 18-bit color depth information

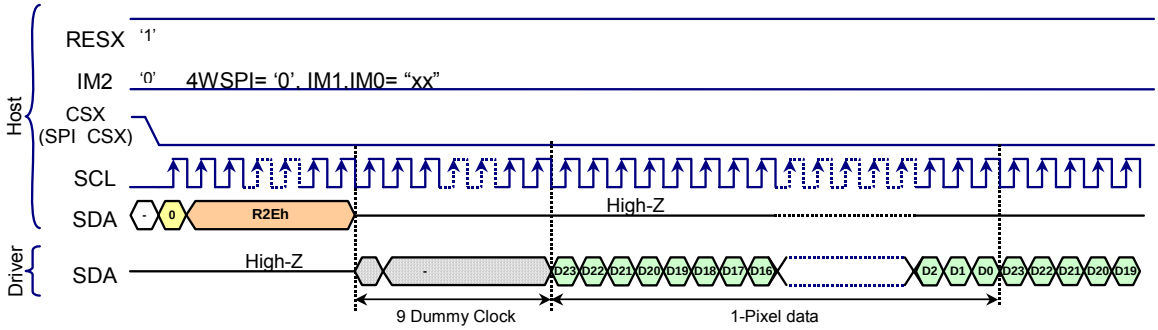
Note 2. The most significant bits are: Rx5, Gx5 and Bx5

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Note 4. X = Don't care - Can be set to '0' or '1'

8.8.5.4 Read data for SPI RGB 6-6-6-bits

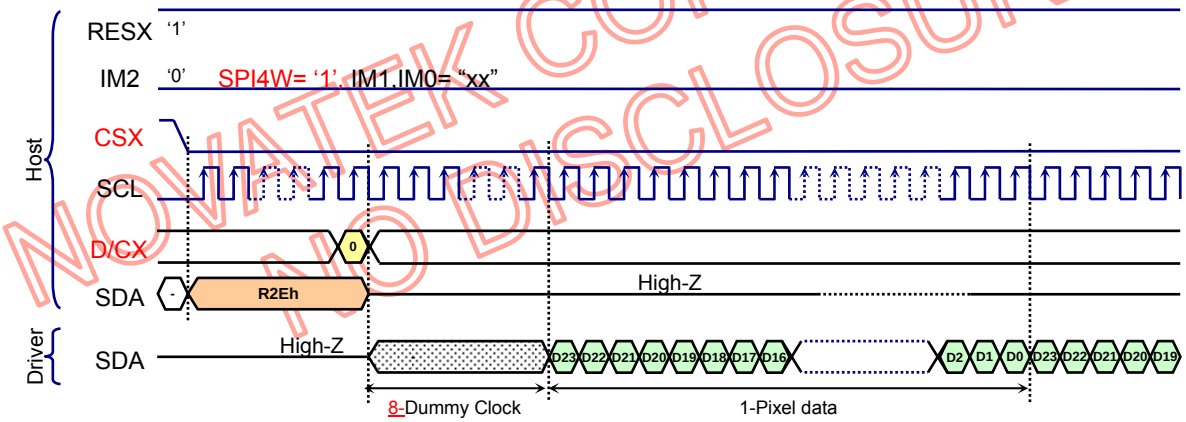
Read data for 3-W SPI RGB



Read Data format as below

Note: X = Don't care - Can be set to '0' or '1'

Read data for 4-W SPI RGB



Read Data format as below

Note: X = Don't care - Can be set to '0' or '1'

8.9 RGB interface

8.9.1 General Description

The module uses 6, 16 and 18-bits parallel RGB interface which includes: VS, HS, DE, PCLK, D[17:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and D[17:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative (‘0’, low) active and its state is read to the display module by a rising edge of he PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative (‘0’, low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received a RGB information that should be transferred on the display. This is a positive (‘1’, high) active and its state is read to the display module by a rising edge of the PCLK signal.

D[17:0] (18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE=’1’ and there is a rising edge of PCLK). D[17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the PCLK signal.

The PCLK cycle is described in the following figure.

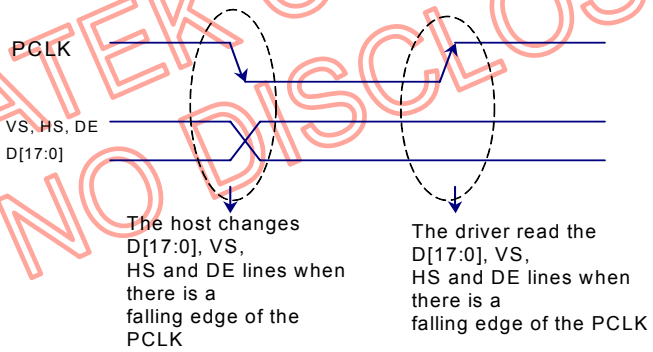


Fig. 8.8.1 PCLK cycle

Note: PCLK is an unsynchronized signal (It can be stopped).

8.9.2 RGB Interface Bus Width Set

All 4-kinds of bus width can be available during RGB interface mode (selected by COLMOD (3Ah) command for 8-bits, 16-bits and 18-bits data width)

VIPF[3:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
0101	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bits data
0110	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bits data
VIPF[3:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
1110	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bits data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Note 1: When VIPF[3:0]=" 1110", 6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 2: Only VIPF[3:0]=" 0101", "0110" and "1110" are valid on RGB I/F, Others are invalid.

Note 3. 'x' Don't care, but need to set VDDI or DGND level.

8.9.3 RGB Interface Mode Set

Table 8.9.5.1 RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	VS	HS	Video Data bus D[17:0]	Register for Blanking Porch setting	Reference clock for Display
RGB Mode 1	Used	Used	Used	Used	Used	Not Used	Internal Oscillator
RGB Mode 2	Used	Used	Used	Used	Used	Used	Internal Oscillator

There are 2-kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

In RGB Mode 1 : (RCM1, RCM0 = "10"), writing data to frame memory is done by PCLK and Video Data Bus (D[23:0]), when DE is high state. The external synchronization signals (PCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer PCLK, VS, HS and DE signals to driver.

In RGB Mode 2 : (RCM1, RCM0 = "11"), blanking porch setting of VS and HS signals are defined by RGBBPCTR (B5h) command. DE pin is used for data making. When DE pin is high, valid data is directly stored to frame memory. In the contrast, if DE pin is low, valid data will becomes "00" and stored to frame memory.

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8.9.4 MCU and RGB Interface Comparisons

Function	RCM1, RCM0		RCM1, RCM0			
Mode selection 1	"0x"		"10"		"11"	
	8080/ 6800 IF + SPI I/F		RGB I/F + SPI I/F			
	MCU Mode		RGB Mode 1		RGB Mode 2	
Mode selection 2	IMx=	IMx="0--"	ICM='0'	ICM='1'	ICM='0'	ICM='1'
	8080/ 6800 IF	SPI I/F	RGB-1 I/F + SPI I/F		RGB-2 I/F + SPI I/F	
Motion /Still selection	Motion or Still picture	Still picture	Motion or Still picture	Still picture	Motion or Still picture	Still picture
Input data	D[17:0]	D0 = SDA	D[17:0]	SDA H/W pin enable	D[17:0]	SDA H/W pin enable
Input signal	CSX	D/CX = SCL	PCLK	D/CX = SCL	PCLK	D/CX = SCL
	WRX (R/WX), RDX(E)	CSX	VS, HS, DE	CSX	VS, HS, DE	CSX
GRAM Write cycle	Refer the WRX cycle	Refer SCL	Refer PCLK	Refer SCL	Refer PCLK	Refer SCL
GRAM Read Cycle	Refer Internal Oscillator	Refer Internal Oscillator	Refer PCLK	Refer Internal Oscillator	Refer PCLK	Refer Internal Oscillator
Command setting	D[7:0]	D0(SDA)	SDA	SDA	SDA	SDA
SRGB	-If the register is not changed, the H/W pin is always valid. If the register is changed, should be follow the register setting. -When Power On or H/W reset, the function follow H/W pin setting first.					
SMX, SMY	-Those H/W pins are always valid.					
Normal / Partial mode	-By command setting	-By command setting	-By command setting		-By Command setting, Partial On/Off, Area function	
Blanking porch	-Don't care in this mode.	-Don't care in this mode.	-Control by DE signal		-Control by RGBBPCTR (B5h)	
Colors format	-Control by IFPF[2:0] of COLMOD(3Ah)		-Control by VIPF[3:0] of COLMOD(3Ah)			
DE setting	-By command setting -Don't care in this mode. But should be set to VDDI or DGND.		-The data latched by rising edge of PCLK when DE='1' -When display data coming the DE signal should be VDDI level		-When DE='0' area, the data of GRAM will become value "00".	
Idle Mode (IDM H/W pin)	-By command setting -Don't care in this mode. But should be set to VDDI or DGND.		-By command setting -Don't care in this mode. But should be set to VDDI or DGND.		-By H/W pin -Refer to IDM On/OFF (39h/38h), CRL (B7h), CTB (B8h), INV On/OFF (21h/20h), SLPIN(10h), SLPOUT(11h), Display On/OFF (29h/28h) -If those registers are not changed, those H/W pins are always valid. If those registers are changed, should be follow registers setting. -When Power On or H/W reset, those function follow H/W pins setting first.	
RL setting						
TB setting						
Display On/ Off (SHUT H/W pin)						
Data inverter setting (REV H/W pin)	-Exclusive OR result of H/W and S/W setting.		-Exclusive OR result of H/W and S/W setting.			
TE Setting	-By command setting					

Note 1: RCM1 and RCM0 are H/W setting pins.

Note 2: In RGB + SPI I/F (RCM="1x"), VS, HS, DE, PCLK and D[17:0] are Hi-Z by Driver and can be stop for Host, when ICM='1'.

Note 3: In RGB + SPI I/F (RCM="1x"), the data deliver via GRAM

Note 4: When Power on Driver IC should be detect SMX, SMY, SRGB H/W setting

Note 5: When Power on Driver IC should be detect RCM1, RCM0 H/W setting and get into the I/F mode.

Note 6: When Power on Driver IC should be detect LCM1, LCM0 H/W setting and get into the setting mode.

Note 7: When Power on Driver IC should be detect GM1, GM0 H/W setting and get into the setting mode.

8.10 Display Data RAM

8.10.1 Configuration (When GM="—")

The display module has an integrated 132x162x18-bit graphic type static RAM. This 384,912-bits memory allows to store on-chip a 132xRGBx162 image with an 18-bpp resolution (262K-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Display Data RAM Organization

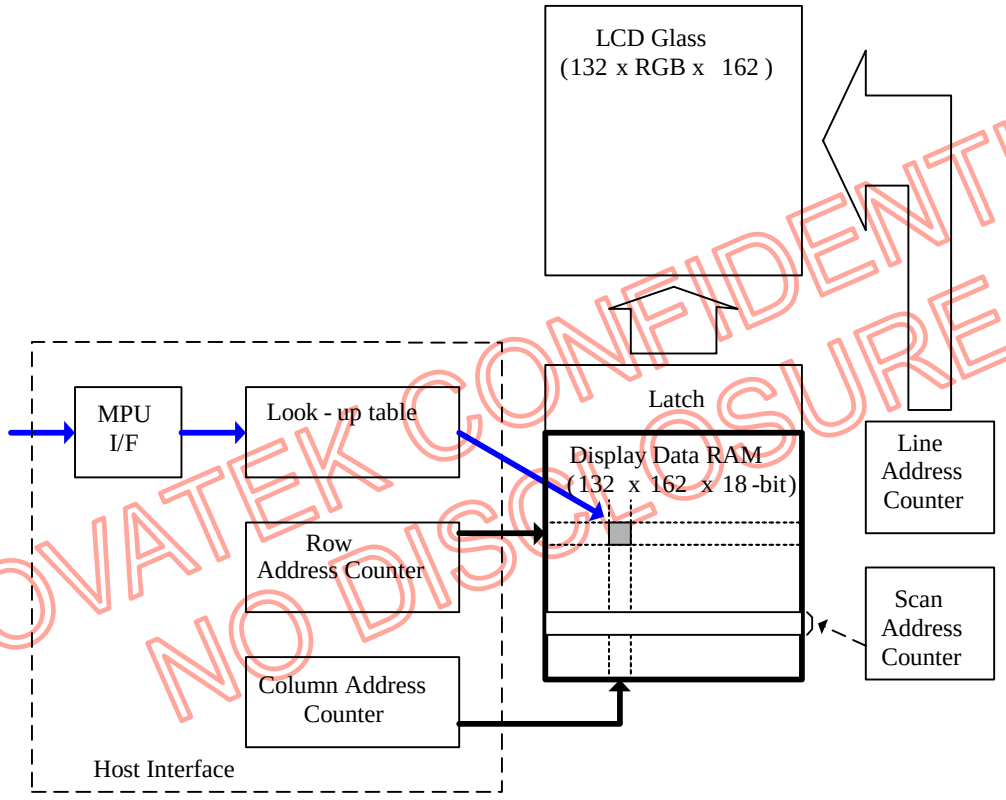
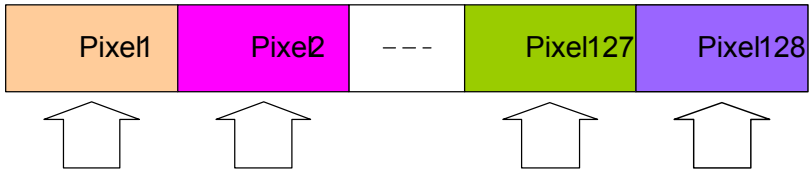


Fig. 8.10.1 Display Data RAM Organization

8.10.2 Memory to Display Address Mapping

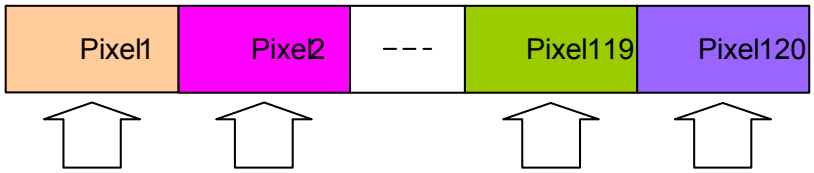
8.10.2.1 When using 128RGB x 160 resolution (GM1, GM0 = “00”, SMX=SMY=SRGB=’0’)



Gate Out	Source Out		S7	S8	S9	S10	S11	S12	– – –	S385	S386	S387	S388	S389	S390		
			RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1		
	RA															SA	
	MY=0	MY=1														ML=0	ML=1
1	1	160	R1	G1	B1	R2	G2	B2	– – –	R127	G127	B127	R128	G128	B128	1	160
2	2	159							– – –							2	159
3	3	158							– – –							3	158
4	4	157							– – –							4	157
5	5	156							– – –							5	156
6	6	155							– – –							6	155
7	7	154							– – –							7	154
8	8	153							– – –							8	153
9	9	152							– – –							9	152
10	10	151							– – –							10	151
11	11	150							– – –							11	150
12	12	149							– – –							12	149
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	– – –	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
153	153	8							– – –							153	8
154	154	7							– – –							154	7
155	155	6							– – –							155	6
156	156	5							– – –							156	5
157	157	4							– – –							157	4
158	158	3							– – –							158	3
159	159	2							– – –							159	2
160	160	1							– – –							160	1
	CA	MX=0	1			2			– – –	127			128				
		MX=1	128			127			– – –	2			1				

Note
RA = Row Address,
CA = Column Address
SA = Scan Address
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command
ML =Scan direction parameter, D4 parameter of MADCTL command
RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

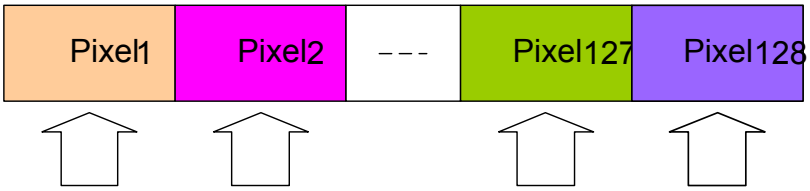
8.10.2.2 When using 120RGB x 160 resolution (GM1, GM0 = “01”, SMX=SMY=SRGB=’0’)



Gate Out	Source Out		S7	S8	S9	S10	S11	S12	– – –	S361	S362	S363	S364	S365	S366		
			RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1		
	RA															SA	
	MY= 0	MY= 1														ML= 0	ML= 1
1	1	160	R1	G1	B1	R2	G2	B2	– – –	R119	G119	B119	R120	G120	B120	1	160
2	2	159							– – –							2	159
3	3	158							– – –							3	158
4	4	157							– – –							4	157
5	5	156							– – –							5	156
6	6	155							– – –							6	155
7	7	154							– – –							7	154
8	8	153							– – –							8	153
9	9	152							– – –							9	152
10	10	151							– – –							10	151
11	11	150							– – –							11	150
12	12	149							– – –							12	149
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	– – –	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
153	153	8							– – –							153	8
154	154	7							– – –							154	7
155	155	6							– – –							155	6
156	156	5							– – –							156	5
157	157	4							– – –							157	4
158	158	3							– – –							158	3
159	159	2							– – –							159	2
160	160	1							– – –							160	1
	CA	MX= 0	1			2			– – –	119			120				
		MX= 1	120			119			– – –	2			1				

Note
RA = Row Address,
CA = Column Address
SA = Scan Address
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command
ML =Scan direction parameter, D4 parameter of MADCTL command
RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

8.10.2.3 When using 128RGB x 128 resolution (GM1, GM0 = “10”, SMX=SMY=SRGB=’0’)



Gate Out	Source Out		S7	S8	S9	S10	S11	S12	– – –	S385	S386	S387	S388	S389	S390		
			RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1		
	RA															SA	
	MY=0	MY=1														ML=0	ML=1
1	1	128	R1	G1	B1	R2	G2	B2	– – –	R127	G127	B127	R128	G128	B128	1	128
2	2	127							– – –							2	127
3	3	126							– – –							3	126
4	4	125							– – –							4	125
5	5	124							– – –							5	124
6	6	123							– – –							6	123
7	7	122							– – –							7	122
8	8	121							– – –							8	121
9	9	120							– – –							9	120
10	10	119							– – –							10	119
11	11	118							– – –							11	118
12	12	117							– – –							12	117
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	– – –	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
121	121	8							– – –							121	8
122	122	7							– – –							122	7
123	123	6							– – –							123	6
124	124	5							– – –							124	5
125	125	4							– – –							125	4
126	126	3							– – –							126	3
127	127	2							– – –							127	2
128	128	1							– – –							128	1
	CA	MX=0	1			2			– – –	127			128				
		MX=1	128			127			– – –	2			1				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

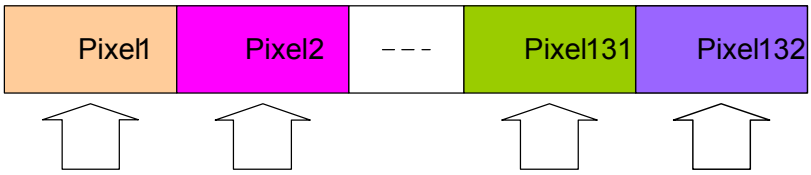
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command

ML =Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

8.10.2.4 When using 132RGB x 162 resolution (GM1, GM0 = “11”, SMX=SMY=SRGB=’0’)



Gate Out	Source Out	S1	S1	S3	S4	S5	S6	– – –	S391	S392	S393	S394	S395	S396		
		RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1		
	RA														SA	
	MY=0	MY=1													ML=0	ML=1
1	1	162	R1	G1	B1	R2	G2	B2	– – –	R131	G131	B131	R132	G132	B132	1	162
2	2	161							– – –							2	161
3	3	160							– – –							3	160
4	4	159							– – –							4	159
5	5	158							– – –							5	158
6	6	157							– – –							6	157
7	7	156							– – –							7	156
8	8	155							– – –							8	155
9	9	154							– – –							9	154
10	10	153							– – –							10	153
11	11	152							– – –							11	152
12	12	151							– – –							12	151
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	– – –	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
155	155	8							– – –							155	8
156	156	7							– – –							156	7
157	157	6							– – –							157	6
158	158	5							– – –							158	5
159	159	4							– – –							159	4
160	160	3							– – –							160	3
161	161	2							– – –							161	2
162	162	1							– – –							162	1
	CA	MX=0	1			2			– – –	131			132				
		MX=1	132			131			– – –	2			1				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command

ML =Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

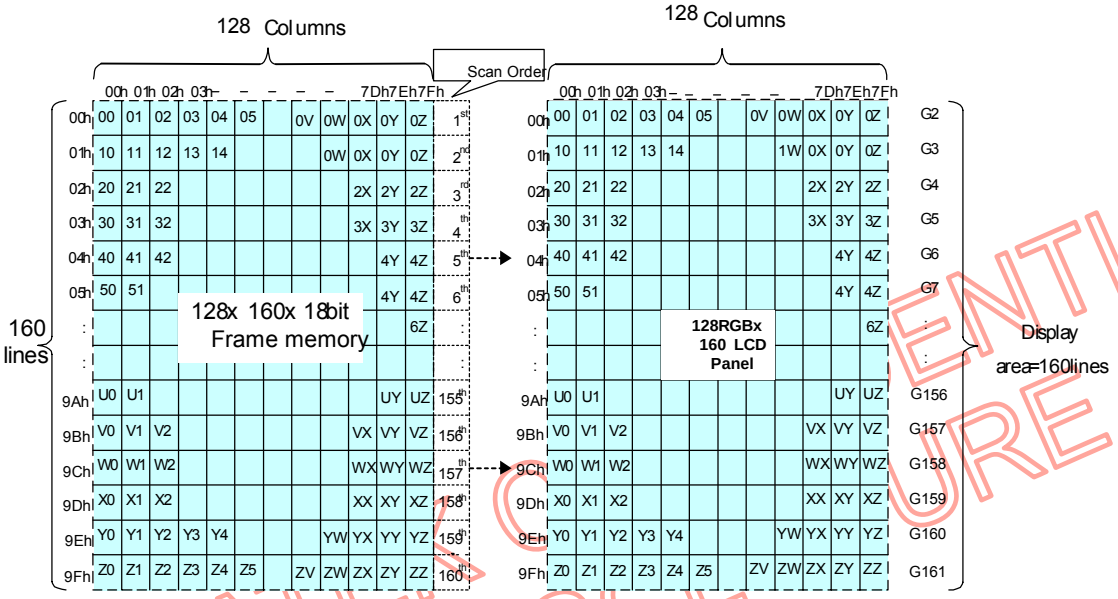
8.10.3 Normal Display On or Partial Mode On, Vertical Scroll Off

8.10.3.1 When using 128RGB x 160 resolution (GM1, GM0 = “00”)

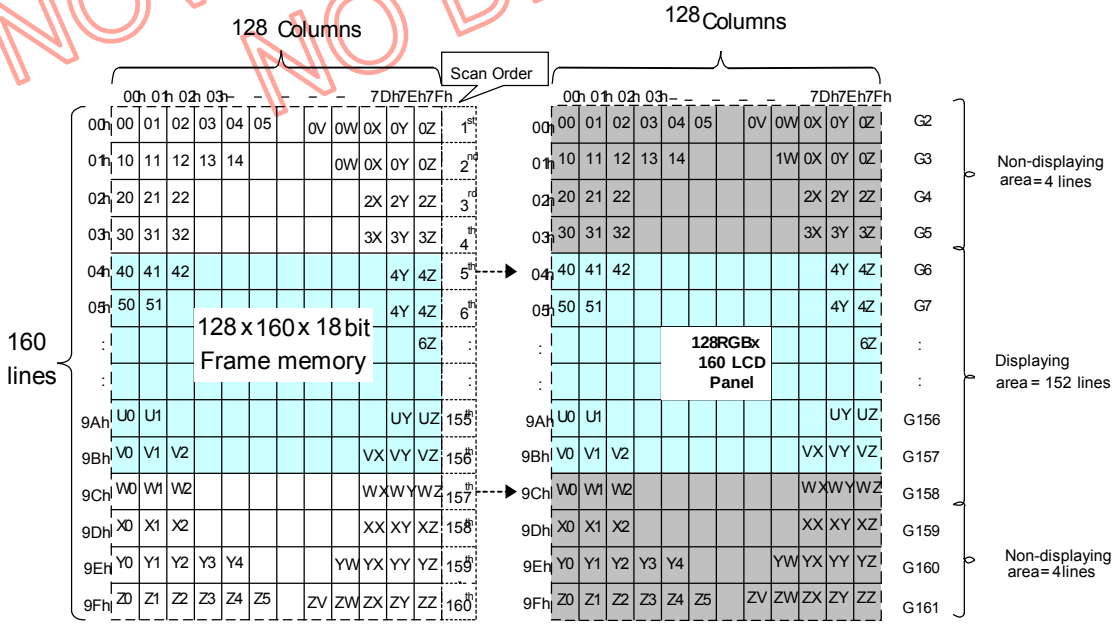
In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=MV=’0’, SMX=SMY=’0’)



2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Bh, MX=MY=MV=’0’ ,SMX=SMY=’0’)

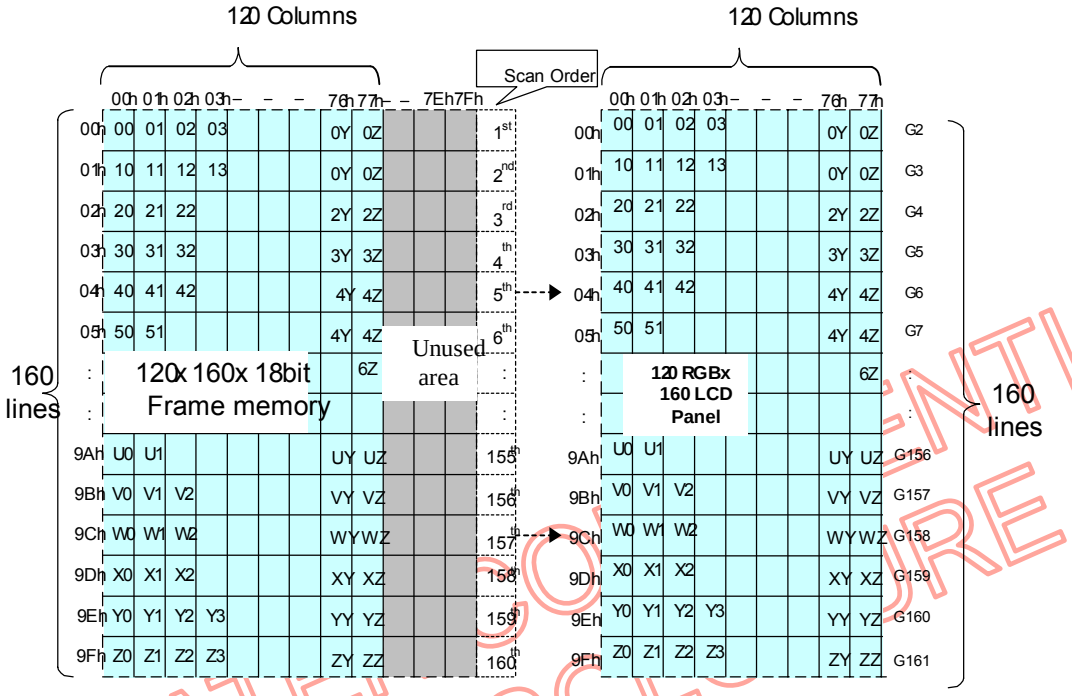


8.10.3.2 When using 120RGB x 160 resolution (GM1, GM0 = “01”)

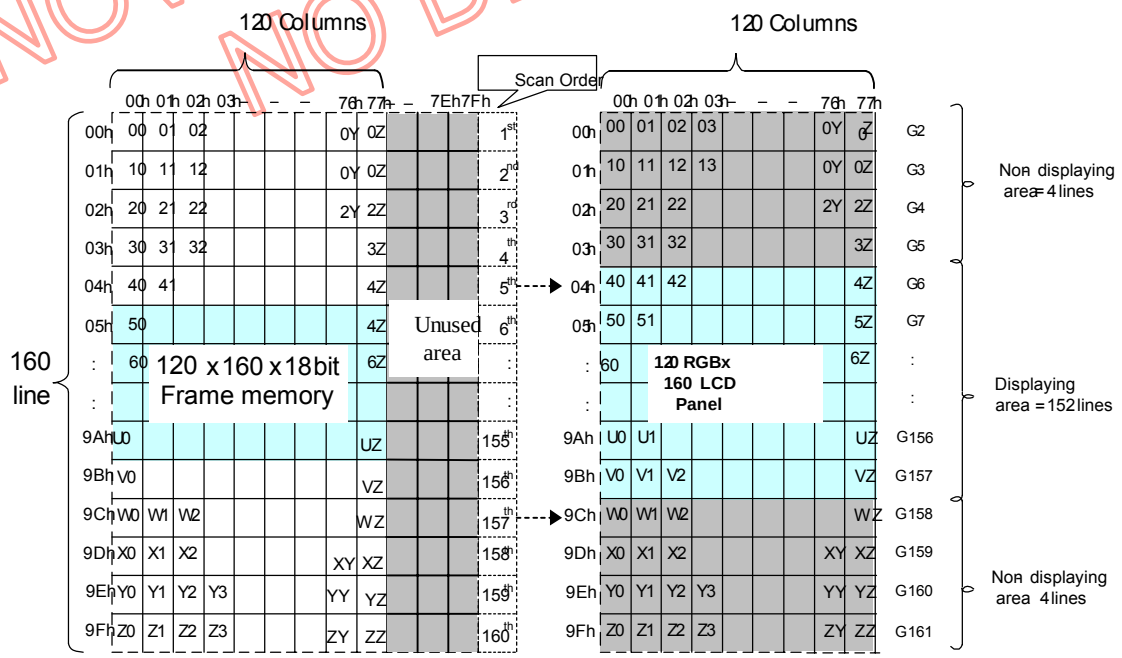
In this mode, contents of the frame memory within an area where column pointer is 00h to 77h and page pointer is 00h to 9Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=MV=’0’, SMX=SMY=’0’)



2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Bh, MX=MY=MV=’0’, SMX=SMY=’0’)

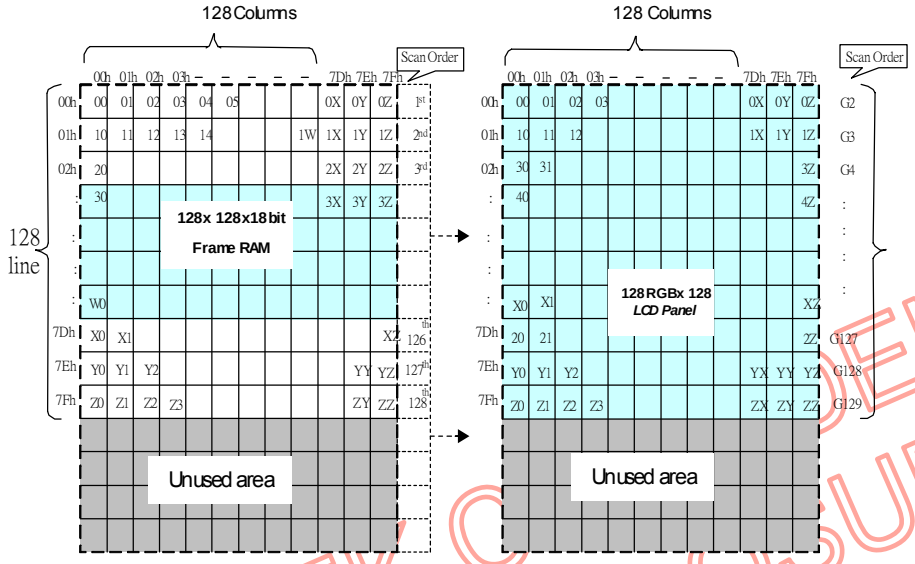


8.10.3.3 When using 128RGB x 128 resolution (GM1, GM0 = “10”)

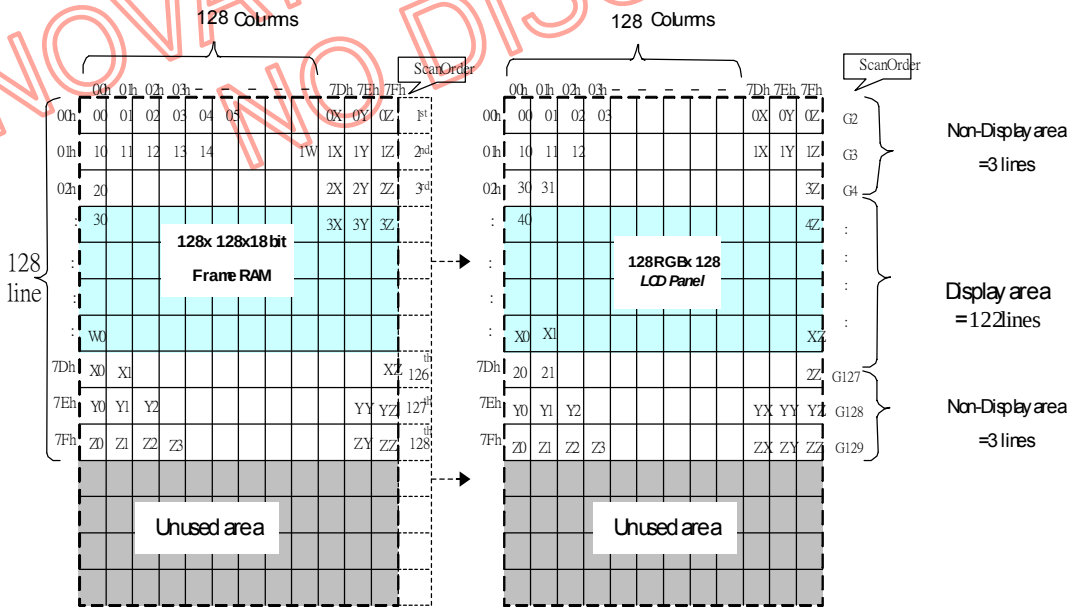
In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 000h to 07Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=MV=’0’, SMX=SMY=’0’)



2). Example for Partial Display On (PSL[7:0]=03h,PEL[7:0]=7Ch, MX=MY=MV=’0’ ,SMX=SMY=’0’)

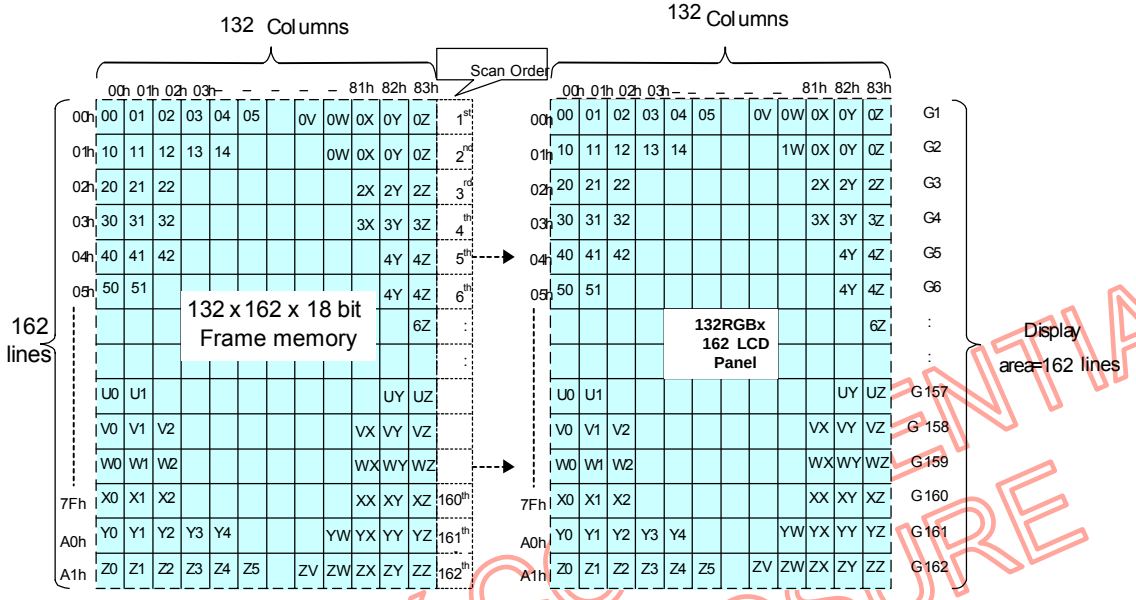


8.10.3.4 When using 132RGB x 162 resolution (GM1, GM0 = “11”)

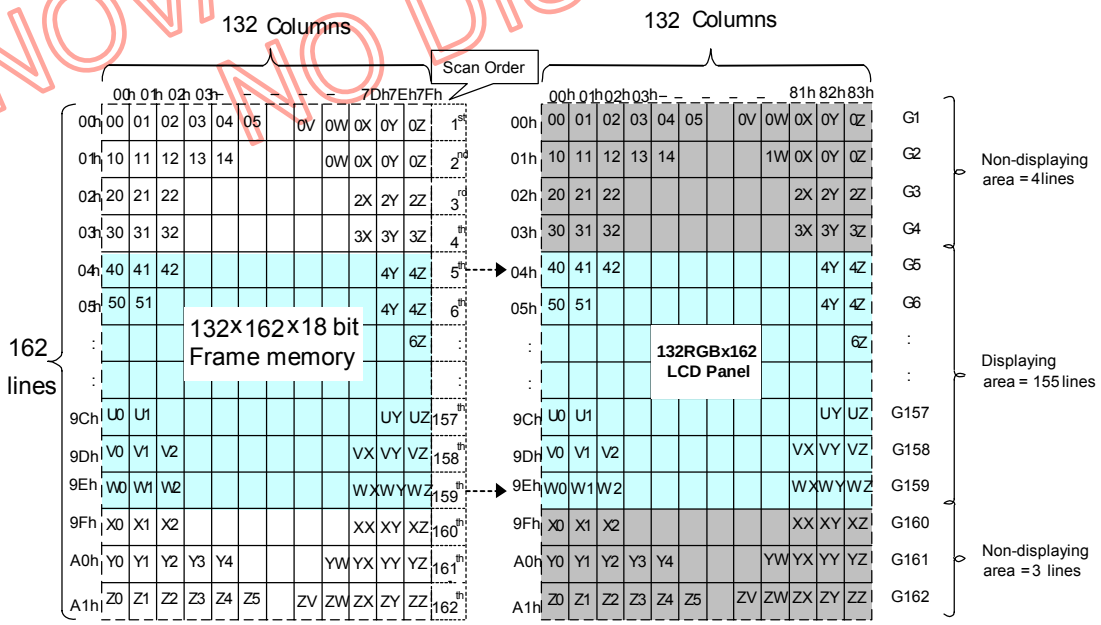
In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed.

To display a dot on left most top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=MV=’0’, SMX=SMY=’0’)



2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Eh, MX=MY=MV=’0’ ,SMX=SMY=’0’)



8.10.4 Vertical Scroll Mode

There is vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

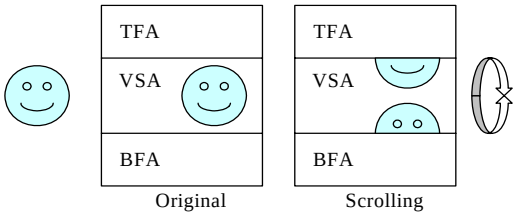
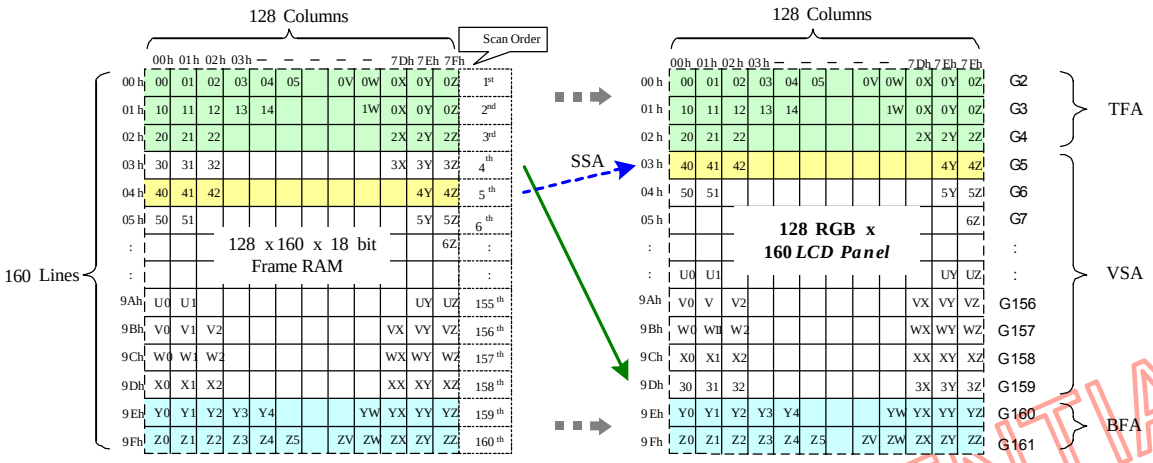


Fig. 8.10.2 Difference between Scrolling and original

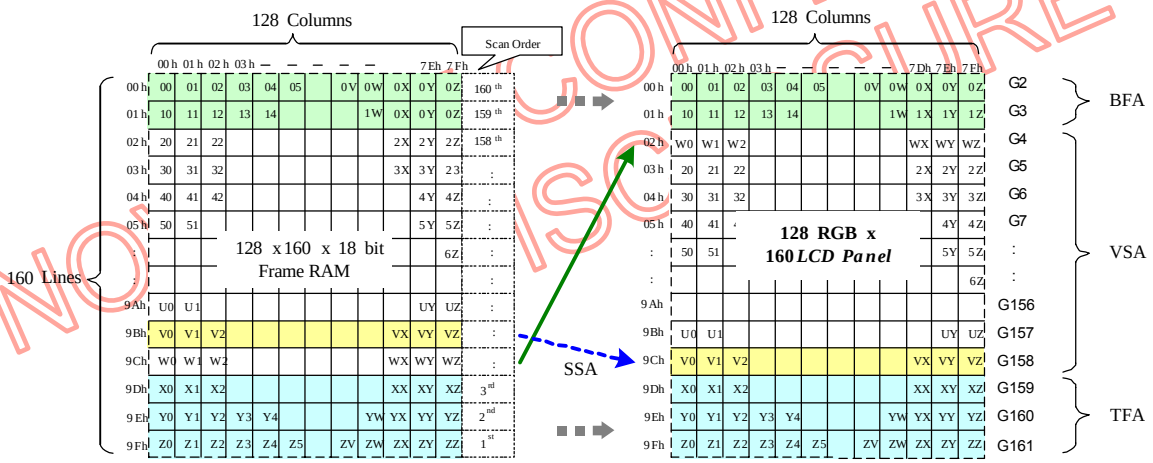
8.10.4.1 When using 128RGB x 160 resolution (GM1, GM0 = “00”)

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=160. In this case, scrolling is applied as shown below.

1). Example for TFA =3, VSA=155, BFA=2, SSA=4, ML=0: Scrolling



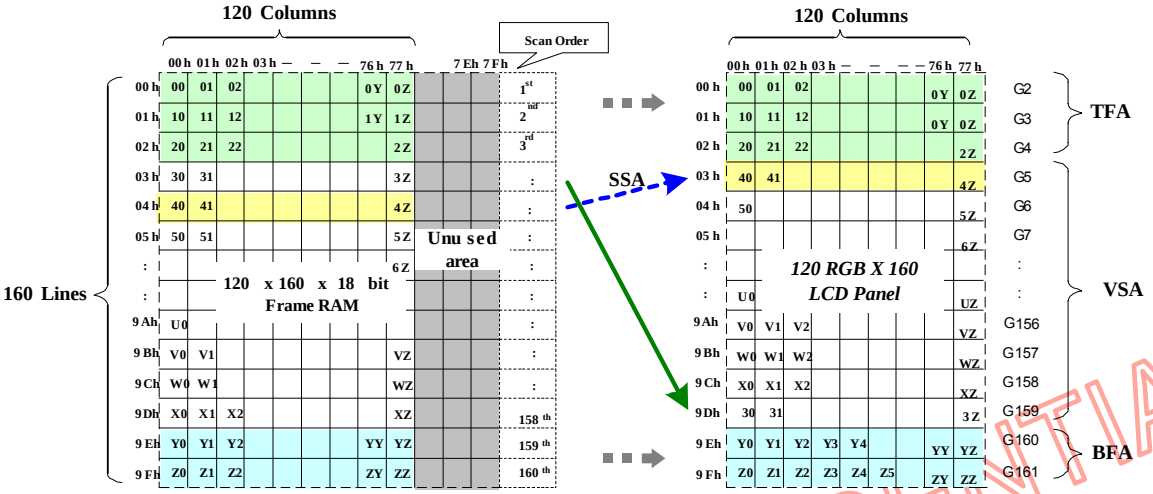
2). Example for TFA =3, VSA=155, BFA=2, SSA=4, ML=1: Scrolling: TFA and BFT are exchanged



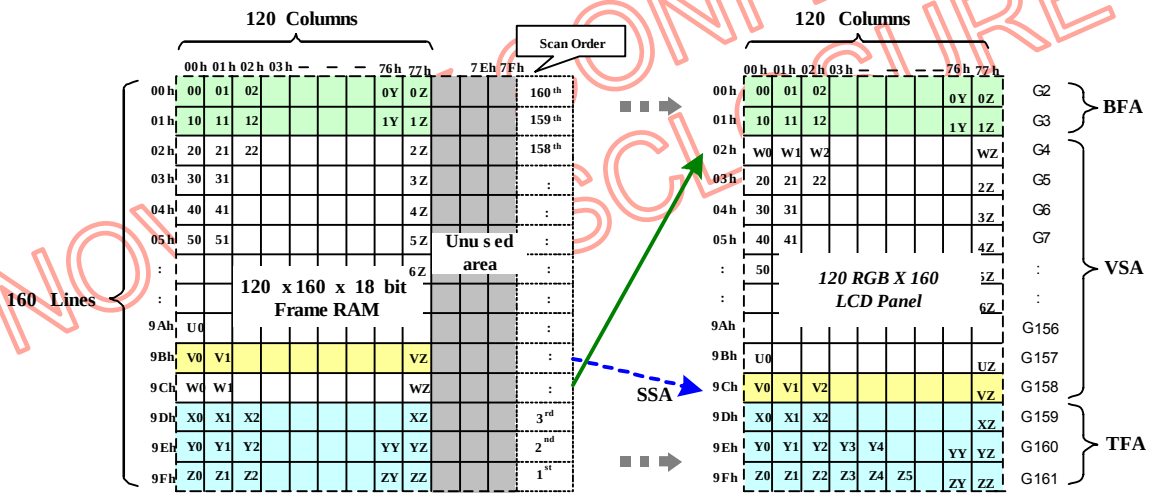
8.10.4.2 When using 120RGB x 160 resolution (GM1, GM0 = “01”)

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=160. In this case, scrolling is applied as shown below.

1). Example for TFA =3, VSA=155, BFA=2, SSA=4, ML=0: Scrolling



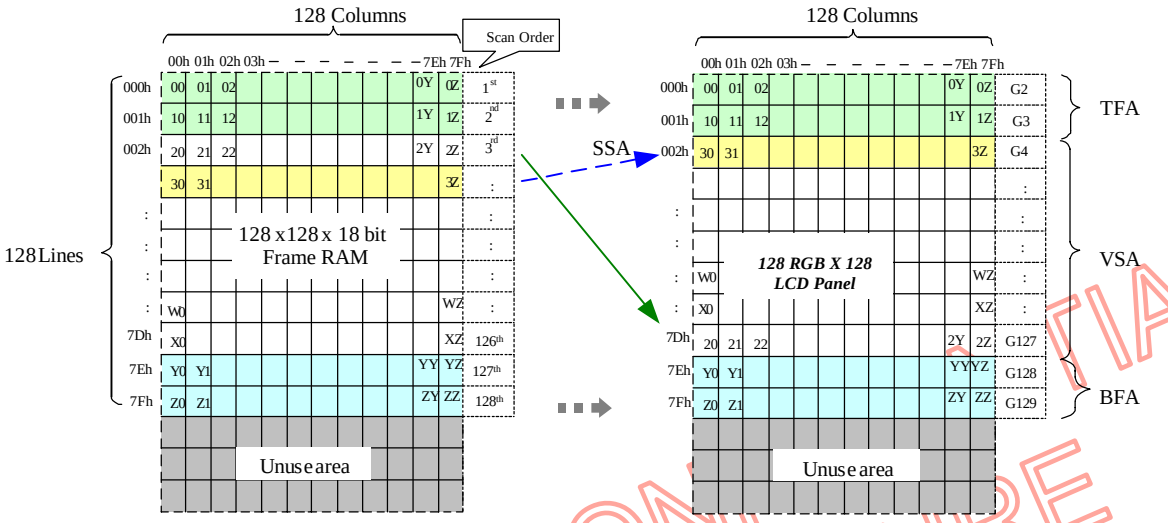
2). Example for TFA =3, VSA=155, BFA=2, SSA=4, ML=1: Scrolling: TFA and BFT are exchanged



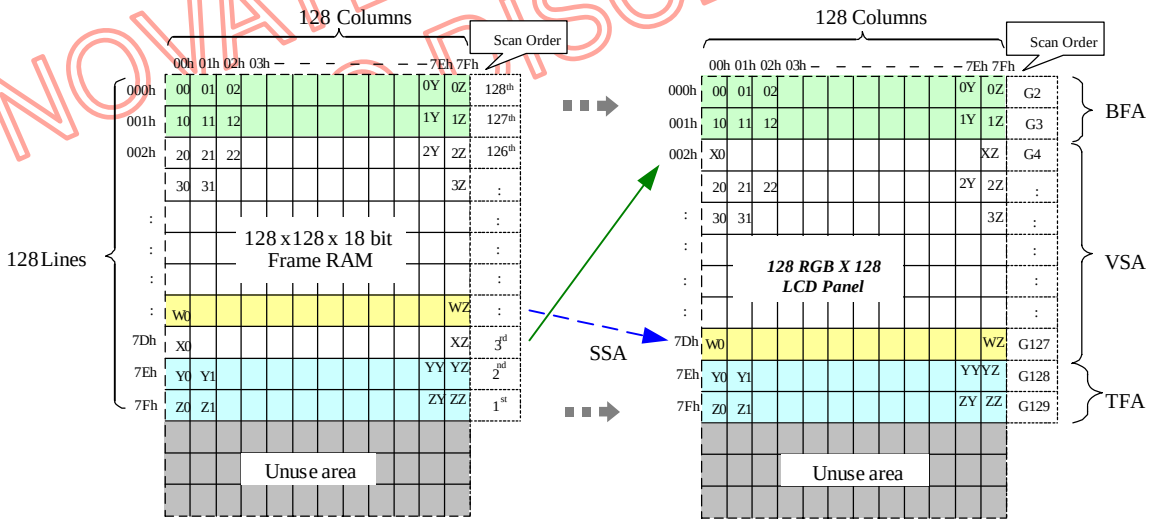
8.10.4.3 When using 128RGB x 128 resolution (GM1, GM0 = “10”)

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=128. In this case, scrolling is applied as shown below.

1). Example for TFA =2, VSA=124, BFA=2, SSA=3, ML=0: Scrolling



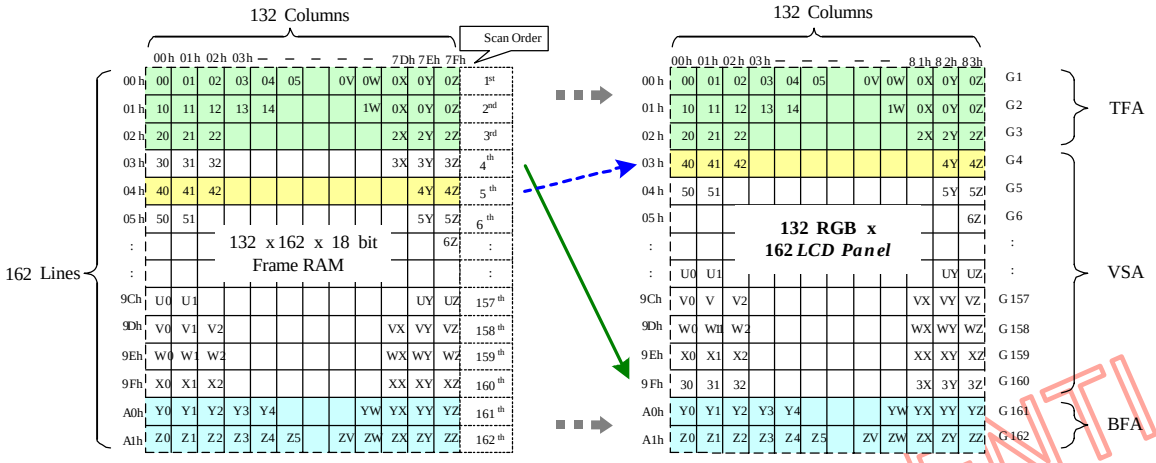
2). Example for TFA =2, VSA=124, BFA=2, SSA=3, ML=1: Scrolling: TFA and BFT are exchanged



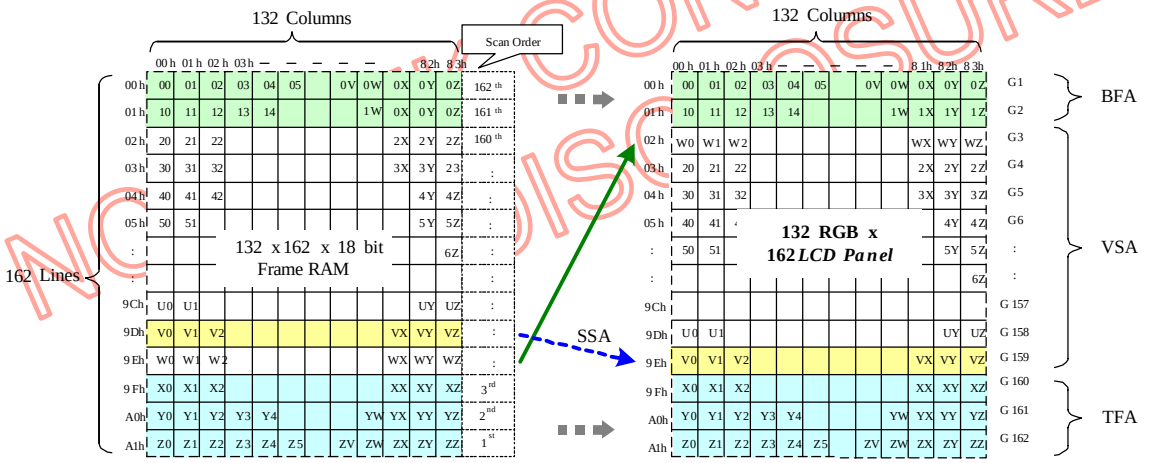
8.10.4.4 When using 132RGB x 162 resolution (GM1, GM0 = “11”)

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=162. In this case, scrolling is applied as shown below.

1). Example for TFA =3, VSA=157, BFA=2, SSA=4, ML=0: Scrolling



2). Example for TFA =3, VSA=157, BFA=2, SSA=4, ML=1: Scrolling: TFA and BFT are exchanged



8.10.5 Vertical Scroll Example

8.10.5.1 Vertical Scroll Example (GM1, GM0 = “00” & GM1, GM0=”01”)

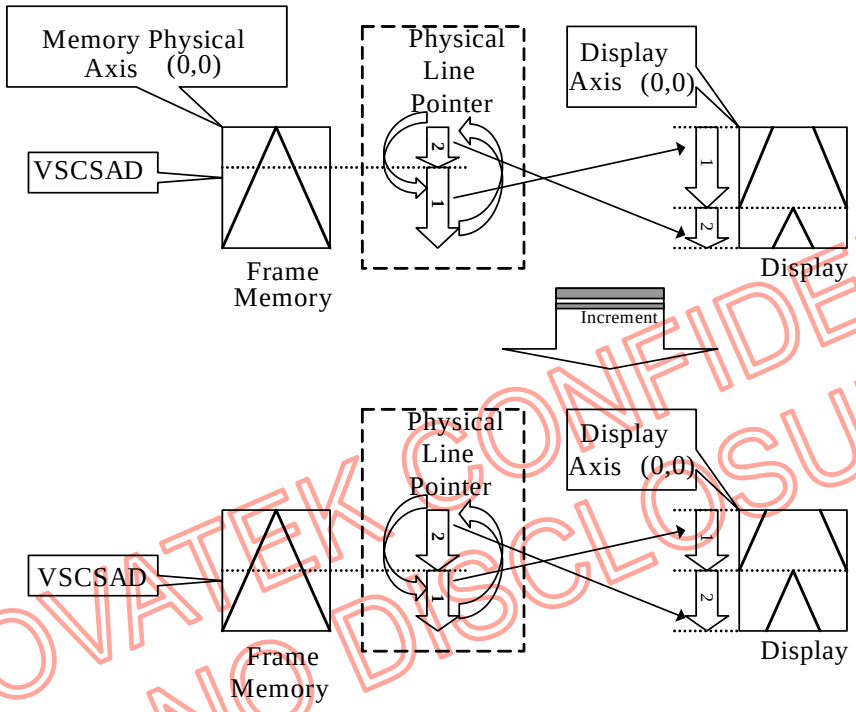
There are 2 types of vertical scrolling, which are determined by the commands “ Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA ≠ 160

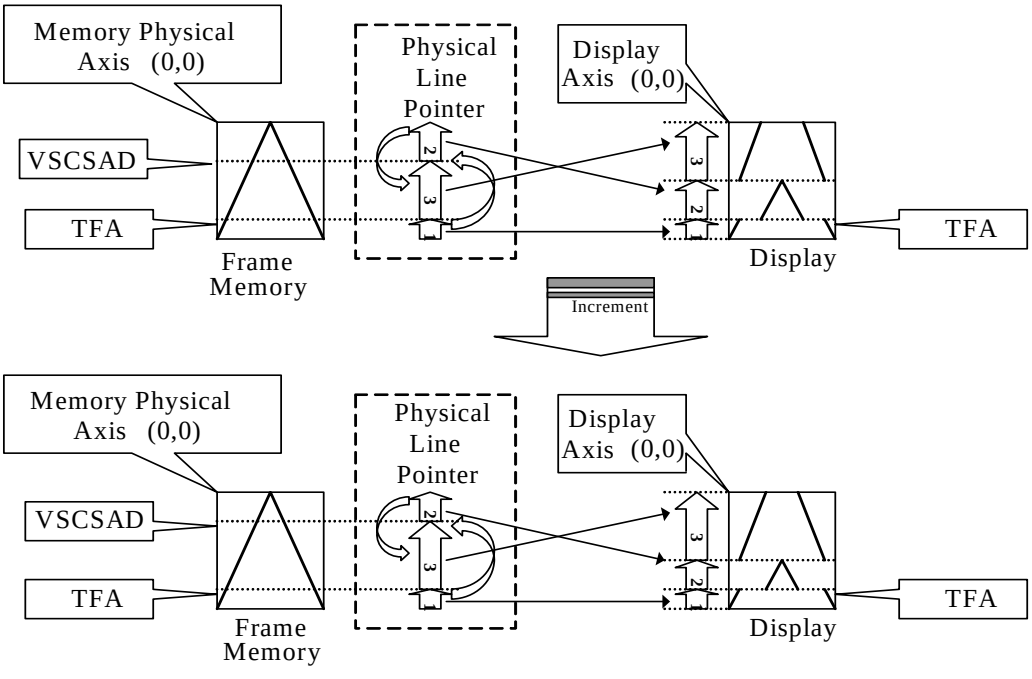
N/A. Do not set TFA + VSA + BFA≠160. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=160 (Scrolling)

Example1) When MADCTR parameter ML=”0”, TFA=0, VSA=160, BFA=0 and VSCSAD=40.



Example2) When MADCTR parameter ML=”1”, TFA=30, VSA=130, BFA=0 and VSCSAD=40.



8.10.5.2 Vertical Scroll Example (GM1, GM0 = “10”)

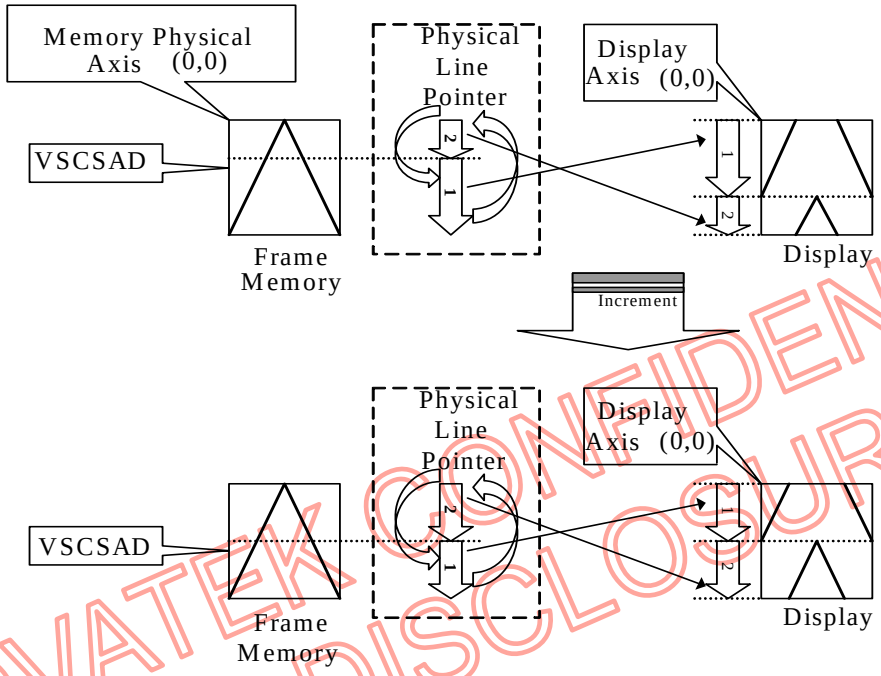
There are 2 types of vertical scrolling, which are determined by the commands “ Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA ≠ 128

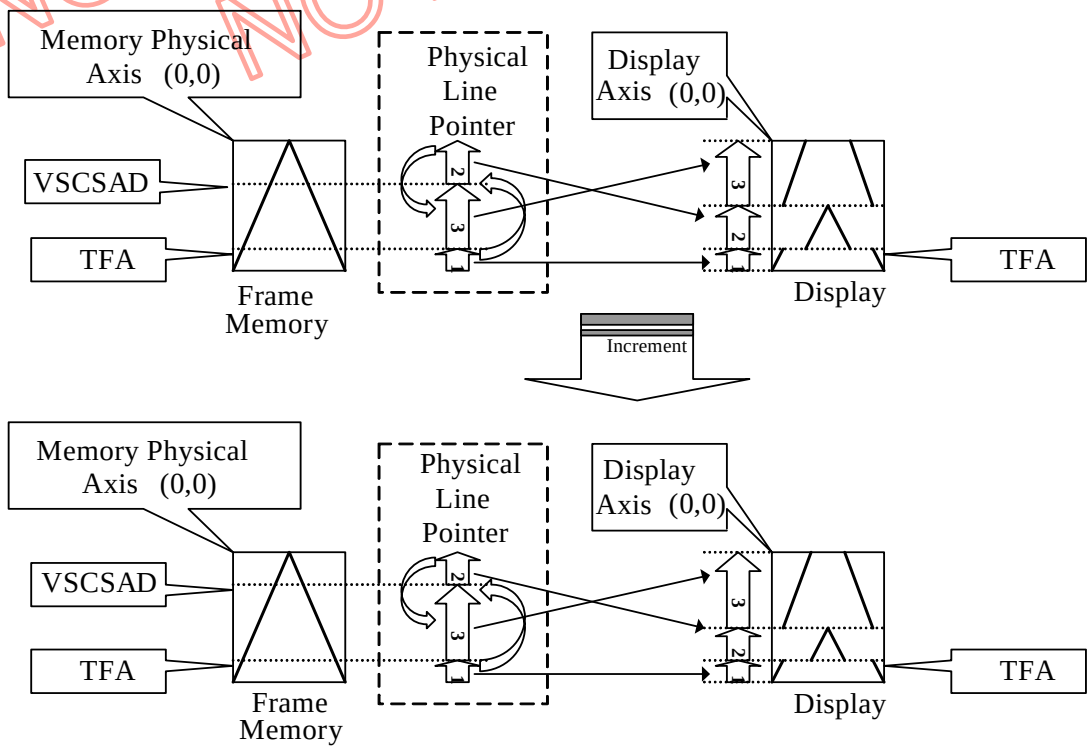
N/A. Do not set TFA + VSA + BFA≠128. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=128 (Scrolling)

Example1) When MADCTR parameter ML=”0”, TFA=0, VSA=128, BFA=0 and VSCSAD=40.



Example2) When MADCTR parameter ML=”1”, TFA=30, VSA=98, BFA=0 and VSCSAD=40.



8.11 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. When GM=11, 132RGB x 162, the address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=131 (83h), YE=161 (A1h).

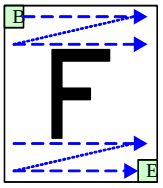
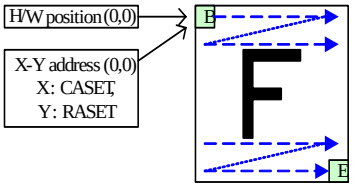
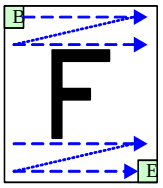
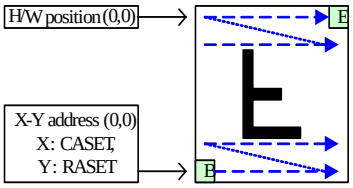
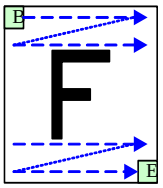
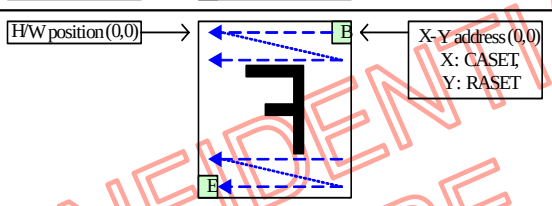
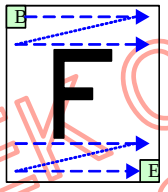
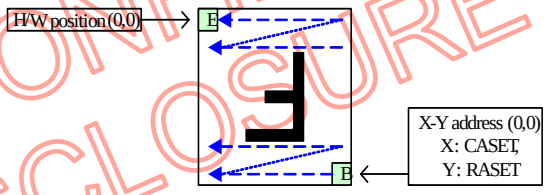
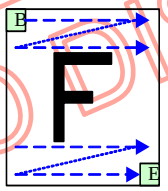
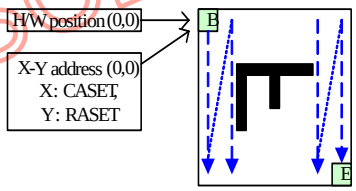
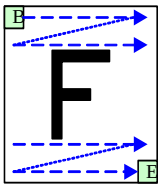
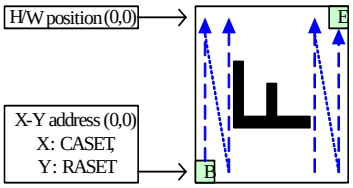
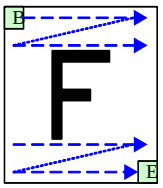
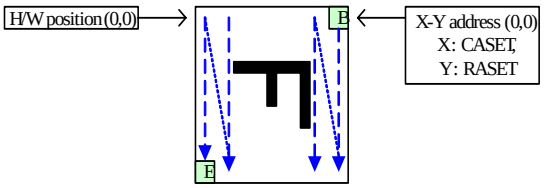
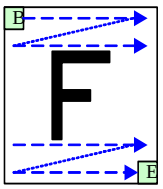
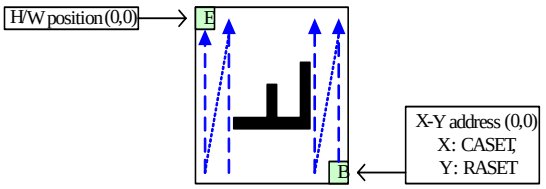
In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTR" (see section 9 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Fig. 8.2.3 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as Fig. 8.2.3 below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

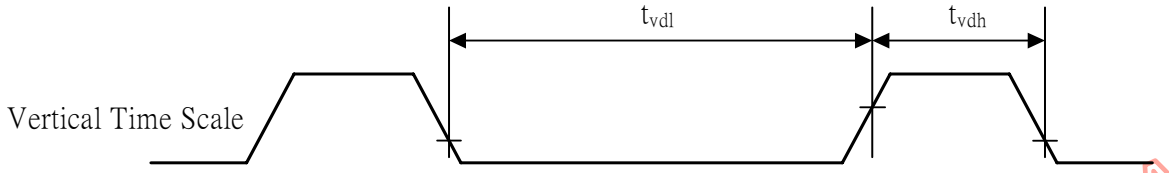
Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y- Mirror	0	0	1		
X- Mirror	0	1	0		
X- Mirror Y- Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y- Mirror	1	0	1		
X-Y Exchange X- Mirror	1	1	0		
X- Y Exchange X- Mirror Y- Mirror	1	1	1		

8.12 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

8.12.1 Tearing Effect Line Modes

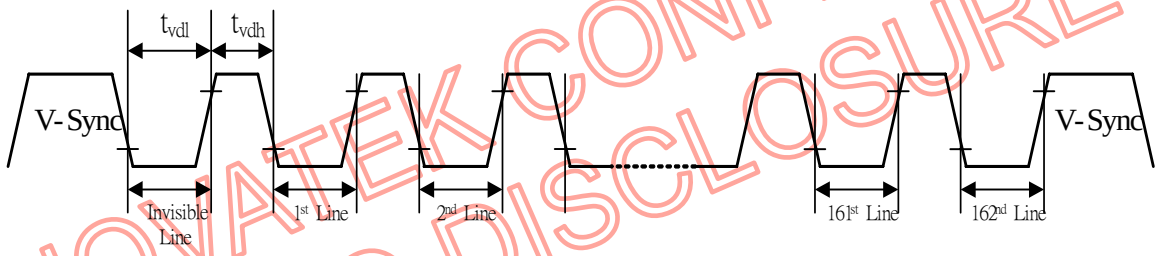
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh= The LCD display is not updated from the Frame Memory

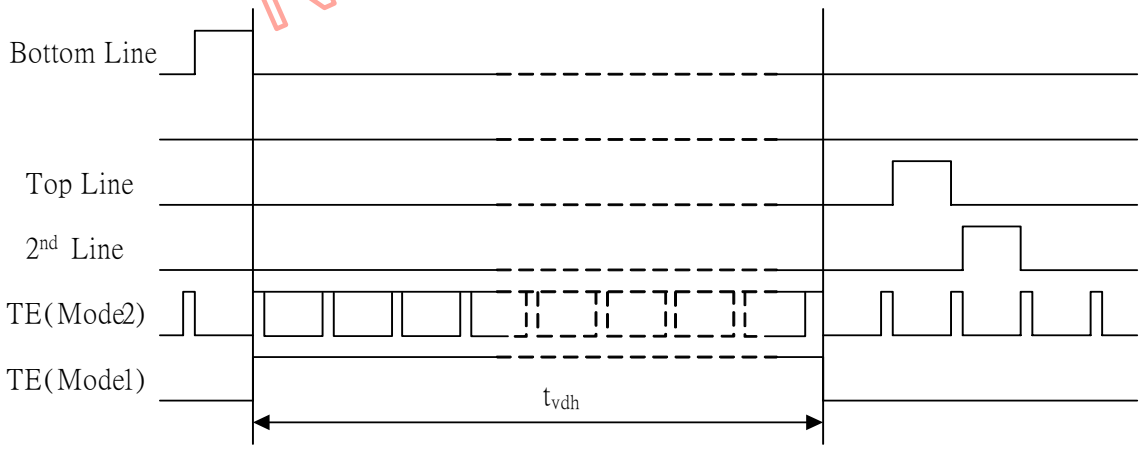
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 162 H-sync pulses per field.



thdh= The LCD display is not updated from the Frame Memory

thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

8.12.2 Tearing Effect Line Timings

The Tearing Effect signal is described below:

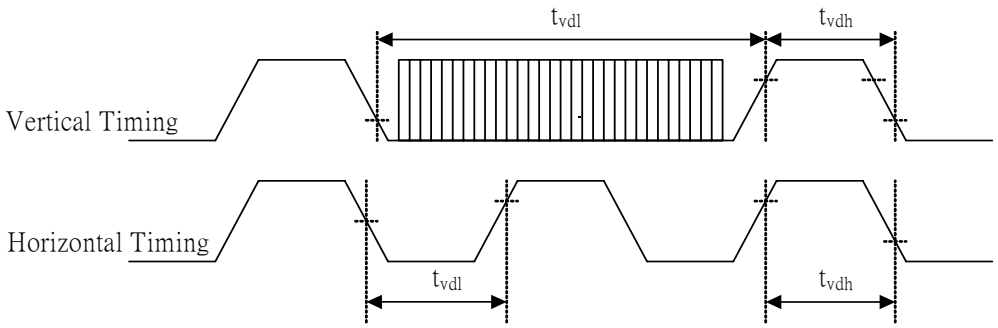


Table 8.3.1 AC characteristics of Tearing Effect Signal

Idle Mode Off (Frame Rate = 58.9 Hz)

Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	μs	
thdl	Horizontal Timing Low Duration	33	-	μs	
thdh	Horizontal Timing High Duration	25	500	μs	

NOTE: The timings in Table 8.3.1 apply when MADCTR ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

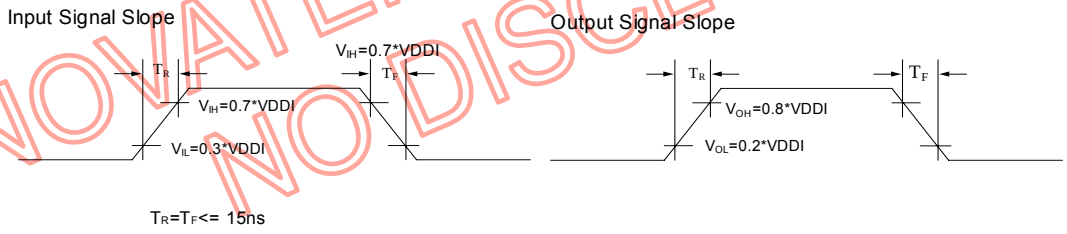
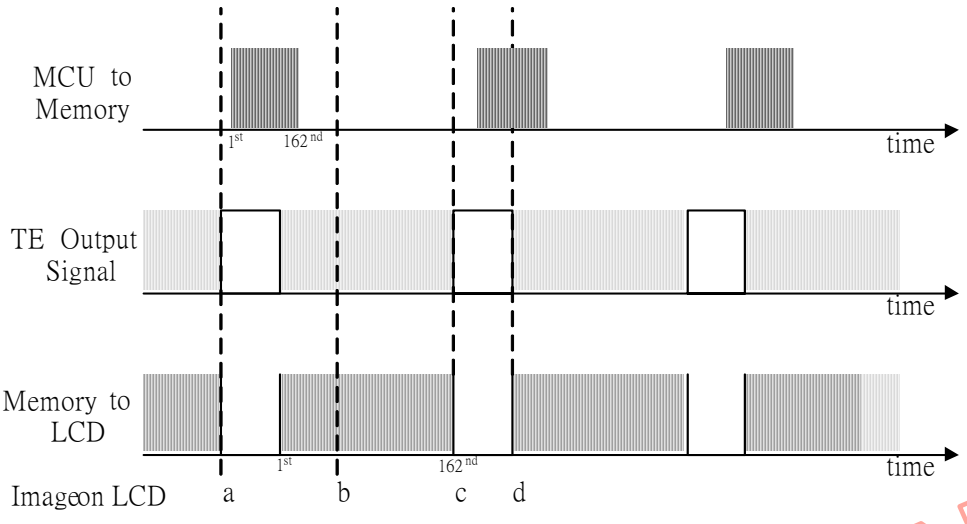


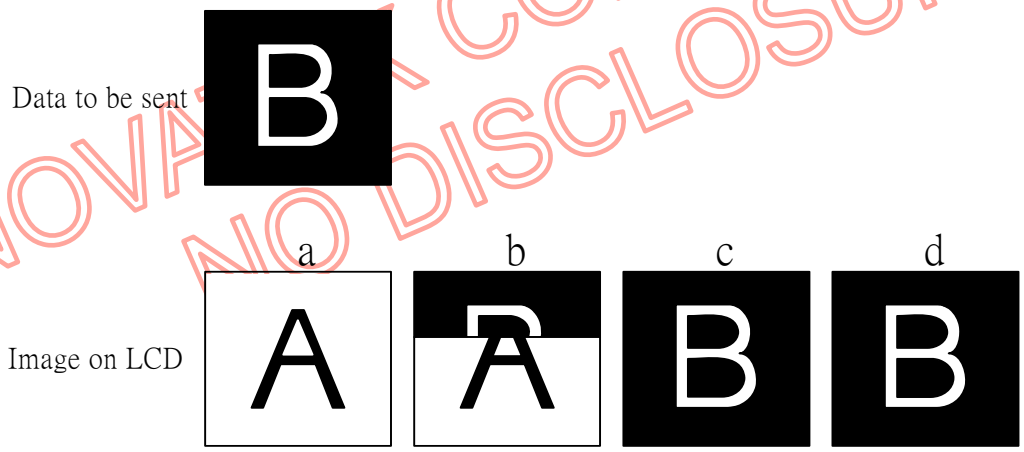
Fig. 7.1.2 Rising and Falling timing for Input and Output signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect.

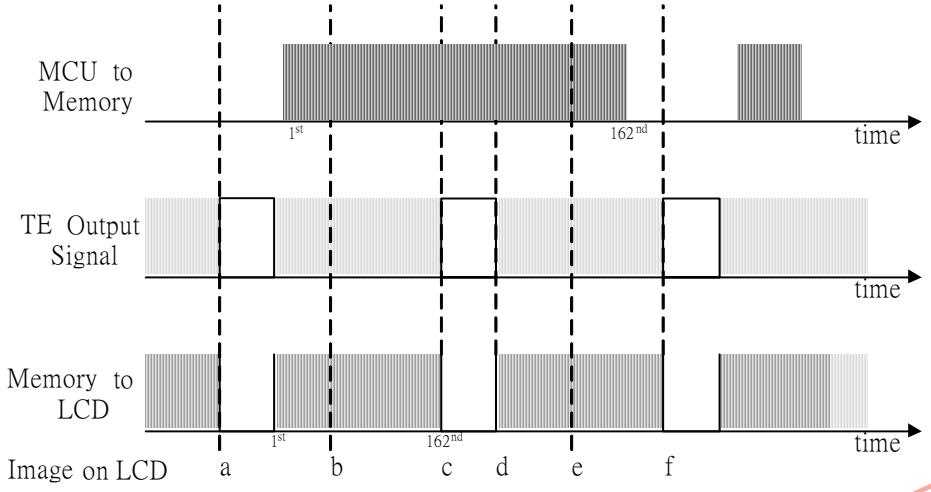
8.12.3 Example 1: MPU Write is faster than panel read.



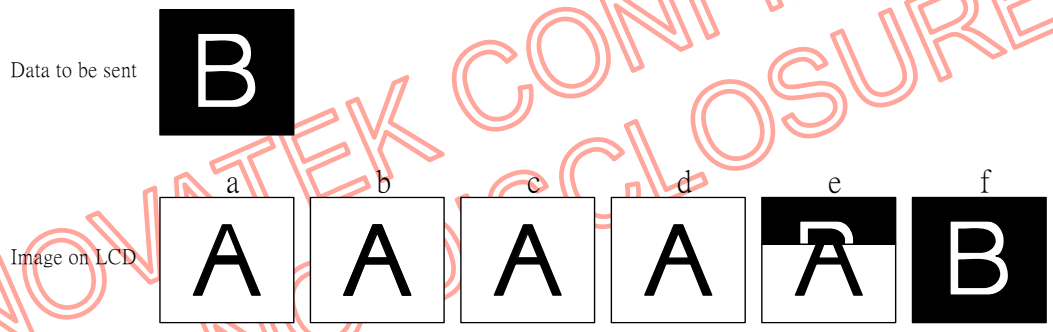
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



8.12.4 Example 2: MPU write is slower than panel read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



8.13 Preset Values

NOVATEK will set preset values on our production line for each display module. Any of these preset values do not need customer's SW support.

8.14 Power ON/OFF Sequence

VDDI and VDD can be applied in any order.
VDDI and VDD can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

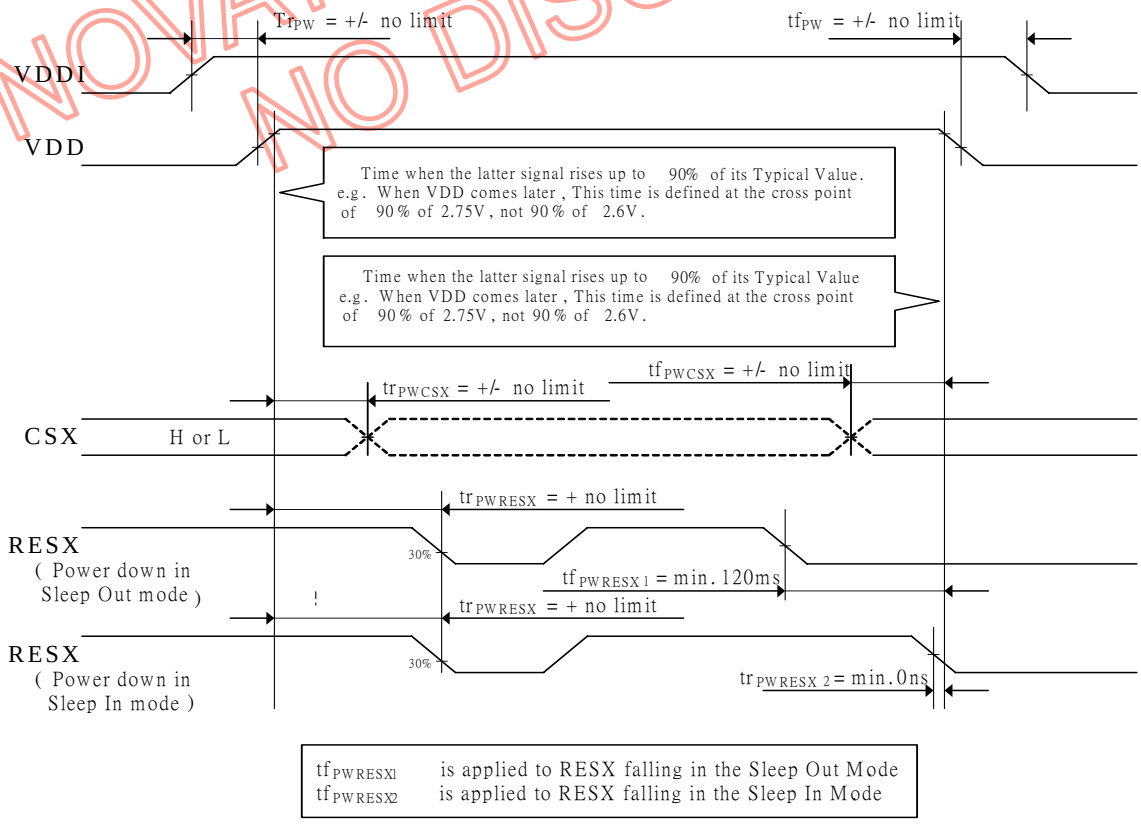
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence as defined in Sections 8.14.1 and 8.14.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

8.14.1 Case 1 – RESX Line is held High or Unstable by Host at Power On

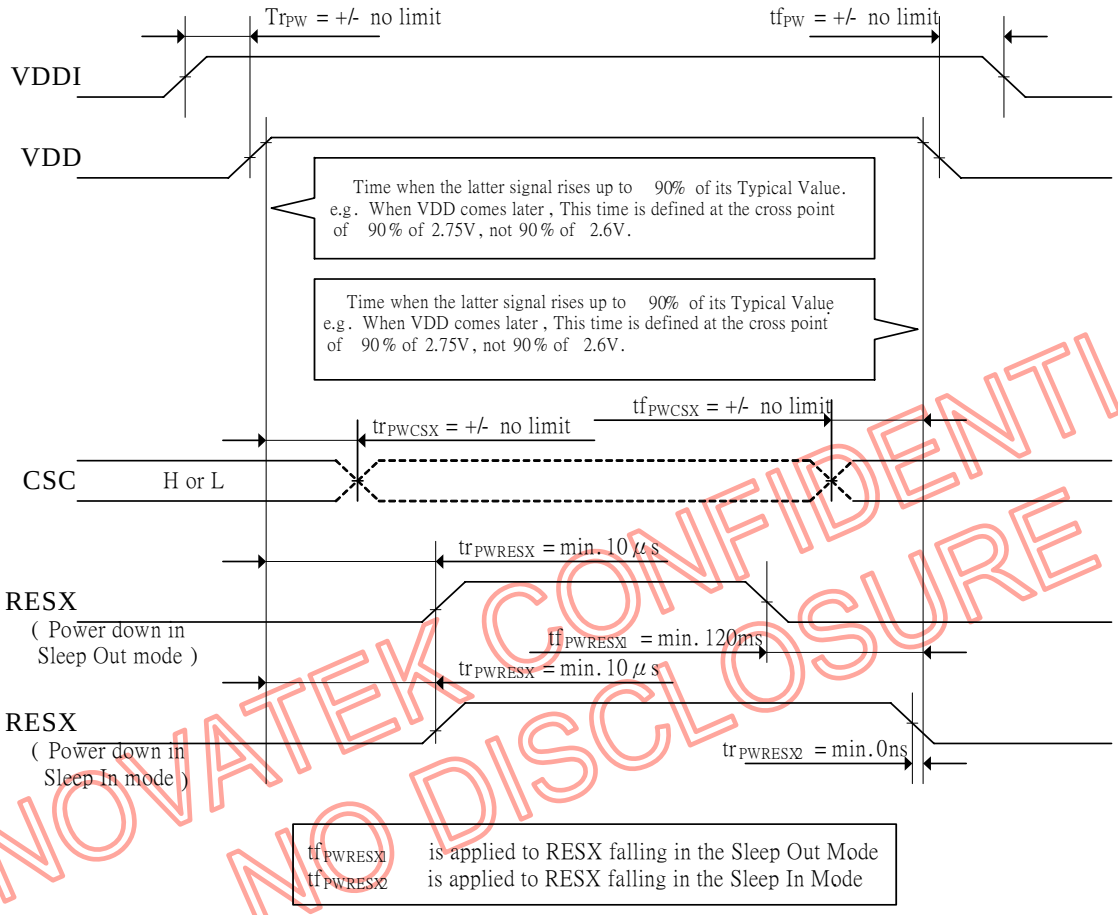
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified , timings herein show cross point at 50 % of signal/power level

8.14.2 Case 2 – RESX Line is Held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after both VDD and VDDI have been applied.



Note: Unless otherwise specified timings herein show cross point at 50 % of signal power level

8.14.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

2. At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

8.15 Power Level Definition

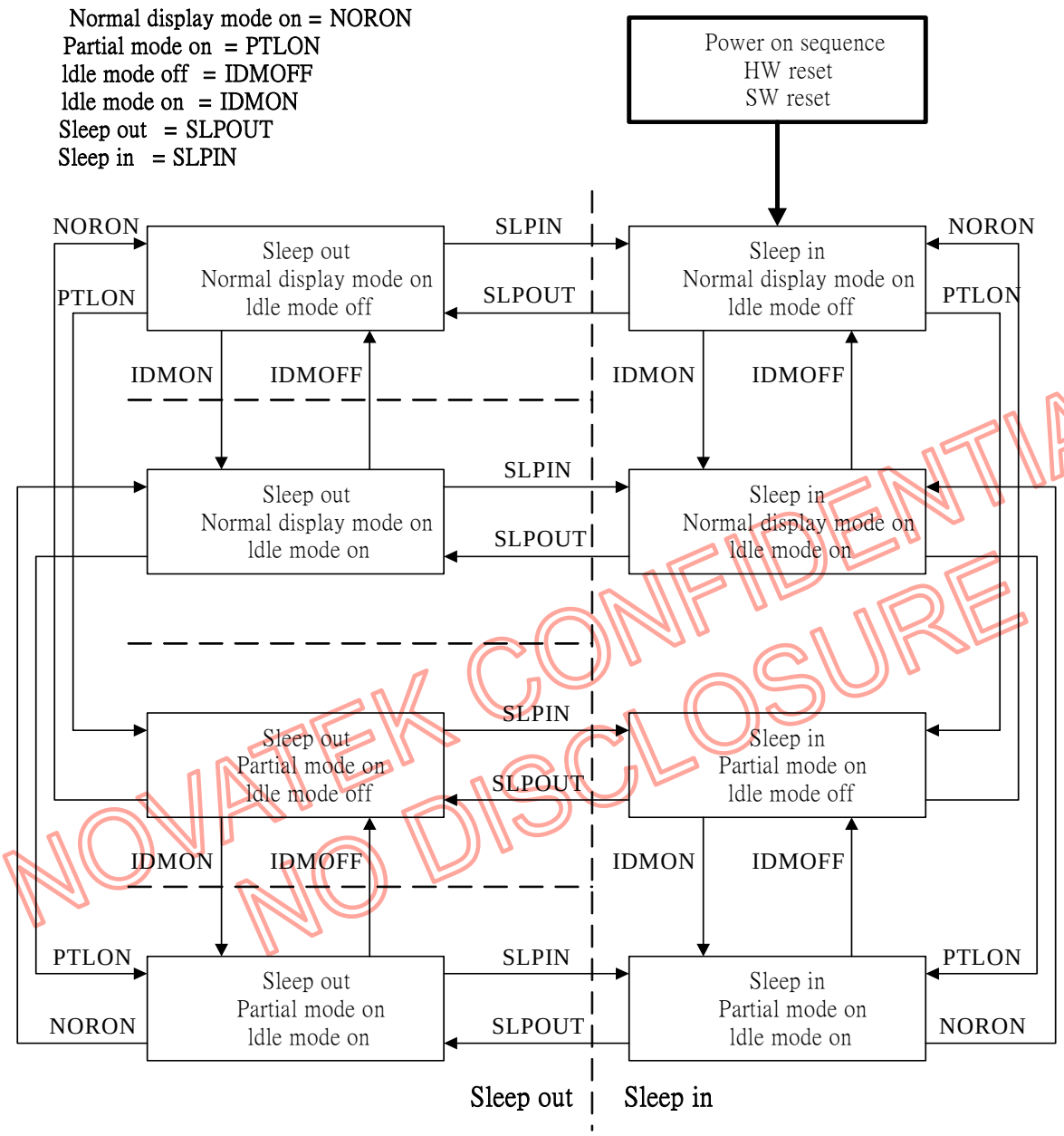
8.15.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. **Normal Mode On (full display), Idle Mode Off, Sleep Out.**
   In this mode, the display is able to show maximum 262,144 colors.
2. **Partial Mode On, Idle Mode Off, Sleep Out.**
   In this mode part of the display is used with maximum 262,144 colors.
3. **Normal Mode On (full display), Idle Mode On, Sleep Out.**
   In this mode, the full display area is used but with 8 colors.
4. **Partial Mode On, Idle Mode On, Sleep Out.**
   In this mode, part of the display is used but with 8 colors.
5. **Sleep In Mode**
   In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU Interface and memory works with VDDI power supply. Contents of the memory are safe.
6. **Power Off Mode**
   In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

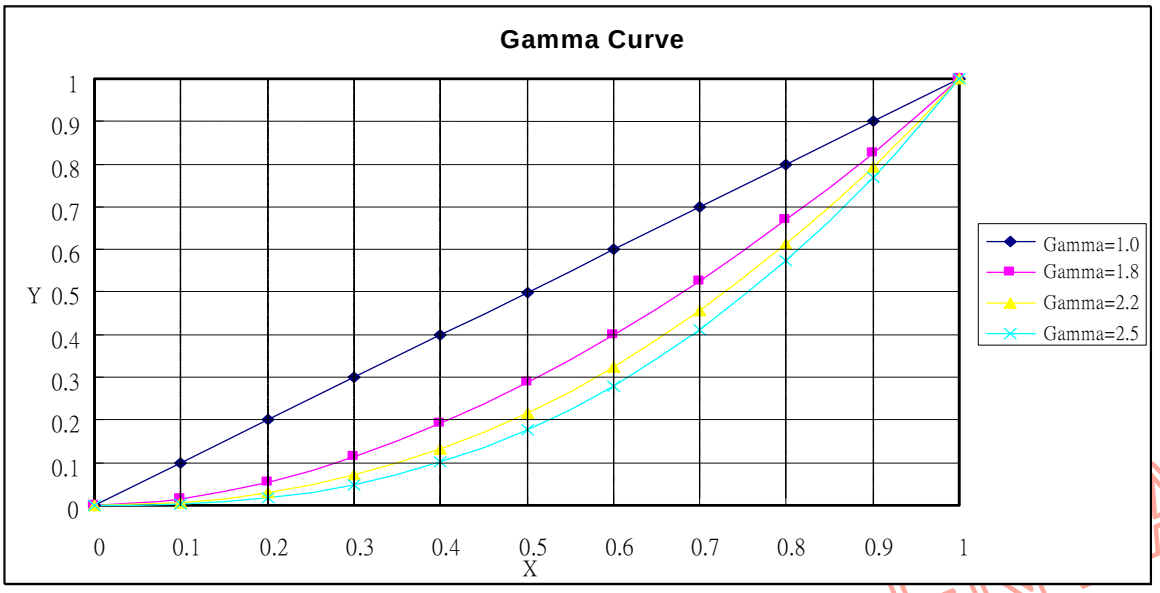
8.15.2 Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

8.16 Gamma Curves



8.17 Reset

8.17.1 Reset Table

8.17.1.1 Reset Table (Default Value, GM=00, 128RGB x 160)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	007Fh	007Fh	007Fh (127d) (when MV=0) 009Fh (159d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	009Fh	009Fh	009Fh (159d) (when MV=0) 007Fh (127d) (when MV=1)
Gamma setting	GC0	GC0	GC0
Colour Set	See Section 8.18	See Section 8.18	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	009Fh	009Fh	009Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00A0h	00A0h	00A0h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	MTP value	MTP value	MTP value
ID3	MTP value	MTP value	MTP value

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.
Notes:2. Powered-On Reset finishes within 10μs after both VDD & VDDI are applied.
Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

8.17.1.2 Reset Table (GM=01, 120RGB x 160)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	0077h	0077h	0077h (119d) (when MV=0) 009Fh (159d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	009Fh	009Fh	009Fh (159d) (when MV=0) 0077h (119d) (when MV=1)
Gamma setting	GC0	GC0	GC0
Colour Set	See Section 8.18	See Section 8.18	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	009Fh	009Fh	009Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00A0h	00A0h	00A0h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	MTP value	MTP value	MTP value
ID3	MTP value	MTP value	MTP value

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.
Notes:2. Powered-On Reset finishes within 10µs after both VDD & VDDI are applied.
Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

8.17.1.3 Reset Table (GM=10, 128RGB x 128)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	007Fh	007Fh	007Fh (127d) (when MV=0) 007Fh (127d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	007Fh	007Fh	007Fh (127d) (when MV=0) 007Fh (127d) (when MV=1)
Gamma setting	GC0	GC0	GC0
Colour Set	See Section 8.18	See Section 8.18	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	007Fh	007Fh	007Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	0080h	0080h	0080h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	MTP value	MTP value	MTP value
ID3	MTP value	MTP value	MTP value

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.
Notes:2. Powered-On Reset finishes within 10µs after both VDD & VDDI are applied.
Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

8.17.1.4 Reset Table (GM=11, 132RGB x 162)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	0083h	0083h	0083h (131d) (when MV=0) 00A1h (161d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	00A1h	00A1h	00A1h (161d) (when MV=0) 0083h (131d) (when MV=1)
Gamma setting	GC0	GC0	GC0
Colour Set	See Section 8.18	See Section 8.18	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	00A1h	00A1h	00A1h
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00A2h	00A2h	00A2h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	MTP value	MTP value	MTP value
ID3	MTP value	MTP value	MTP value

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.
Notes:2. Powered-On Reset finishes within 10µs after both VDD & VDDI are applied.
Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

8.17.2 Module Input/Output Pins

8.17.2.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D17 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

8.17.2.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 8.14	Input valid	Input valid	Input valid	See 8.14
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input Invalid
D17 to D0	Input invalid	Input valid	Input valid	Input valid	input invalid
SDA	Input invalid	Input valid	Input valid	Input valid	input invalid

8.17.3 Reset Timing

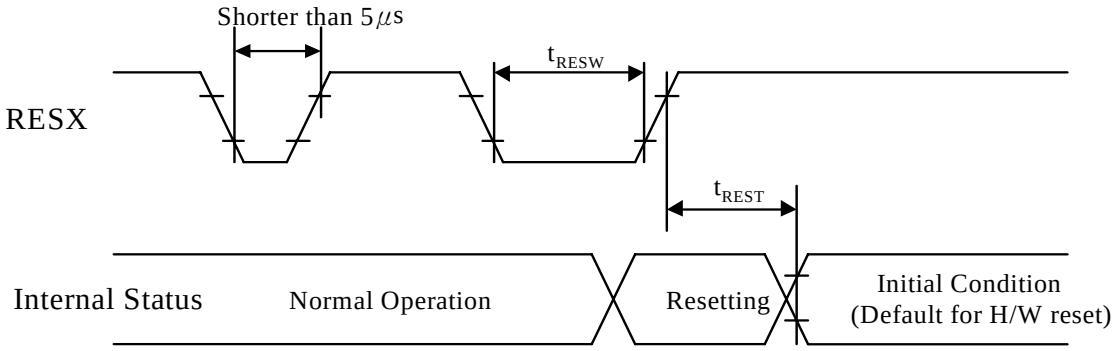


Table 8.7.1 Reset input timing
(VSS=0V, VDDI=1.65V to 1.95V, VDD=2.6V to 2.9V,Ta = -30 to 70°C)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	10	-	-	-	μs
tREST	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

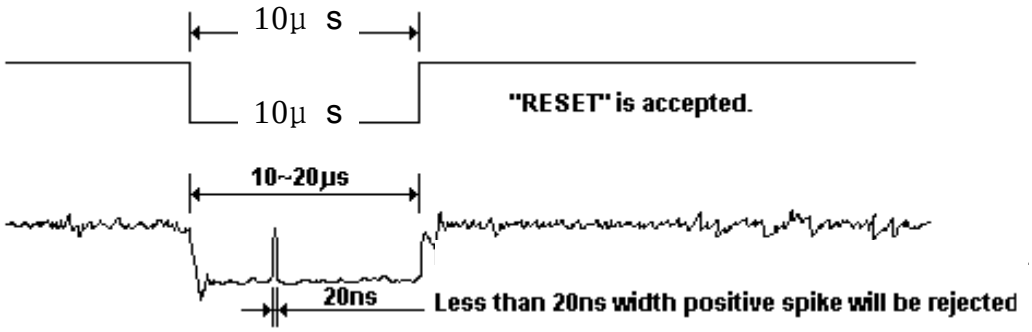
Note 1 Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8.18 Colour Depth Conversion Look Up Tables

8.18.1 65,536 Colour (R-G-B=5-6-5) to 262,144 Colour

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data
				65,536 Color
RED	R_{005} R_{004} R_{003} R_{002} R_{001} R_{000}	000000	1	00000
	R_{015} R_{014} R_{013} R_{012} R_{011} R_{010}	000010	2	00001
	R_{025} R_{024} R_{023} R_{022} R_{021} R_{020}	000100	3	00010
	R_{035} R_{034} R_{033} R_{032} R_{031} R_{030}	000110	4	00011
	R_{045} R_{044} R_{043} R_{042} R_{041} R_{040}	001000	5	00100
	R_{055} R_{054} R_{053} R_{052} R_{051} R_{050}	001010	6	00101
	R_{065} R_{064} R_{063} R_{062} R_{061} R_{060}	001100	7	00110
	R_{075} R_{074} R_{073} R_{072} R_{071} R_{070}	001110	8	00111
	R_{085} R_{084} R_{083} R_{082} R_{081} R_{080}	010000	9	01000
	R_{095} R_{094} R_{093} R_{092} R_{091} R_{090}	010010	10	01001
	R_{105} R_{104} R_{103} R_{102} R_{101} R_{100}	010100	11	01010
	R_{115} R_{114} R_{113} R_{112} R_{111} R_{110}	010110	12	01011
	R_{125} R_{124} R_{123} R_{122} R_{121} R_{120}	011000	13	01100
	R_{135} R_{134} R_{133} R_{132} R_{131} R_{130}	011010	14	01101
	R_{145} R_{144} R_{143} R_{142} R_{141} R_{140}	011100	15	01110
	R_{155} R_{154} R_{153} R_{152} R_{151} R_{150}	011110	16	01111
	R_{165} R_{164} R_{163} R_{162} R_{161} R_{160}	100001	17	10000
	R_{175} R_{174} R_{173} R_{172} R_{171} R_{170}	100011	18	10001
	R_{185} R_{184} R_{183} R_{182} R_{181} R_{180}	100101	19	10010
	R_{195} R_{194} R_{193} R_{192} R_{191} R_{190}	100111	20	10011
	R_{205} R_{204} R_{203} R_{202} R_{201} R_{200}	101001	21	10100
	R_{215} R_{214} R_{213} R_{212} R_{211} R_{210}	101011	22	10101
	R_{225} R_{224} R_{223} R_{222} R_{221} R_{220}	101101	23	10110
	R_{235} R_{234} R_{233} R_{232} R_{231} R_{230}	101111	24	10111
	R_{245} R_{244} R_{243} R_{242} R_{241} R_{240}	110001	25	11000
	R_{255} R_{254} R_{253} R_{252} R_{251} R_{250}	110011	26	11001
	R_{265} R_{264} R_{263} R_{262} R_{261} R_{260}	110101	27	11010
	R_{275} R_{274} R_{273} R_{272} R_{271} R_{270}	110111	28	11011
	R_{285} R_{284} R_{283} R_{282} R_{281} R_{280}	111001	29	11100
	R_{295} R_{294} R_{293} R_{292} R_{291} R_{290}	111011	30	11101
	R_{305} R_{304} R_{303} R_{302} R_{301} R_{300}	111101	31	11110
	R_{315} R_{314} R_{313} R_{312} R_{311} R_{310}	111111	32	11111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data 65,536 Color
GREEN	G_{005} $G_{004}G_{003}G_{002}G_{001}G_{000}$	000000	33	000000
	$G_{015}G_{014}G_{013}G_{012}G_{011}G_{010}$	000001	34	000001
	$G_{025}G_{024}G_{023}G_{022}G_{021}G_{020}$	000010	35	000010
	$G_{035}G_{034}G_{033}G_{032}G_{031}G_{030}$	000011	36	000011
	$G_{045}G_{044}G_{043}G_{042}G_{041}G_{040}$	000100	37	000100
	$G_{055}G_{054}G_{053}G_{052}G_{051}G_{050}$	000101	38	000101
	$G_{065}G_{064}G_{063}G_{062}G_{061}G_{060}$	000110	39	000110
	$G_{075}G_{074}G_{073}G_{072}G_{071}G_{070}$	000111	40	000111
	$G_{085}G_{084}G_{083}G_{082}G_{081}G_{080}$	001000	41	001000
	$G_{095}G_{094}G_{093}G_{092}G_{091}G_{090}$	001001	42	001001
	$G_{105}G_{104}G_{103}G_{102}G_{101}G_{100}$	001010	43	001010
	$G_{115}G_{114}G_{113}G_{112}G_{111}G_{110}$	001011	44	001011
	$G_{125}G_{124}G_{123}G_{122}G_{121}G_{120}$	001100	45	001100
	$G_{135}G_{134}G_{133}G_{132}G_{131}G_{130}$	001101	46	001101
	$G_{145}G_{144}G_{143}G_{142}G_{141}G_{140}$	001110	47	001110
	$G_{155}G_{154}G_{153}G_{152}G_{151}G_{150}$	001111	48	001111
	G_{165} $G_{164}G_{163}G_{162}G_{161}G_{160}$	010000	49	010000
	$G_{175}G_{174}G_{173}G_{172}G_{171}G_{170}$	010001	50	010001
	$G_{185}G_{184}G_{183}G_{182}G_{181}G_{180}$	010010	51	010010
	$G_{195}G_{194}G_{193}G_{192}G_{191}G_{190}$	010011	52	010011
	$G_{205}G_{204}G_{203}G_{202}G_{201}G_{200}$	010100	53	010100
	$G_{215}G_{214}G_{213}G_{212}G_{211}G_{210}$	010101	54	010101
	$G_{225}G_{224}G_{223}G_{222}G_{221}G_{220}$	010110	55	010110
	$G_{235}G_{234}G_{233}G_{232}G_{231}G_{230}$	010111	56	010111
	$G_{245}G_{244}G_{243}G_{242}G_{241}G_{240}$	011000	57	011000
	$G_{255}G_{254}G_{253}G_{252}G_{251}G_{250}$	011001	58	011001
	$G_{265}G_{264}G_{263}G_{262}G_{261}G_{260}$	011010	59	011010
	$G_{275}G_{274}G_{273}G_{272}G_{271}G_{270}$	011011	60	011011
	$G_{285}G_{284}G_{283}G_{282}G_{281}G_{280}$	011100	61	011100
	$G_{295}G_{294}G_{293}G_{292}G_{291}G_{290}$	011101	62	011101
	$G_{305}G_{304}G_{303}G_{302}G_{301}G_{300}$	011110	63	011110
	$G_{315}G_{314}G_{313}G_{312}G_{311}G_{310}$	011111	64	011111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data
				65,536 Color
GREEN	G_{325} $G_{324}G_{323}G_{322}G_{321}G_{320}$	100000	65	100000
	$G_{335}G_{334}G_{333}G_{332}G_{331}G_{330}$	100001	66	100001
	$G_{345}G_{344}G_{343}G_{342}G_{341}G_{340}$	100010	67	100010
	$G_{355}G_{354}G_{353}G_{352}G_{351}G_{350}$	100011	68	100011
	$G_{365}G_{364}G_{363}G_{362}G_{361}G_{360}$	100100	69	100100
	$G_{375}G_{374}G_{373}G_{372}G_{371}G_{370}$	100101	70	100101
	$G_{385}G_{384}G_{383}G_{382}G_{381}G_{380}$	100110	71	100110
	$G_{395}G_{394}G_{393}G_{392}G_{391}G_{390}$	100111	72	100111
	$G_{405}G_{404}G_{403}G_{402}G_{401}G_{400}$	101000	73	101000
	$G_{415}G_{414}G_{413}G_{412}G_{411}G_{410}$	101001	74	101001
	$G_{425}G_{424}G_{423}G_{422}G_{421}G_{420}$	101010	75	101010
	$G_{435}G_{434}G_{433}G_{432}G_{431}G_{430}$	101011	76	101011
	$G_{445}G_{444}G_{443}G_{442}G_{441}G_{440}$	101100	77	101100
	$G_{455}G_{454}G_{453}G_{452}G_{451}G_{450}$	101101	78	101101
	$G_{465}G_{464}G_{463}G_{462}G_{461}G_{460}$	101110	79	101110
	$G_{475}G_{474}G_{473}G_{472}G_{471}G_{470}$	101111	80	101111
	G_{485} $G_{484}G_{483}G_{482}G_{481}G_{480}$	110000	81	110000
	$G_{495}G_{494}G_{493}G_{492}G_{491}G_{490}$	110001	82	110001
	$G_{505}G_{504}G_{503}G_{502}G_{501}G_{500}$	110010	83	110010
	$G_{515}G_{514}G_{513}G_{512}G_{511}G_{510}$	110011	84	110011
	$G_{525}G_{524}G_{523}G_{522}G_{521}G_{520}$	110100	85	110100
	$G_{535}G_{534}G_{533}G_{532}G_{531}G_{530}$	110101	86	110101
	$G_{545}G_{544}G_{543}G_{542}G_{541}G_{540}$	110110	87	110110
	$G_{555}G_{554}G_{553}G_{552}G_{551}G_{550}$	110111	88	110111
	$G_{565}G_{564}G_{563}G_{562}G_{561}G_{560}$	111000	89	111000
	$G_{575}G_{574}G_{573}G_{572}G_{571}G_{570}$	111001	90	111001
	$G_{585}G_{584}G_{583}G_{582}G_{581}G_{580}$	111010	91	111010
	$G_{595}G_{594}G_{593}G_{592}G_{591}G_{590}$	111011	92	111011
	$G_{605}G_{604}G_{603}G_{602}G_{601}G_{600}$	111100	93	111100
	$G_{615}G_{614}G_{613}G_{612}G_{611}G_{610}$	111101	94	111101
	$G_{625}G_{624}G_{623}G_{622}G_{621}G_{620}$	111110	95	111110
	$G_{635}G_{634}G_{633}G_{632}G_{631}G_{630}$	111111	96	111111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data
				65,536 Color
BLUE	B_{005} $B_{004}B_{003}B_{002}B_{001}B_{000}$	000000	97	00000
	$B_{015}B_{014}B_{013}B_{012}B_{011}B_{010}$	000010	98	00001
	$B_{025}B_{024}B_{023}B_{022}B_{021}B_{020}$	000100	99	00010
	$B_{035}B_{034}B_{033}B_{032}B_{031}B_{030}$	000110	100	00011
	$B_{045}B_{044}B_{043}B_{042}B_{041}B_{040}$	001000	101	00100
	$B_{055}B_{054}B_{053}B_{052}B_{051}B_{050}$	001010	102	00101
	$B_{065}B_{064}B_{063}B_{062}B_{061}B_{060}$	001100	103	00110
	$B_{075}B_{074}B_{073}B_{072}B_{071}B_{070}$	001110	104	00111
	$B_{085}B_{084}B_{083}B_{082}B_{081}B_{080}$	010000	105	01000
	$B_{095}B_{094}B_{093}B_{092}B_{091}B_{090}$	010010	106	01001
	$B_{105}B_{104}B_{103}B_{102}B_{101}B_{100}$	010100	107	01010
	$B_{115}B_{114}B_{113}B_{112}B_{111}B_{110}$	010110	108	01011
	$B_{125}B_{124}B_{123}B_{122}B_{121}B_{120}$	011000	109	01100
	$B_{135}B_{134}B_{133}B_{132}B_{131}B_{130}$	011010	110	01101
	$B_{145}B_{144}B_{143}B_{142}B_{141}B_{140}$	011100	111	01110
	$B_{155}B_{154}B_{153}B_{152}B_{151}B_{150}$	011110	112	01111
	B_{165} $B_{164}B_{163}B_{162}B_{161}B_{160}$	100001	113	10000
	$B_{175}B_{174}B_{173}B_{172}B_{171}B_{170}$	100011	114	10001
	$B_{185}B_{184}B_{183}B_{182}B_{181}B_{180}$	100101	115	10010
	$B_{195}B_{194}B_{193}B_{192}B_{191}B_{190}$	100111	116	10011
	$B_{205}B_{204}B_{203}B_{202}B_{201}B_{200}$	101001	117	10100
	$B_{215}B_{214}B_{213}B_{212}B_{211}B_{210}$	101011	118	10101
	$B_{225}B_{224}B_{223}B_{222}B_{221}B_{220}$	101101	119	10110
	$B_{235}B_{234}B_{233}B_{232}B_{231}B_{230}$	101111	120	10111
	$B_{245}B_{244}B_{243}B_{242}B_{241}B_{240}$	110001	121	11000
	$B_{255}B_{254}B_{253}B_{252}B_{251}B_{250}$	110011	122	11001
	$B_{265}B_{264}B_{263}B_{262}B_{261}B_{260}$	110101	123	11010
	$B_{275}B_{274}B_{273}B_{272}B_{271}B_{270}$	110111	124	11011
	$B_{285}B_{284}B_{283}B_{282}B_{281}B_{280}$	111001	125	11100
	$B_{295}B_{294}B_{293}B_{292}B_{291}B_{290}$	111011	126	11101
	$B_{305}B_{304}B_{303}B_{302}B_{301}B_{300}$	111101	127	11110
	$B_{315}B_{314}B_{313}B_{312}B_{311}B_{310}$	111111	128	11111

8.18.2 4,096 Colour (R-G-B=4-4-4) to 262,144 Colour

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data
				4,096 Color
RED	R_{005} R_{004} R_{003} R_{002} R_{001} R_{000}	000000	1	0000
	R_{015} R_{014} R_{013} R_{012} R_{011} R_{010}	000100	2	0001
	R_{025} R_{024} R_{023} R_{022} R_{021} R_{020}	001000	3	0010
	R_{035} R_{034} R_{033} R_{032} R_{031} R_{030}	001100	4	0011
	R_{045} R_{044} R_{043} R_{042} R_{041} R_{040}	010001	5	0100
	R_{055} R_{054} R_{053} R_{052} R_{051} R_{050}	010101	6	0101
	R_{065} R_{064} R_{063} R_{062} R_{061} R_{060}	011001	7	0110
	R_{075} R_{074} R_{073} R_{072} R_{071} R_{070}	011101	8	0111
	R_{085} R_{084} R_{083} R_{082} R_{081} R_{080}	100010	9	1000
	R_{095} R_{094} R_{093} R_{092} R_{091} R_{090}	100110	10	1001
	R_{105} R_{104} R_{103} R_{102} R_{101} R_{100}	101010	11	1010
	R_{115} R_{114} R_{113} R_{112} R_{111} R_{110}	101110	12	1011
	R_{125} R_{124} R_{123} R_{122} R_{121} R_{120}	110011	13	1100
	R_{135} R_{134} R_{133} R_{132} R_{131} R_{130}	110111	14	1101
	R_{145} R_{144} R_{143} R_{142} R_{141} R_{140}	111011	15	1110
	R_{155} R_{154} R_{153} R_{152} R_{151} R_{150}	111111	16	1111
	R_{165} R_{164} R_{163} R_{162} R_{161} R_{160}	-	17	Not Used
	|	|	|	
	R_{315} R_{314} R_{313} R_{312} R_{311} R_{310}	-	32	

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data
				4,096 Color
GREEN	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	000000	33	0000
	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	000100	34	0001
	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	001000	35	0010
	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	001100	36	0011
	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	010001	37	0100
	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	010101	38	0101
	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	011001	39	0110
	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	011101	40	0111
	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	100010	41	1000
	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}	100110	42	1001
	G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}	101010	43	1010
	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}	101110	44	1011
	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}	110011	45	1100
	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}	110111	46	1101
	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}	111011	47	1110
	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}	111111	48	1111
	G_{165} G_{164} G_{163} G_{162} G_{161} G_{160}	-	49	Not Used
	|	|	|	
	G_{635} G_{634} G_{633} G_{632} G_{631} G_{630}	-	96	

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data
				4,096 Color
BLUE	B_{005} $B_{004}B_{003}B_{002}B_{001}B_{000}$	000000	97	0000
	$B_{015}B_{014}B_{013}B_{012}B_{011}B_{010}$	000100	98	0001
	$B_{025}B_{024}B_{023}B_{022}B_{021}B_{020}$	001000	99	0010
	$B_{035}B_{034}B_{033}B_{032}B_{031}B_{030}$	001100	100	0011
	$B_{045}B_{044}B_{043}B_{042}B_{041}B_{040}$	010001	101	0100
	$B_{055}B_{054}B_{053}B_{052}B_{051}B_{050}$	010101	102	0101
	$B_{065}B_{064}B_{063}B_{062}B_{061}B_{060}$	011001	103	0110
	$B_{075}B_{074}B_{073}B_{072}B_{071}B_{070}$	011101	104	0111
	$B_{085}B_{084}B_{083}B_{082}B_{081}B_{080}$	100010	105	1000
	$B_{095}B_{094}B_{093}B_{092}B_{091}B_{090}$	100110	106	1001
	$B_{105}B_{104}B_{103}B_{102}B_{101}B_{100}$	101010	107	1010
	$B_{115}B_{114}B_{113}B_{112}B_{111}B_{110}$	101110	108	1011
	$B_{125}B_{124}B_{123}B_{122}B_{121}B_{120}$	110011	109	1100
	$B_{135}B_{134}B_{133}B_{132}B_{131}B_{130}$	110111	110	1101
	$B_{145}B_{144}B_{143}B_{142}B_{141}B_{140}$	111011	111	1110
	$B_{155}B_{154}B_{153}B_{152}B_{151}B_{150}$	111111	112	1111
	B_{165} $B_{164}B_{163}B_{162}B_{161}B_{160}$	-	113	Not Used
	|	|	|	
	$B_{315}B_{314}B_{313}B_{312}B_{311}B_{310}$	-	128	

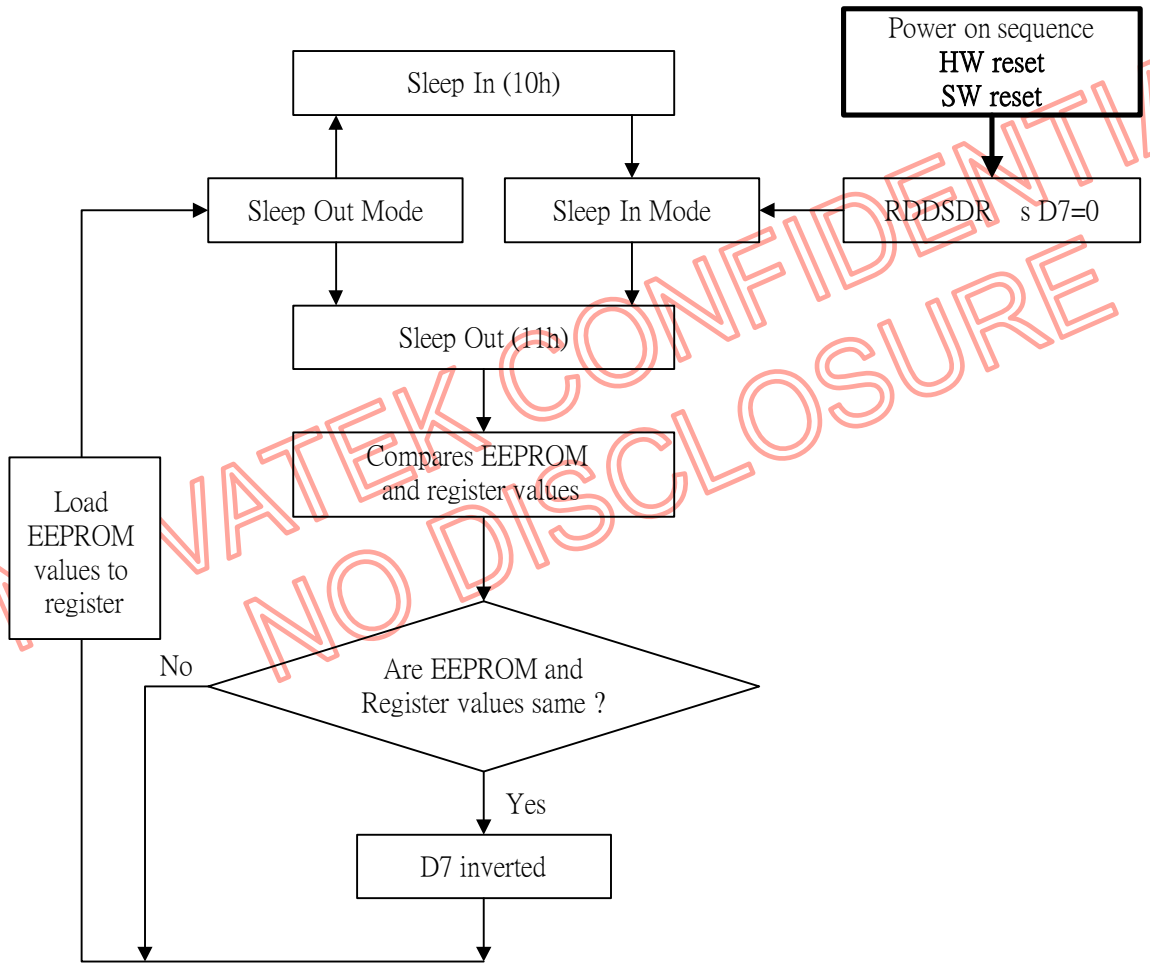
8.19 Sleep Out-Command and Self-Diagnostic Functions of the Display Module

8.19.1 Register Loading Detection

Sleep Out-command (See section 9.1.12 "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command 9.1.10 "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:



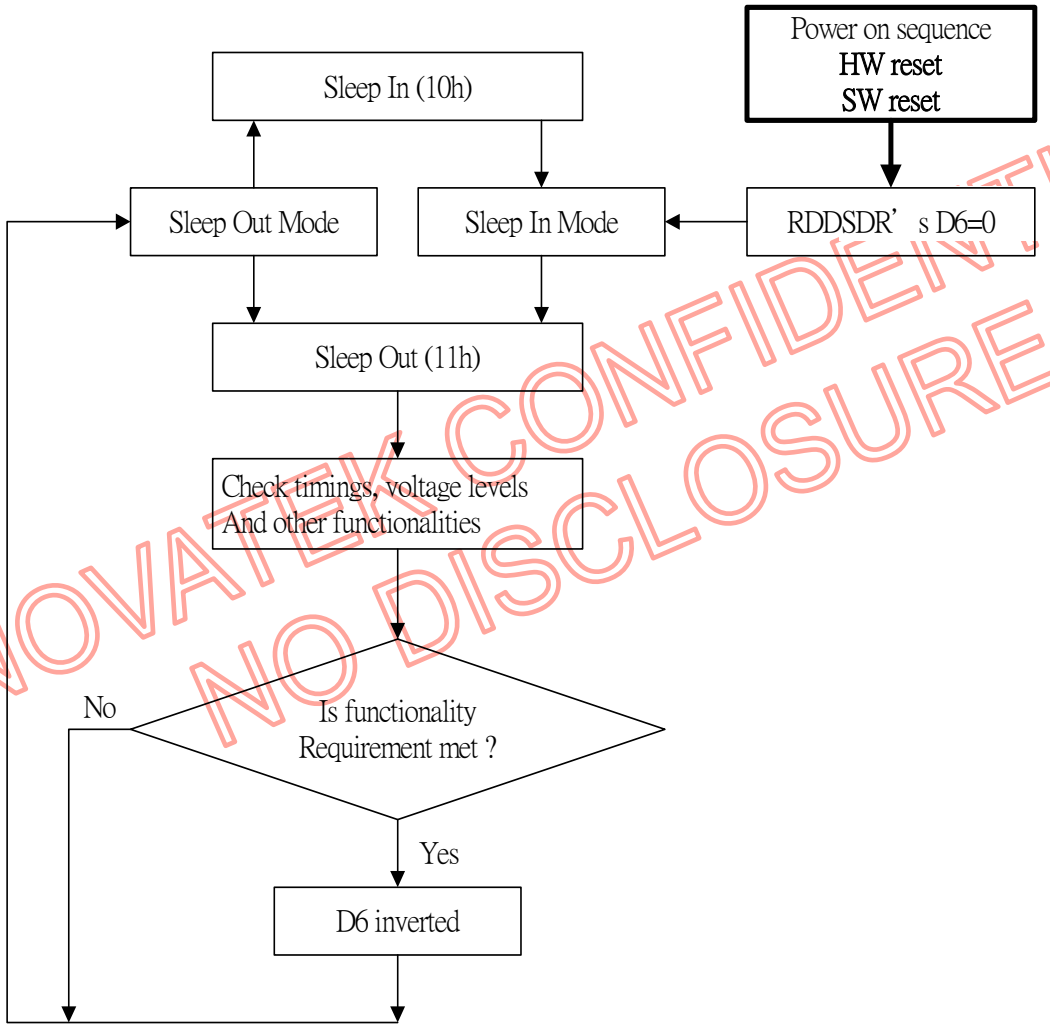
Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

8.19.2 Functionality Detection

Sleep Out-command (See section 9.1.12 "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command 9.1.10 "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).

The flow chart for this internal function is following:



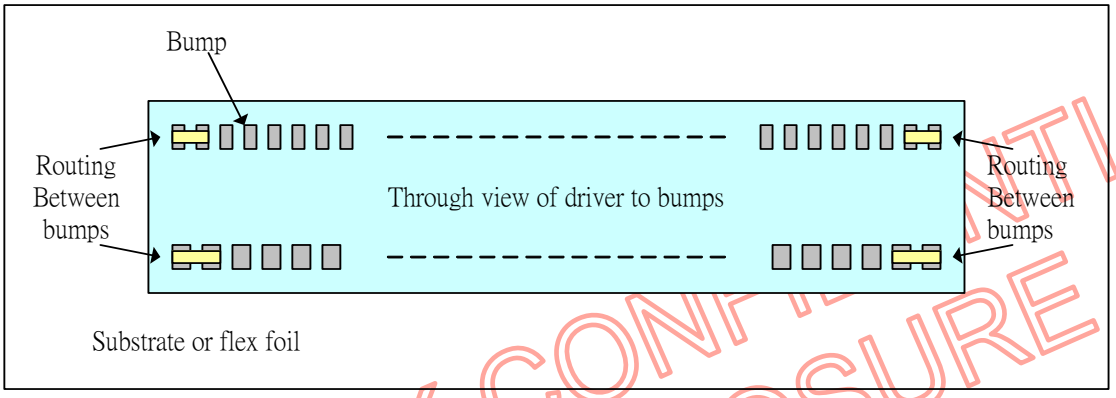
Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.

8.19.3 Chip Attachment Detection

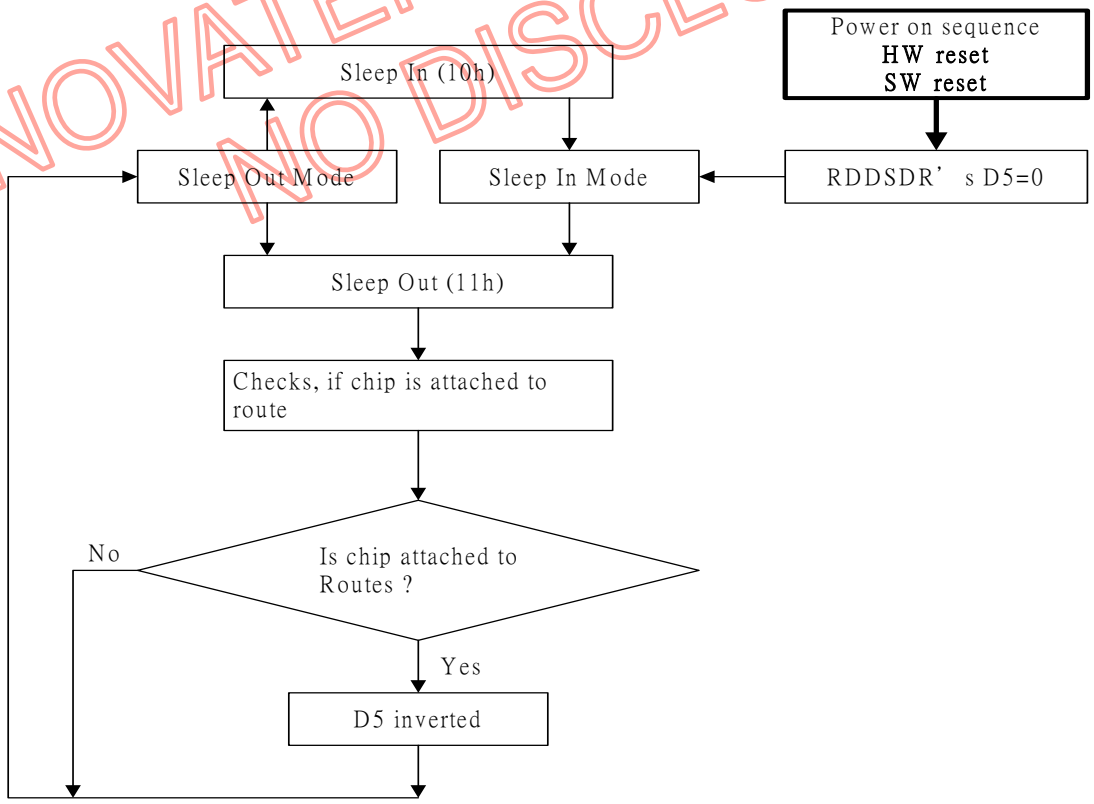
Sleep Out-command (See section 9.1.12 "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if a chip or chips (e.g. driver, etc.) of the display module is/are attached to the circuit route of a flex foil or display glass ITO.

There is inverted (= increased by 1) a bit, which is defined in command 9.1.10 "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D5), if the chip or chips is/are attached to the circuit route of the flex or display glass. If this chip is or those chips are not attached to the circuit route of the flex or display glass, this bit (D5) is not inverted (= increased by 1).

The following figure is for reference purposes; how this chip attachment can be implemented e.g. there are connected together 2 bumps via route of ITO or the flex foil on 4 corners of the driver (chip).



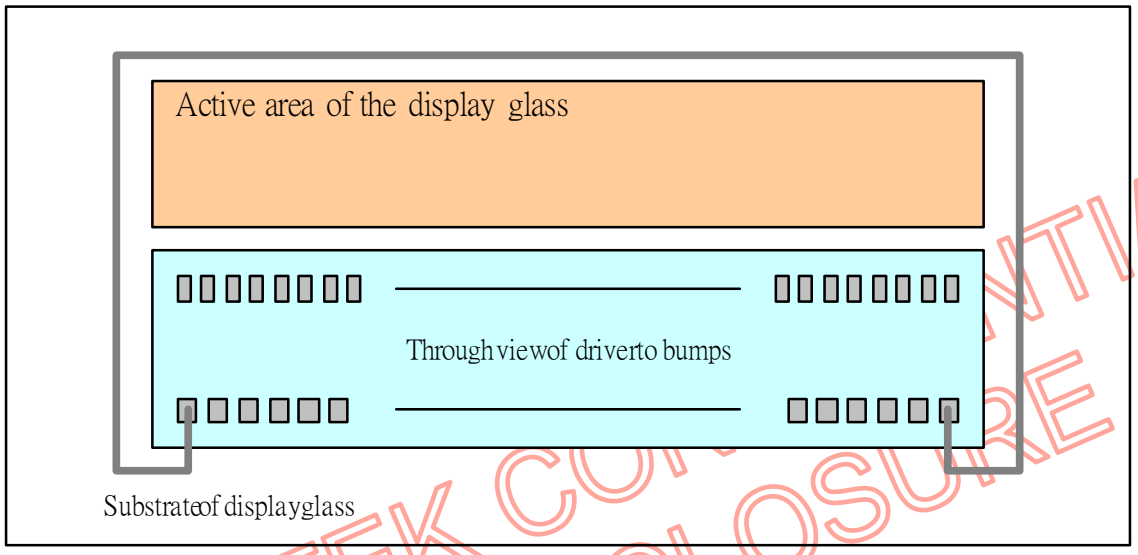
The flow chart for this internal function is following:



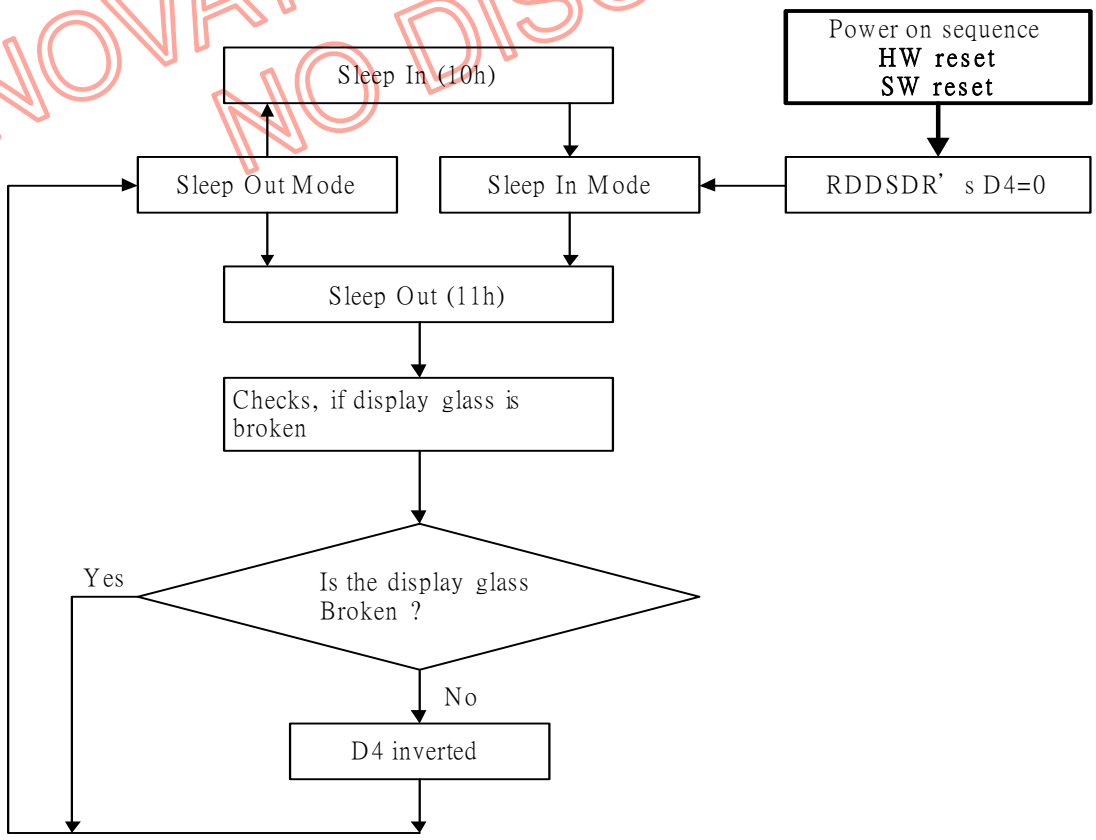
8.19.4 Display Glass Break Detection

Sleep Out-command (See section 9.1.12 "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display glass of the display module is broken or not.

There is inverted (= increased by 1) a bit, which is defined in command 9.1.10 "Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D4), if the display glass is not broken. If this display glass is broken, this bit (D4) is not inverted (= increased by 1).
The following figure is a reference, how this glass break detection can be implemented e.g. there is connected together 2 bumps via route of ITO. This route of ITO is the nearest route of the edge of the display glass.



The flow chart for this internal function is following:



9. Command

9.1 System function Command List and Description

Table 9.1.1 System Function command List (1)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
NOP	9.1.1	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	9.1.2	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	9.1.3	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	38h	ID1 read
		1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h	ID2 read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	4Fh	ID3 read
RDDST	9.1.4	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	00h	-
		1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	71h	-
		1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	00h	-
		1	1	↑	-	GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0	00h	-
RDDPM	9.1.5	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	08h	-
RDD MADCTR	9.1.6	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display MADCTR
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	MY	MX	MV	ML	RGB	MH	D1	D0	00h	-
RDD COLMOD	9.1.7	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h	-
RDDIM	9.1.8	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	00h	-
RDDSM	9.1.9	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	TEON	TELOM	HSON	VSON	PCKON	DEON	D1	D0	00h	-
RDDSDR	9.1.10	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read Display Self-diagnostic result
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	RELD	FUND	ATTD	BRD	D3	D2	D1	D0	00h	-

"-": Don't care

Table 9.1.1 System Function command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
SLPIN	9.1.11	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in & booster off
SLPOUT	9.1.12	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out & booster on
PTLON	9.1.13	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	9.1.14	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	9.1.15	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off (normal)
INVON	9.1.16	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	9.1.17	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma curve select
		1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h	-
DISPOFF	9.1.18	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	9.1.19	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET X=7Fh,	9.1.20	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
		1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	-	X address start: 0 ≤XS ≤X
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-	
		1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	-	X address end: XS ≤XE ≤X
		1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-	
RASET Y=9Fh	9.1.21	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
		1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-	Y address start: 0 ≤ YS ≤ Y
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-	
		1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	-	Y address end: YS ≤ YE ≤ Y
		1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-	
RAMWR	9.1.22	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
		1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0		Write data
RAMHD	9.1.23	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0		Read data
RGBSET a = 31, b = 63, c = 31	9.1.24	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)	LUT for 65k , 262K color display
		1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000		Red tone 0
		1	↑	1	:	:	:	:	:	:	:	:	:		: -
		1	↑	1	-	-	-	Ra5	Ra4	Ra3	Ra2	Ra1	Ra0		Red tone “a”
		1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000		Green tone 0
		1	↑	1	:	:	:	:	:	:	:	:	:		: -
		1	↑	1	-	-	-	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0		Green tone “b”
		1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000		Blue tone 0
		1	↑	1	:	:	:	:	:	:	:	:	:		: -
		1	↑	1	-	-	-	Bc5	Bc4	Bc3	Bc2	Bc1	Bc0		Blue tone “c”

“-“: Don’t care

Table 9.1.1 System Function command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PTLAR	9.1.25	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set
		1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-	Partial start address (0,1,2, .., P)
		1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-	
		1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	-	Partial end address (0,1,2, .., P)
		1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-	
SCRLAR	9.1.26	1	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Scroll area set
		1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	-	Top fixed area (0,1,2, .., S)
		1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-	
		1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	-	Vertical scroll area (0,1,2, .., S)
		1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-	
		1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	-	Bottom fixed area (0,1,2, .., S)
		1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-	
TEOFF	9.1.27	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	9.1.28	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect mode set & on
		1	↑	1	-	0	0	0	0	0	0	0	M	00h	M="0": Mode1, M="1": Mode2
MADCTR	9.1.29	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
		1	↑	1	-	MY	MX	MV	ML	RGB	MH	0	0	00h	-
VSCSAD V=159	9.1.30	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Scroll start address of RAM
		1	↑	1	-	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8	00h	SSA = 0, 1, 2, …, V
		1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	00h	
IDMOFF	9.1.31	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	9.1.32	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	9.1.33	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
		1	↑	1	-	VIPF3	VIPF2	VIPF1	VIPF0	0	IFPF2	IFPF1	IFPF0	66h	Interface format
RDID1	9.1.34	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	38h	Read parameter
RDID2	9.1.35	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h	Read parameter
RDID3	9.1.36	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	4Fh	Read parameter

"-": Don't care

Note 1. After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2. Undefined commands are treated as NOP (00 h) command.

Note 3. B0 to D9 and DE to FF are for factory use of driver supplier.

Note 4. Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTR (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) and Read Display Self Diagnostic Result (0Fh) of these commands are updated immediately both in Sleep In mode and Sleep Out mode.

9.1.1 NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is empty command. It does not have effect on the display module. -However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands.
Restriction	-
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: N/A Status: S/W Reset — Default Value: N/A Status: H/W Reset — Default Value: N/A
Flow Chart	-

9.1.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-

NOTE: "-" Don't care

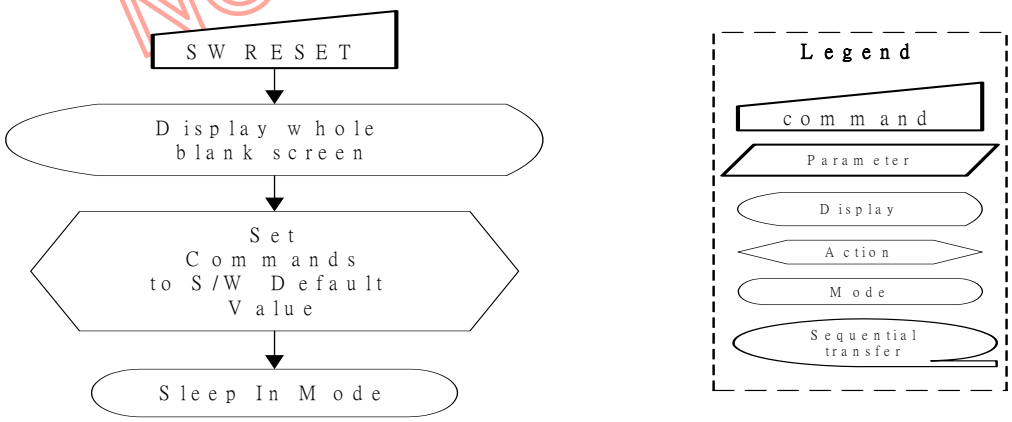
Description	-When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off). (See default tables in each command description) *Note: The Frame Memory contents are not affected by this command.*
Restriction	-It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during 5msec. -If Software Reset is applied during Sleep Out mode, it will be necessary to wait *120msec* before sending Sleep Out command. -Software Reset command cannot be sent during Sleep Out sequence.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



9.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	38h
3rd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h
4th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	4Fh

NOTE: "-" Don't care

Description

-This read byte returns 24-bit display identification information.
-The 1stparameter is dummy data
-The 2ndparameter (ID17 to ID10): LCD module's manufacturer ID.
-The 3rdparameter (ID27 to ID20): LCD module/driver version ID.
-The 4th parameter (ID37 to UD30): LCD module/driver ID.
NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.

Restriction

-

Register Availability

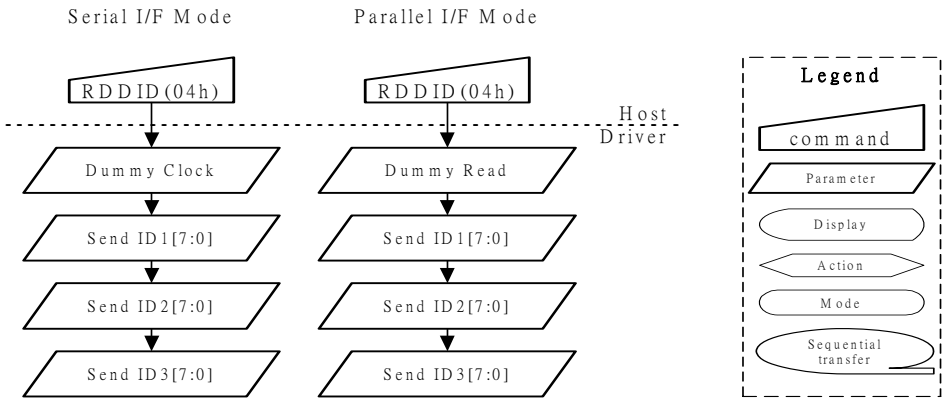
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	38h	80h	4Fh
S/W Reset	38h	80h	4Fh
H/W Reset	38h	80h	4Fh

Note: ID1 can be modified by metal option.

Flow Chart



9.1.4 RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1stParameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	-
3rd Parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	-
4th Parameter	1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	-
5thParameter	1	1	↑		GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0	-

NOTE: "-" Don't care

Description: This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	"1"=Booster on,"0"= Booster off,
MY	Row Address Order (MY)	"1"=Decrement, (Bottom to Top, when MADCTL (36h) D7='1') "0"=Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order (MX)	"1"=Decrement, (Right to Left, when MADCTL (36h) D6='1') "0"=Increment, (Left to Right, when MADCTL (36h) D6='1')
MV	Row/Column Exchange (MV)	"1"= Row/column exchange, (when MADCTL (36h) D5='1') "0"= Normal (MV=0), (when MADCTL (36h) D5='0')
ML	Vertical refresh Order (ML)	"1"=Decrement, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1') "0"=Increment, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0')
RGB	RGB/BGR Order (RGB)	"1"=BGR, (When MADCTL (36h) D3='1') "0"=RGB, (When MADCTL (36h) D3='0')
MH	Horizontal refresh Order (MH)	"1"=Decrement, (LCD refresh Right to Left, when MADCTL (36h) D2='1') "0"=Increment, (LCD refresh Left to Right, when MADCTL (36h) D2='0')
ST24	Not Used	
ST23	Not Used	
IFPF2 IFPF1 IFPF0	Interface Color Pixel Format Definition	"011" = 12-bit / pixel, "101" = 16-bit / pixel, "110" = 18-bit / pixel,
IDMON	Idle Mode On/Off	"1" = On, "0" = Off
PTLON	Partial Mode On/Off	"1" = On, "0" = Off
SLOUT	Sleep In/Out	"1" = Out, "0" = In
NORON	Display Normal Mode On/Off	"1" = Normal Display, "0" = Normall Display off
VSSON	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
ST14	Horizontal Scroll Status	"0"
INVON	Inversion Status	"1" = On, "0" = Off
ST12	All Pixels On (Not Used)	"0"
ST11	All Pixels Off (Not Used)	"0"
DISON	Display On/Off	"1" = On, "0" = Off
TEON	Tearing effect line on/off	"1" = On, "0" = Off
NORON	Display Normal Mode On/Off	"1" = Normal Display, "0" = Normall Display off
VSSON	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
ST14	Horizontal Scroll Status	"0"
INVON	Inversion Status	"1" = On, "0" = Off
ST12	All Pixels On (Not Used)	"0"
ST11	All Pixels Off (Not Used)	"0"
DISON	Display On/Off	"1" = On, "0" = Off
TEON	Tearing effect line on/off	"1" = On, "0" = Off
GCS2 GCS1 GCS	Gamma Curve Selection	"000" = GC0 "001" = GC1 "010" = GC2 "011" = GC3 "100" to "111" = Not defined
TELOM	Tearing effect line mode	"0" = mode1, "1" = mode2
HSON	Horizontal Sync. (HS, RGB I/F)	'1' = On, '0' = Off
VSON	Vertical Sync, (VS, RGB I/F)	'1' = On, '0' = Off
PCKON	Pixel Clock (PCLK, RGB I/F)	'1' = On, '0' = Off
DEON	Data Enable (DE, RGB I/F)	'1' = On, '0' = Off
ST0	For Future Use	"0"

Note: For Bits ST30 to ST28, also refer to Section 8-11

Note: ST0, ST5, ST9, ST11-ST15, ST19, ST23, ST24 are set to '0', when RGB I/F.

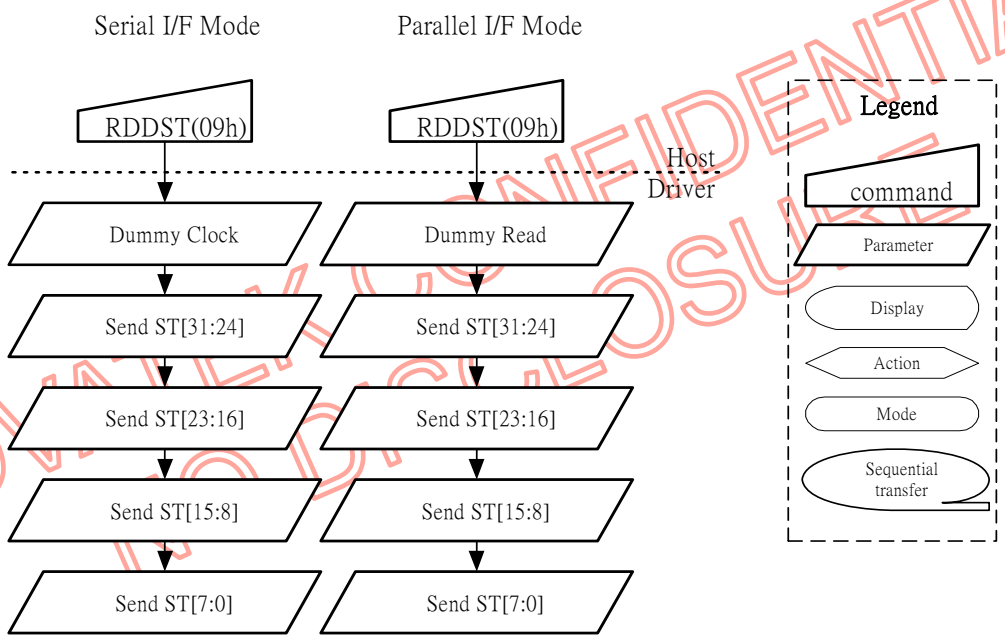
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (ST31 to ST0):			
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
S/W Reset	0xxx-xx00	0xxx-0001	0000-0000	0000-0000
H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000

Flow Chart



9.1.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑		D7	D6	D5	D4	D3	D2	D1	D0	08h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	
D7	Booster Voltage Status	"1"=Booster on,	"0"=Booster off
D6	Idle Mode On/Off	"1" = Idle Mode On,	"0"= Idle Mode Off
D5	Partial Mode On/Off	"1" = Partial Mode On,	"0" = Partial Mode Off
D4	Sleep In/Out	"1" = Sleep Out,	"0" = Sleep In
D3	Display Normal Mode On/Off	"1" = Normal Display,	"0" = Partial Display
D2	Display On/Off	"1" = Display On,	"0" = Display Off
D1	Not Used	"0"	
D0	Not Used	"0"	

Restriction

-

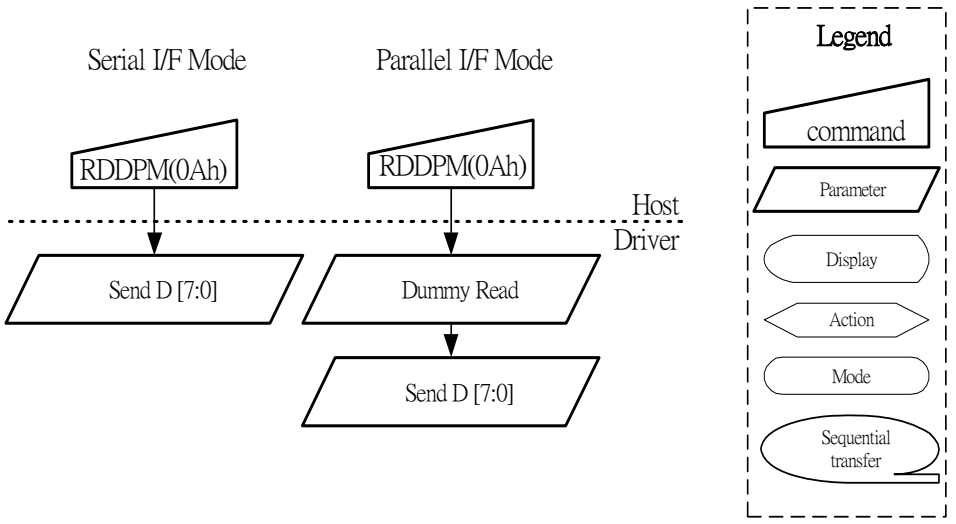
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_1000 (08h)
S/W Reset	0000_1000 (08h)
H/W Reset	0000_1000 (08h)

Flow Chart



9.1.6 RDDMADCTR (0Bh): Read Display MADCTR

0BH	RDDMADCTR (Read Display MADCTR)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDMADCTR	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	00h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Row Address Order	"1"=Decrement, "0"=Increment
D6	Column Address Order	"1"=Decrement, "0"=Increment
D5	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
D4	Scan Address Order	'1' =LCD Refresh Bottom to Top '0' =LCD Refresh Top to Bottom
D3	RGB/BGR Order	"1"=BGR, "0"=RGB
D2	Display data latch order	'1' =LCD Refresh right to left '0' =LCD Refresh left to right
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

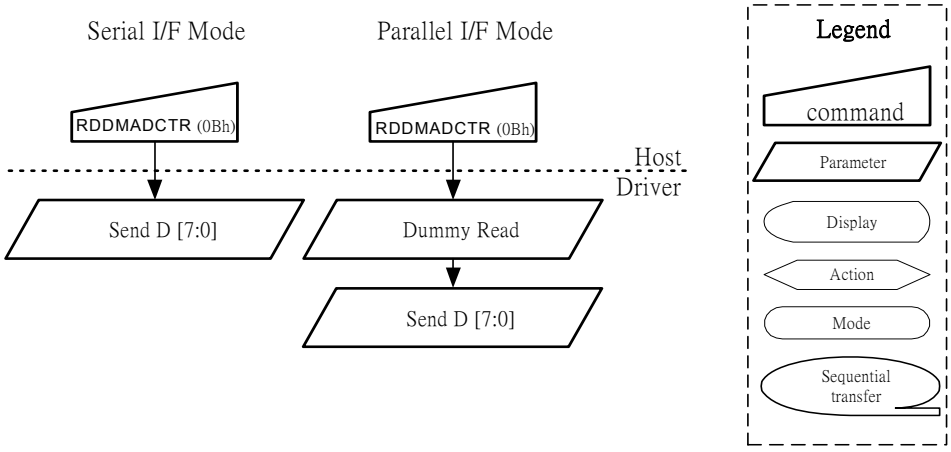
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	No change

Flow Chart



9.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
VIPF3 VIPF2 VIPF1 VIPF0	RGB Interface Color Format	"0101"=16 bit/pixel (1 times data transfer) "0110"=18 bit/pixel (1 times data transfer) "1110"=18 bit/pixel (3 times data transfer) The others = not defined
D3		"0" (Not Used)
IFPF2 IFPF1 IFPF0	Control Interface Color Format	"011"=12 bit/pixel "101"=16 bit/pixel "110"=18 bit/pixel The others = not defined

Restriction

-

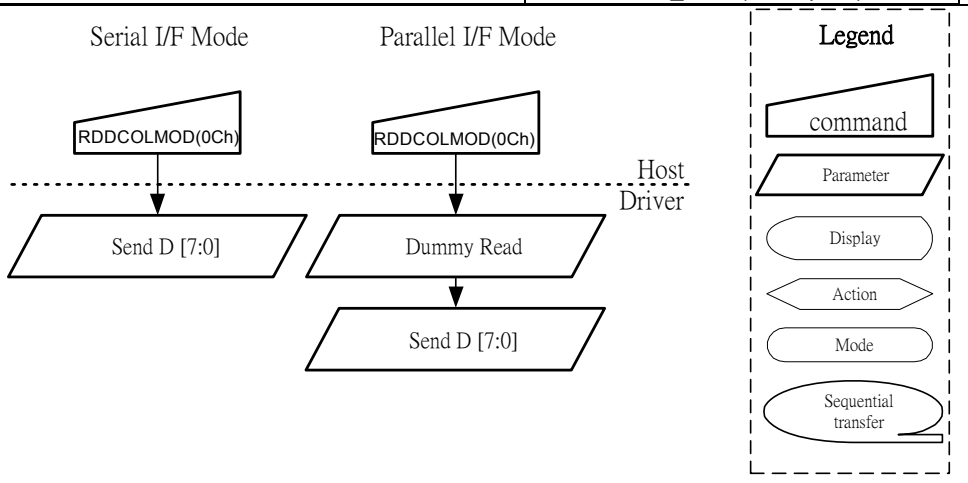
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0110_0110 (18 bit/pixel)
S/W Reset	No Change
H/W Reset	0110_0110 (18 bit/pixel)

Flow Chart



9.1.8 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	00h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Vertical Scrolling On/Off	"1" = Vertical scrolling is On, "0" = Vertical scrolling is Off
D6	Horizontal Scrolling On/Off	"0" (Not used)
D5	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	All Pixels On	"0" (Not used)
D3	All Pixels Off	"0" (Not used)
D2	Gamma Curve Selection	"000" = GC0 ; "001" = GC1 ; "010" = GC2 ; "011" = GC3 "100" to "111" = Not defined
D1		
D0		

Restriction

-

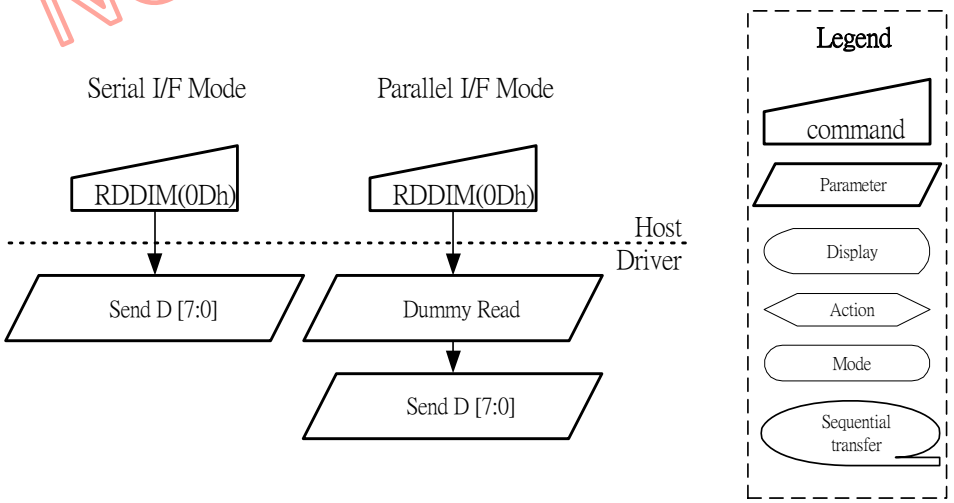
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)

Flow Chart



9.1.9 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	00h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	
D7	Tearing Effect Line On/Off	"1" = On,	"0" = Off
D6	Tearing effect line mode	"0" = mode1,	"1" = mode2
D5	Horizontal Sync. (RGB I/F) On/Off	"1" = On,	"0" = Off
D4	Vertical Sync. (RGB I/F) On/Off	"1" = On,	"0" = Off
D3	Pixel Clock (PCLK, RGB I/F) On/Off	"1" = On,	"0" = Off
D2	Data Enable (DE, RGB I/F) On/Off	"1" = On,	"0" = Off
D1	Not Used	"1" = On,	"0" = Off
D0	Not Used	"1" = On,	"0" = Off

Restriction

-

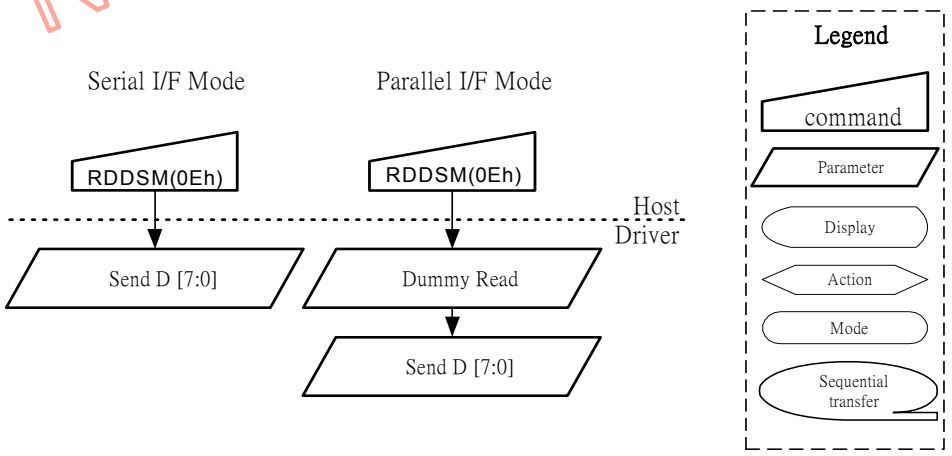
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)

Flow Chart



9.1.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSD (Read Display Self-Diagnostic Result)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	00h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Register Loading Detection	See section 8.19.1
D6	Functionality Detection	See section 8.19.2
D5	Chip Attachment Detection	See section 8.19.3
D4	Display Glass Break Detection	See section 8.19.4
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

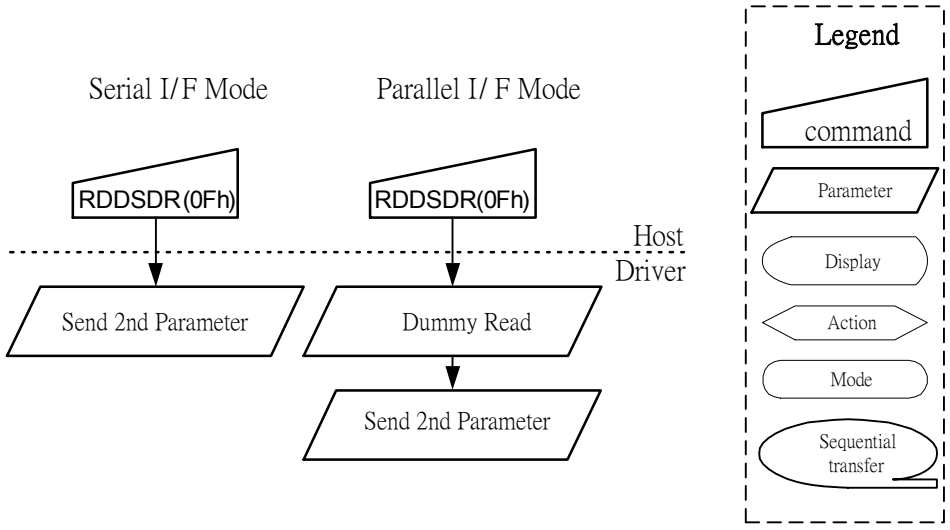
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)

Flow Chart



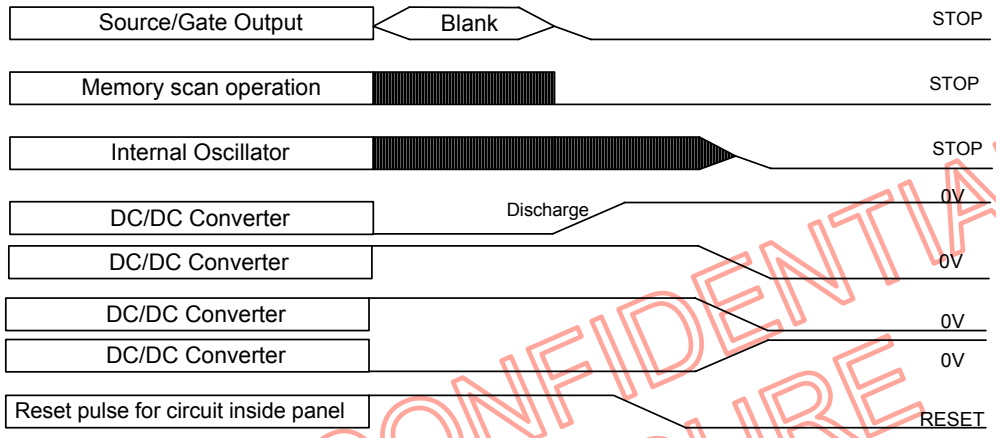
9.1.11 SLPIN (10h): Sleep In

10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

-This command causes the LCD module to enter the minimum power consumption mode.
-In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



-MPU interface and memory are still working and the memory keeps its contents.

Restriction

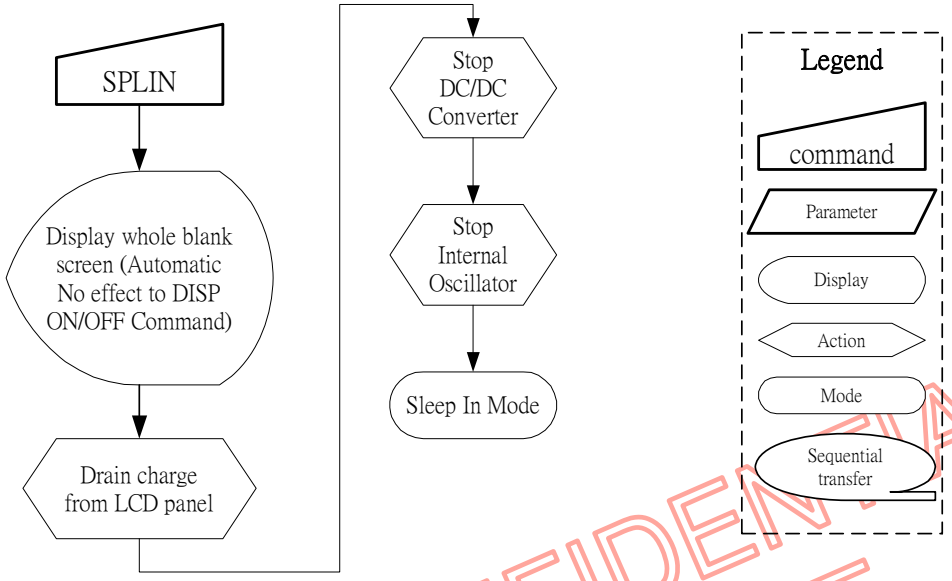
-This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).
-It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
-It will be necessary to wait *120msec* after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode

Flow Chart	-It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. -The results of booster off can be check by RDDST (09h) command Bit31. 

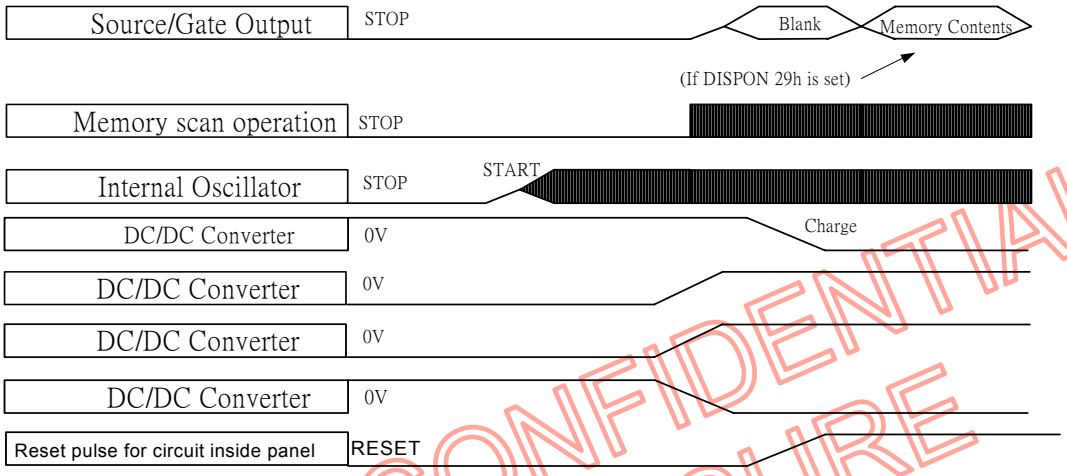
9.1.12 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

This command turns off sleep mode.
In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



Restriction

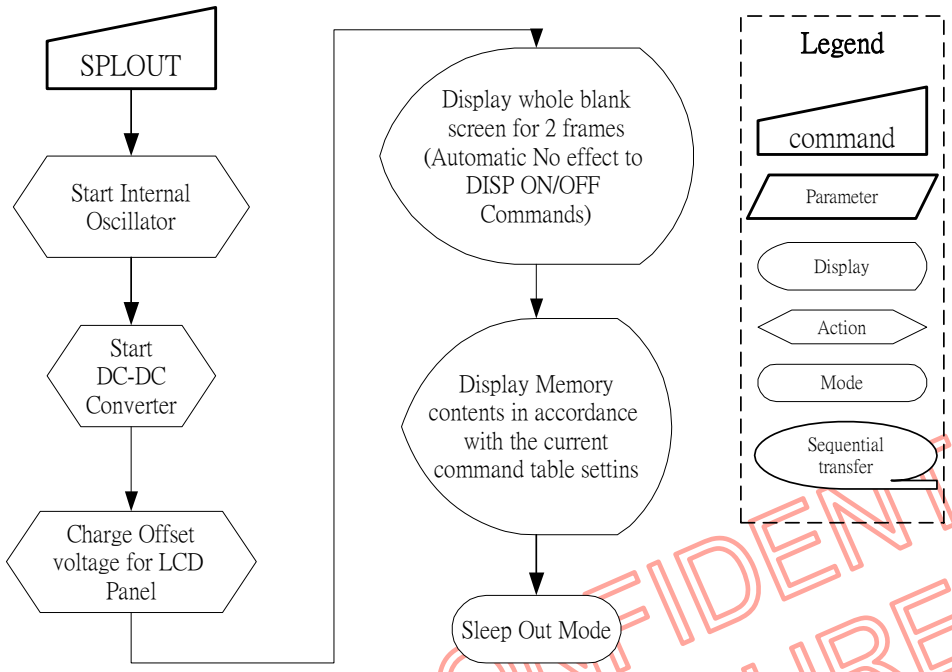
This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
NT39153 loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the NT39153 is already Sleep Out –mode.
NT39153 is doing self-diagnostic functions during this 5msec. See also section 8.19. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. The results of booster on can be checked by RDDST (09h) command Bit31. 

9.1.13 PTLON (12h): Partial Display Mode On

12H	PTLON (Partial Display Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H) -To leave Partial mode, the Normal Display Mode On command (13H) should be written. -There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	-This command has no effect when Partial mode is active.
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: Normal Mode On Status: S/W Reset — Default Value: Normal Mode On Status: H/W Reset — Default Value: Normal Mode On
Flow Chart	See Partial Area (30h)

9.1.14 NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command returns the display to normal mode. -Normal display mode on means Partial mode off, Scroll mode Off. -Exit from NORON by the Partial mode On command (12h) -There is no abnormal visual effect during mode change from Normal mode On to Partial mode On.
Restriction	-This command has no effect when Normal Display mode is active.
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value Power On Sequence: Normal Mode On S/W Reset: Normal Mode On H/W Reset: Normal Mode On
Flow Chart	-See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command

9.1.15 INVOFF (20h): Display Inversion Off

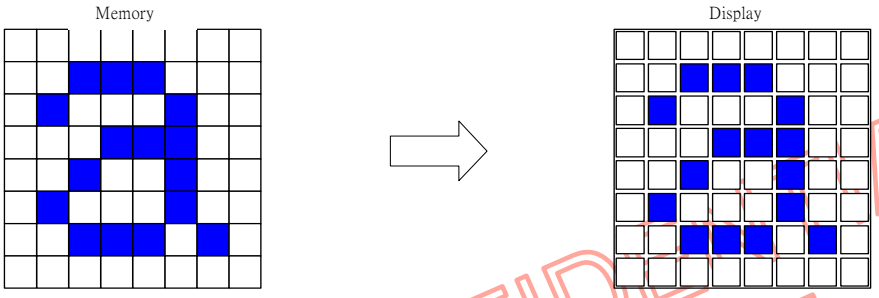
20H	INVOFF (Display Inversion Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already inversion off mode.

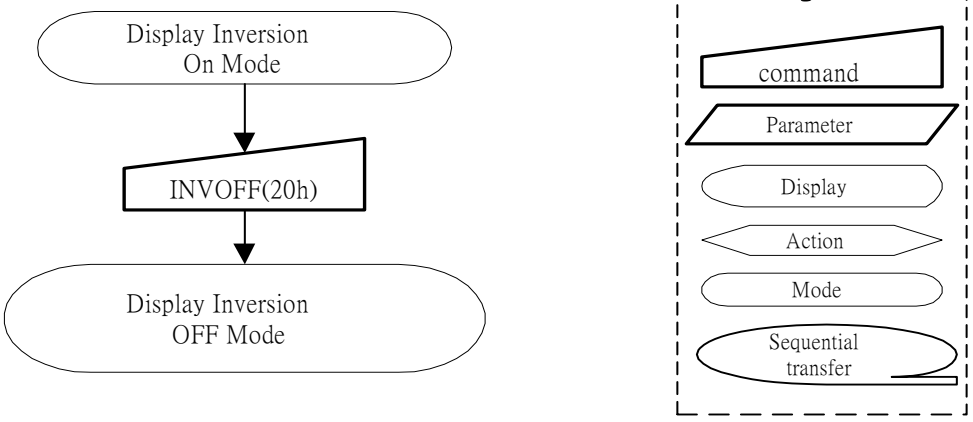
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



9.1.16 INVON (21h): Display Inversion On

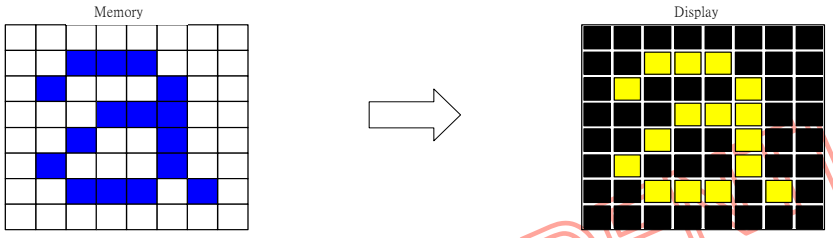
21H	INVON (Display Inversion On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

This command is used to enter into display inversion mode
This command makes no change of contents of frame memory.
This command does not change any other status.
To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

(Example)



Restriction

This command has no effect when module is already Inversion On mode.

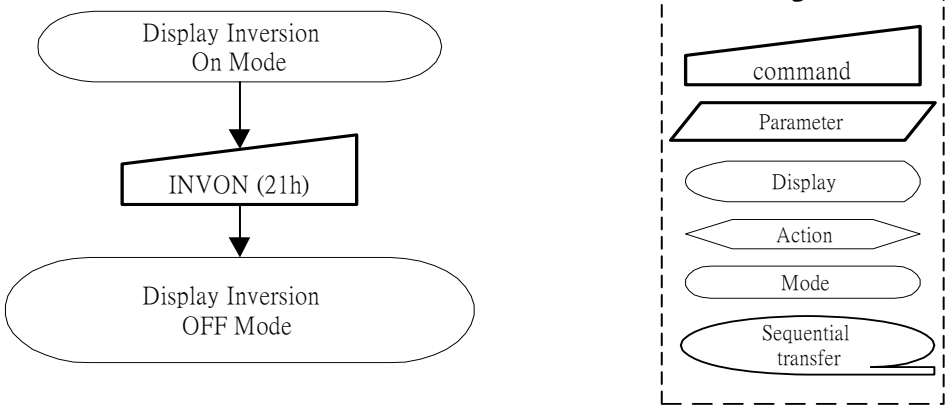
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



9.1.17 GAMSET (26h): Gamma Set

26H	GAMSET (Gamma Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMSET	0	↑	1	-	0	0	1	0	0	1	0	1	(26h)
1st parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h

NOTE: "-" Don't care

Description

-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curves are defined in section 8.16.The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC[7:0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1
02h	GC1	Gamma Curve 2
04h	GC2	Gamma Curve 3
08h	GC3	Gamma Curve 4

Note: All other values are undefined.

Restriction

-Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid is received.

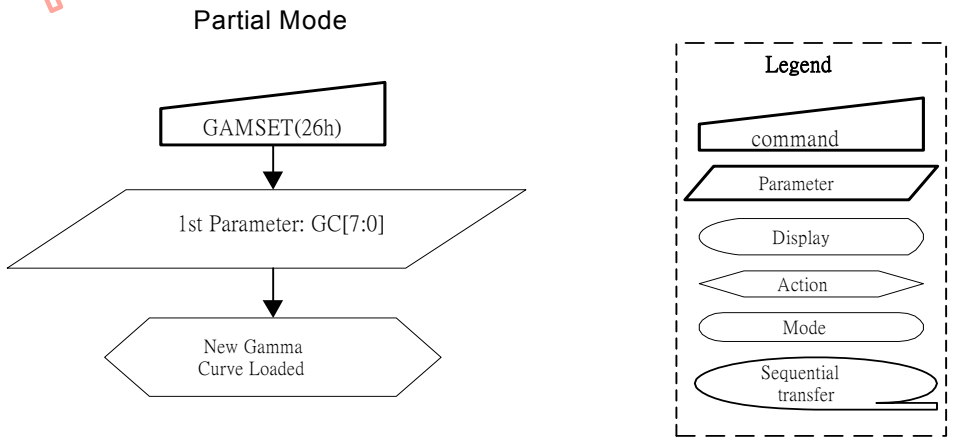
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



9.1.18 DISPOFF (28h): Display Off

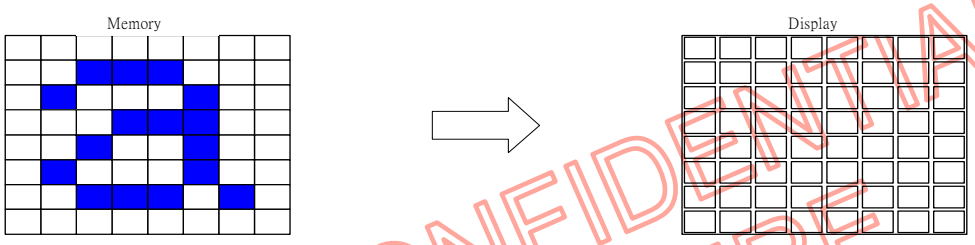
28H	DISPOFF (Display Off)												
nst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

-This command is used to enter into DISPLAY OFF mode. In this mode, the output from -Frame Memory is disables and blank page inserted.
-This command makes no change of contents of frame memory.
-This command does not change any other status.
-There will be no abnormal visible effect on the display.
-Exit from this command by Display On (29h)

(Example)



Restriction

This command has no effect when module is already in Display Off mode.

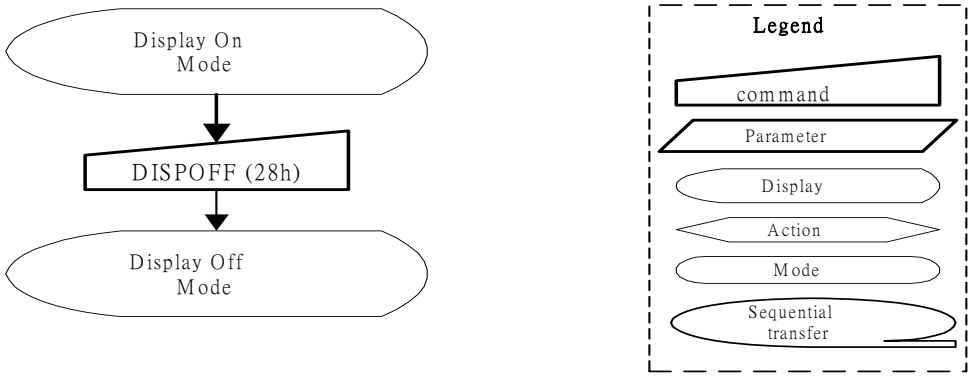
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



9.1.19 DISPON (29h): Display On

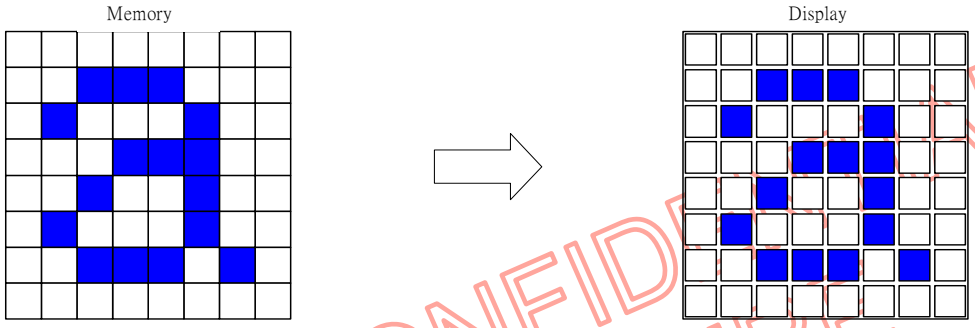
29H	DISPON (Display On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

-This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
-This command makes no change of contents of frame memory.
-This command does not change any other status.

(Example)



Restriction

-This command has no effect when module is already in Display On mode.

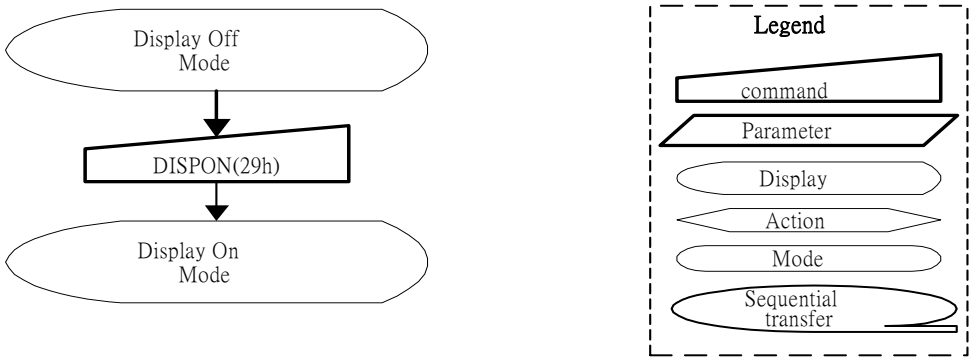
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



9.1.20 CASET (2Ah): Column Address Set

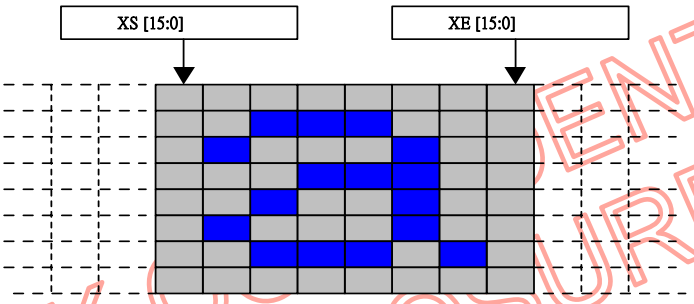
2Ah	CASET (Column Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1st Parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	-
2nd Parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-
3rd Parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	-
4th Parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-

NOTE: "-" Don't care

Description

-This command is used to define area of frame memory where MPU can access.
-This command makes no change on the other driver status.
-The value of XS [15:0] and XE [15:0] are referred when RAMWR command comes.
-Each value represents one column line in the Frame Memory.

(Example)



Restriction

XS [15:0] always must be equal to or less than XE [15:0]
When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.

1. 128X160 memory base (GM = '00')
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 127 (007Fh)): MV="0")
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 159 (009Fh)): MV="1")
2. 120x160 memory base (GM = '01')
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 119 (0077h)): MV="0")
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 159 (009Fh)): MV="1")
3. 128x128 memory base (GM = '10')
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 127 (007Fh)): MV="0")
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 127 (007Fh)): MV="1")
4. 132X162 memory base (GM = '11')
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 131 (0083h)): MV="0")
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 161 (00A1h)): MV="1")

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

1. 128X160 memory base (GM = ’00’)

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	007Fh (127)	
S/W Reset	0000h	007Fh (127)	009Fh (159)
H/W Reset	0000h	007Fh (127)	

2. 120x160 memory base (GM = ‘01’)

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	0077h (119)	
S/W Reset	0000h	0077h (119)	009Fh (159)
H/W Reset	0000h	0077h (119)	

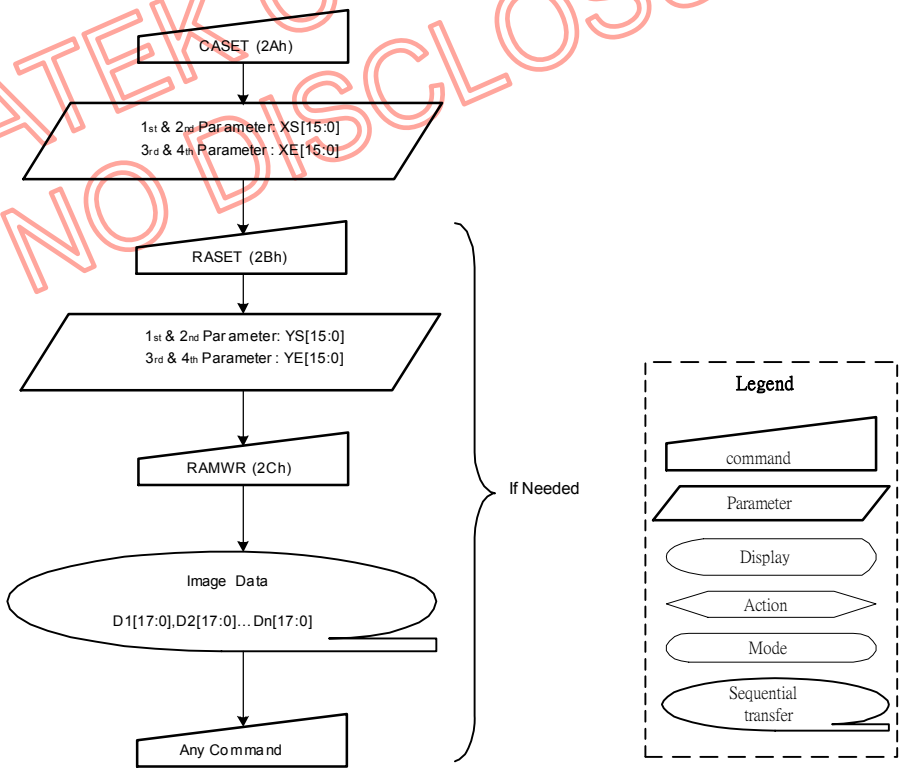
3. 128x128 memory base (GM = ‘10’)

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	007Fh (127)	
S/W Reset	0000h	007Fh (127)	007Fh (127)
H/W Reset	0000h	007Fh (127)	

1. 132X162 memory base (GM = ’11’)

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	0083h (131)	
S/W Reset	0000h	0083h (131)	00A1h (161)

Flow Chart



9.1.21 RASET (2Bh): Row Address Set

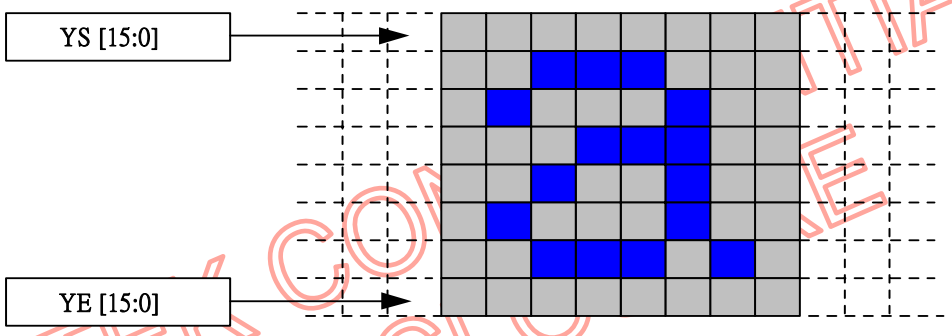
2Bh	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st Parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-
2nd Parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-
3rd Parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	-
4th Parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-

NOTE: "-" Don't care

Description

-This command is used to define area of frame memory where MPU can access.
-This command makes no change on the other driver status.
-The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.
-Each value represents one column line in the Frame Memory.

(Example)



Restriction

YS [15:0] always must be equal to or less than YE [15:0]
When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.

1. 128X160 memory base (GM = '00')

   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 159 (009Fh)): MV="0"

   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 127 (007Fh)): MV="1"

2. 120x160 memory base (GM = '01')

   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 159 (009Fh)): MV="0"

   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 119 (0077h)): MV="1"

3. 128x128 memory base (GM = '10')

   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 127 (007Fh)): MV="0"
   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 127 (007Fh)): MV="1"

4. 132X162 memory base (GM = '11')

   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 161 (00A1h)): MV="0"

   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 131 (0083h)): MV="1"

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

1. 128X160 memory base (GM = ’00’)

Status	Default Value		
	YS [15:0]	YE [15:0] (MV=0)	YE [15:0] (MV=1)
Power On Sequence	0000h	009Fh (159)	
S/W Reset	0000h	009Fh (159)	007Fh (127)
H/W Reset	0000h	009Fh (159)	

2. 120x160 memory base (GM = ‘01’)

Status	Default Value		
	YS [15:0]	YE [15:0] (MV=0)	YE [15:0] (MV=1)
Power On Sequence	0000h	009Fh (159)	
S/W Reset	0000h	009Fh (159)	0077h (119)
H/W Reset	0000h	009Fh (159)	

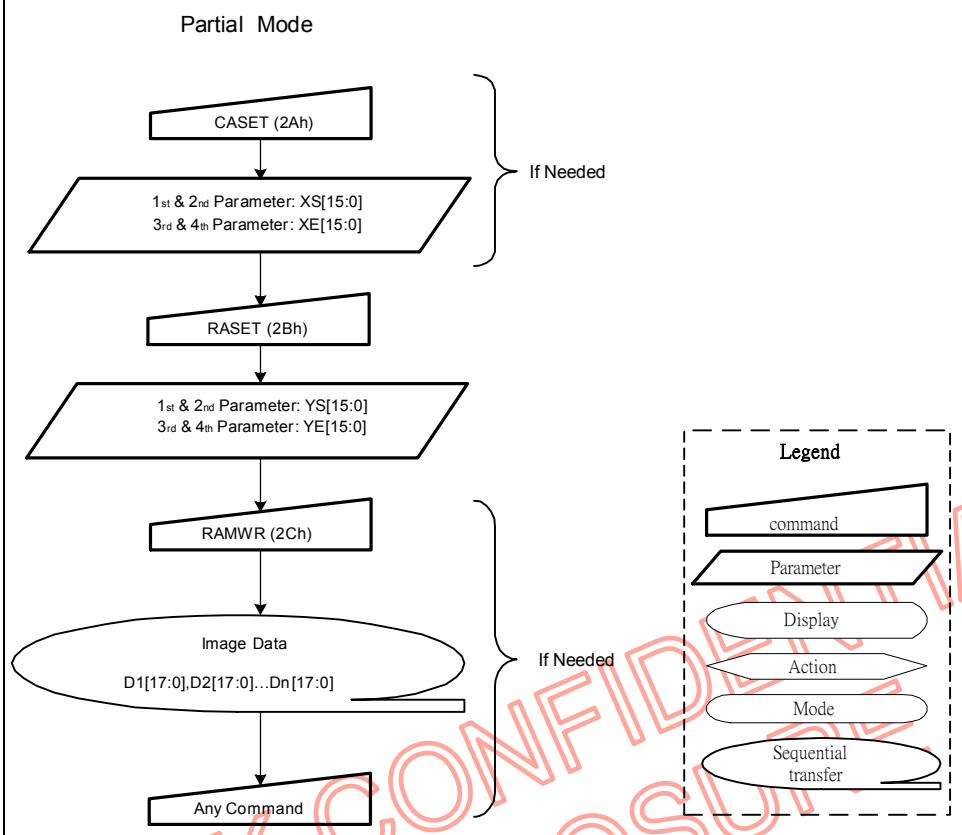
3. 128x128 memory base (GM = ‘10’)

Status	Default Value		
	YS [15:0]	YE [15:0] (MV=0)	YE [15:0] (MV=1)
Power On Sequence	0000h	007Fh (127)	
S/W Reset	0000h	007Fh (127)	007Fh (127)
H/W Reset	0000h	007Fh (127)	

4. 132X162 memory base (GM = ’11’)

Status	Default Value		
	YS [15:0]	YE [15:0] (MV=0)	YE [15:0] (MV=1)
Power On Sequence	0000h	00A1h (161)	
S/W Reset	0000h	00A1h (161)	0083h (131)

Flow Chart



9.1.22 RAMWR (2Ch): Memory Write

2Ch	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
:	1	↑	1	-	:	:	:	:	:	:	:	:	:
Nth Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

-This command is used to transfer data MPU to frame memory.
-This command makes no change to the other driver status.
-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
-The Start Column/Start Row positions are different in accordance with MADCTR setting. (See section 8.11)
-Then D [17:0] is stored in frame memory and the column register and the row register incremented as section 8.10.2
-Sending any other command can stop Frame Write.

Restriction

In all color modes, there is no restriction on length of parameters.

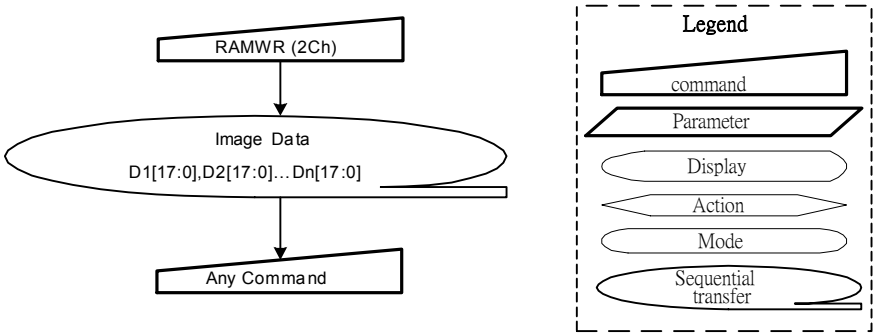
1. 128X160 memory base (GM = '00')
   128x160x18-bit memory can be written by this command
   Memory range: (0000h, 0000h) -> (007Fh, 09Fh)
2. 120x160 memory base (GM = '01')
   120x160x18-bit memory can be written on this command.
   Memory range: (0000h, 0000h) -> (0077h, 09Fh)
3. 128x128 memory base (GM = '10')
   128x128x18-bit memory can be written on this command.
   Memory range: (0000h, 0000h) -> (007Fh, 007Fh)
4. 132x162 memory base (GM = '11')
   132x162x18-bit memory can be written on this command.
   Memory range: (0000h, 0000h) -> (0083h, 00A1h)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	

9.1.23 RGBSET (2Dh): Colour Setting for 4K, 65K and 262K

2Dh	RGBSET (Colour Setting for 4K, 65K, and 262K)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBSET	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)
1st parameter	1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000	-
:	1	↑	1	-	-	-	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	-
32th parameter	1	↑	1	-	-	-	R315	R314	R313	R312	R311	R310	-
33th parameter	1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000	-
:	1	↑	1	-	-	-	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	-
96th parameter	1	↑	1	-	-	-	G635	G634	G633	G632	G631	G630	-
97th parameter	1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000	-
:	1	↑	1	-	-	-	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	-
128th parameter	1	↑	1	-	-	-	B315	B314	B313	B312	B311	B310	-

NOTE: "-" Don't care

Description

This command is used to define the LUT for 12bit-to-18bit / 16-bit -to-18-bit color depth conversations. 128-Bytes must be written to the LUT regardless of the color mode. Only the values in section 8.18 are referred.
In this condition, 4K-color (4-4-4), and 65K-color(5-6-5) data input are transferred 6(R)-6(G)-6(B) through RGB LUT table.
This command has no effect on other commands/parameters and Contents of frame memory.
Visible change takes effect next time the Frame Memory is written to.

Restriction

Do not send any command before the last data is sent or LUT is not defined correctly.

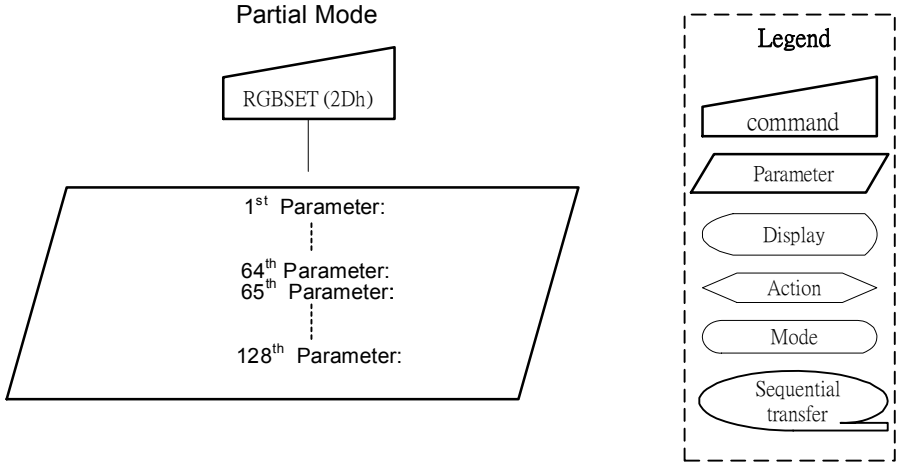
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See Section 8.18
S/W Reset	Contents of the look-up table protected
H/W Reset	See Section 8.18

Flow Chart



9.1.24 RAMRD (2Eh): Memory Read

2Eh	RAMRD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	D17	D16	D15	D14	D13	D12	D11	D10	-
:	1	1	↑	-	:	:	:	:	:	:	:	:	:
Nth Parameter	1	1	↑	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-

NOTE: "-" Don't care

Description

-This command is used to transfer data from frame memory to MPU.
-This command makes no change to the other driver status.
-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
-The Start Column/Start Row positions are different in accordance with MADCTR setting. (See section 8.11)
-Then D[17:0] is read back from the frame memory and the column register and the row register incremented as section 8.10.2
-Frame Read can be canceled by sending any other command.
-See section 8.8 "Display Data Format" for color coding (18 bit cases), when there is used 8, 9, 16 or 18 data lines for image data.

Restriction

In all color modes, the Frame Read is always 24-bit and there is no restriction on length of parameters. Note – Memory Read is only possible via the Parallel Interface.

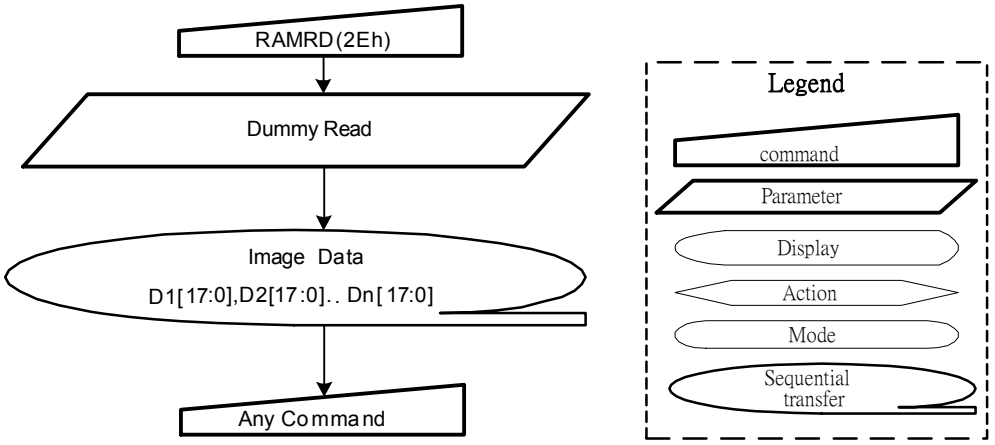
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



9.1.25 PTLAR (30h): Partial Area

30h	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1st parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-
2nd parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-
3rd parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	-
4th parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-

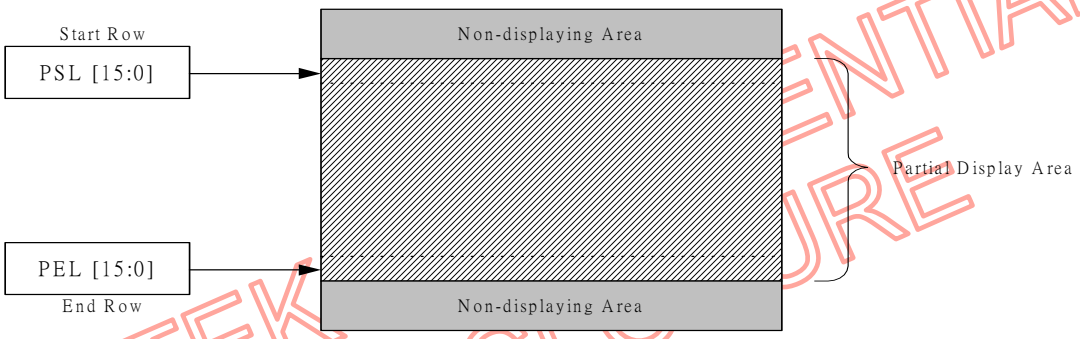
NOTE: "-" Don't care

Description

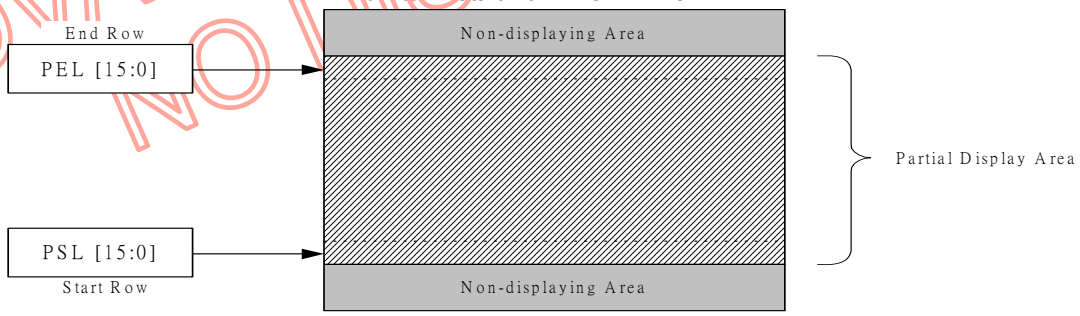
-This command defines the partial mode's display area.

-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

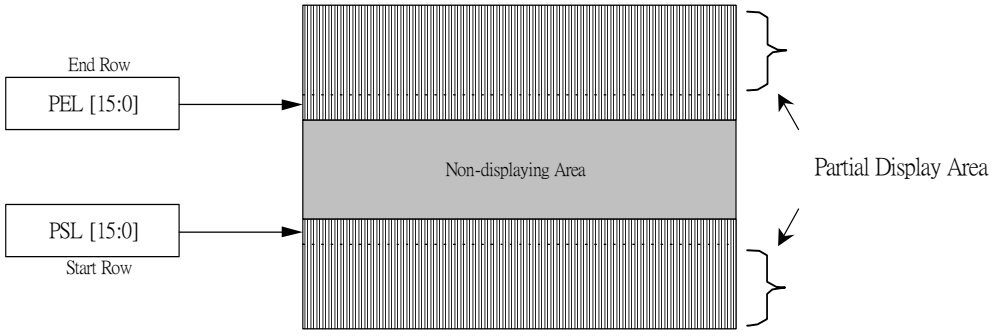
-If End Row > Start Row when MADCTL ML=0:



-If End Row > Start Row when MADCTL ML=1:



-If End Row < Start Row when MADCTL ML=0:



-If End Row = Start Row then the Partial Area will be one row deep.

Restriction	-

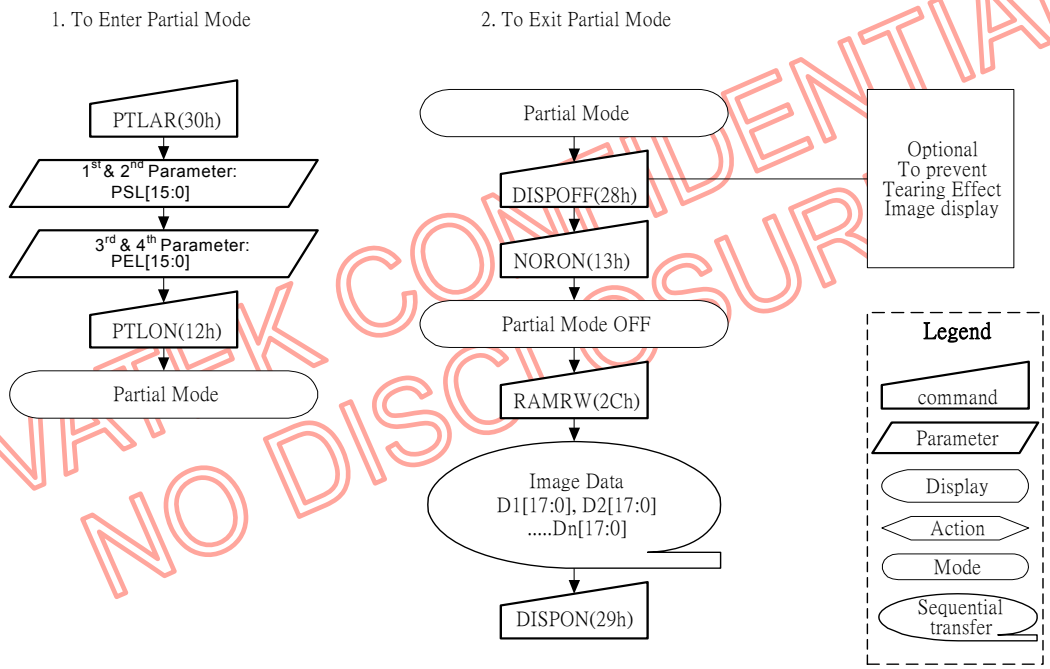
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	PSL[15:0]	PEL[15:0]			
GM	"xx"	"00"	"01"	"10"	"11"
Power On Sequence	0000h	009Fh	009Fh	007Fh	00A1h
S/W Reset	0000h	009Fh	009Fh	007Fh	00A1h
H/W Reset	0000h	009Fh	009Fh	007Fh	00A1h

Flow Chart



9.1.26 SCRLAR (33h): Scroll Area

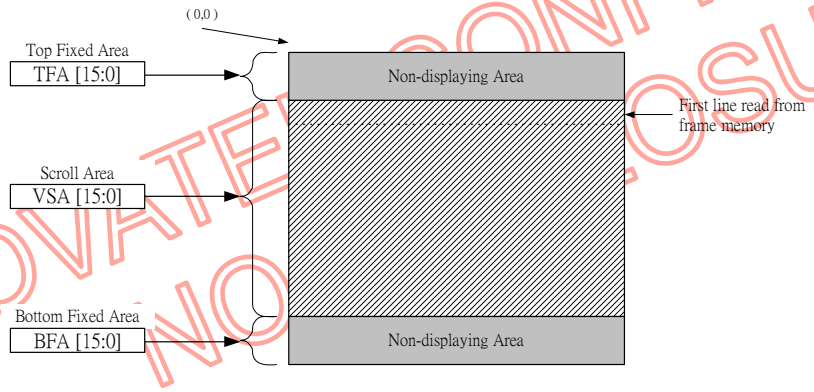
33h	SCRLAR (Scroll Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SCRLAR	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)
1st parameter	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	-
2nd parameter	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-
3rd parameter	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	-
4th parameter	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-
5th parameter	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	-
6th parameter	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-

NOTE: "-" Don't care

Description

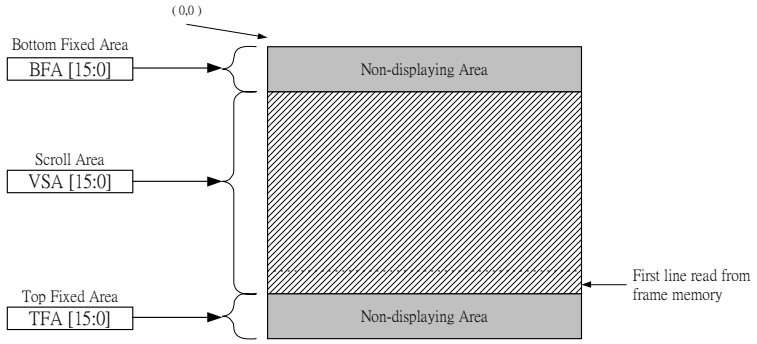
This command defines the Vertical Scrolling Area of the display.
When MADCTL ML=0

- The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
- The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
- The first line appears immediately after the bottom most line of the Top Fixed Area.
- The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from TFA, Bottom of the Frame Memory and Display).
- TFA, VSA and BFA refer to the Frame Memory row address.



When MADCTL ML=1

- The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
- The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
- The first line appears immediately after the bottom most line of the Top Fixed Area.
- The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from TFA, Top of the Frame Memory and Display).

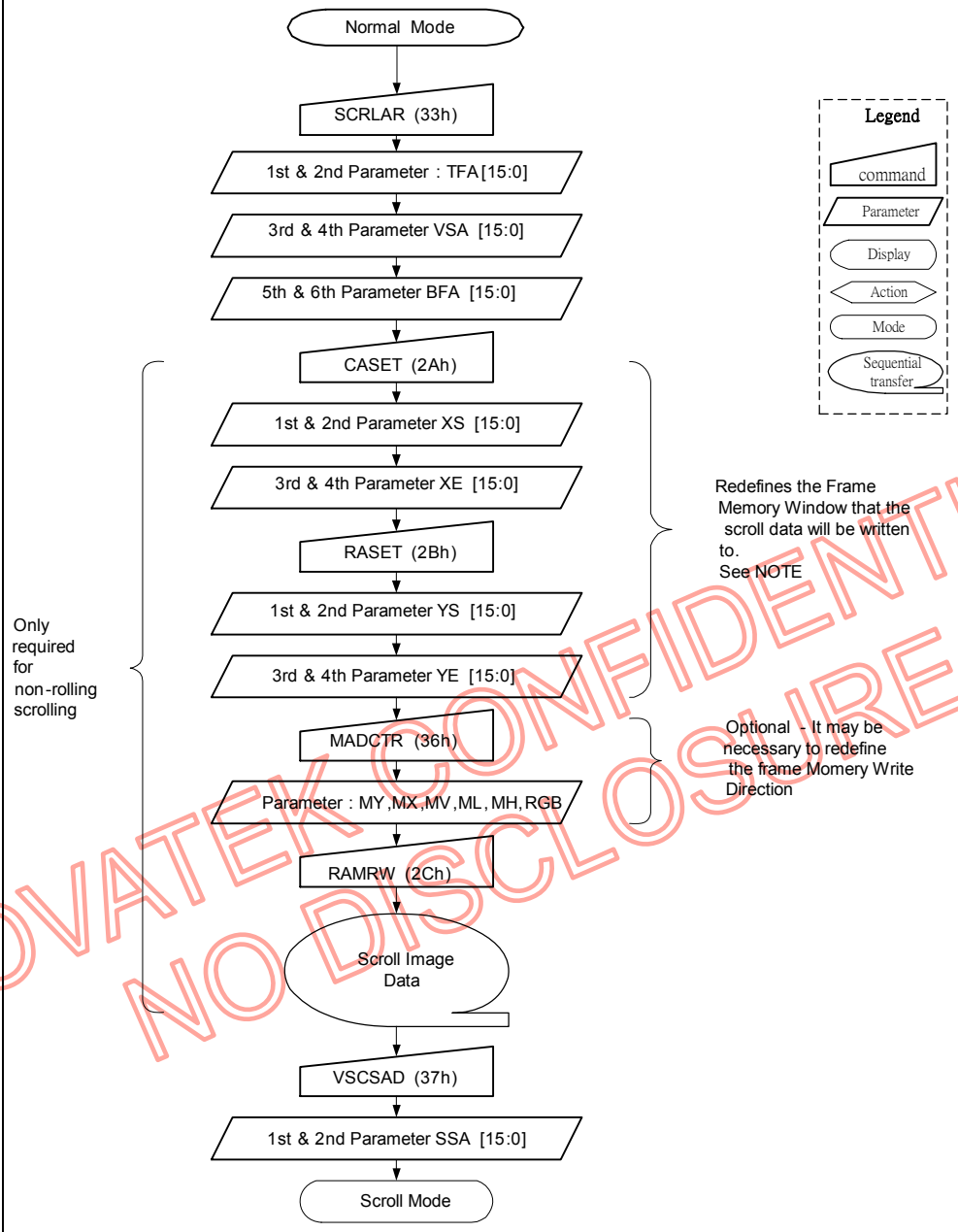


See Section 8.10.4 for details of the Memory to Display Mapping.

<table>
<tr><td>Restriction</td><td>-The condition is (TFA+VSA+BFA) = 128 in 128RGB x128 (GM=”10”)
-The condition is (TFA+VSA+BFA) = 160 in 128RGB x160 (GM=”00”) or 120RGB x 160 (GM=”01”)
-The condition is (TFA+VSA+BFA) = 162 in 132RGB x162 (GM=”11”)
-Otherwise Scrolling mode is undefined.
-In Vertical Scroll Mode, MADCTR parameter MV should be set to ‘0’-this only affects the Frame Memory Write.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="6">Default Value</th></tr>
<tr><th>TFA [15:0]</th><th colspan="4">VSA [15:0]</th><th>BFA [15:0]</th></tr>
<tr><td>GM</td><td>“xx”</td><td>“00”</td><td>“01”</td><td>“10”</td><td>“11”</td><td>“xx”</td></tr>
<tr><td>Power On Sequence</td><td>0000h</td><td>00A0h</td><td>00A0h</td><td>0080h</td><td>00A2h</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td><td>00A0h</td><td>00A0h</td><td>0080h</td><td>00A2h</td><td>0000h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td><td>00A0h</td><td>00A0h</td><td>0080h</td><td>00A2h</td><td>0000h</td></tr>
</table>
</td></tr>
</table>

Flow Chart

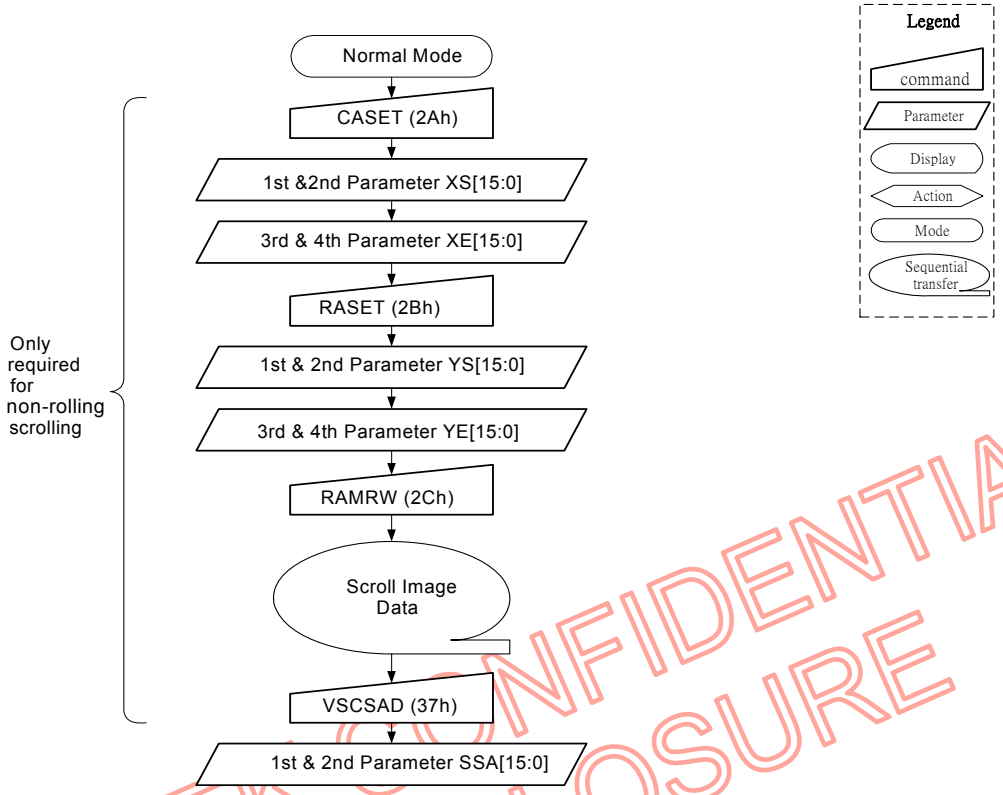
1.To enter Vertical Scroll Mode:



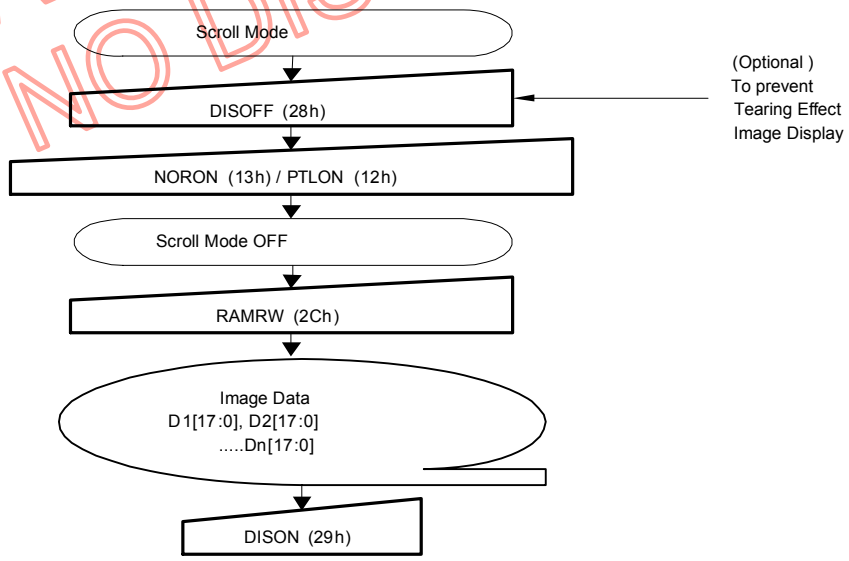
NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

Flow Chart

2. Continuous Scroll:



3. To Exit Vertical Scroll Mode:



NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On (12h) commands.

9.1.27 TEOFF (34h): Tearing Effect Line OFF

34h	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	-This command has no effect when Tearing Effect output is already OFF.

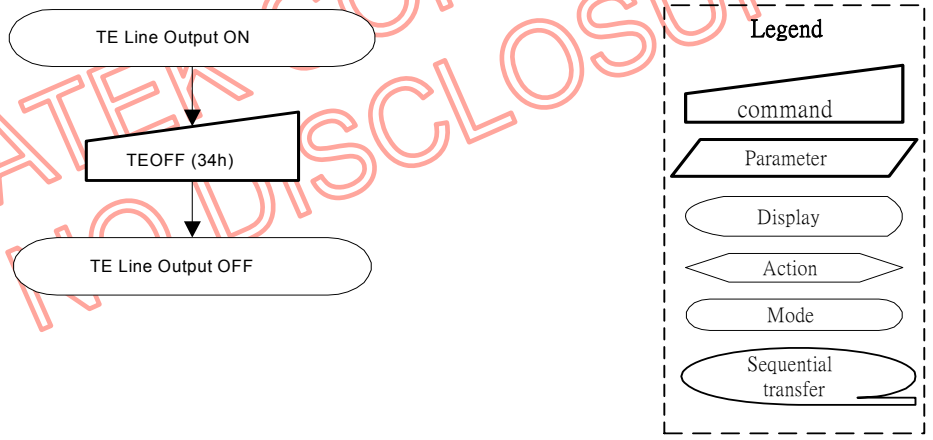
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



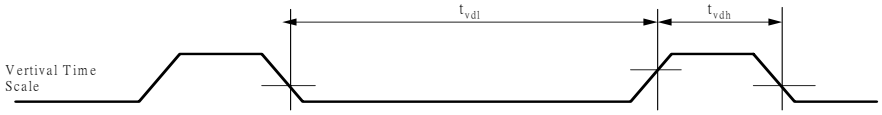
9.1.28 TEON (35h): Tearing Effect Line ON

35h	TEON (Tearing Effect Line ON)												
Inst / Para	D/CX	WRX	RDX	**D17-8**	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
Parameter	1	↑	1	-	-	-	-	-	-	-	-	M	00h

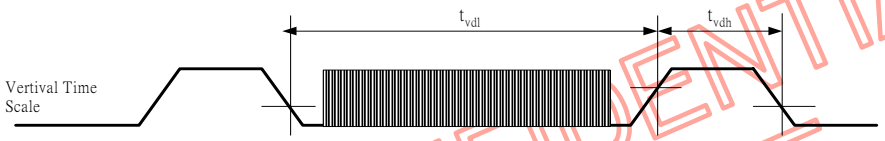
NOTE: "-" Don't care

Description

-This command is used to turn ON the Tearing Effect output signal from the TE signal line.
-This output is not affected by changing MADCTR bit ML.
-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).



—When M='0': The Tearing Effect Output line consists of V-Blanking information only.



—When M='1': The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

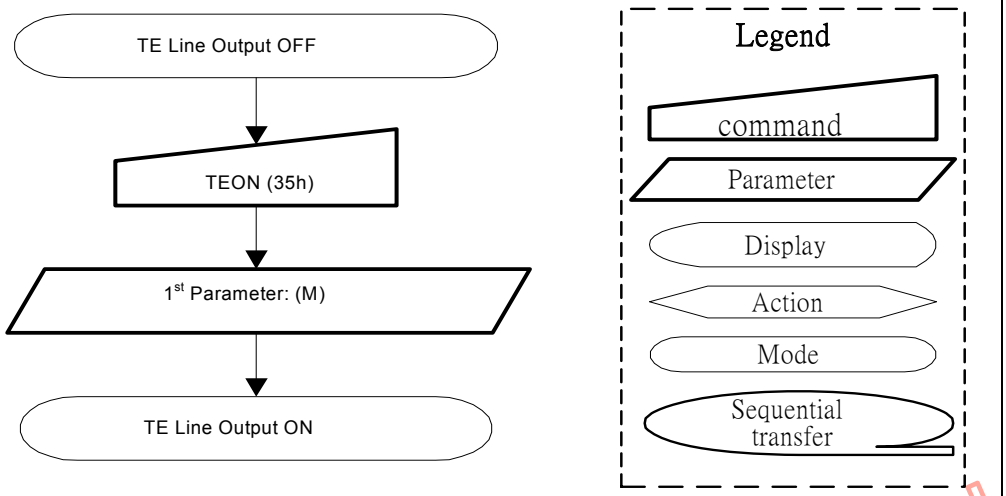
-This command has no effect when Tearing Effect output is already OFF.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off & M=0
S/W Reset	Tearing effect off & M=0
H/W Reset	Tearing effect off & M=0

Flow Chart	

9.1.29 MADCTR (36h): Memory Data Access Control

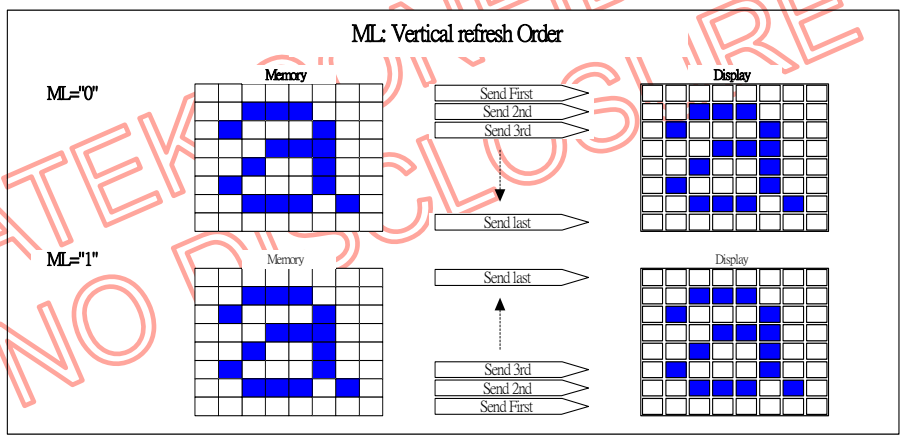
36h	MADCTR (Memory Data Access Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
Parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-	00h

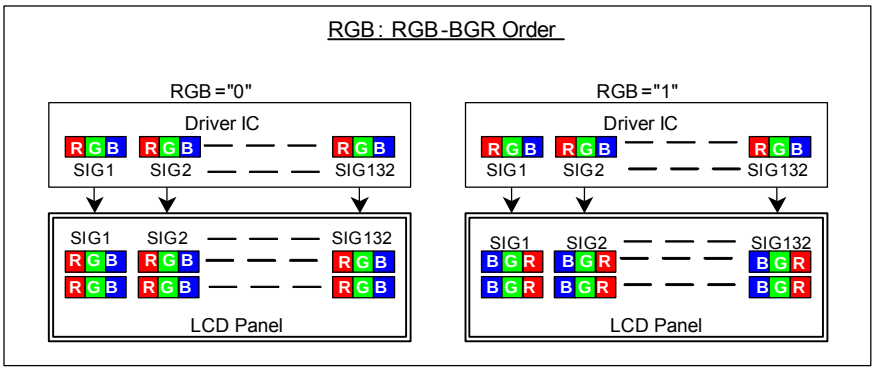
NOTE: "-" Don't care

Description

-This command defines read/ write scanning direction of frame memory.
-This command makes no change on the other driver status.
-Bit Assignment

Bit	NAME	DESCRIPTION
MY	ROW ADDRESS ORDER	These 3bits controls MPU to memory write/read direction. (See Section 8.11)
MX	COLUMN ADDRESS ORDER	
MV	ROW/COLUMN EXCHANGE	
ML	Vertical refresh ORDER	LCD Vertical refresh direction control
RGB	RGB-BGR ORDER	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel
MH	Display data latch order	'1' =LCD Refresh right to left '0' =LCD Refresh left to right





Restriction

-D1 and D0 of the 1st parameter are set to "00" internally.

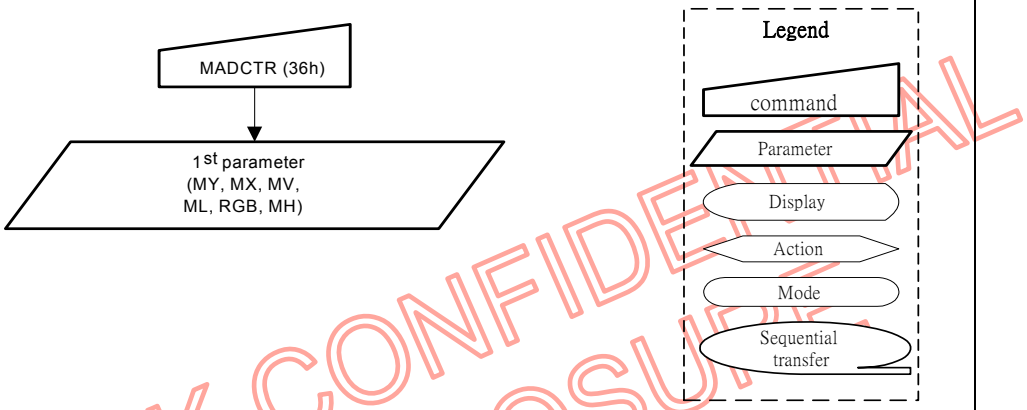
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0, MH=0
S/W Reset	No Change
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0, MH=0

Flow Chart



9.1.30 VSCSAD (37h): Vertical Scroll Start Address of RAM

37h	VSCSAD (Vertical Scroll Start Address of RAM)												
Inst / Para	D/CX	WRX	RDX	**D17-8**	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1st parameter	1	↑	1	-	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8	00h
2nd parameter	1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	00h

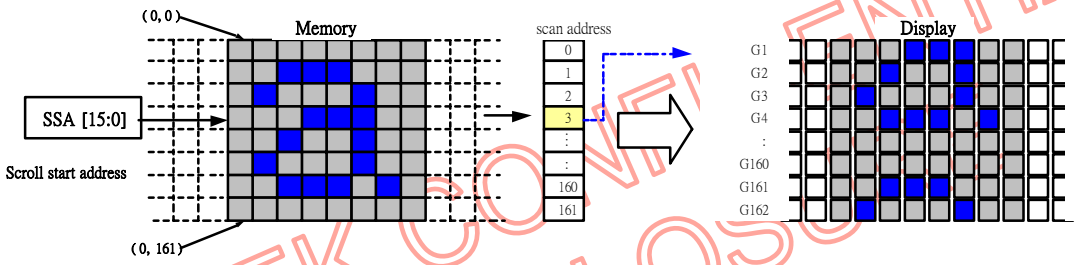
NOTE: "-" Don't care

Description

-This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.
-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:
-This command Start the scrolling.

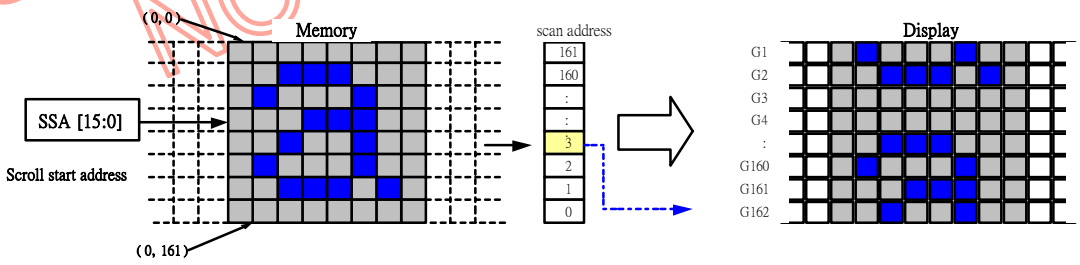
When MADCTL ML=0

Example: GM=11, 132RGB x 162
-When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=162 and Vertical Scrolling Pointer SSA='3'.



When MADCTL ML =1

Example: GM=11, 132RGB x 162
When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=162 and SSA='3'



NOTE: -When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
-SSA refers to the Frame Memory scan address.
-When new Pointer position and Picture Data, internal system works as 128x128 and maximum scan address becomes 127 internal of 161.

Restriction

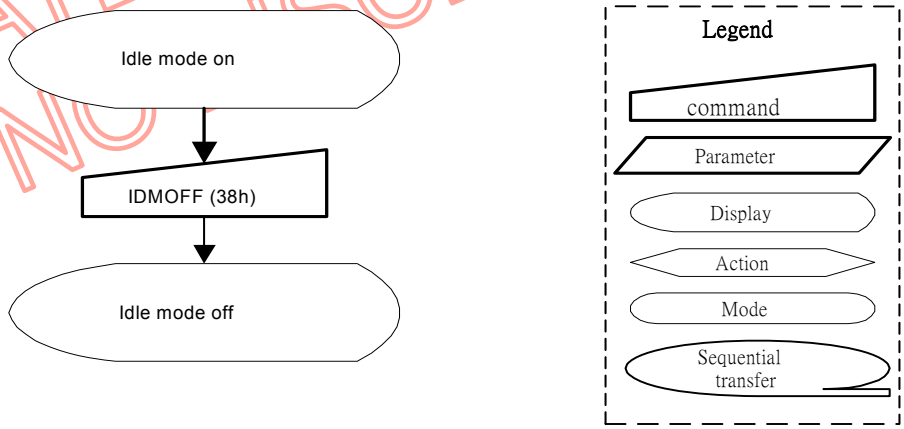
-Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.
SSA [15:0] is based on 1-line unit.
-SSA [15:0] = 0000h, 0001h, 0002h, 0003h, … , 00A1h

Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>S/W Reset</td><td>0000h</td></tr><tr><td>H/W Reset</td><td>0000h</td></tr></table>
Flow Chart	See Vertical Scrolling Definition (33h) description.

9.1.31 IDMOFF (38h): Idle Mode Off

38h	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is used to recover from Idle mode on. -There will be no abnormal visible effect on the display mode change transition. -In the idle off mode, 1. LCD can display maximum 4096,65k, 262k colors. 2. Normal frame frequency is applied.
Restriction	-This command has no effect when module is already in idle off mode.
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: Idle Mode Off Status: S/W Reset — Default Value: Idle Mode Off
Flow Chart	

9.1.32 IDMON (39h): Idle Mode On

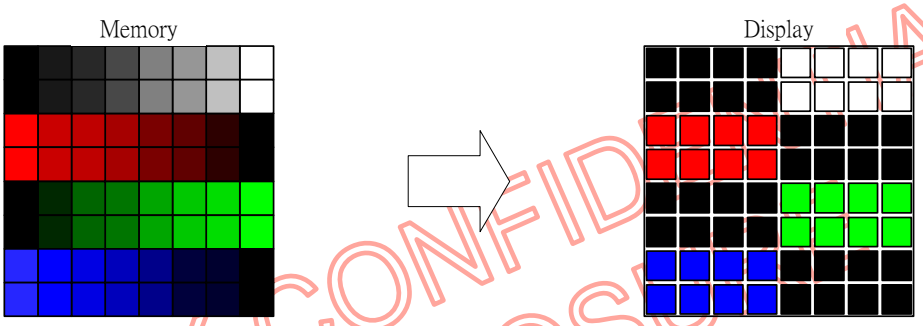
39h	IDMON (Idle Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

-This command is used to enter Idle mode on.
-There will be no abnormal visible effect on the display mode change transition.
-In the idle on mode,
1. Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)



Color	R5R4R3R2R1R0	G5G4G3G2G1G0	B5B4B3B4B1B0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

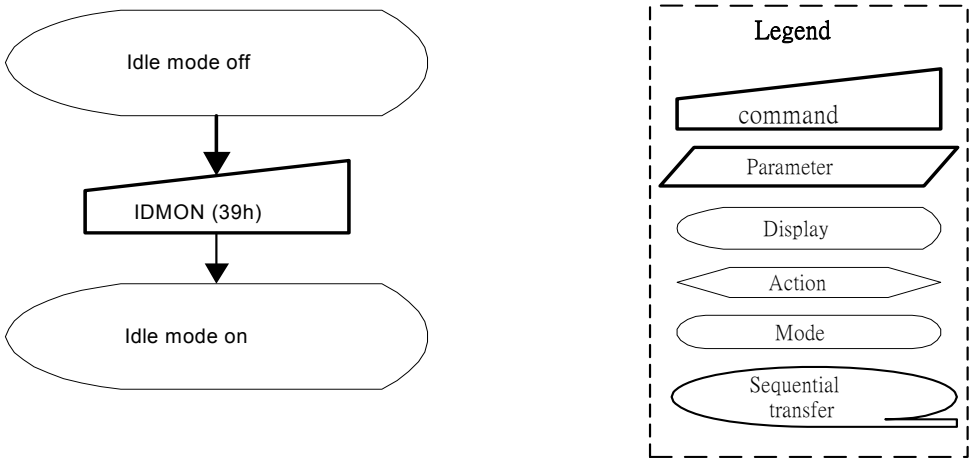
This command has no effect when module is already in idle on mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off

Flow Chart	

9.1.33 COLMOD (3Ah): Interface Pixel Format

3Ah	COLMOD (Interface Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
1st parameter	1	↑	1	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h

NOTE: "-" Don't care

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MPU Interface. The formats are shown in the table:

Bit	Description	Value
VIPF3 VIPF2 VIPF1 VIPF0	RGB Interface Color Format	"0101"=16 bit/pixel (1 times data transfer) "0110"=18 bit/pixel (1 times data transfer) "1110"=18 bit/pixel (3 times data transfer) The others = not defined
D3		"0" (Not Used)
IFPF2 IFPF1 IFPF0	Control Interface Color Format	"011"=12 bit/pixel "101"=16 bit/pixel "110"=18 bit/pixel The others = not defined

Note1: In 12-bits/Pixel, 16-bits/Pixel or 18-bits/Pixel mode, the LUT is applied to transfer data into the Frame Memory.
Note2: When RGB I/F the 12-bit/pixel don't care
Note 3: When VIPF[3:0]=" 1110" ,6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Restriction

There is no visible effect until the Frame Memory is written to.

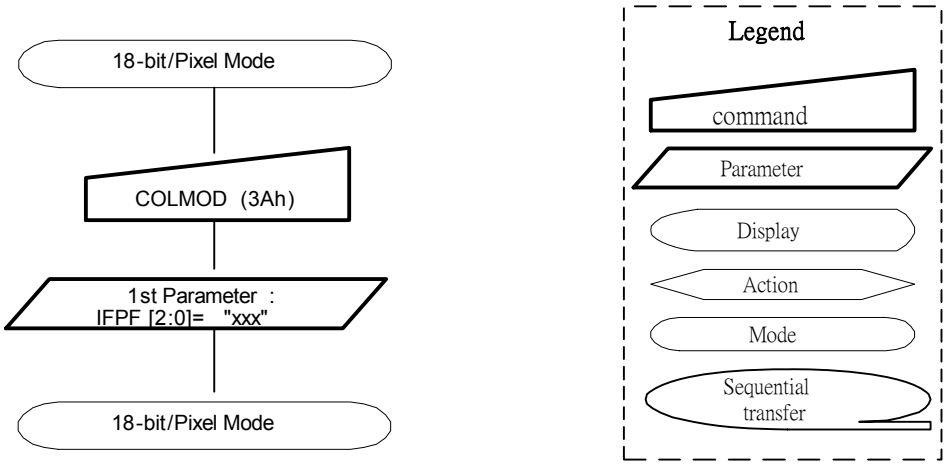
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18-Bit/Pixel
S/W Reset	No Change

Flow Chart



9.1.34 RDID1 (DAh): Read ID1 Value

DAh	RDID1 (Read ID1 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	38h

NOTE: "-" Don't care

Description

-This read byte returns 8-bit LCD module's manufacturer ID
-The 1st parameter is dummy data
-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.
NOTE: See command RDDID (04h), 2nd parameter.

Restriction

Register Availability

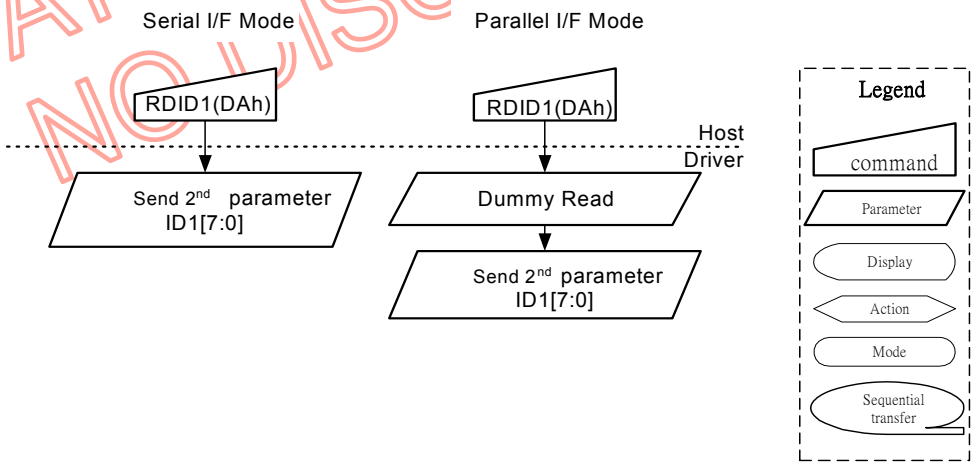
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	38h
S/W Reset	38h
H/W Reset	38h

Note: ID1 can be modified by metal option.

Flow Chart



9.1.35 RDID2 (DBh): Read ID2 Value

DBh	RDID2 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h

NOTE: "-" Don't care

Description

-This read byte returns 8-bit LCD module/driver version ID
-The 1st parameter is dummy data
-The 2nd parameter (ID26 to ID20): LCD module/driver version ID
-Parameter Range: ID=80h to FFh

D7 to D0	Version	Changes
80h	TBD	TBD
81h	TBD	TBD
82h	TBD	TBD
83h	TBD	TBD
-	TBD	TBD

NOTE: See command RDDID (04h), 3rd parameter.

Restriction

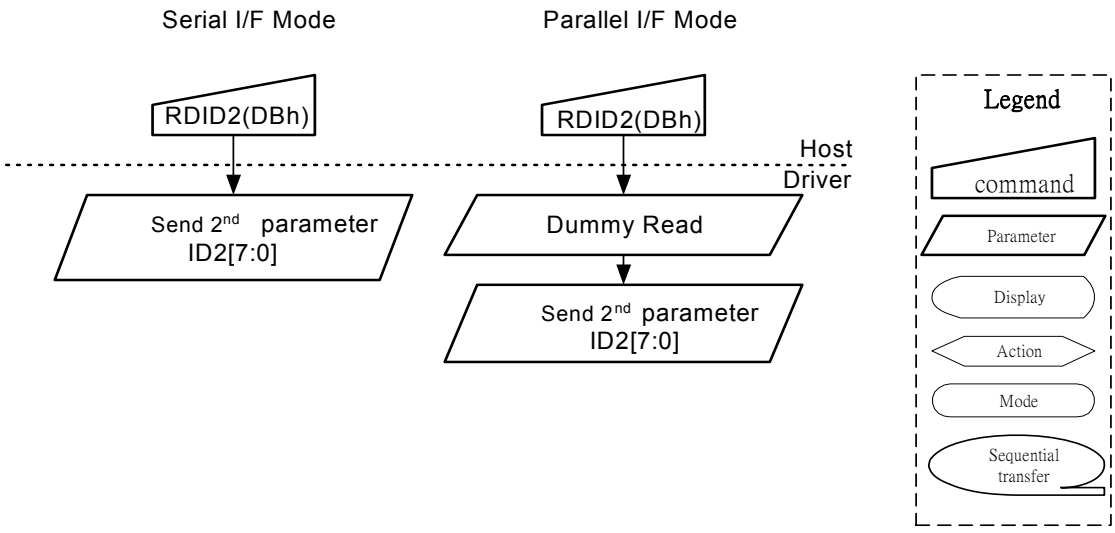
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

Flow Chart



9.1.36 RDID3 (DCh): Read ID3 Value

DBh	RDID3 (Read ID3 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	4Fh

NOTE: "-" Don't care

Description

-This read byte returns 8-bit LCD module/driver ID
-The 1st parameter is dummy data
-The 2nd parameter (ID37 to ID30): LCD module/driver ID
-Parameter Range: ID=00h to FFh
NOTE: See command RDDID (04h), 4th parameter.

Restriction

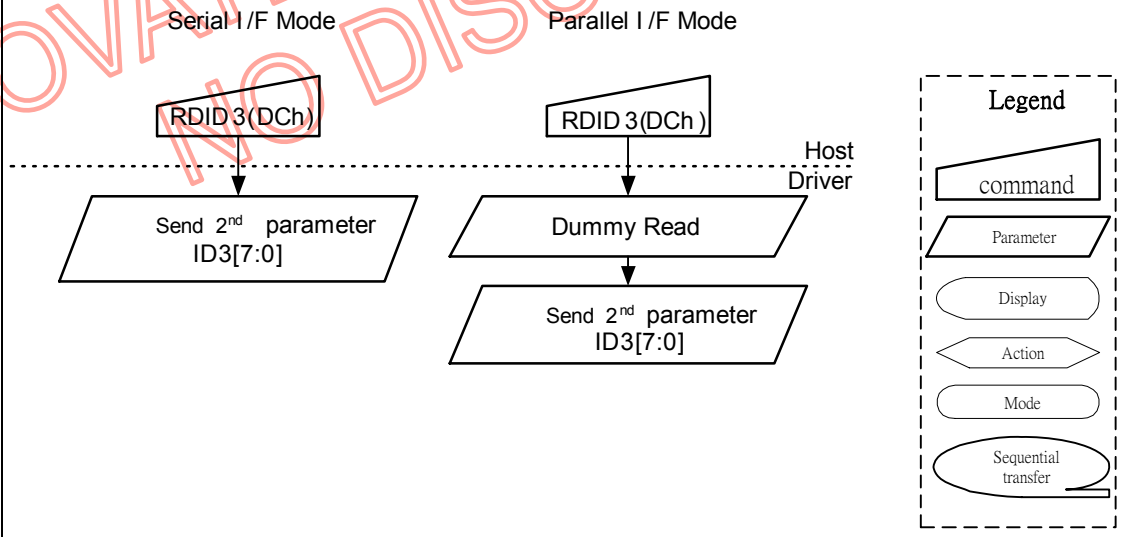
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	4Fh
S/W Reset	4Fh
H/W Reset	4Fh

Flow Chart



9.2 Panel Function Command List and Description

Table 9.2.1 Panel Function Command List (1)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
RGBCTR	9.2.1	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)	Set RGB signal control ICM: RGB data access select DP, HSP, VSP: PCLK, HS, VS polarity set
		1	↑	1	-	0	0	SWX	ICM	DP	EP	HSP	VSP	-	
					-	0	0	0	0	0	0	0	0	00h	
FRMCTR1	9.2.2	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	In normal mode (Full colors)
		1	↑	1	-				DIVA4	DIVA3	DIVA2	DIVA1	DIVA0		
					-	0	0	0	0	0	0	0	0	-	
		1	↑	1	-			VPA5	VPA4	VPA3	VPA2	VPA1	VPA0		
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
FRMCTR2	9.2.3	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	In Idle mode (8-colors)
		1	↑	1	-				DIVB4	DIVB3	DIVB2	DIVB1	DIVB0		
					-	0	0	0	0	0	0	0	0	-	
		1	↑	1	-			VPB5	VPB4	VPB3	VPB2	VPB1	VPB0		
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
FRMCTR3	9.2.4	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	In partial mode (Full colors)
		1	↑	1	-				DIVC4	DIVC3	DIVC2	DIVC1	DIVC0		
					-	0	0	0	0	0	0	0	0	-	
		1	↑	1	-			VPC5	VPC4	VPC3	VPC2	VPC1	VPC0		
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
INVCTR	9.2.5	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	Display inversion control
		1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC	02h	NLA, NLB, NLC: set inversion
					-	0	0	0	0	0	0	1	0		
RGB PRCTR	9.2.6	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)	RGB I/F Blanking porch setting
		1	↑	1	-			HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	08h	HS back porch setting
					-	0	0	0	0	0	0	0	0		
		1	↑	1		VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	03h	VS back porch setting
		1	↑	1								VBP9	VBP8	00h	
DISSET5	9.2.7	0	↑	1	-	1	0	1	1	0	1	1	1	(B6h)	Display function setting
		1	↑	1	-	0	0	NO1	NO0	SDT1	SDT0	EQ1	EQ0	16h	NO: the amount of non-overlap SDT: set amount of source delay PT: No display area source/ VCOM/ Gate output control EQ: set EQ period
					-	0	0	0	1	0	1	1	0		
		1	↑	1	-	0	0	0	0	PTG1	PTG0	PT1	PT0	02h	
					-	0	0	0	0	0	0	1	0		
DISSET6	9.2.8	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)	SD output direction control
		1	↑	1	-								CRL	00h	
					-	0	0	0	0	0	0	0	0		
DISSET7	9.2.9	0	↑	1	-	1	0	1	1	1	0	0	0	(B8h)	GD output direction control
		1	↑	1	-								CTB	00h	
					-	0	0	0	0	0	0	0	0		
DISSET8		0	↑	1	-	1	0	1	1	1	0	0	1	(B9h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
LTPSSET1		0	↑	1	-	1	0	1	1	1	0	1	0	(BAh)	LTPS function setting 1
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
LTPSSET2		0	↑	1	-	1	0	1	1	1	0	1	1	(BBh)	LTPS function setting 2
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
LTPSSET3		0	↑	1	-	1	0	1	1	1	1	0	0	(BCh)	LTPS function setting 3
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
LTPSSET4		0	↑	1	-	1	0	1	1	1	1	0	1	(BDh)	LTPS function setting 4
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
LTPSSET5		0	↑	1	-	1	0	1	1	1	1	1	0	(BEh)	LTPS function setting 5
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
LTPSSET6		0	↑	1	-	1	0	1	1	1	1	1	1	(BFh)	LTPS function setting 6
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		

"-": Don't care

Note 1: B0h to BFh are fixed for about display function setting

Note 2: BAh to BFh registers are fixed for LTPS function setting.

Note 3: B7h to B9h registers are reserved for future using.

Table 9.2.1 Panel Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PWCTR1	9.2.8	0	↑	1	-	1	0	1	1	0	0	0	0	(C0h)	Power control setting
		1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	-	VRH: Set the GVDD voltage
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	0	0	0	0	VC2	VC1	VC0	03h	VC: Set the VCI1 voltage
					-	0	0	0	0	0	0	1	1		
PWCTR2	9.2.9	0	↑	1	-	1	0	1	1	0	0	0	1	(C1h)	Power control setting
		1	↑	1	-	0	0	0	0	0	BT2	BT1	BT0	07h	BT:set AVDD/VCL/VGH/ VGL voltage
					-	0	0	0	0	0	1	1	1		
PWCTR3	9.2.10	0	↑	1	-	1	0	1	1	0	0	1	0	(C2h)	In normal mode (Full colors)
		1	↑	1	-	0	0	0	0	0	APA2	APA 1	APA 0	04h	AP: adjust the operational amplifier
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	0	0	0	0	DCA2	DCA1	DCA0	06h	DC: adjust the booster circuit for Idle mode
					-	0	0	0	0	0	0	0	0		
PWCTR4	9.2.11	0	↑	1	-	1	0	1	1	0	0	1	1	(C3h)	In Idle mode (8-colors)
		1	↑	1	-	0	0	0	0	0	APB2	APB1	APB0	02h	AP: adjust the operational amplifier
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	0	0	0	0	DCB2	DCB1	DCB0	07h	DCT: adjust the booster circuit for Idle mode
					-	0	0	0	0	0	0	0	0		
PWCTR5	9.2.12	0	↑	1	-	1	0	1	1	0	1	0	0	(C4h)	In partial mode + Full colors
		1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0	03h	AP: adjust the operational amplifier
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	0	0	0	0	DCC2	DCC1	DCC0	07h	DCT: adjust the booster circuit for Idle mode
					-	0	0	0	0	0	0	0	0		
VMCTR1	9.2.13	0	↑	1	-	1	0	1	1	0	1	0	1	(C5h)	VCOM control 1
		1	↑	1	-	nVM	VMH6	VMH5	VMH4	VMH3	VMH	VMH1	VMH0	-	nVM: VCOM input select
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	VML6	VML5	VML4	VML3	VML2	VML1	VML0	-	VMH: VCOMH voltage control VML: VCOML voltage control
					-	0	0	0	0	0	0	0	0		
VMCTR2	9.2.14	0	↑	1	-	1	0	1	1	0	1	1	0	(C6h)	VCOM control 2
		1	↑	1	-	0	0	VMA5	VMA4	VMA3	VMA2	VMA	VMA0		VMA: VCOMAC voltage control
					-	0	0	0	0	0	0	0	0		
VMOF CTR	9.2.15	0	↑	1	-	1	0	1	1	0	1	1	1	(C7h)	VCOM control 3
		1	↑	1	-	nVM	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	00h	VMF: VCOM offset control
					-	0	0	0	0	0	0	0	0		
RVMOF CTR	9.2.16	0	1	↑	-	1	0	1	1	1	0	0	0	(C8h)	VCOM control 4
		1	1	↑	-	nVM	RVMF6	RVMF5	RVMF4	RVMF3	RVMF2	RVMF1	RVMF0	-	Read the VMOF value form NV memory
					-	0	0	0	0	0	0	0	0	-	
PWCTR6		0	↑	1	-	1	0	1	1	1	0	0	1	(C9h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
PWCTR7		0	↑	1	-	1	0	1	1	1	0	1	0	(CAh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
PWCTR8		0	↑	1	-	1	0	1	1	1	0	1	1	(CBh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	0	1	1	1	1	0	0	(CCh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	0	1	1	1	1	0	1	(CDh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	0	1	1	1	1	1	0	(CEh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	0	1	1	1	1	1	1	(CFh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		

"-": Don't care

Note 1: C0h to CFh are fixed for about power controller.

Note 2: The C9h to CFh are reserved for further using.

Table 9.2.1 Panel Function Command List (3)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
ID1		0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
WRID2	9.2.18	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	LCM version code
		1	↑	1	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Write ID2 value to NV memory Set the LCM version code at ID2
					-	0	0	0	0	0	0	0	0		
WRID3	9.2.19	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Customer Project code
		1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Write ID3 value to NV memory Set the project code at ID3
					-	0	0	0	0	0	0	0	0		
RDID4	9.2.20	0	↑	1	-	1	1	0	1	0	0	1	1	(D3h)	IC Vender Coder
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
					-	-	-	-	-	-	-	-	-		
		1	1	↑	-	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410		ID41: IC Vender Coder ID42: IC Part Number Coder ID43: Chip version coder
					-	0	0	0	0	0	0	0	0		
		1	1	↑	-	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420		
					-	0	0	0	0	0	0	0	0		
		1	1	↑	-	-	-	-	-	ID433	ID432	ID431	ID430		
					-	-	-	-	-	0	0	0	0		
		1	1	↑	-	-	-	-	-	-	-	-	-		
					-	-	-	-	-	-	-	-	-		
ID5		0	↑	1	-	1	1	0	1	0	1	0	0	(D4h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
ID6		0	↑	1	-	1	1	0	1	0	1	0	1	(D5h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
ID7		0	↑	1	-	1	1	0	1	0	1	1	0	(D6h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
ID8		0	↑	1	-	1	1	0	1	0	1	1	1	(D7h)	Reserved for future using
		1	↑	1											
					-										
Reserved		0	↑	1	-	1	1	0	1	1	1	0	0	(D8h)	Reserved for future using
		1	↑	1											
					-										
NVCTR1	9.2.22	0	↑	1	-	1	1	0	1	1	1	0	1	(D9h)	NV memory function controller 1
		1	↑	1	-	MTP Cnt[3:0]				-	-	MTP_PON	MTPWR_EN	00h	
					-	0	0	0	0	0	0	0	0		
NVCTR2	9.2.23	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)	NV memory function controller 2
		1	↑	1	-	0	1	0	1	0	1	0	1	55h	
					-	1	0	1	0	1	0	1	0	AAh	
					-	0	1	1	0	0	1	1	0	66h	
Reserved		0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	
		1	↑	1	-	-	-	-	-	-	-	-	-	-	
					-	-	-	-	-	-	-	-	-		

"-": Don't care

Note 1: The D0h to D8h registers are fixed for about ID code setting.

Note 2: The D9h, DEh and DFh registers are used for NV Memory function controller. (Ex: write, clear, etc.)

Note 3: The D4h to D8h registers are reserved for future using.

Table 9.2.1 Panel Function Command List (4)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
GAMCTRP0	9.2.25	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Set Gamma correction
		0	↑	1	-	-	-	VP0[5:0]						-	Gamma adjustment (+ polarity)
		0	↑	1	-	-	-	VP1[5:0]							
		0	↑	1	-	-	-	VP2[5:0]							
		0	↑	1	-	-	-	VP4[5:0]							
		0	↑	1	-	-	-	VP6[5:0]							
		0	↑	1	-	-	-	VP13[5:0]							
		0	↑	1	-	-	-	VP20[5:0]							
		0	↑	1	-	VP36[3:0]				VP27[3:0]					
		0	↑	1	-	-	-	VP43[5:0]							
		0	↑	1	-	-	-	VP50[5:0]							
		0	↑	1	-	-	-	VP57[5:0]							
		0	↑	1	-	-	-	VP59[5:0]							
		0	↑	1	-	-	-	VP61[5:0]							
		0	↑	1	-	-	-	VP62[5:0]							
		0	↑	1	-	-	-	VP63[5:0]							
GAMCTRN0	9.2.26	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Set Gamma correction
		0	↑	1	-	-	-	VN0[5:0]						-	Gamma adjustment (- polarity)
		0	↑	1	-	-	-	VN1[5:0]							
		0	↑	1	-	-	-	VN2[5:0]							
		0	↑	1	-	-	-	VN4[5:0]							
		0	↑	1	-	-	-	VN6[5:0]							
		0	↑	1	-	-	-	VN13[5:0]							
		0	↑	1	-	-	-	VN20[5:0]							
		0	↑	1	-	VN36[3:0]				VN27[3:0]					
		0	↑	1	-	-	-	VN43[5:0]							
		0	↑	1	-	-	-	VN50[5:0]							
		0	↑	1	-	-	-	VN57[5:0]							
		0	↑	1	-	-	-	VN59[5:0]							
		0	↑	1	-	-	-	VN61[5:0]							
		0	↑	1	-	-	-	VN62[5:0]							
		0	↑	1	-	-	-	VN63[5:0]							
GAMCTR1		0	↑	1	-	1	1	1	0	0	0	1	0	(E2h)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
GAMCTR2		0	↑	1	-	1	1	1	0	0	0	1	1	(E3h)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
GAMCTR3		0	↑	1	-	1	1	1	0	0	1	0	0	(E4h)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
GAMCTR4		0	↑	1	-	1	1	1	0	0	1	0	1	(E5h)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
GAMCTR5		0	↑	1	-	1	1	1	0	0	1	1	0	(E6h)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
GAMCTR6		0	↑	1	-	1	1	1	0	0	1	1	1	(E7h)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	1	0	0	0	(E8h)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	1	0	0	1	(E9h)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	1	0	1	0	(EAh)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	1	0	1	1	(EBh)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	1	1	0	0	(ECh)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	1	1	0	1	(EDh)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	1	1	1	0	(EEh)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	1	1	1	1	(EFh)	Reserved for

		1	↑	1	-											future using
					-	0	0	0	0	0	0	0	0			

"-": Don't care

Note 1: E0-E7 registers are fixed for about Gamma adjusting.

Note 2: The E8h to EFh are reserved for future using.

Table 9.2.1 Panel Function Command List (5)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
Reserved		0	↑	1	-	1	1	1	0	0	0	0	0	(F0h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	0	0	0	0	(F1h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
GAM_R_SEL	9.2.28	0	↑	1	-	1	1	1	0	0	0	1	0	(F2h)	Gamma switch control
		1	↑	1	-	-	-	-	-	-	-	-	GAM_R_SEL	00h	
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	0	0	1	1	(F3h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	0	1	0	0	(F4h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	0	1	0	1	(F5h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	0	1	1	0	(F6h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	0	1	1	1	(F7h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	0	0	0	(F8h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	0	0	1	(F9h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	0	1	0	(FAh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	0	1	1	(FBh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	1	0	0	(FCh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	1	0	1	(FDh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	1	1	0	(FEh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	1	1	1	(FFh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		

"-": Don't care

Note 1: F6h to FFh registers are reserved for about special or chip test using

Note 2: The F0h to F1h and F3h to F5h registers are reserved for future using

9.2.1 RGBCTR (B0h): RGB signal control

B0h	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RASET	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)
1st Parameter	1	↑	1	-	0	0	SWX	ICM	DP	EP	HSP	VSP	00h

NOTE: "-" Don't care

Description

-Set the operation status on the RGB interface. The setting becomes effective as soon as the command is received.

SWX	RGB Mode 2		
	INV On/Off (21h/20h)	Idle Mode On/Off (39h/38h)	Display On/Off (29h/28h)
0	Enable	Enable	Enable
1	Disable	Disable	Disable

-ICM: GRAM Write/Read frequency and data input select on the RGB interface

ICM	Write/ Read frequency and input data select		
	Write cycle	Read cycle	Data input
0	PCLK	PCLK	D[17:0]
1	SCL	Internal oscillator	SDA

Symbol	Name	Clock polarity set for RGB Interface
DP	PCLK polarity set	'1' = data fetched at the falling edge '0' = data fetched at the rising edge
EP	Enable polarity set	'1' = Low enable for RGB interface '0' = High enable for RGB interface
HSP	Hsync polarity set	'1' = High level sync clock '0' = Low level sync clock
VSP	Vsync polarity set	'1' = High level sync clock '0' = Low level sync clock

Restriction

-If this register not using the register need be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	SWX	ICM	DW	DP/EP/HSP/VSP
Power On Sequence	0d	0d	0d	0d/0d/0d/0d
S/W Reset	0d	0d	0d	0d/0d/0d/0d
H/W Reset	0d	0d	0d	0d/0d/0d/0d

Flow Chart	

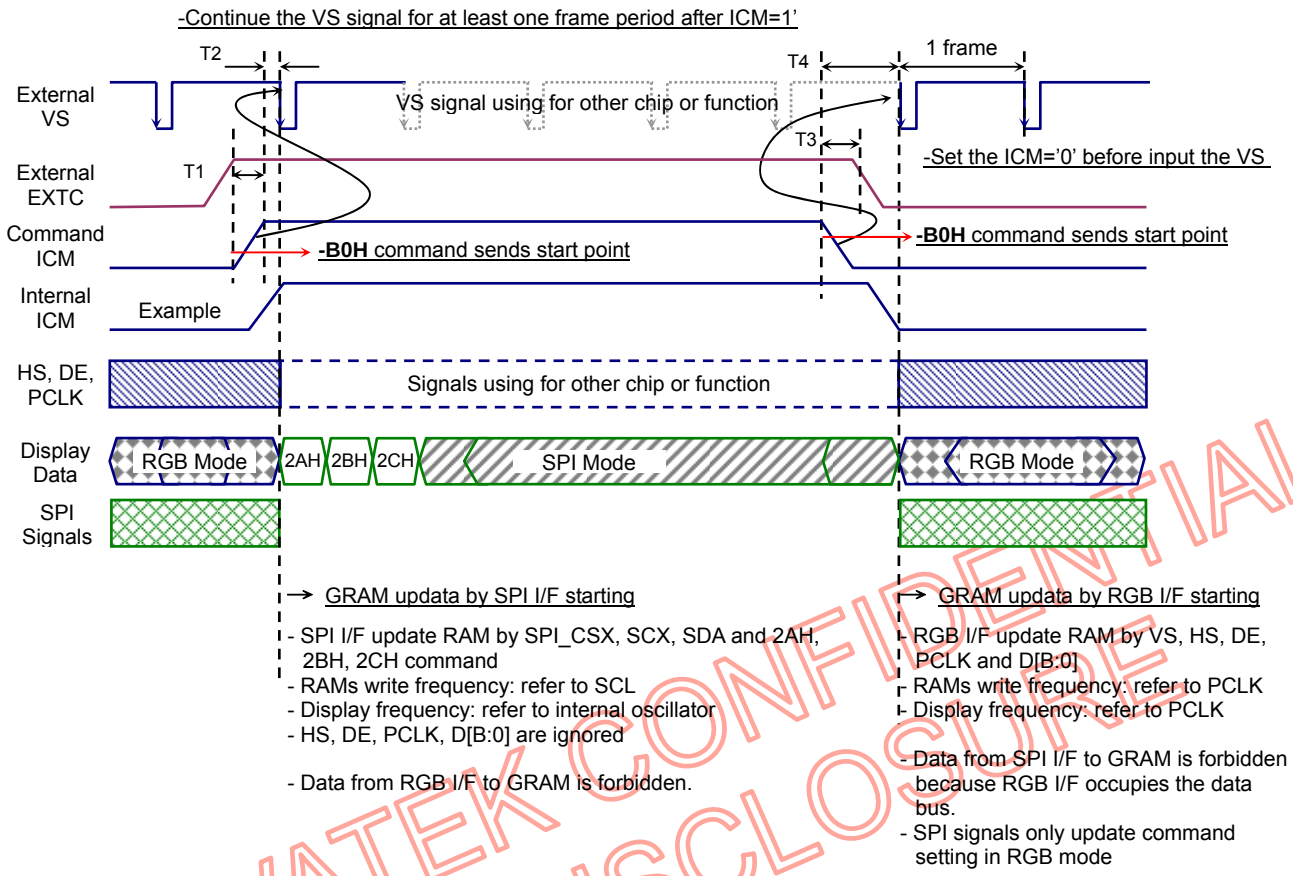


Fig. 9.2.1 RAM Access via RGB & SPI Interface in RGB Mode

Table 9.2.1 RAM Access via RGB & SPI Interface in RGB Mode

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
EXTC rising to ICM rising	T1	200ns + 18xT_{SCL}			ns	Note 3
ICM rising to VS falling	T2	200		< 1 frame	ns	
ICM falling to EXTC falling	T3	200ns + 18xT_{SCL}			ns	
EXTC falling to VS falling	T4	200ns + 18xT_{SCL}		< 1 frame	ns	Note 3

Note 1: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0H) command and RCM1, RCM0 = "1x".

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Note 3: B=17

9.2.2 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

B1H	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR1	0	↑	1	1	0	1	1	0	0	0	1	(B1h)
1st parameter	1	↑	1	-	-	-	DIVA4	DIVA3	DIVA2	DIVA1	DIVA0	-
2nd parameter	1	↑	1	-	-	VPA5	VPA4	VPA3	VPA2	VPA1	VPA0	-

NOTE: "-" Don't care

Description

Sets the division ratio for internal clocks of Normal mode at CPU interface mode.
DIVA[4:0]: division ratio for internal clocks when Normal mode.
VPA[5:0]: Vsync porch for internal clocks when Normal mode.

$$Frame\_rate = \frac{200kHz}{(Line + VPA[5:0])(DIVA[4:0] + 4)}$$

(1)When GM=00(128*160)
In Normal mode, line=160, Default value DIVA[4:0]=14, VPA[5:0]=20, Frame rate=61.7Hz

(2)When GM=01(120*160)
In Normal mode, line=160, Default value DIVA[4:0]=14, VPA[5:0]=20, Frame rate=61.7Hz

(3)When GM=10(128*128)
In Normal mode, line=128, Default value DIVA[4:0]=18, VPA[5:0]=20, Frame rate=61.4Hz

(4)When GM=11(132*162)
In Normal mode, line=162, Default value DIVA[4:0]=14, VPA[5:0]=20, Frame rate=61Hz

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

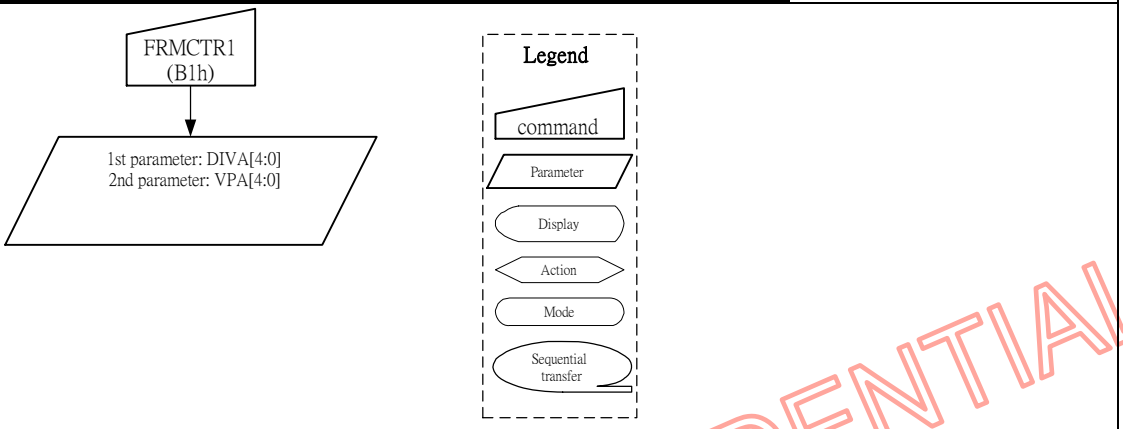
(1)When GM=11(132*162), GM=00(128*160) or GM=01(120*160)

Status	Default Value	
	DIVA[4:0]	VPA[5:0]
Power On Sequence	0Eh/14d	14h/20d
S/W Reset	0Eh/14d	14h/20d
H/W Reset	0Eh/14d	14h/20d

(2)When GM=10(128*128)

Status	Default Value	
	DIVA[4:0]	VPA[5:0]
Power On Sequence	12h/18d	14h/20d
S/W Reset	12h/18d	14h/20d
H/W Reset	12h/18d	14h/20d

Flow Chart



9.2.3 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-color)

B2H	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR2	0	↑	1	1	0	1	1	0	0	1	0	(B2h)
1st parameter	1	↑	1	-	-	-	DIVB4	DIVB3	DIVB2	DIVB1	DIVB0	-
2nd parameter	1	↑	1	-	-	VPB5	VPB4	VPB3	VPB2	VPB1	VPB0	-

NOTE: "-" Don't care

Description

Sets the division ratio for internal clocks of Idle mode at CPU interface mode.
DIVB[4:0]: division ratio for internal clocks when Idle mode.
VPB[5:0]: Vsync porch for internal clocks when Idle mode.

$$Frame\_rate = \frac{200kHz}{(Line + VPB[5:0])(DIVB[4:0] + 4)}$$

(1)When GM=00(128*160)
In 8-color mode, line=160, DIVB[4:0]=14, VPB[5:0]=20, Frame rate=61.7Hz

(2)When GM=01(120*160)
In 8-color mode, line=160, DIVB[4:0]=14, VPB[5:0]=20, Frame rate=61.7Hz

(3)When GM=10(128*128)
In 8-color mode, line=128, DIVB[4:0]=18, VPB[5:0]=20, Frame rate=61.4Hz

(4)When GM=11(132*162)
In 8-color mode, line=162, DIVB[4:0]=14, VPB[5:0]=20, Frame rate=61Hz

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

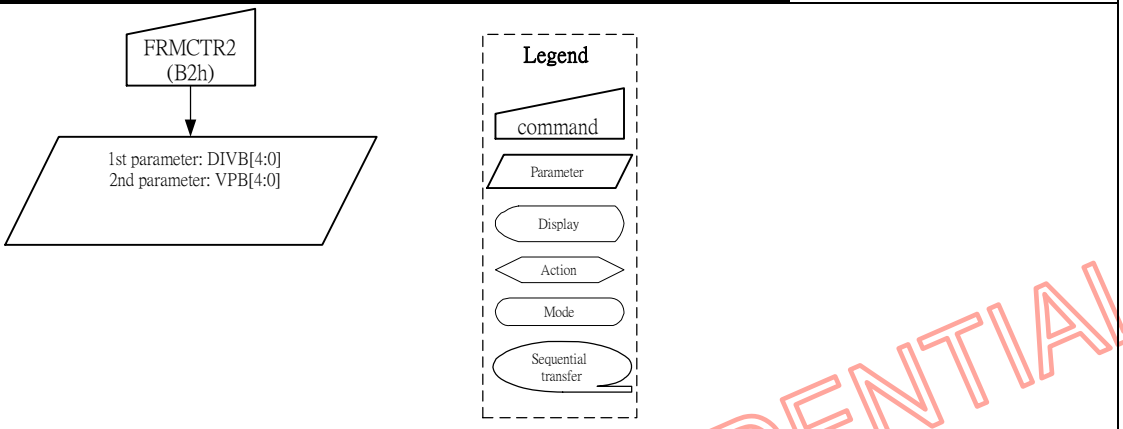
(1)When GM=11(132*162), GM=00(128*160) or GM=01(120*160)

Status	Default Value	
	DIVB[4:0]	VPB[5:0]
Power On Sequence	0Eh/14d	14h/20d
S/W Reset	0Eh/14d	14h/20d
H/W Reset	0Eh/14d	14h/20d

(2)When GM=10(128*128)

Status	Default Value	
	DIVB[4:0]	VPB[5:0]
Power On Sequence	12h/18d	14h/20d
S/W Reset	12h/18d	14h/20d
H/W Reset	12h/18d	14h/20d

Flow Chart



9.2.4 FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

B3H	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR3	0	↑	1	1	0	1	1	0	0	1	1	(B3h)
1st parameter	1	↑	1	-	-	-	DIVC4	DIVC3	DIVC2	DIVC1	DIVC0	-
2nd parameter	1	↑	1	-	-	VPC5	VPC4	VPC3	VPC2	VPC1	VPC0	-

NOTE: "-" Don't care

Description

Sets the division ratio for internal clocks of Partial mode at CPU interface mode.
DIVC[4:0]: division ratio for internal clocks when Partial mode.
VPC[5:0]: Vsync porch for internal clocks when Partial mode.

$$Frame\_rate = \frac{200kHz}{(Line + VPC[5:0])(DIVC[4:0] + 4)}$$

(1)When GM=00(128*160)
In Partial mode, line=160, DIVC[4:0]=14, VPC[5:0]=20, Frame rate=61.7Hz

(2)When GM=01(120*160)
In Partial mode, line=160, DIVC[4:0]=14, VPC[5:0]=20, Frame rate=61.7Hz

(3)When GM=10(128*128)
In Partial mode, line=128, DIVC[4:0]=18, VPC[5:0]=20, Frame rate=61.4Hz

(4)When GM=11(132*162)
In Partial mode, line=162, DIVC[4:0]=14, VPC[5:0]=20, Frame rate=61Hz

Restriction

-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

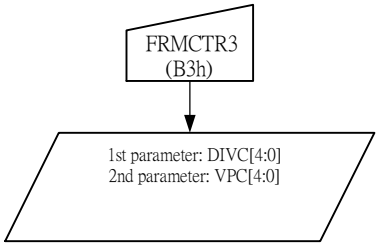
(1)When GM=11(132*162), GM=00(128*160) or GM=01(120*160)

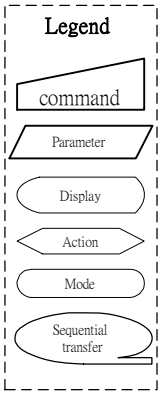
Status	Default Value	
	DIVC[4:0]	VPC[5:0]
Power On Sequence	0Eh/14d	14h/20d
S/W Reset	0Eh/14d	14h/20d
H/W Reset	0Eh/14d	14h/20d

(2)When GM=10(128*128)

Status	Default Value	
	DIVC[4:0]	VPC[5:0]
Power On Sequence	12h/18d	14h/20d
S/W Reset	12h/18d	14h/20d
H/W Reset	12h/18d	14h/20d

Flow Chart





9.2.5 INVCTR (B4h): Display Inversion Control

B4H	INVCTR (Display Inversion Control)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
1st Parameter	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC	02h

NOTE: "-" Don't care

Description

-Display Inversion mode control

-NLA: Inversion setting in full colors normal mode (Normal mode on)

NLA	Inversion setting in full colours normal mode
0	Line Inversion
1	Frame Inversion

-NLB: Inversion setting in Idle mode (Idle mode on)

NLB	Inversion setting in Idle mode
0	Line Inversion
1	Frame Inversion

-NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

NLC	Inversion setting in full colours partial mode
0	Line Inversion
1	Frame Inversion

Restriction

-If this register not using the register need be reserved.

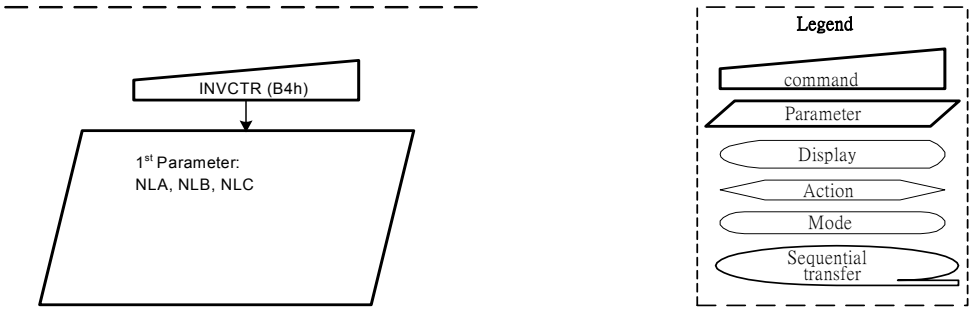
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	NLA	NLB	NLC	D7-0
Power On Sequence	0d	1d	0d	02h
S/W Reset	0d	1d	0d	02h
H/W Reset	0d	1d	0d	02h

Flow Chart



9.2.6 RGBBPCTR (B5h): RGB Interface Blanking Porch setting

B5H	RGBPSET (RGB Interface Blanking Porch setting)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBBPCTR	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)
1st Parameter	1	↑	1	-	-	-	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	08h
2nd Parameter	1	↑	1	-	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	03h
3rd Parameter	1	↑	1	-	-	-	-	-	-	-	VBP9	VBP8	00h

NOTE: "-" Don't care

Description

Vertical and Horizontal back porch control when RGB I/F mode 2 (RCM[1:0]=11)

HBP[5:0]: Set the delay period from falling edge of HSYNC signal to first valid data.

HBP[5:0]	No. of clock cycle of DOTCLK
00d	2
01d	3
02d	4
03d	5
⋮	⋮ (STEP 1) ⋮
62d	64
63d	65

VBP[9:0]: Set the delay period from falling edge of VSYNC signal to first valid line.

VBP[9:0]	No. of clock cycle of HSYNC
00d	(invalid)
01d	1
02d	2
03d	3
⋮	⋮ (STEP 1) ⋮
1022d	1022

Restriction

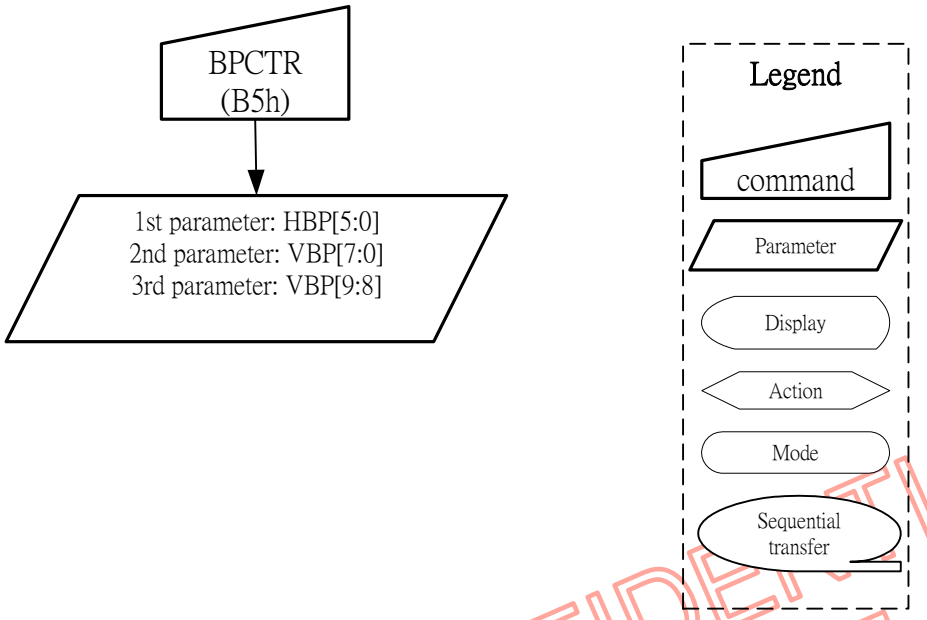
-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	HBP[5:0]	VBP[9:0]
Power On Sequence	08h	03h
S/W Reset	08h	03h
H/W Reset	08h	03h

Flow Chart	

9.2.7 DISSET5 (B6h): Display Function set 5

B6H	RGBPSET (RGB Interface Blanking Porch setting)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISSET5	0		1	-	1	0	1	1	0	1	1	0	(B6h)
1st Parameter	1	↑	1	-	0	0	NO1	NO0	SDT1	STD0	EQ1	EQ0	06h
2nd Parameter	1	↑	1	-	0	0	0	0	PTG1	PTG0	PT1	PT0	02h

NOTE: "-" Don't care

Description

-1st parameter: Set output waveform relation.

-NO[1:0]: Set the amount for non-overlap of the gate output

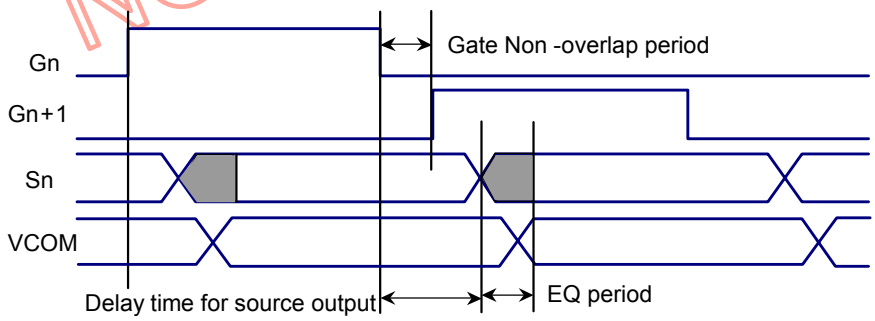
NO[1:0]		Amount of non-overlap of the gate output	
		Refer the Internal oscillator	Refer the PCLK
00	0	1 clock cycle	4 clock cycle
01	1	4 clock cycle	16 clock cycle
10	2	6 clock cycle	24 clock cycle
11	3	8 clock cycle	32 clock cycle

-SDT[1:0]: Set delay amount from gate signal falling edge to the source output.

SDT[1:0]		Amount of non-overlap of the source output	
		Refer the Internal oscillator	Refer the PCLK
00	0	1 clock cycle	4 clock cycle
01	1	2 clock cycle	8 clock cycle
10	2	3 clock cycle	12 clock cycle
11	3	4 clock cycle	16 clock cycle

-EQ[1:0]: Set the Equalizing period

EQ[1:0]		EQ period	
		Refer the Internal oscillator	Refer the PCLK
00	0	No EQ	No EQ
01	1	2 clock cycle	4 clock cycle
10	2	4 clock cycle	16 clock cycle
11	3	6 clock cycle	24 clock cycle



-2nd parameter: Set the output waveform in non-display area.

-PTG[1:0]: Determine gate output in a non-display area in the partial mode

PTG[1:0]		Gate output in a non-display area
00	0	Normal scan
01	1	Fix on VGL
10	2	Fix on VGL
11	3	Fix on VGL

-PT[1:0]: Determine Source /VCOM output in a non-display area in the partial mode

PT[1:0]		Source output on non-display area		VCOM output on non-display area	
		Positive	Negative	Positive	Negative
00	0	V63	V0	VCOML	VCOMH
01	1	V0	V63	VCOML	VCOMH
10	2	AGND	AGND	AGND	AGND
11	3	Hi-z	Hi-z	AGND	AGND

Restriction

-If this register not using the register need be reserved.

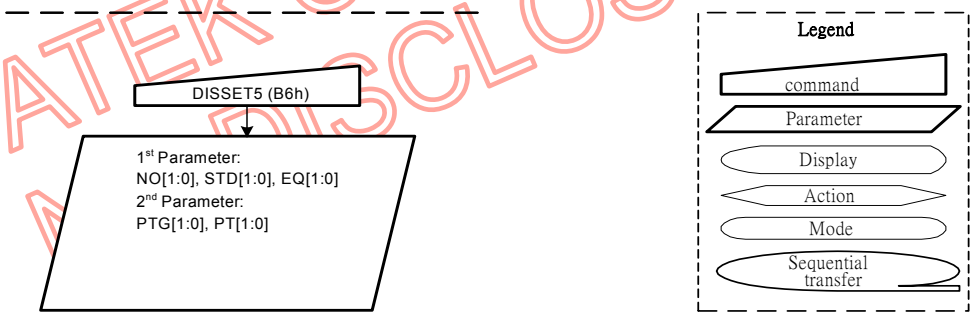
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	NO[1:0]	STD[1:0]	EQ[1:0]	PTG[1:0]	PT[1:0]
Power On Sequence	0d	1d	2d	0d	2d
S/W Reset	0d	1d	2d	0d	2d
H/W Reset	0d	1d	2d	0d	2d

Flow Chart



9.2.8 SDOCTR (B7h): Source Driver Direction Control

B7H	INVCTR (Display Inversion Control)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SDOCTR	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	CRL	00h

NOTE: "-" Don't care

Description

-CRL: Source output direction select register

CRL	Module source output direction			
	GM='00'	GM= '01'	GM='10'	GM='11'
0	**S7** -> S390	**S7** -> S366	**S7** -> S390	**S1** -> S396
1	S390 -> **S7**	S366 -> **S7**	S390 -> **S7**	S396 -> **S1**

-Please refer RGB I/F for detail using.

Restriction

-If this register not using the register need be reserved.

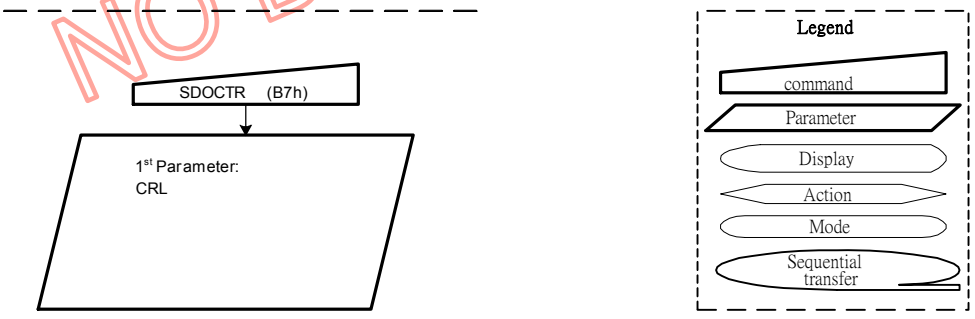
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CRL
Power On Sequence	0d
S/W Reset	0d
H/W Reset	0d

Flow Chart



9.2.9 GDOCTR (B8h): Gate Driver Direction Control

B8H	INVCTR (Display Inversion Control)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GDOCTR	0	↑	1	-	1	0	1	1	1	0	0	0	(B8h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	CTB	00h

NOTE: "-" Don't care

Description

-CTB: Gate output direction select register

CTB	Module Gate output direction		
	GM='00', '01'	GM='10'	GM='11'
0	**G2** -> G161	**G2** -> G129	**G1** -> G162
1	G161 -> **G2**	G129 -> **G2**	G162 -> **G1**

-Please refer RGB I/F for detail using.

Restriction

-If this register not using the register need be reserved.

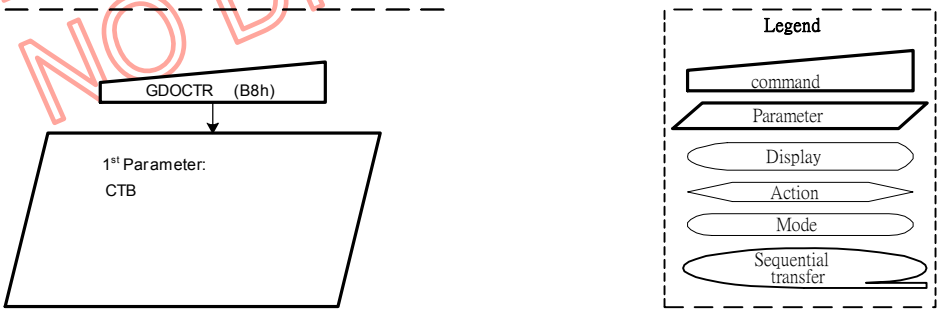
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CTB
Power On Sequence	0d
S/W Reset	0d
H/W Reset	0d

Flow Chart



9.2.10 PWCTR1 (C0h): Power Control 1

C0H	PWCTR1 (Power Control 1)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1st Parameter	1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	-
2nd Parameter	1	↑	1	-	0	0	0	0	0	VC2	VC1	VC0	02h

NOTE: "-" Don't care

Description

- -Set the GVDD and voltage

VRH[4:0]		GVDD
00000	0	5.00
00001	1	4.75
00010	2	4.70
00011	3	4.65
00100	4	4.60
00101	5	**4.55**
00110	6	4.50
00111	7	4.45
01000	8	4.40
01001	9	4.35
01010	10	4.30
01011	11	4.25
01100	12	4.20
01101	13	4.15
01110	14	4.10
01111	15	4.05
10000	16	4.00
10001	17	3.95
10010	18	3.90
10011	19	3.85
10100	20	3.80
10101	21	**3.75**
10110	22	3.70
10111	23	3.65
11000	24	3.60
11001	25	3.55
11010	26	3.50
11011	27	3.45
11100	28	3.40
11101	29	3.35
11110	30	3.25
11111	31	3.00

VC[2:0]		VCI1
000	0	2.75
001	1	2.70
010	2	**2.65**
011	3	2.60
100	4	2.55
101	5	2.50
110	6	2.45
111	7	2.40

Restriction

-If this register not using the register need be reserved.
-The deviation value of GVDD between with Measurement and Specification: **Max <=50mV**
-The deviation value of VCI1 between with Measurement and Specification: **Max <= 5%**

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	LCM = "00"	LCM = "01"	LCM = "10"	LCM = "11"	VC[2:0]
	TR LCD	TM LCD	Low Voltage	MVA LCD	
	VRH[4:0]	VRH[4:0]	VRH[4:0]	VRH[4:0]	
Power On Sequence	21d	5d	TBD	5d	2d
S/W Reset	21d	5d	TBD	5d	2d
H/W Reset	21d	5d	TBD	5d	2d

Flow Chart

9.2.11 PWCTR2 (C1h): Power Control 2

C1H	PWCTR2 (Power Control 2)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1st Parameter	1	↑	1	-	0	0	0	0	0	BT2	BT1	BT0	07h

NOTE: "-" Don't care

Description

- Set the AVDD, VCL, VGH and VGL supply power level

BT[2:0]		AVDD	VCL	VGH	VGL
000	0	4.75	-2.45	4xVCI1	-3xVCI1
001	1	4.75	-2.45	4xVCI1	-4xVCI1
010	2	4.75	-2.45	5xVCI1	-3xVCI1
011	3	4.75	-2.45	5xVCI1	-4xVCI1
100	4	4.75	-2.45	5xVCI1	-5xVCI1
101	5	4.75	-2.45	6xVCI1	-3xVCI1
110	6	4.75	-2.45	6xVCI1	-4xVCI1
111	7	**4.75**	**-2.45**	6xVCI1	-5xVCI1

Note: When VCI1=2.65V

Restriction

-If this register not using the register need be reserved.
-The deviation value of VGH/ VGL between with Measurement and Specification:
-VGH-VGL <= 32V

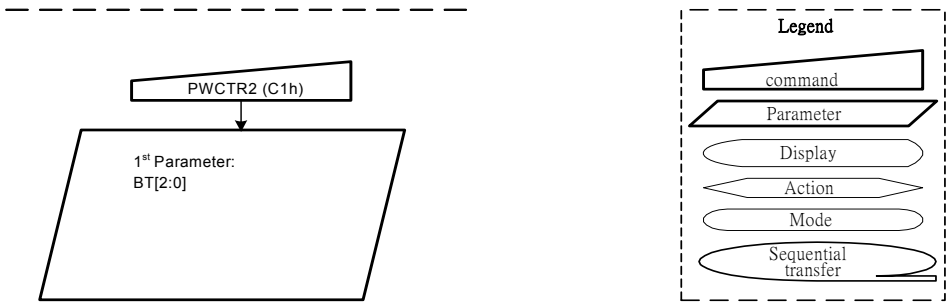
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	BT[2:0]
Power On Sequence	7d
S/W Reset	7d
H/W Reset	7d

Flow Chart



9.2.12 PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors)

C2H	PWCTR3 (Power Control 3)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)
1st Parameter	1	↑	1		0	0	0	0	0	APA2	APA1	APA0	02h
2nd Parameter	1	↑	1		0	0	0	0	0	DCA2	DCA1	DCA0	06h

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in normal mode/full colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APA[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	**2**	**Medium Low**
011	3	Medium
100	4	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Normal mode/ full colors.

DCA[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 4
001	1	BCLK / 1	BCLK / 8
010	2	BCLK / 1	BCLK / 16
011	3	BCLK / 2	BCLK / 8
100	4	BCLK / 2	BCLK / 16
101	5	BCLK / 4	BCLK / 32
110	**6**	**BCLK / 4**	**BCLK / 64**
111	7	BCLK / 8	BCLK / 64

Note: BCLK is Clock frequency for Booster circuit

Restriction

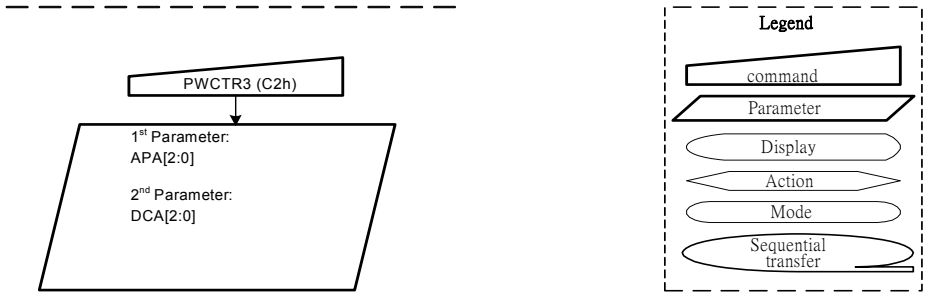
-If some parameter of the register not use the register need to be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	APA[2:0]	DCA[2:0]
Power On Sequence	4d	6d
S/W Reset	4d	6d
H/W Reset	4d	6d

Flow Chart	

9.2.13 PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)

C3H	PWCTR4 (Power Control 4)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR4	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)
1st Parameter	1	↑	1		0	0	0	0	0	APB2	APB1	APB0	01h
2nd Parameter	1	↑	1		0	0	0	0	0	DCB2	DCB1	DCB0	07h

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in Idle mode/ 8-colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APB[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	**1**	**Small**
010	2	Medium Low
011	3	Medium
100	4	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Idle mode/ 8-colors.

DCB[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 4
001	1	BCLK / 1	BCLK / 8
010	2	BCLK / 1	BCLK / 16
011	3	BCLK / 2	BCLK / 8
100	4	BCLK / 2	BCLK / 16
101	5	BCLK / 4	BCLK / 32
110	6	BCLK / 4	BCLK / 64
111	**7**	**BCLK / 8**	**BCLK / 64**

Note: BCLK is Clock frequency for Booster circuit

Restriction

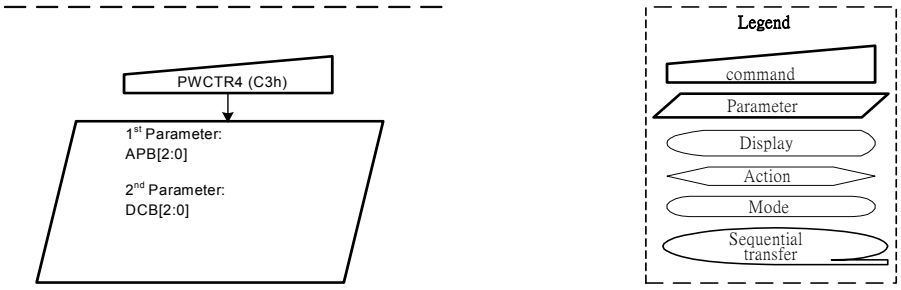
-If some parameter of the register not use, the register need to be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	APB[2:0]	DCB[2:0]
Power On Sequence	1d	7d
S/W Reset	1d	7d
H/W Reset	1d	7d

Flow Chart	

9.2.14 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)

C4H	PWCTR5 (Power Control 5)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR5	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)
1st Parameter	1	↑	1		0	0	0	0	0	APC2	APC1	APC0	01h
2nd Parameter	1	↑	1		0	0	0	0	0	DCC2	DCC1	DCC0	07h

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in Partial mode/ full-colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APC[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	**1**	**Small**
010	2	Medium Low
011	3	Medium
100	4	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Partial mode/ full-colors.

DCC[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 4
001	1	BCLK / 1	BCLK / 8
010	2	BCLK / 1	BCLK / 16
011	3	BCLK / 2	BCLK / 8
100	4	BCLK / 2	BCLK / 16
101	5	BCLK / 4	BCLK / 32
110	6	BCLK / 4	BCLK / 64
111	**7**	**BCLK / 8**	**BCLK / 64**

Note: BCLK is Clock frequency for Booster circuit

Restriction

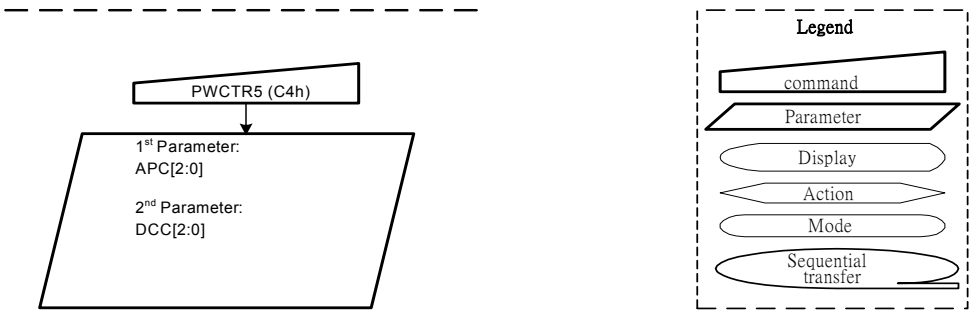
-If some parameter of the register not use the register need to be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	APC[2:0]	DCC[2:0]
Power On Sequence	1d	7d
S/W Reset	1d	7d
H/W Reset	1d	7d

Flow Chart	

9.2.15 VMCTR1 (C5h): VCOM Control 1

C5H	VMCTR1 (VCOM Control 1)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR1	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1st Parameter	1	↑	1		-	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	-
2nd Parameter	1	↑	1		0	VML6	VML5	VML4	VML3	VML2	VML1	VML0	-

NOTE: "-" Don't care

Description

-Set VCOMH Voltage

VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH
0000000	0	2.500	0011011	27	3.175	0110110	54	3.850	1010001	81	4.525
0000001	1	2.525	0011100	28	3.200	0110111	55	3.875	1010010	82	4.550
0000010	2	2.550	0011101	29	3.225	0111000	56	3.900	1010011	83	4.575
0000011	3	2.575	0011110	30	3.250	0111001	57	3.925	1010100	84	4.600
0000100	4	2.600	0011111	31	3.275	0111010	58	3.950	1010101	85	4.625
0000101	5	2.625	0100000	32	3.300	0111011	59	3.975	1010110	86	4.650
0000110	6	2.650	0100001	33	3.325	0111100	60	4.000	1010111	87	4.675
0000111	7	2.675	0100010	34	3.350	0111101	61	4.025	1011000	88	4.700
0001000	8	2.700	0100011	35	3.375	0111110	62	4.050	1011001	89	4.725
0001001	9	2.725	0100100	36	3.400	0111111	63	4.075	1011010	90	4.750
0001010	10	2.750	**0100101**	**37**	**3.425**	1000000	64	4.100	1011011	91	4.775
0001011	11	2.775	0100110	38	3.450	**1000001**	**65**	**4.125**	1011100	92	4.800
0001100	12	2.800	0100111	39	3.475	1000010	66	4.150	1011101	93	4.825
0001101	13	2.825	0101000	40	3.500	1000011	67	4.175	1011110	94	4.850
0001110	14	2.850	0101001	41	3.525	1000100	68	4.200	1011111	95	4.875
0001111	15	2.875	0101010	42	3.550	1000101	69	4.225	1100000	96	4.900
0010000	16	2.900	0101011	43	3.575	1000110	70	4.250	1100001	97	4.925
0010001	17	2.925	0101100	44	3.600	1000111	71	4.275	1100010	98	4.950
0010010	18	2.950	0101101	45	3.625	1001000	72	4.300	1100011	99	4.975
0010011	19	2.975	0101110	46	3.650	1001001	73	4.325	1100100	100	5.000
0010100	20	3.000	0101111	47	3.675	1001010	74	4.350	1100101	101	Not
0010101	21	3.025	0110000	48	3.700	1001011	75	4.375		|	Permitted
0010110	22	3.050	0110001	49	3.725	1001100	76	4.400	1111111	127	
0010111	23	3.075	0110010	50	3.750	1001101	77	4.425			
0011000	24	3.100	0110011	51	3.775	1001110	78	4.450			
0011001	25	3.125	0110100	52	3.800	**1001111**	**79**	**4.475**			
0011010	26	3.150	0110101	53	3.825	1010000	80	4.500			

-Set VCOML Voltage

VML[6:0]		VCOML	VML[6:0]		VCOML	VML[6:0]		VCOML	VML[6:0]		VCOML
0000000	0	-2.500	0011011	27	-1.825	0110110	54	-1.150	1010001	81	-0.475
0000001	1	-2.475	0011100	28	-1.800	0110111	55	-1.125	1010010	82	-0.450
0000010	2	-2.450	0011101	29	-1.775	0111000	56	-1.100	1010011	83	-0.425
0000011	3	-2.425	0011110	30	-1.750	0111001	57	-1.075	1010100	84	-0.400
0000100	4	-2.400	0011111	31	-1.725	0111010	58	-1.050	1010101	85	-0.375
0000101	5	-2.375	0100000	32	-1.700	0111011	59	-1.025	1010110	86	-0.350
0000110	6	-2.350	0100001	33	-1.675	0111100	60	-1.000	1010111	87	-0.325
0000111	7	-2.325	0100010	34	-1.650	0111101	61	-0.975	1011000	88	-0.300
0001000	8	-2.300	0100011	35	-1.625	0111110	62	-0.950	1011001	89	-0.275
0001001	9	-2.275	0100100	36	-1.600	0111111	63	-0.925	1011010	90	-0.250
0001010	10	-2.250	0100101	37	-1.575	1000000	64	-0.900	1011011	91	-0.225
0001011	11	-2.225	0100110	38	-1.550	1000001	65	-0.875	1011100	92	-0.200
0001100	12	-2.200	0100111	39	-1.525	1000010	66	-0.850	1011101	93	-0.175
0001101	13	-2.175	0101000	40	-1.500	1000011	67	-0.825	1011110	94	-0.150

0001110	14	-2.150	0101001	41	-1.475	1000100	68	-0.800	1011111	95	-0.125
0001111	15	-2.125	**0101010**	**42**	**-1.450**	1000101	69	-0.775	1100000	96	-0.100
0010000	16	-2.100	0101011	43	-1.425	1000110	70	-0.750	1100001	97	-0.075
0010001	17	-2.075	0101100	44	-1.400	1000111	71	-0.725	1100010	98	-0.050
0010010	18	-2.050	**0101101**	**45**	**-1.375**	1001000	72	-0.700	1100011	99	-0.025
0010011	19	-2.025	0101110	46	-1.350	1001001	73	-0.675	1100100	100	0.000
0010100	20	-2.000	0101111	47	-1.325	1001010	74	-0.650	1100101	101	Not Permitted
0010101	21	-1.975	0110000	48	-1.300	1001011	75	-0.625		|	
0010110	22	-1.950	0110001	49	-1.275	1001100	76	-0.600	1111111	127	
0010111	23	-1.925	0110010	50	-1.250	**1001101**	**77**	**-0.575**			
0011000	24	-1.900	0110011	51	-1.225	1001110	78	-0.550			
0011001	25	-1.875	0110100	52	-1.200	1001111	79	-0.525			
0011010	26	-1.850	0110101	53	-1.175	1010000	80	-0.500			

Restriction

-If this register not using the register need be reserved.
-The VCOM amplitude: **VCOMH-VCOML<=5.5V**
-The deviation value of VCOMH/VCOML between with Measurement and Specification: **Max<=25mV**
-The deviation value of VCOMAC between with Measurement and Specification: **Max <=50mV**

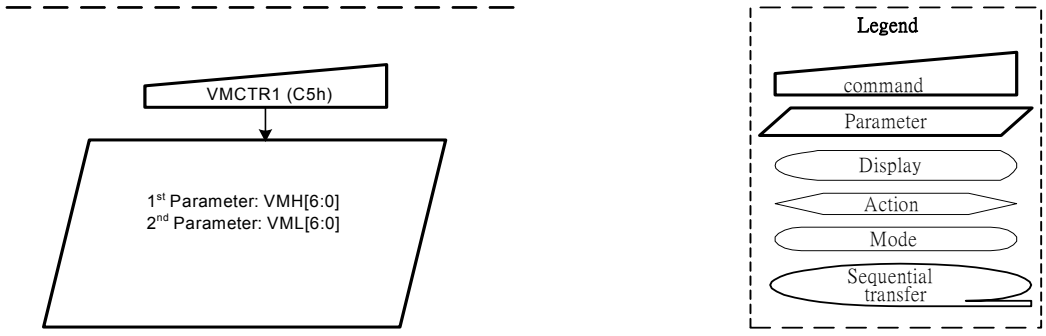
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	nVM	LCM = "00" TR LC Type	LCM = "01" TM LC type	LCM = "10" Low Voltage LC type	LCM = "11" MVA LC
		VMH[6:0] / VML[6:0]	VMH[6:0] / VML[6:0]	VMH[6:0] / VML[6:0]	VMH[6:0] / VML[6:0]
Power On Sequence	0d	37d / 45d	79d / 77d	TBD	65d / 42d
S/W Reset	0d	37d / 45d	79d / 77d	TBD	65d / 42d
H/W Reset	0d	37d / 45d	79d / 77d	TBD	65d / 42d

Flow Chart



9.2.16 VMCTR2 (C6h): VCOM Control 2

C6H	VMCTR2 (VCOM Control 2)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR2	0	↑	1	-	1	1	0	0	0	1	1	0	(C6h)
1stParameter	1	↑	1		0	0	VMA5	VMA4	VMA3	VMA2	VMA1	VMA0	13h/06h

NOTE: "-" Don't care

Description	-Set VCOMAC Voltage In this case, these registers don't be used.
Restriction	-
Register Availability	-
Default	-
Flow Chart	-

9.2.17 VMOFCTR (C7h): VCOM Offset Control

C7H	VMOFCTR (VCOM Offset Control)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR2	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)
1stParameter	1	↑	1		nVM*	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	40h

NOTE: "-" Don't care

Description

-Set VCOMH Voltage

VMF[6:0]	VCOMH Output Level	VCOML Output Level
0	"VMH"	"VML"
1	"VMH" – 63d	"VML" –63d
2	"VMH" – 62d	"VML" –62d
:	:	:
62	"VMH" –2d	"VML" –2d
63	"VMH" –1d	"VML" –1d
64	**"VMH"**	**"VML"**
65	"VMH" + 1d	"VML"+ 1d
66	"VMH" + 2d	"VML"+ 2d
:	:	:
126	"VMH"+ 62d	"VML" + 62d
127	"VMH"+ 63d	"VML" + 63d

-IF "VMH" + xd or "VML" + xd is less than 0d, it becomes 0d.
-IF "VMH" + xd or "VML" + xd is large than 100d, it becomes 100d.
-VMF[5:0] are stored in NV memory to contrast.
-
-Select the VMF[6:0] value

nVM	VMF[6:0] value
0	**VCOM offset value from NV memory**
1	VCOM offset value in the VMF[6:0] registers

-When the VCOM circuit use VCOMH (C5h) + VCOML (C5h) + VCOM-offset (C7h) structure, the nVM need to be used in this case.

Restriction

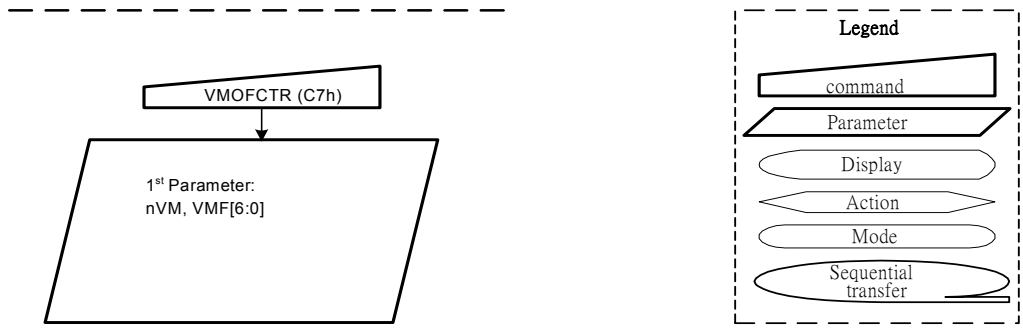
-If this register not use the register need be reserved.
-To control the VCOM output voltage with VMF[5:0] command, nVM parameter should be set '1'.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value VMF[6:0]
Power On Sequence	40h
S/W Reset	40h
H/W Reset	40h

Flow Chart	

9.2.18 RDVMOF (C8h): Read the VCOM Offset Value NV memory

C8H	RDVMOF (Read the VCOM Offset Value NV memory)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDVMOF	0	↑	1	-	1	1	0	0	1	0	0	0	(C8h)
1st Parameter	0	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	nVM	RVMF6	RVMF5	RVMF4	RVMF3	RVMF2	RVMF1	RVMF0	-

NOTE: "-" Don't care

Description

-Read the VCOM offset value from NV memory
-The 1st parameter is dummy data.
-The 2nd parameter is VMF[6:0] value from NV memory or register value.

Restriction

-If this register not use the register need be reserved.

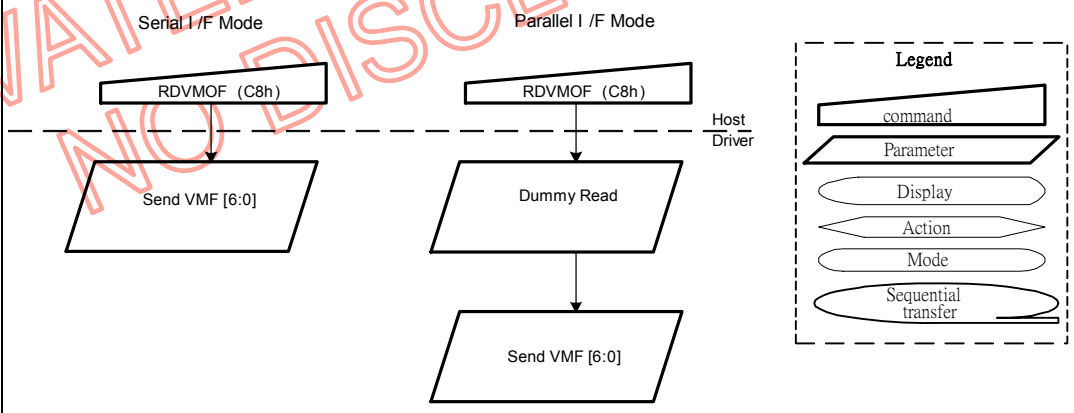
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value VMF[5:0]
Power On Sequence	40h
S/W Reset	No change
H/W Reset	40h

Flow Chart



9.2.19 WRID2 (D1h): Write ID2 Value

D0H	WRID2 (Write ID2 Value)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRID2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)
1st Parameter	1	↑	1	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: "-" Don't care

Description

-Write 7-bits data of LCD module version to save it to NV memory.
-The 1st parameter ID2[6:0] is LCD Module version ID.

Restriction

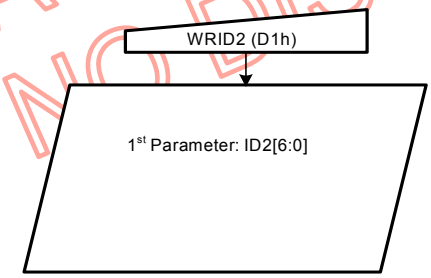
Register Availability

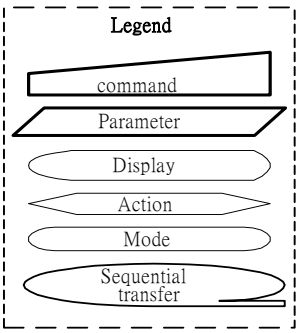
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MTP value
S/W Reset	MTP value
H/W Reset	MTP value

Flow Chart





9.2.20 WRID3 (D2h): Write ID3 Value

D2H	WRID3 (Write ID3 Value)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRID3	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)
1st Parameter	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-" Don't care

Description

-Write 8-bits data of project code module to save it to NV memory.
-The 1st parameter ID3[7:0] is product project ID.
- The default value needs to be defined later.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MTP value
S/W Reset	MTP value
H/W Reset	MTP value

Flow Chart

9.2.21 RDID4 (D3h): Read the ID4 value

D4H	RDID4 (Read the ID4 value)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID4	0	↑	1	-	1	1	0	1	0	0	1	1	(D3h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410	01h
3rd Parameter	1	1	↑	-	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420	03h
4th Parameter	1	1	↑	-	-	-	-	-	ID433	ID432	ID431	ID430	-
5th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-

NOTE: "-" Don't care

Description

-Read the Driver IC information from mask value.
-Ignored the EXTC pin.
-The 1st parameter is dummy data.
-The 2nd parameter ID41[7:0] is Driver IC ID code. (Default value= 01h)
-The value be defined later.
-Currently, "01h", "02h" , "03h" , "05h" can't be used.
-The 3rd parameter ID42[7:0] is Driver IC Part number ID. (The code be define by Driver IC Vender, and default value= 03h)
-The 4th parameter ID43[7:0] is Driver IC version ID.
-When the Driver maker modifies any function it should be modify the parameters at this ID code before sample out also.
-If Driver Maker don't need 2 parameter If can't reduce to one parameter.
-If the parameters are not enough Driver makers can add or reduce yourself.

Restriction

-

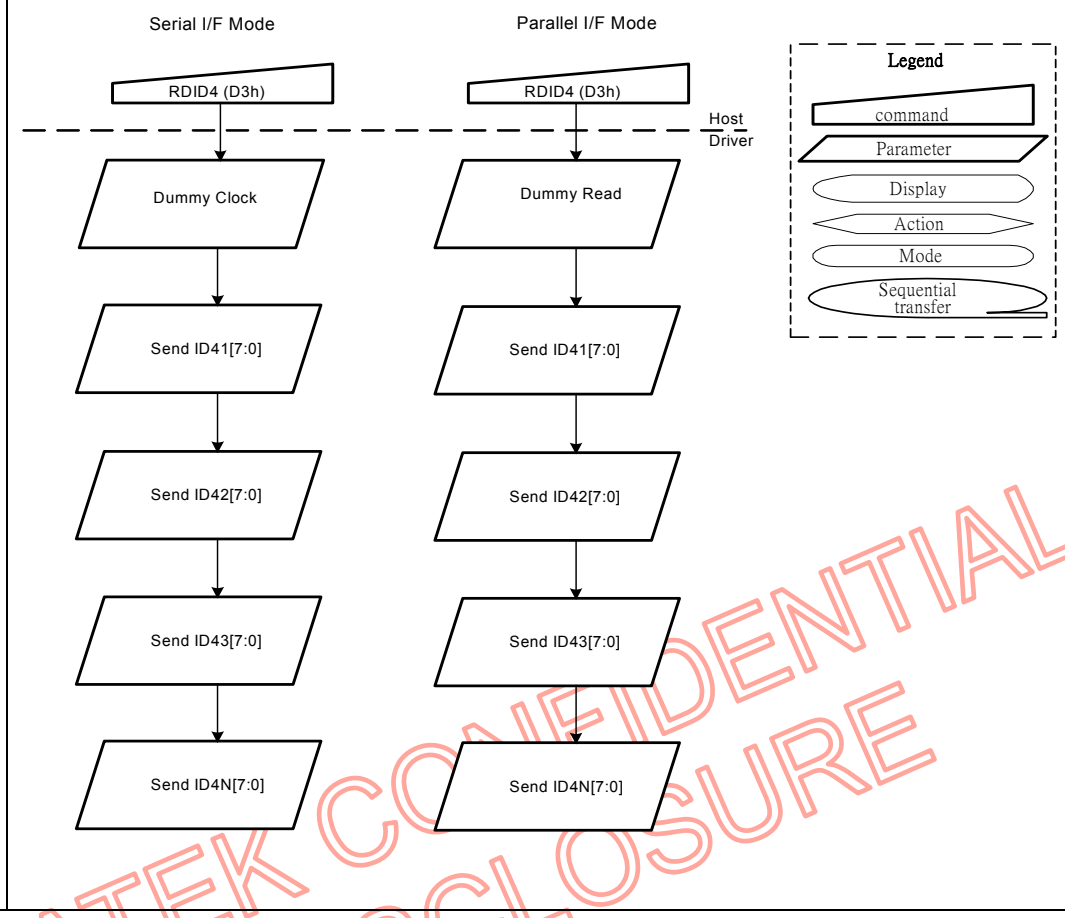
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID41[7:0]	ID42[7:0]	ID43[7:0]
Power On Sequence	01h	03h	TBD
S/W Reset	01h	03h	TBD
H/W Reset	01h	03h	TBD

Flow Chart



9.2.22 NVFCTR1 (D9h): NV Memory Function Controller 1

D9H	NVFCTR3 (NV Memory Function Controller 3)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR3	0	↑	1	-	1	1	0	1	1	0	0	1	(D9h)
1st parameter	1	↑	1	-	MTP_Cnt[3:0]				-	-	MTP_PON	MTPWR_EN	00h

NOTE: "-" Don't care

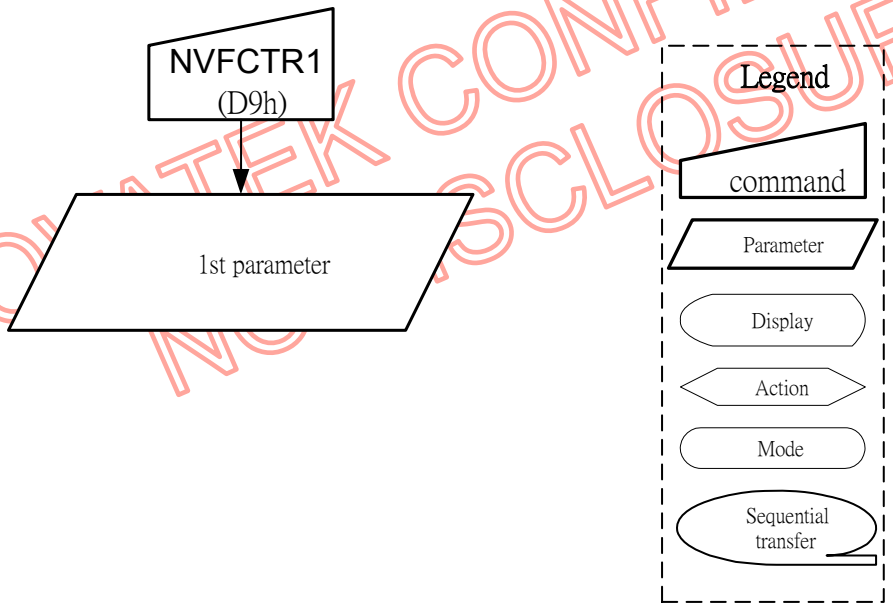
Description	MTP Function command.
Restriction	-
Register Available	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00
S/W Reset	00
H/W Reset	00

Flow Chart



9.2.23 NVFCTR2 (DEh): NV Memory Function Controller 2

DEH	NVFCTR2 (NV Memory Function Controller 2)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR2	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)
1st parameter	1	↑	1	-	0	1	0	1	0	1	0	1	55h
2nd parameter	1	↑	1	-	1	0	1	0	1	0	1	0	AAh
3rd parameter	1	↑	1	-	0	1	1	0	0	1	1	0	66h

NOTE: "-" Don't care

Description

MTP write EPWRITE command.
Please see ***9.2.25 MTP Access sequence for program (Data write)*** for more detail.

Restriction

-

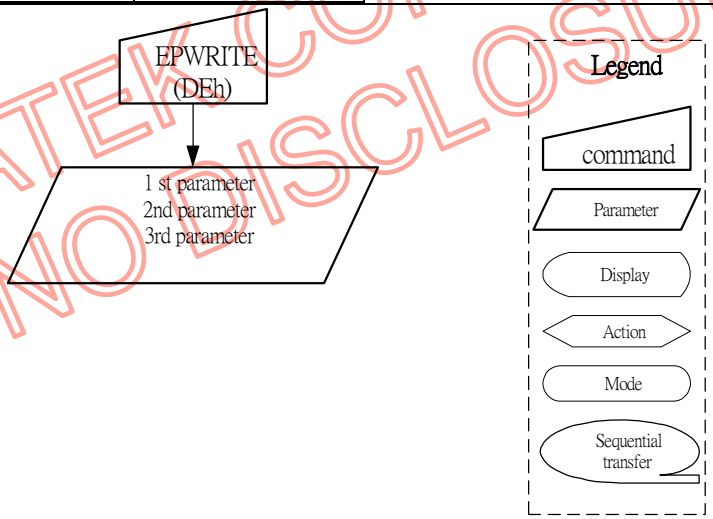
Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

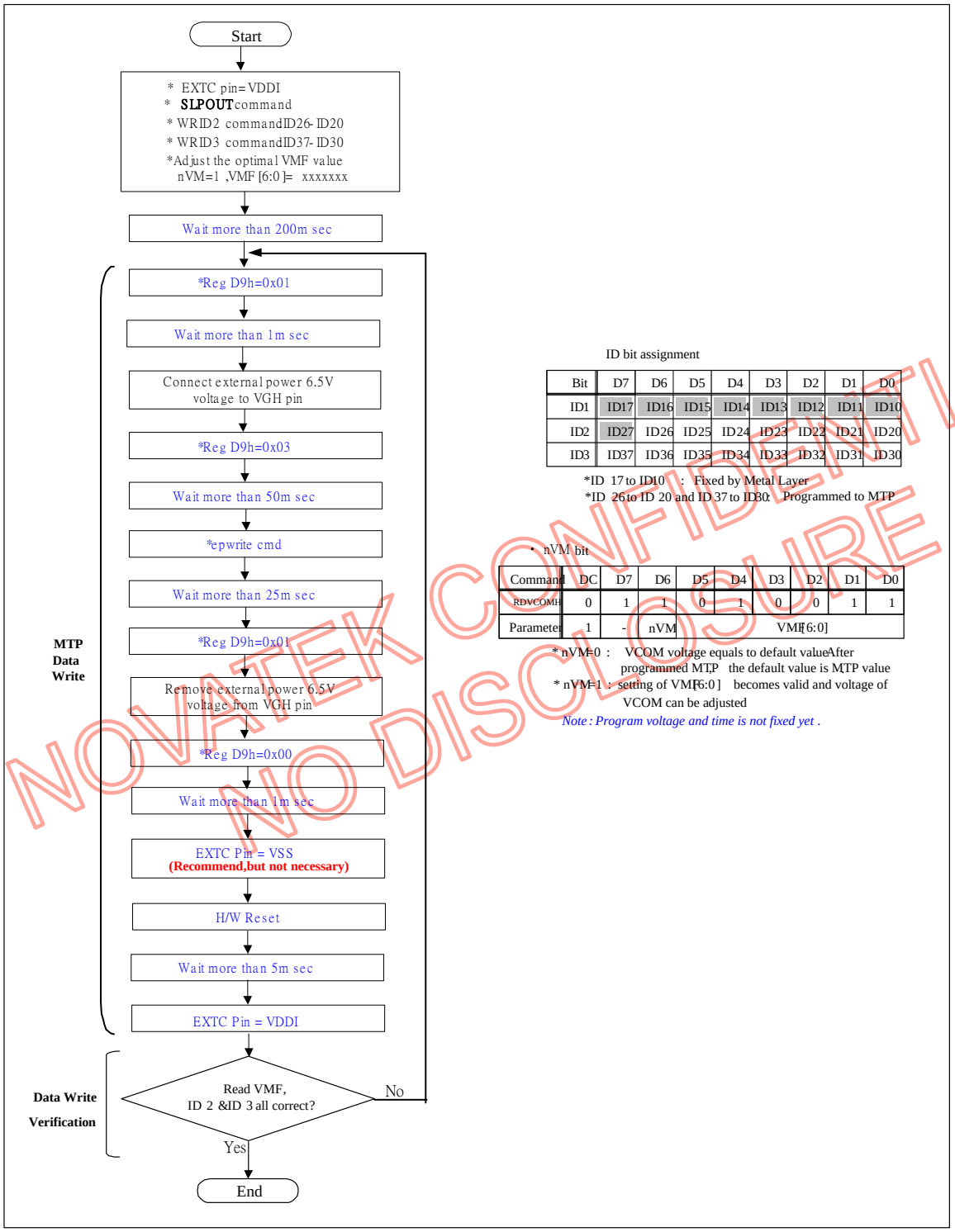
Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



9.2.24 MTP Access Sequence



ID bit assignment

Bit	D7	D6	D5	D4	D3	D2	D1	D0
ID1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
ID2	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
ID3	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

*ID 17 to ID10 : Fixed by Metal Layer
*ID 26 to ID 20 and ID 37 to ID30 : Programmed to MTP

• nVM bit

Command	DC	D7	D6	D5	D4	D3	D2	D1	D0
RDVCOMH	0	1	1	0	1	0	0	1	1
Parameter	1	-	nVM	VMF[6:0]					

* nVM=0 : VCOM voltage equals to default value After programmed MTP the default value is MTP value
* nVM=1 : setting of VMF[6:0] becomes valid and voltage of VCOM can be adjusted

Note : Program voltage and time is not fixed yet .

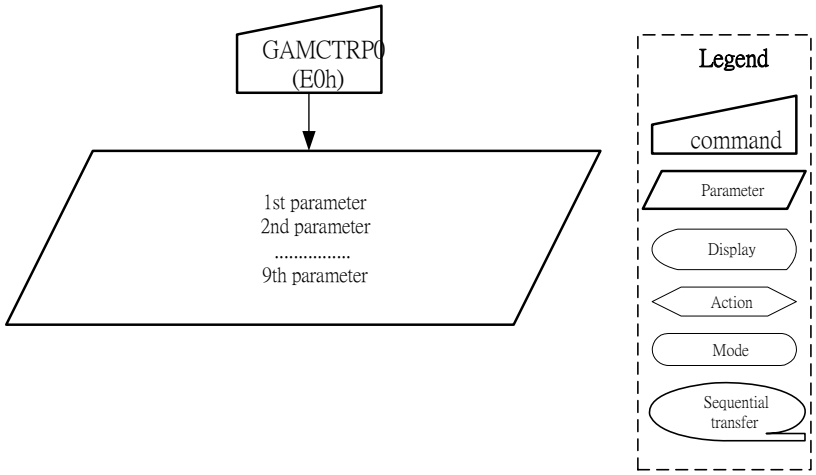
9.2.25 GMCTRP0 (E0h): Gamma (‘+’polarity) Correction Characteristics Setting

Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMCTRP0	0	↑	1	1	1	1	0	0	0	0	0	(E0h)
1st parameter	1	↑	1	-	-	VP0[5:0]						-
2nd parameter	1	↑	1	-	-	VP1[5:0]						-
3rd parameter	1	↑	1	-	-	VP2[5:0]						-
4th parameter	1	↑	1	-	-	VP4[5:0]						-
5th parameter	1	↑	1	-	-	VP6[5:0]						-
6th parameter	1	↑	1	-	-	VP13[5:0]						-
7th parameter	1	↑	1	-	-	VP20[5:0]						-
8th parameter	1	↑	1	VP36[3:0]				VP27[3:0]				-
9th parameter	1	↑	1	-	-	VP43[5:0]						-
10th parameter	1	↑	1	-	-	VP50[5:0]						-
11th parameter	1	↑	1	-	-	VP57[5:0]						-
12th parameter	1	↑	1	-	-	VP59[5:0]						-
13th parameter	1	↑	1	-	-	VP61[5:0]						-
14th parameter	1	↑	1	-	-	VP62[5:0]						-
15th parameter	1	↑	1	-	-	VP63[5:0]						-

NOTE: “-“ Don’t care

Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. It apply to gamma curve selection for only activate when EXTC=1 and GAM_R_SEL=1.
Restriction	-
Register Available	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value (1st ~9rd Parameter): Power On Sequence: All “00” S/W Reset: All “00” H/W Reset: All “00”

Flow Chart



9.2.26 GMCTRN0 (E1h): Gamma ('-'polarity) Correction Characteristics Setting

Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMCTRN0	0	↑	1	1	1	1	0	0	0	0	1	(E1h)
1st parameter	1	↑	1	-	-	VN0[5:0]						-
2nd parameter	1	↑	1	-	-	VN1[5:0]						-
3rd parameter	1	↑	1	-	-	VN2[5:0]						-
4th parameter	1	↑	1	-	-	VN4[5:0]						-
5th parameter	1	↑	1	-	-	VN6[5:0]						-
6th parameter	1	↑	1	-	-	VN13[5:0]						-
7th parameter	1	↑	1	-	-	VN20[5:0]						-
8th parameter	1	↑	1	VN36[3:0]				VN27[3:0]				-
9th parameter	1	↑	1	-	-	VN43[5:0]						-
10th parameter	1	↑	1	-	-	VN50[5:0]						-
11th parameter	1	↑	1	-	-	VN57[5:0]						-
12th parameter	1	↑	1	-	-	VN59[5:0]						-
13th parameter	1	↑	1	-	-	VN61[5:0]						-
14th parameter	1	↑	1	-	-	VN62[5:0]						-
15th parameter	1	↑	1	-	-	VN63[5:0]						-

NOTE: "-" Don't care

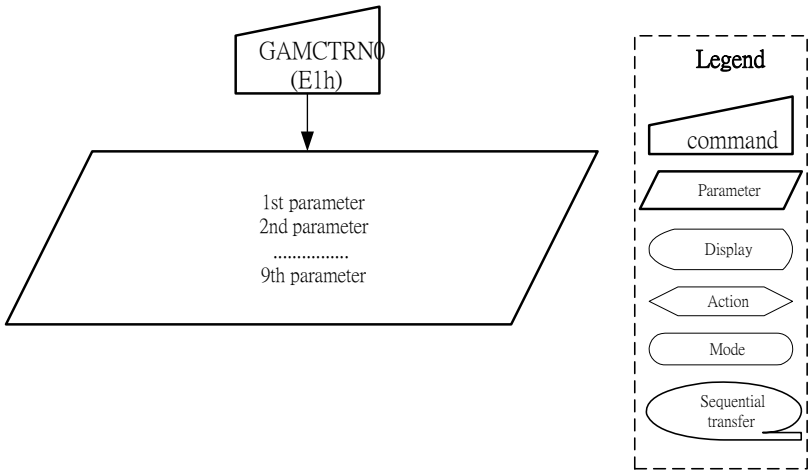
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. It apply to gamma curve selection for only activate when EXTC=1 and GAM_R_SEL=1.
Restriction	-
Register Available	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	1st ~9rd Parameter
Power On Sequence	All "00"
S/W Reset	All "00"
H/W Reset	All "00"

Flow Chart



9.2.28 GAM_R_SEL (F2h):

Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TRIMCTR	0	↑	1	1	1	1	1	0	0	1	0	(F2h)
1st Parameter	1	↑	1	-	-	-	-	-	-	-	GAM_R_SEL	Write

NOTE: "-" Don't care

Description	**GAM_R_SEL:** Gamma adjustment E0h and E1h enable control 0: Disable. (Default) 1: Enable.
Restriction	-
Register Available	

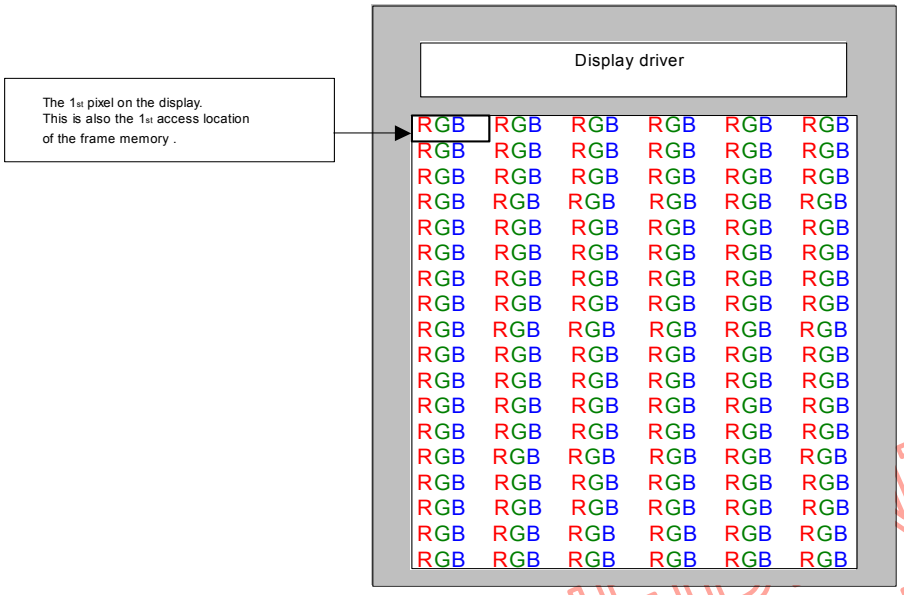
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0h
S/W Reset	0h
H/W Reset	0h

10. Display Module Default Position

The default position of the display is always as follow, when MADCTR's (36h) parameter is 00h.



11. Power structure

11.1. Driver IC Operating voltages Specification

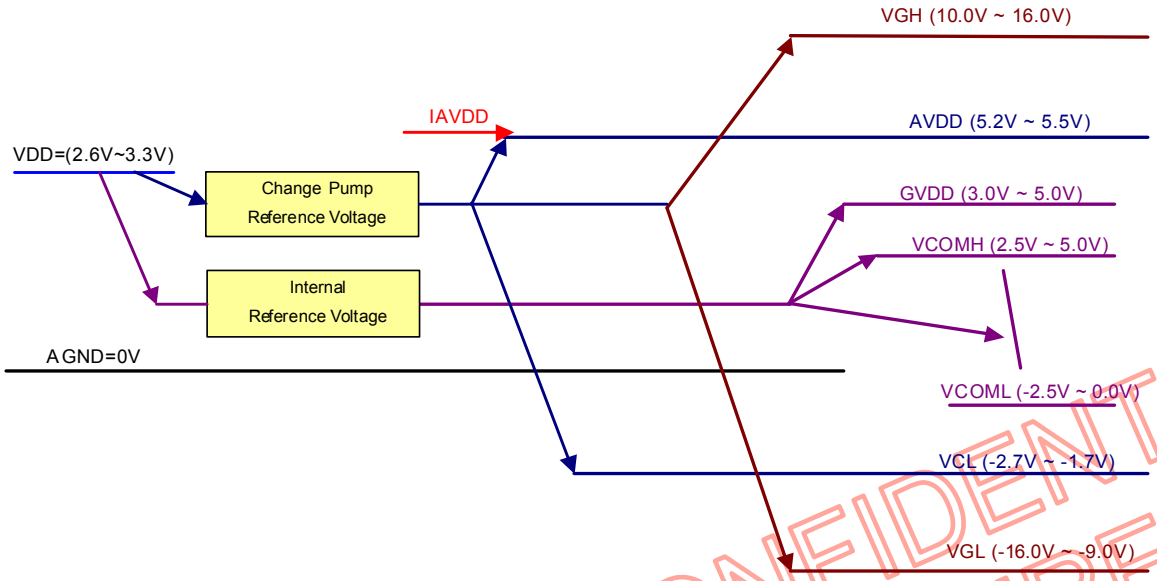


Fig. 11.1.1 Power Booster Level

Remark

1. AVDD supply to all power source (exclude VGH, VGL)
2. Source output range: 0.1V ~ AVDD-0.1V
3. Linear Range: 0.2V ~ AVDD-0.2V
   (For all output voltage, but exclude VGH, VGL)
4. Above operating voltages.

11.2 Power Booster Circuit

11.2.1 VCI1 generate from VDD regulator

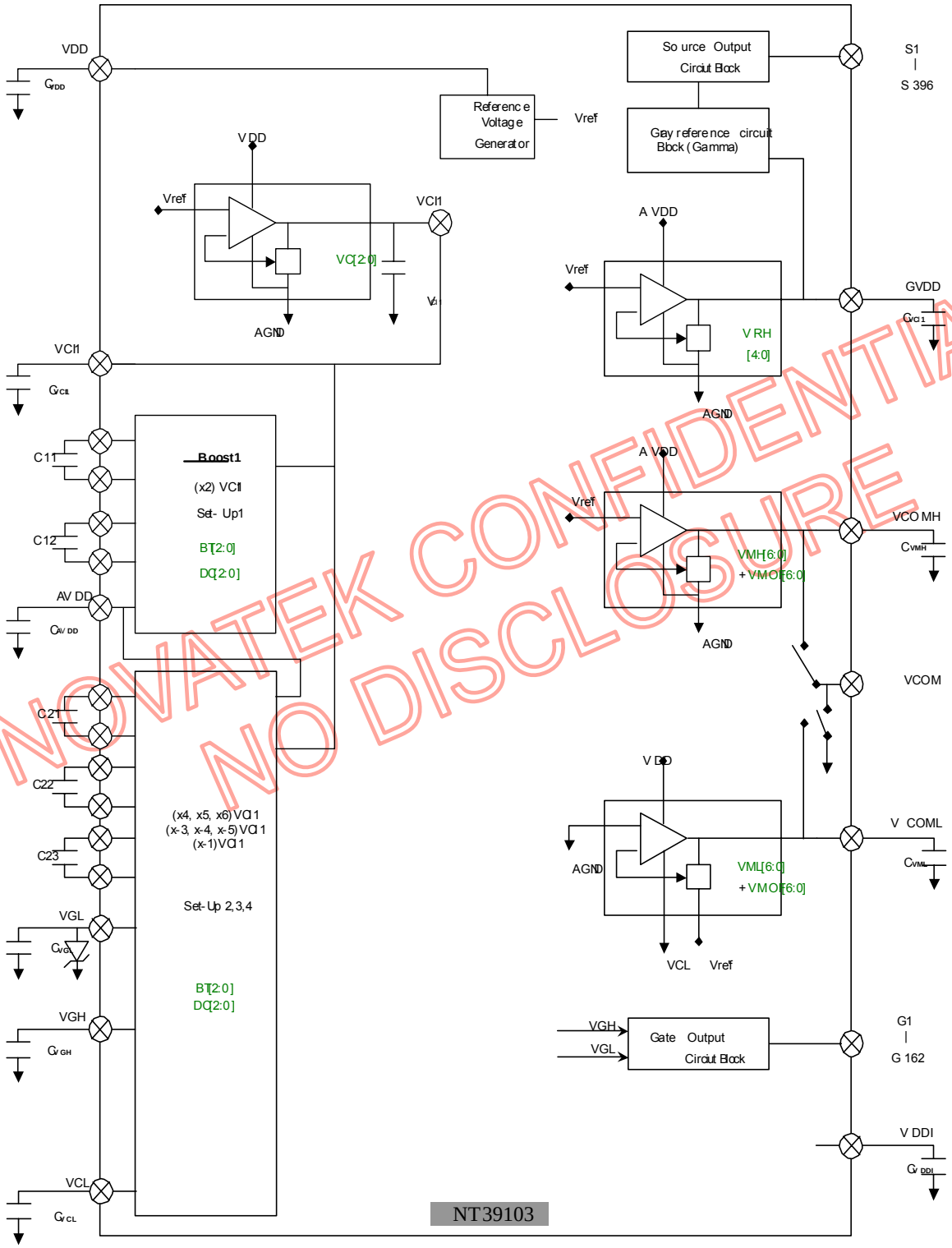


Fig. 11.2.1 Power Booster Structure (1)

11.2.2 VCI1 = VDD

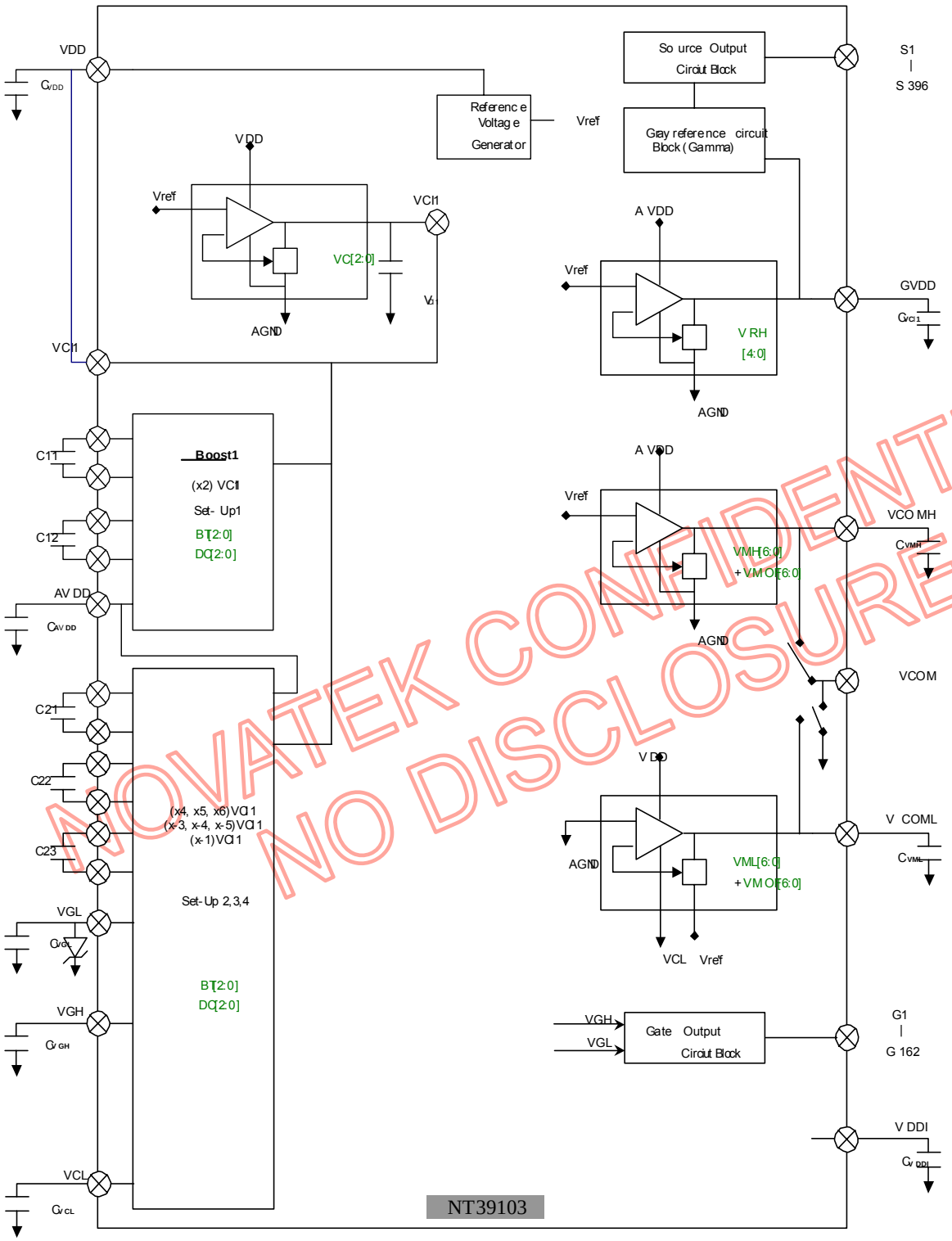


Fig. 11.2.2 Power Booster Structure (2) VCI1 = VDD

Note: In this case, external power VDD ≤ VCI1 setting value.

11.2.3 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Rated (Min)Voltage	Typical capacitance value
VDDI	VDDI (Logic Power)		
VDD	VDD (Analog Power)		
AGND	Analog ground (Connect to GND)		
DGND	Digital ground (Connect to GND)		
VCC	Connect to Capacitor (Max 2V): VCC -------||-------- GND	5.0V	1.0 uF
VCI1	Connect to Capacitor (Max 2.75V): VCI1 -------||----- GND	5.0V	1.0 uF
C23P, C23N	Connect to Capacitor: C23P -------||--------C23N	6.0V	1.0 uF
C22P, C22N	Connect to Capacitor: C22P -------||--------C22N	6.0V	1.0 uF
C21P, C22N	Connect to Capacitor: C21P -------||--------C21N	6.0V	1.0 uF
C12P, C12N	Connect to Capacitor: C12P -------||--------C12N	6.0V	1.0 uF
C11P, C11N	Connect to Capacitor: C11P -------||--------C11N	6.0V	1.0 uF
AVDD	Connect to Capacitor: AVDD -------||-------- GND	6.0V	2.2 uF
VGH	Connect to Capacitor: VGH -------||-------- GND	18.0V	0.1 uF
VGL	Connect to Capacitor: VGL -------||-------- GND	16.0V	0.1 uF
VCL	Connect to Capacitor: VCL -------||-------- GND	5.0V	1.0 uF
VREF	Connect to Capacitor: VREF -------||-------- GND	6.0V	1.0 uF
GVDD	Connect to Capacitor: GVDD -------||-------- GND	6.0V	1.0 uF
VCOMH	Connect to Capacitor: VCOMH-------||--------- GND	6.0V	1.0 uF
VCOML	Connect to Capacitor: VCOML -------||-------- GND	5.0V	1.0 uF
VGL	Connect to Schottky diode: VGL -------►|-------- GND	30V	Schottky diode VF<=0.4V at 20mA VR>=30V

12. Gamma structure

12.1 Gamma Correction Curve Circuit

12.1.1 Relationship between RAM Data and Output for TR-type default setting.

(Please refer to 9.2.27 ~9.2.28 for more detail)

Data (Hex)	Output Voltage (LCM=00, TR-type)									
	VCOM = Low					VCOM = High				
	Gamma	1	1.8	2.2	2.5	Gamma	1	1.8	2.2	2.5
0	V0+	3.490	3.490	3.490	3.490	V0-	0.260	0.260	0.260	0.260
1	V1+	2.625	3.346	3.433	3.462	V1-	1.125	0.404	0.317	0.288
2	V2+	2.394	3.173	3.346	3.433	V2-	1.327	0.577	0.404	0.317
3	V3+	2.280	3.020	3.235	3.353	V3-	1.455	0.730	0.515	0.397
4	V4+	2.173	2.876	3.130	3.278	V4-	1.574	0.874	0.620	0.472
5	V5+	2.097	2.764	3.032	3.184	V5-	1.653	0.986	0.718	0.566
6	V6+	2.026	2.660	2.941	3.098	V6-	1.726	1.090	0.809	0.652
7	V7+	1.978	2.585	2.857	3.013	V7-	1.777	1.165	0.893	0.737
8	V8+	1.929	2.509	2.772	2.928	V8-	1.827	1.241	0.978	0.822
9	V9+	1.885	2.440	2.695	2.850	V9-	1.872	1.310	1.055	0.900
0A	V10+	1.840	2.371	2.618	2.773	V10-	1.918	1.379	1.132	0.977
0B	V11+	1.800	2.308	2.547	2.702	V11-	1.960	1.442	1.203	1.048
0C	V12+	1.764	2.251	2.484	2.639	V12-	1.998	1.499	1.266	1.111
0D	V13+	1.731	2.201	2.428	2.582	V13-	2.031	1.549	1.322	1.168
0E	V14+	1.698	2.151	2.369	2.522	V14-	2.063	1.599	1.381	1.228
0F	V15+	1.664	2.102	2.311	2.462	V15-	2.094	1.648	1.439	1.288
10	V16+	1.635	2.059	2.261	2.410	V16-	2.121	1.691	1.489	1.340
11	V17+	1.606	2.017	2.211	2.359	V17-	2.149	1.733	1.539	1.391
12	V18+	1.577	1.975	2.161	2.307	V18-	2.176	1.775	1.589	1.443
13	V19+	1.553	1.939	2.119	2.264	V19-	2.199	1.811	1.631	1.486
14	V20+	1.529	1.904	2.077	2.221	V20-	2.221	1.846	1.673	1.529
15	V21+	1.505	1.873	2.042	2.179	V21-	2.243	1.877	1.708	1.571
16	V22+	1.482	1.843	2.007	2.136	V22-	2.265	1.907	1.743	1.614
17	V23+	1.458	1.812	1.972	2.094	V23-	2.287	1.938	1.778	1.656
18	V24+	1.435	1.781	1.937	2.052	V24-	2.309	1.969	1.813	1.698
19	V25+	1.411	1.751	1.902	2.009	V25-	2.330	1.999	1.848	1.741
1A	V26+	1.392	1.726	1.874	1.975	V26-	2.348	2.024	1.876	1.775
1B	V27+	1.374	1.702	1.846	1.942	V27-	2.365	2.048	1.904	1.808
1C	V28+	1.355	1.676	1.817	1.908	V28-	2.384	2.074	1.933	1.842
1D	V29+	1.337	1.650	1.787	1.875	V29-	2.402	2.100	1.963	1.875
1E	V30+	1.318	1.624	1.757	1.842	V30-	2.421	2.126	1.993	1.908
1F	V31+	1.300	1.598	1.728	1.808	V31-	2.439	2.152	2.022	1.942
20	V32+	1.281	1.572	1.698	1.775	V32-	2.458	2.178	2.052	1.975
21	V33+	1.263	1.547	1.669	1.742	V33-	2.476	2.203	2.081	2.008
22	V34+	1.244	1.521	1.639	1.709	V34-	2.495	2.229	2.111	2.041
23	V35+	1.226	1.495	1.609	1.675	V35-	2.513	2.255	2.141	2.075
24	V36+	1.207	1.469	1.580	1.642	V36-	2.532	2.281	2.170	2.108
25	V37+	1.191	1.445	1.552	1.613	V37-	2.549	2.305	2.198	2.137
26	V38+	1.175	1.420	1.524	1.585	V38-	2.567	2.330	2.226	2.165
27	V39+	1.160	1.396	1.496	1.556	V39-	2.584	2.354	2.254	2.194
28	V40+	1.144	1.371	1.468	1.528	V40-	2.602	2.379	2.282	2.222
29	V41+	1.128	1.347	1.440	1.499	V41-	2.619	2.403	2.310	2.251
2A	V42+	1.112	1.322	1.413	1.471	V42-	2.636	2.428	2.337	2.279
2B	V43+	1.096	1.298	1.385	1.442	V43-	2.654	2.452	2.365	2.308
2C	V44+	1.075	1.272	1.356	1.411	V44-	2.675	2.478	2.394	2.339
2D	V45+	1.054	1.247	1.328	1.379	V45-	2.696	2.503	2.422	2.371
2E	V46+	1.033	1.221	1.300	1.348	V46-	2.717	2.529	2.450	2.402
2F	V47+	1.012	1.195	1.272	1.316	V47-	2.738	2.555	2.478	2.434
30	V48+	0.991	1.169	1.243	1.284	V48-	2.759	2.581	2.507	2.466
31	V49+	0.970	1.143	1.215	1.253	V49-	2.780	2.607	2.535	2.497
32	V50+	0.949	1.118	1.187	1.221	V50-	2.801	2.632	2.563	2.529
33	V51+	0.928	1.090	1.155	1.190	V51-	2.822	2.660	2.595	2.560
34	V52+	0.907	1.063	1.123	1.159	V52-	2.843	2.687	2.627	2.591
35	V53+	0.886	1.035	1.092	1.127	V53-	2.864	2.715	2.658	2.623
36	V54+	0.860	1.001	1.052	1.088	V54-	2.890	2.749	2.698	2.662
37	V55+	0.834	0.967	1.012	1.049	V55-	2.916	2.783	2.738	2.701
38	V56+	0.808	0.933	0.973	1.010	V56-	2.942	2.817	2.777	2.740
39	V57+	0.782	0.899	0.933	0.971	V57-	2.968	2.851	2.817	2.779
3A	V58+	0.750	0.857	0.894	0.923	V58-	2.995	2.893	2.856	2.820
3B	V59+	0.713	0.808	0.848	0.868	V59-	3.027	2.942	2.902	2.867
3C	V60+	0.676	0.754	0.788	0.812	V60-	3.069	2.996	2.962	2.930
3D	V61+	0.635	0.692	0.721	0.750	V61-	3.115	3.058	3.029	3.000
3E	V62+	0.577	0.635	0.635	0.663	V62-	3.173	3.115	3.115	3.087
3F	V63+	0.519	0.519	0.519	0.519	V63-	3.231	3.231	3.231	3.231

12.1.2 Relationship between RAM Data and Output for TM-type default setting.

(Please refer to 9.2.27 ~9.2.28 for more detail)

Data	Output Voltage (LCM=01, TM-type)									
(Hex)	VCOM = Low					VCOM = High				
	Gamma	1	1.8	2.2	2.5	Gamma	1	1.8	2.2	2.5
0	V0+	4.550	4.550	4.515	4.550	V0-	0.210	0.210	0.280	0.245
1	V1+	3.325	4.375	4.480	4.550	V1-	1.435	0.420	0.350	0.280
2	V2+	3.150	4.025	4.305	4.480	V2-	1.645	0.770	0.490	0.350
3	V3+	3.015	3.856	4.156	4.362	V3-	1.774	0.935	0.639	0.468
4	V4+	2.889	3.697	4.017	4.251	V4-	1.895	1.089	0.778	0.579
5	V5+	2.812	3.543	3.851	4.132	V5-	1.969	1.255	0.944	0.698
6	V6+	2.740	3.399	3.697	4.021	V6-	2.038	1.409	1.098	0.809
7	V7+	2.695	3.321	3.602	3.908	V7-	2.085	1.485	1.193	0.922
8	V8+	2.649	3.243	3.507	3.795	V8-	2.132	1.562	1.288	1.035
9	V9+	2.607	3.171	3.420	3.691	V9-	2.175	1.632	1.375	1.139
0A	V10+	2.564	3.099	3.333	3.588	V10-	2.218	1.702	1.462	1.242
0B	V11+	2.526	3.034	3.254	3.493	V11-	2.258	1.765	1.541	1.337
0C	V12+	2.492	2.975	3.183	3.409	V12-	2.293	1.823	1.612	1.421
0D	V13+	2.461	2.923	3.120	3.333	V13-	2.324	1.874	1.675	1.497
0E	V14+	2.430	2.873	3.067	3.268	V14-	2.351	1.917	1.728	1.562
0F	V15+	2.399	2.824	3.013	3.202	V15-	2.378	1.961	1.782	1.628
10	V16+	2.373	2.781	2.968	3.146	V16-	2.401	1.998	1.827	1.684
11	V17+	2.346	2.738	2.922	3.090	V17-	2.424	2.035	1.873	1.740
12	V18+	2.319	2.696	2.876	3.034	V18-	2.447	2.073	1.919	1.796
13	V19+	2.297	2.660	2.838	2.987	V19-	2.466	2.104	1.957	1.843
14	V20+	2.275	2.625	2.800	2.940	V20-	2.485	2.135	1.995	1.890
15	V21+	2.257	2.597	2.766	2.902	V21-	2.506	2.167	2.031	1.928
16	V22+	2.239	2.568	2.731	2.864	V22-	2.527	2.200	2.067	1.966
17	V23+	2.221	2.540	2.697	2.826	V23-	2.549	2.232	2.104	2.004
18	V24+	2.203	2.512	2.663	2.788	V24-	2.570	2.264	2.140	2.042
19	V25+	2.185	2.484	2.629	2.750	V25-	2.591	2.297	2.176	2.080
1A	V26+	2.171	2.461	2.601	2.719	V26-	2.608	2.323	2.205	2.111
1B	V27+	2.157	2.438	2.574	2.689	V27-	2.625	2.349	2.234	2.141
1C	V28+	2.139	2.416	2.547	2.659	V28-	2.642	2.372	2.260	2.171
1D	V29+	2.121	2.394	2.520	2.629	V29-	2.659	2.396	2.287	2.201
1E	V30+	2.104	2.371	2.493	2.599	V30-	2.675	2.420	2.313	2.231
1F	V31+	2.086	2.349	2.466	2.569	V31-	2.692	2.444	2.340	2.261
20	V32+	2.069	2.327	2.439	2.539	V32-	2.709	2.467	2.366	2.291
21	V33+	2.051	2.304	2.412	2.509	V33-	2.726	2.491	2.393	2.321
22	V34+	2.034	2.282	2.385	2.479	V34-	2.742	2.515	2.419	2.351
23	V35+	2.016	2.260	2.358	2.449	V35-	2.759	2.538	2.446	2.381
24	V36+	1.999	2.237	2.332	2.419	V36-	2.776	2.562	2.472	2.411
25	V37+	1.983	2.213	2.308	2.394	V37-	2.794	2.586	2.499	2.436
26	V38+	1.968	2.188	2.285	2.368	V38-	2.813	2.610	2.526	2.462
27	V39+	1.952	2.163	2.262	2.343	V39-	2.831	2.634	2.553	2.487
28	V40+	1.937	2.139	2.239	2.317	V40-	2.850	2.658	2.580	2.513
29	V41+	1.921	2.114	2.216	2.291	V41-	2.868	2.682	2.606	2.539
2A	V42+	1.906	2.090	2.193	2.266	V42-	2.887	2.706	2.633	2.564
2B	V43+	1.890	2.065	2.170	2.240	V43-	2.905	2.730	2.660	2.590
2C	V44+	1.869	2.043	2.143	2.212	V44-	2.923	2.750	2.683	2.618
2D	V45+	1.849	2.021	2.116	2.183	V45-	2.941	2.771	2.706	2.647
2E	V46+	1.828	1.999	2.090	2.155	V46-	2.959	2.791	2.729	2.675
2F	V47+	1.807	1.976	2.063	2.127	V47-	2.976	2.812	2.752	2.703
30	V48+	1.786	1.954	2.036	2.099	V48-	2.994	2.832	2.775	2.731
31	V49+	1.766	1.932	2.009	2.070	V49-	3.012	2.853	2.798	2.760
32	V50+	1.745	1.910	1.982	2.042	V50-	3.030	2.873	2.821	2.788
33	V51+	1.724	1.883	1.952	2.012	V51-	3.052	2.901	2.851	2.818
34	V52+	1.703	1.856	1.922	1.982	V52-	3.074	2.930	2.881	2.848
35	V53+	1.682	1.830	1.892	1.952	V53-	3.097	2.958	2.911	2.878
36	V54+	1.656	1.796	1.854	1.914	V54-	3.124	2.993	2.949	2.916
37	V55+	1.630	1.763	1.816	1.877	V55-	3.152	3.029	2.987	2.953
38	V56+	1.603	1.729	1.779	1.839	V56-	3.180	3.064	3.024	2.991
39	V57+	1.577	1.696	1.741	1.801	V57-	3.207	3.099	3.062	3.029
3A	V58+	1.541	1.657	1.704	1.756	V58-	3.241	3.138	3.105	3.074
3B	V59+	1.499	1.612	1.661	1.702	V59-	3.280	3.183	3.156	3.128
3C	V60+	1.436	1.562	1.604	1.642	V60-	3.334	3.233	3.219	3.188
3D	V61+	1.365	1.505	1.540	1.575	V61-	3.395	3.290	3.290	3.255
3E	V62+	1.015	1.365	1.400	1.435	V62-	3.780	3.430	3.395	3.395
3F	V63+	0.525	0.490	0.630	0.560	V63-	4.270	4.305	4.165	4.270

12.1.3 Relationship between RAM Data and Output for LV-type default setting.

(Please refer to 9.2.27 ~9.2.28 for more detail)

Data	Output Voltage (LCM=10, LV-type)									
(Hex)	VCOM = Low					VCOM = High				
	Gamma	1	1.8	2.2	2.5	Gamma	1	1.8	2.2	2.5
0	V0+	TBD	TBD	TBD	TBD	V0-	TBD	TBD	TBD	TBD
1	V1+	TBD	TBD	TBD	TBD	V1-	TBD	TBD	TBD	TBD
2	V2+	TBD	TBD	TBD	TBD	V2-	TBD	TBD	TBD	TBD
3	V3+	TBD	TBD	TBD	TBD	V3-	TBD	TBD	TBD	TBD
4	V4+	TBD	TBD	TBD	TBD	V4-	TBD	TBD	TBD	TBD
5	V5+	TBD	TBD	TBD	TBD	V5-	TBD	TBD	TBD	TBD
6	V6+	TBD	TBD	TBD	TBD	V6-	TBD	TBD	TBD	TBD
7	V7+	TBD	TBD	TBD	TBD	V7-	TBD	TBD	TBD	TBD
8	V8+	TBD	TBD	TBD	TBD	V8-	TBD	TBD	TBD	TBD
9	V9+	TBD	TBD	TBD	TBD	V9-	TBD	TBD	TBD	TBD
0A	V10+	TBD	TBD	TBD	TBD	V10-	TBD	TBD	TBD	TBD
0B	V11+	TBD	TBD	TBD	TBD	V11-	TBD	TBD	TBD	TBD
0C	V12+	TBD	TBD	TBD	TBD	V12-	TBD	TBD	TBD	TBD
0D	V13+	TBD	TBD	TBD	TBD	V13-	TBD	TBD	TBD	TBD
0E	V14+	TBD	TBD	TBD	TBD	V14-	TBD	TBD	TBD	TBD
0F	V15+	TBD	TBD	TBD	TBD	V15-	TBD	TBD	TBD	TBD
10	V16+	TBD	TBD	TBD	TBD	V16-	TBD	TBD	TBD	TBD
11	V17+	TBD	TBD	TBD	TBD	V17-	TBD	TBD	TBD	TBD
12	V18+	TBD	TBD	TBD	TBD	V18-	TBD	TBD	TBD	TBD
13	V19+	TBD	TBD	TBD	TBD	V19-	TBD	TBD	TBD	TBD
14	V20+	TBD	TBD	TBD	TBD	V20-	TBD	TBD	TBD	TBD
15	V21+	TBD	TBD	TBD	TBD	V21-	TBD	TBD	TBD	TBD
16	V22+	TBD	TBD	TBD	TBD	V22-	TBD	TBD	TBD	TBD
17	V23+	TBD	TBD	TBD	TBD	V23-	TBD	TBD	TBD	TBD
18	V24+	TBD	TBD	TBD	TBD	V24-	TBD	TBD	TBD	TBD
19	V25+	TBD	TBD	TBD	TBD	V25-	TBD	TBD	TBD	TBD
1A	V26+	TBD	TBD	TBD	TBD	V26-	TBD	TBD	TBD	TBD
1B	V27+	TBD	TBD	TBD	TBD	V27-	TBD	TBD	TBD	TBD
1C	V28+	TBD	TBD	TBD	TBD	V28-	TBD	TBD	TBD	TBD
1D	V29+	TBD	TBD	TBD	TBD	V29-	TBD	TBD	TBD	TBD
1E	V30+	TBD	TBD	TBD	TBD	V30-	TBD	TBD	TBD	TBD
1F	V31+	TBD	TBD	TBD	TBD	V31-	TBD	TBD	TBD	TBD
20	V32+	TBD	TBD	TBD	TBD	V32-	TBD	TBD	TBD	TBD
21	V33+	TBD	TBD	TBD	TBD	V33-	TBD	TBD	TBD	TBD
22	V34+	TBD	TBD	TBD	TBD	V34-	TBD	TBD	TBD	TBD
23	V35+	TBD	TBD	TBD	TBD	V35-	TBD	TBD	TBD	TBD
24	V36+	TBD	TBD	TBD	TBD	V36-	TBD	TBD	TBD	TBD
25	V37+	TBD	TBD	TBD	TBD	V37-	TBD	TBD	TBD	TBD
26	V38+	TBD	TBD	TBD	TBD	V38-	TBD	TBD	TBD	TBD
27	V39+	TBD	TBD	TBD	TBD	V39-	TBD	TBD	TBD	TBD
28	V40+	TBD	TBD	TBD	TBD	V40-	TBD	TBD	TBD	TBD
29	V41+	TBD	TBD	TBD	TBD	V41-	TBD	TBD	TBD	TBD
2A	V42+	TBD	TBD	TBD	TBD	V42-	TBD	TBD	TBD	TBD
2B	V43+	TBD	TBD	TBD	TBD	V43-	TBD	TBD	TBD	TBD
2C	V44+	TBD	TBD	TBD	TBD	V44-	TBD	TBD	TBD	TBD
2D	V45+	TBD	TBD	TBD	TBD	V45-	TBD	TBD	TBD	TBD
2E	V46+	TBD	TBD	TBD	TBD	V46-	TBD	TBD	TBD	TBD
2F	V47+	TBD	TBD	TBD	TBD	V47-	TBD	TBD	TBD	TBD
30	V48+	TBD	TBD	TBD	TBD	V48-	TBD	TBD	TBD	TBD
31	V49+	TBD	TBD	TBD	TBD	V49-	TBD	TBD	TBD	TBD
32	V50+	TBD	TBD	TBD	TBD	V50-	TBD	TBD	TBD	TBD
33	V51+	TBD	TBD	TBD	TBD	V51-	TBD	TBD	TBD	TBD
34	V52+	TBD	TBD	TBD	TBD	V52-	TBD	TBD	TBD	TBD
35	V53+	TBD	TBD	TBD	TBD	V53-	TBD	TBD	TBD	TBD
36	V54+	TBD	TBD	TBD	TBD	V54-	TBD	TBD	TBD	TBD
37	V55+	TBD	TBD	TBD	TBD	V55-	TBD	TBD	TBD	TBD
38	V56+	TBD	TBD	TBD	TBD	V56-	TBD	TBD	TBD	TBD
39	V57+	TBD	TBD	TBD	TBD	V57-	TBD	TBD	TBD	TBD
3A	V58+	TBD	TBD	TBD	TBD	V58-	TBD	TBD	TBD	TBD
3B	V59+	TBD	TBD	TBD	TBD	V59-	TBD	TBD	TBD	TBD
3C	V60+	TBD	TBD	TBD	TBD	V60-	TBD	TBD	TBD	TBD
3D	V61+	TBD	TBD	TBD	TBD	V61-	TBD	TBD	TBD	TBD
3E	V62+	TBD	TBD	TBD	TBD	V62-	TBD	TBD	TBD	TBD
3F	V63+	TBD	TBD	TBD	TBD	V63-	TBD	TBD	TBD	TBD

12.1.4 Relationship between RAM Data and Output for MVA type default setting.

(Please refer to 9.2.27 ~9.2.28 for more detail)

Data	Output Voltage (LCM=11, MVA-type)									
(Hex)	VCOM = Low					VCOM = High				
	Gamma	1	1.8	2.2	2.5	Gamma	1	1.8	2.2	2.5
0	V0+	4.500	4.500	4.500	4.500	V0-	0.312	0.312	0.312	0.312
1	V1+	4.431	4.362	4.292	4.292	V1-	0.415	0.519	0.554	0.554
2	V2+	4.327	4.188	4.119	4.050	V2-	0.519	0.658	0.762	0.796
3	V3+	4.236	4.008	3.920	3.877	V3-	0.622	0.839	0.942	0.982
4	V4+	4.150	3.838	3.733	3.715	V4-	0.718	1.008	1.112	1.157
5	V5+	4.036	3.747	3.666	3.621	V5-	0.810	1.099	1.190	1.237
6	V6+	3.929	3.663	3.604	3.534	V6-	0.895	1.184	1.262	1.312
7	V7+	3.871	3.593	3.532	3.462	V7-	0.957	1.254	1.332	1.384
8	V8+	3.813	3.523	3.460	3.390	V8-	1.018	1.324	1.402	1.456
9	V9+	3.760	3.459	3.394	3.324	V9-	1.075	1.388	1.466	1.522
0A	V10+	3.706	3.394	3.328	3.258	V10-	1.132	1.452	1.531	1.588
0B	V11+	3.658	3.336	3.268	3.198	V11-	1.183	1.510	1.589	1.648
0C	V12+	3.614	3.284	3.213	3.144	V12-	1.229	1.563	1.641	1.702
0D	V13+	3.576	3.237	3.165	3.096	V13-	1.270	1.609	1.688	1.750
0E	V14+	3.528	3.199	3.123	3.053	V14-	1.318	1.647	1.730	1.793
0F	V15+	3.480	3.162	3.080	3.010	V15-	1.366	1.684	1.772	1.836
10	V16+	3.439	3.130	3.043	2.973	V16-	1.407	1.717	1.807	1.873
11	V17+	3.398	3.097	3.006	2.937	V17-	1.448	1.749	1.843	1.909
12	V18+	3.357	3.065	2.969	2.900	V18-	1.489	1.781	1.879	1.946
13	V19+	3.323	3.038	2.938	2.869	V19-	1.523	1.808	1.909	1.977
14	V20+	3.288	3.012	2.908	2.838	V20-	1.558	1.835	1.938	2.008
15	V21+	3.260	2.980	2.873	2.804	V21-	1.586	1.867	1.973	2.042
16	V22+	3.233	2.948	2.839	2.770	V22-	1.614	1.899	2.007	2.076
17	V23+	3.205	2.916	2.805	2.736	V23-	1.642	1.931	2.041	2.111
18	V24+	3.177	2.884	2.771	2.701	V24-	1.670	1.963	2.076	2.145
19	V25+	3.149	2.852	2.736	2.667	V25-	1.698	1.995	2.110	2.179
1A	V26+	3.126	2.826	2.709	2.640	V26-	1.720	2.020	2.137	2.207
1B	V27+	3.104	2.800	2.681	2.612	V27-	1.742	2.046	2.165	2.234
1C	V28+	3.080	2.775	2.658	2.589	V28-	1.766	2.073	2.190	2.257
1D	V29+	3.057	2.750	2.634	2.565	V29-	1.790	2.100	2.215	2.281
1E	V30+	3.033	2.725	2.611	2.542	V30-	1.813	2.126	2.240	2.304
1F	V31+	3.009	2.700	2.587	2.518	V31-	1.837	2.153	2.265	2.328
20	V32+	2.986	2.675	2.564	2.495	V32-	1.861	2.180	2.291	2.351
21	V33+	2.962	2.649	2.541	2.471	V33-	1.884	2.207	2.316	2.375
22	V34+	2.938	2.624	2.517	2.448	V34-	1.908	2.234	2.341	2.398
23	V35+	2.914	2.599	2.494	2.424	V35-	1.932	2.260	2.366	2.422
24	V36+	2.891	2.574	2.470	2.401	V36-	1.955	2.287	2.391	2.445
25	V37+	2.869	2.552	2.449	2.379	V37-	1.978	2.307	2.411	2.467
26	V38+	2.846	2.531	2.427	2.358	V38-	2.000	2.326	2.430	2.488
27	V39+	2.824	2.509	2.405	2.336	V39-	2.022	2.345	2.449	2.510
28	V40+	2.802	2.488	2.384	2.315	V40-	2.045	2.365	2.469	2.531
29	V41+	2.779	2.466	2.362	2.293	V41-	2.067	2.384	2.488	2.553
2A	V42+	2.757	2.445	2.341	2.272	V42-	2.089	2.404	2.508	2.575
2B	V43+	2.735	2.423	2.319	2.250	V43-	2.112	2.423	2.527	2.596
2C	V44+	2.708	2.399	2.296	2.225	V44-	2.138	2.447	2.550	2.621
2D	V45+	2.681	2.374	2.273	2.201	V45-	2.165	2.472	2.573	2.646
2E	V46+	2.654	2.350	2.250	2.176	V46-	2.192	2.496	2.596	2.670
2F	V47+	2.627	2.326	2.227	2.151	V47-	2.219	2.520	2.620	2.695
30	V48+	2.600	2.302	2.203	2.126	V48-	2.246	2.545	2.643	2.720
31	V49+	2.573	2.277	2.180	2.102	V49-	2.273	2.569	2.666	2.745
32	V50+	2.546	2.253	2.157	2.077	V50-	2.299	2.593	2.689	2.769
33	V51+	2.524	2.228	2.125	2.047	V51-	2.323	2.618	2.721	2.800
34	V52+	2.502	2.203	2.092	2.016	V52-	2.346	2.643	2.754	2.830
35	V53+	2.480	2.178	2.060	1.986	V53-	2.370	2.669	2.786	2.860
36	V54+	2.452	2.146	2.019	1.948	V54-	2.399	2.700	2.827	2.898
37	V55+	2.425	2.115	1.979	1.910	V55-	2.428	2.731	2.867	2.936
38	V56+	2.397	2.083	1.938	1.872	V56-	2.458	2.763	2.908	2.974
39	V57+	2.369	2.052	1.898	1.835	V57-	2.487	2.794	2.948	3.012
3A	V58+	2.326	1.995	1.838	1.499	V58-	2.528	2.859	3.008	3.347
3B	V59+	2.275	1.928	1.768	1.108	V59-	2.575	2.933	3.078	3.738
3C	V60+	2.231	1.819	1.311	0.880	V60-	2.634	3.035	3.535	3.967
3D	V61+	2.181	1.696	0.796	0.623	V61-	2.700	3.150	4.050	4.223
3E	V62+	2.077	0.865	0.588	0.519	V62-	2.769	3.981	4.258	4.327
3F	V63+	0.485	0.485	0.485	0.485	V63-	4.362	4.362	4.362	4.362

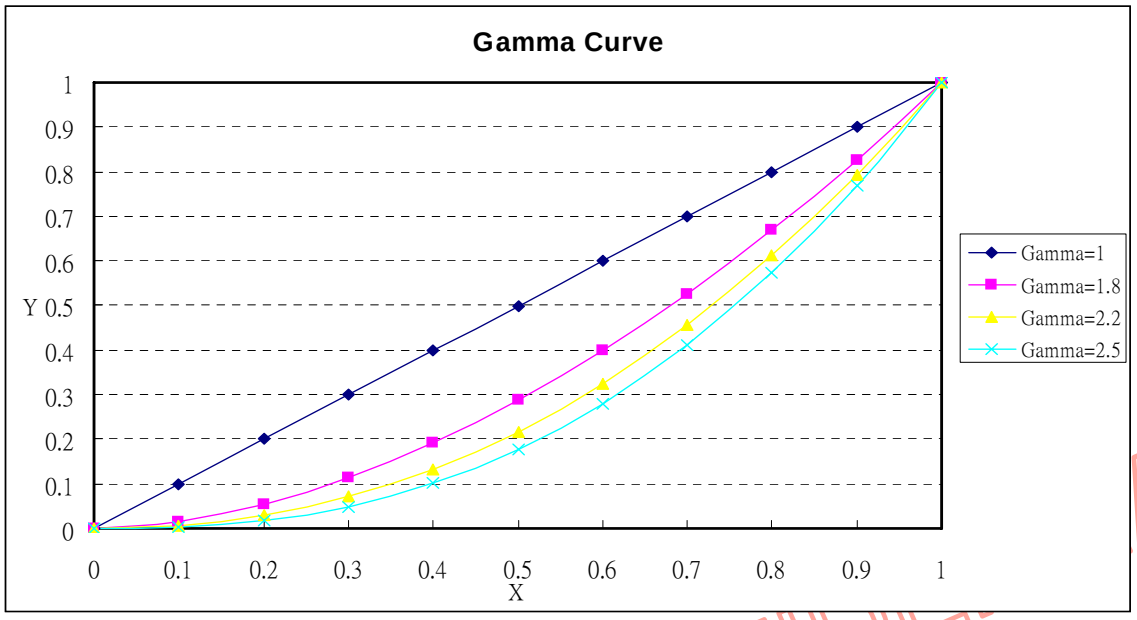


Fig. 5.9.3 Gamma Curve according to the GC0 to GC3 bit

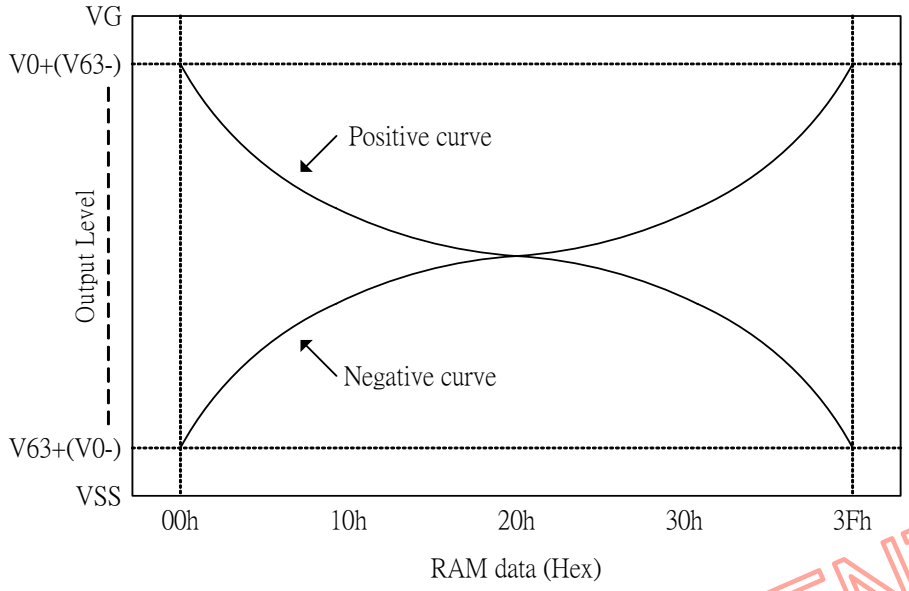


Fig. 5.9.4 Relationship between RAM data and output level

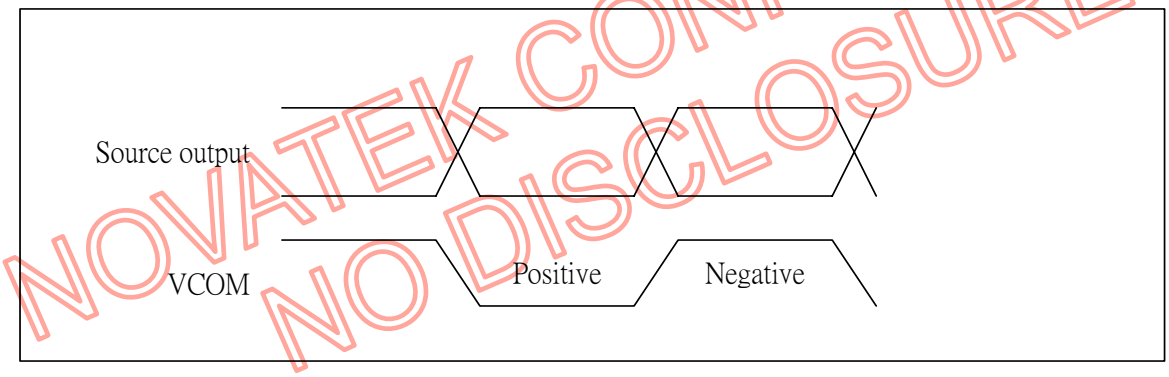


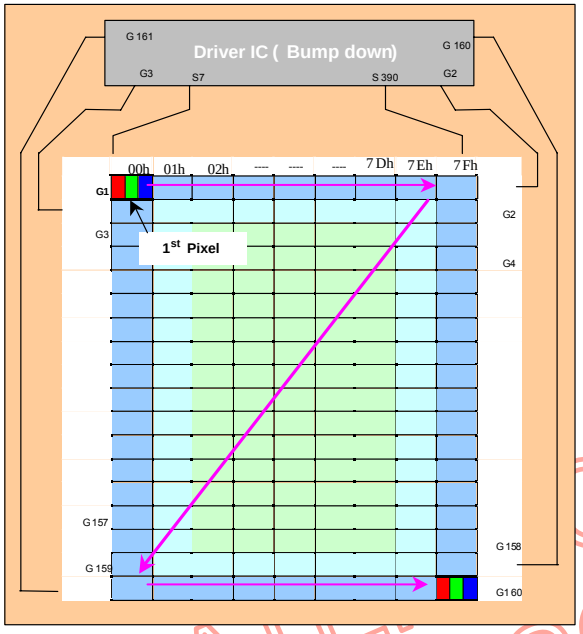
Fig. 5.9.5 Relationship between source output and VCOM

13. Example Connection with Panel direction and Different Resolution

13.1 Application of connection with panel direction (When GM="00")

Case 1: (This is default case)

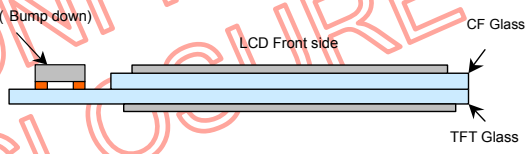
- 1st Pixel is at *Left Top* of the panel
- RGB filter order = RGB



- Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

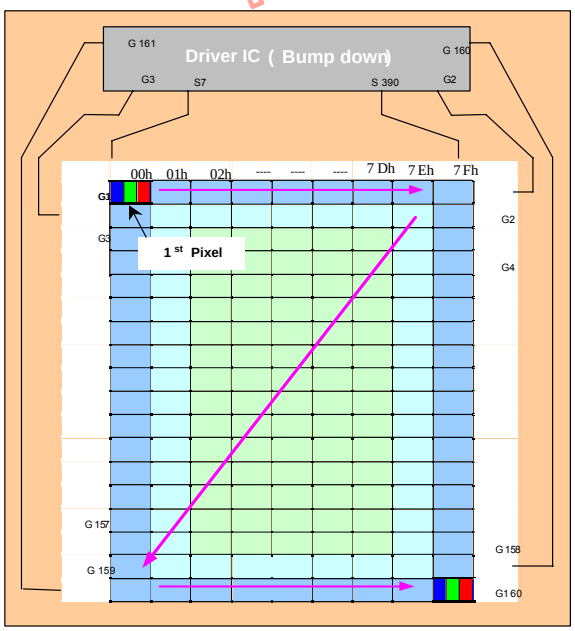
S1 = Filter R
S2 = Filter G
S3 = Filter B

- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV



Case 2:

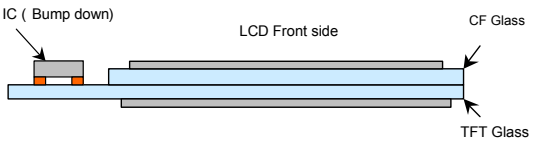
- 1st Pixel is at *Left Top* of the panel
- RGB filter order = BGR



- Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 1

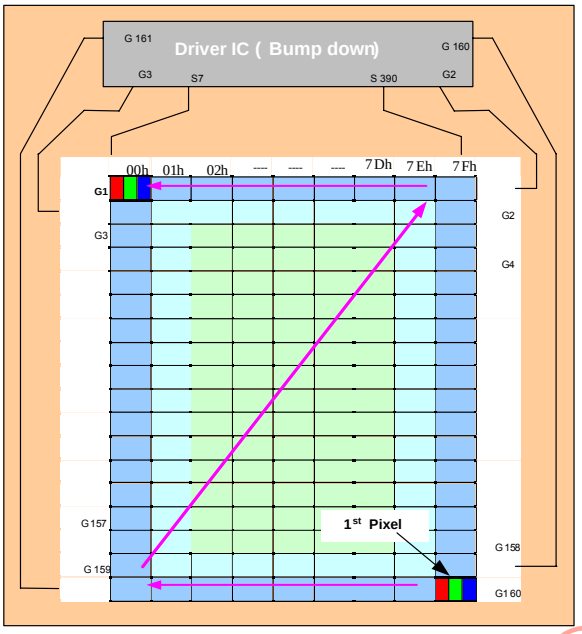
S1 = Filter B
S2 = Filter G
S3 = Filter R

- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV



Case 3:

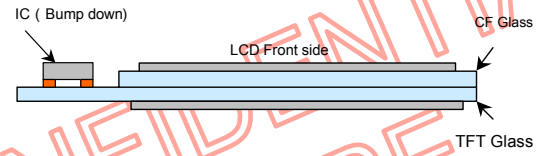
- 1st Pixel is at *Righ Bottom* of the panel
- RGB filter order = RGB



- Direction default setting (H/W)
SMX = 1
SMY = 1
SRGB = 0

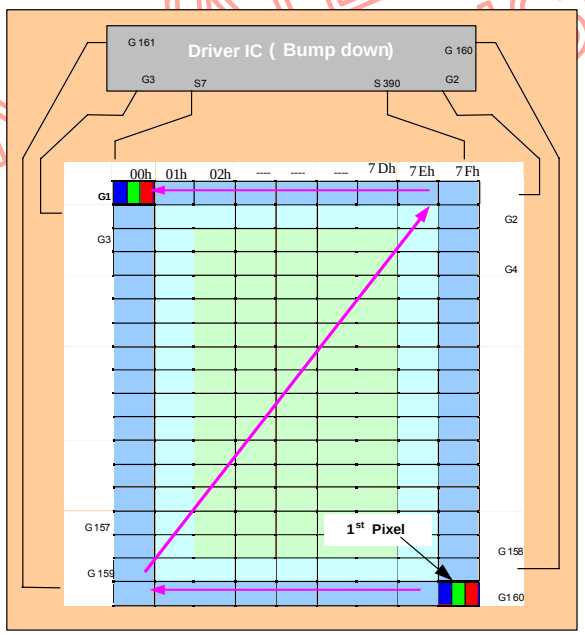
S1 = Filter R
S2 = Filter G
S3 = Filter B

- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV



Case 4:

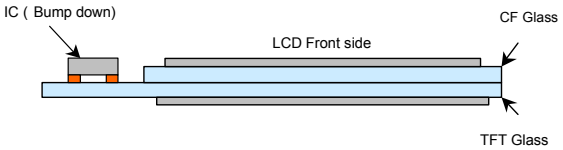
- 1st Pixel is at *Righ Bottom* of the panel
- RGB filter order = BGR



- Direction default setting (H/W)
SMX = 1
SMY = 1
SRGB = 1

S1 = Filter B
S2 = Filter G
S3 = Filter R

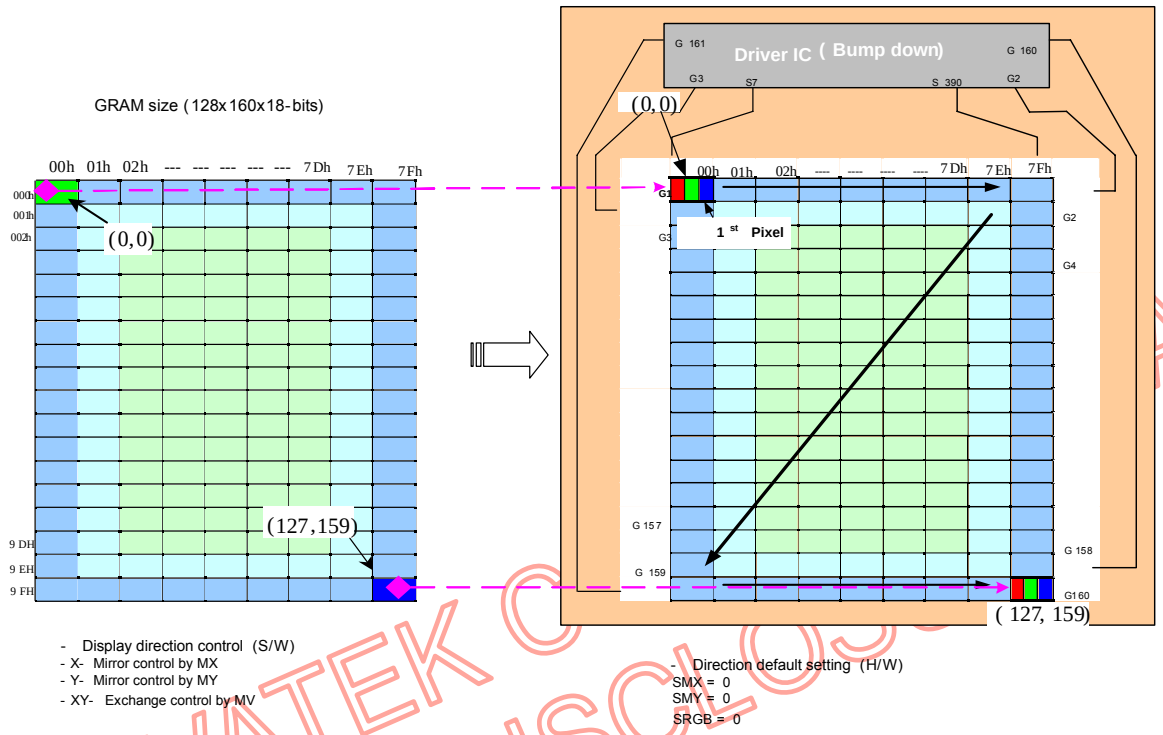
- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV



13.2 Application of connection with Different resolution

Case 1 of Resolution (128RGB x 160) (GM1, GM0 = “00”) RAM size=128 x 160 x 18-bits (Used)
Display size = 128RGB x 160

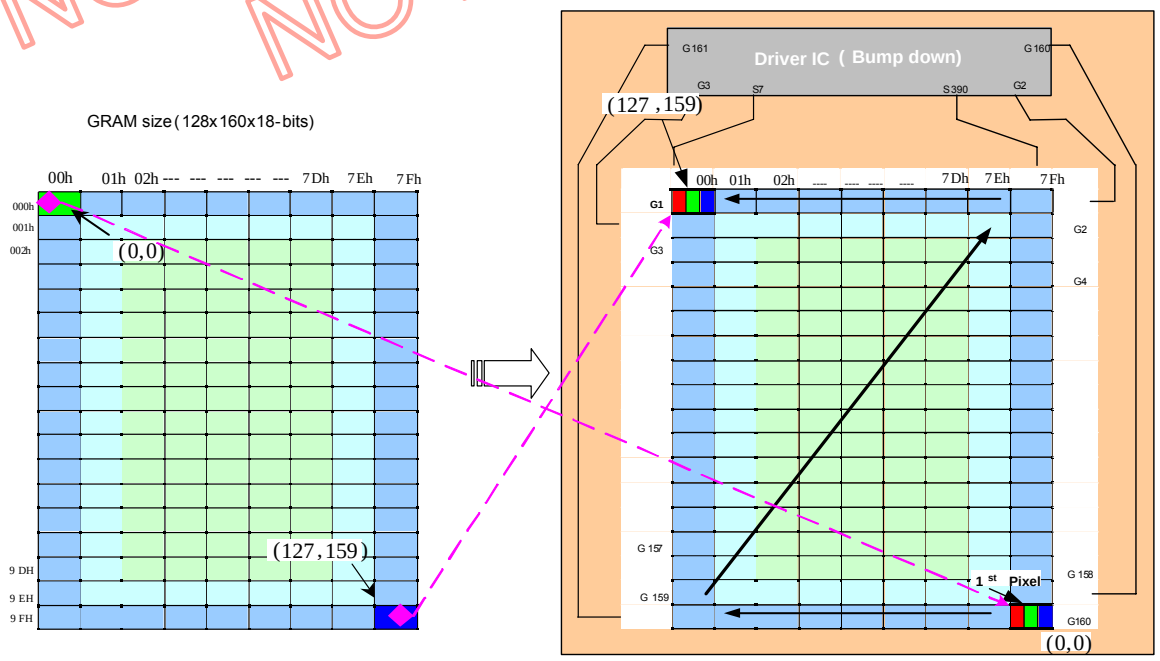
1). Example for SMX=SMY=’0’



- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV

- Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

2). Example for SMX=SMY=’1’

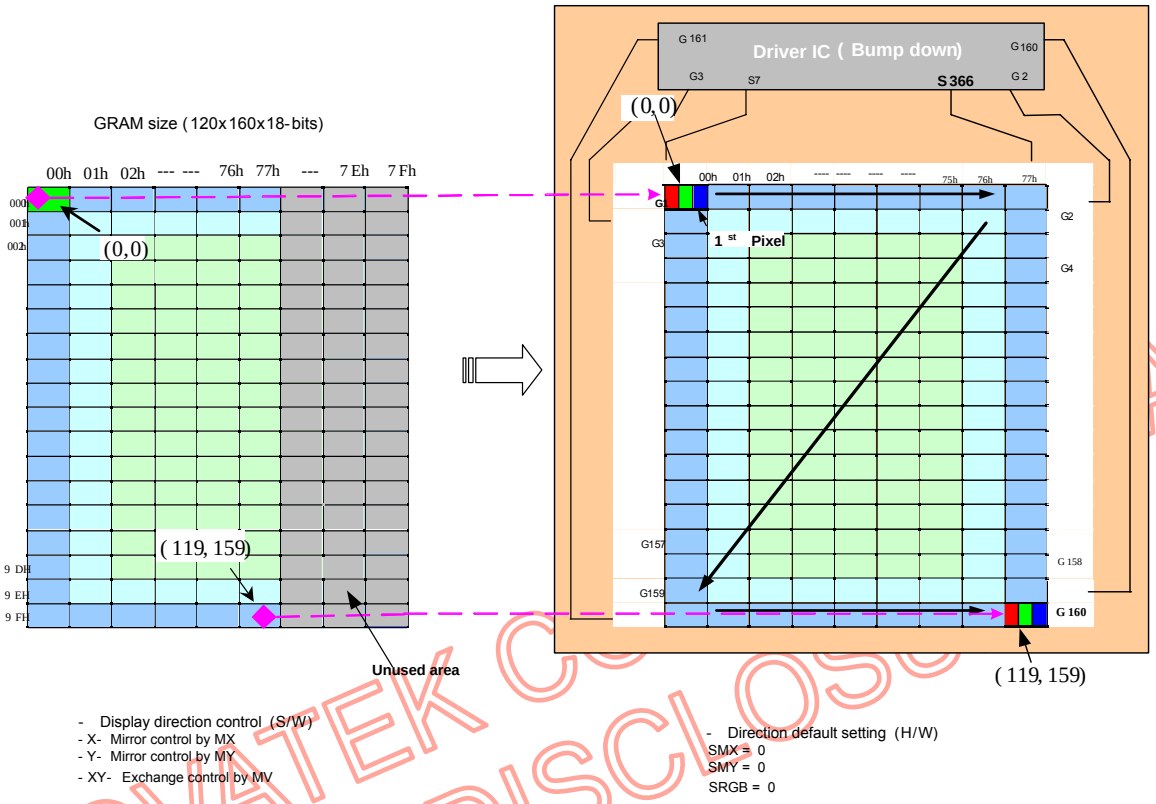


- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV

- Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

Case 2 of Resolution (120RGB x 160) (GM1, GM0 = “01”) RAM size=120 x 160 x 18-bits (Used)
Display size = 120RGB x 160

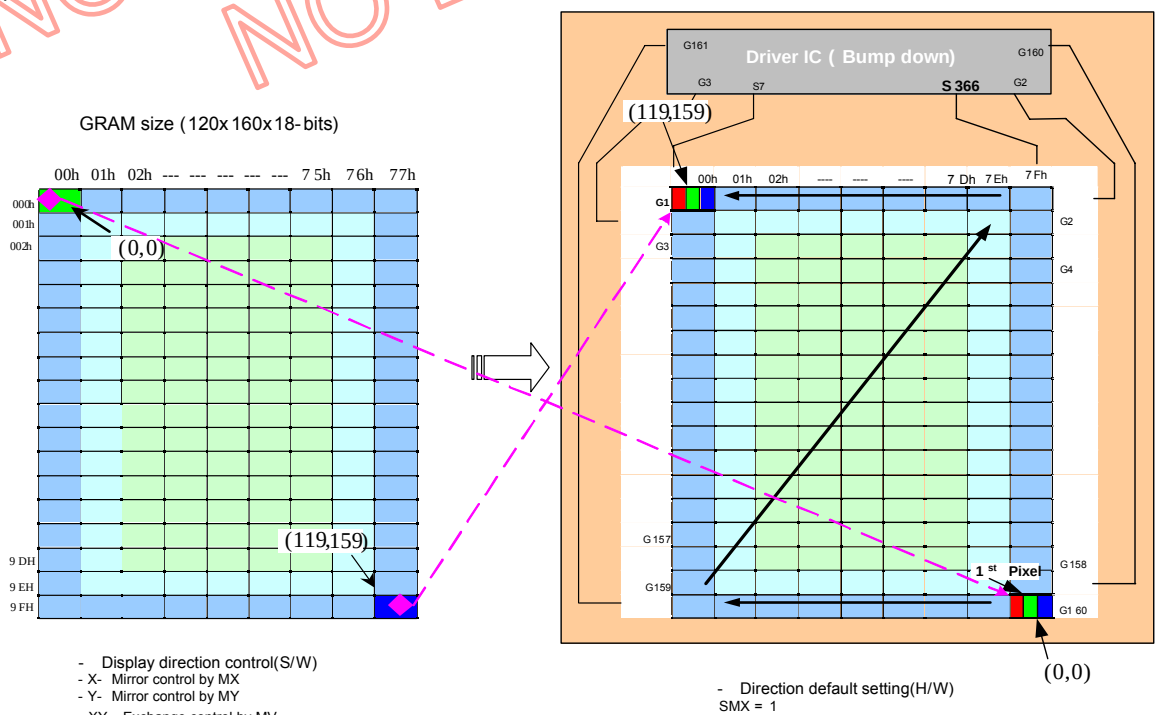
1). Example for SMX=SMY=’0’



- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV

- Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

2). Example for SMX=SMY=’1’

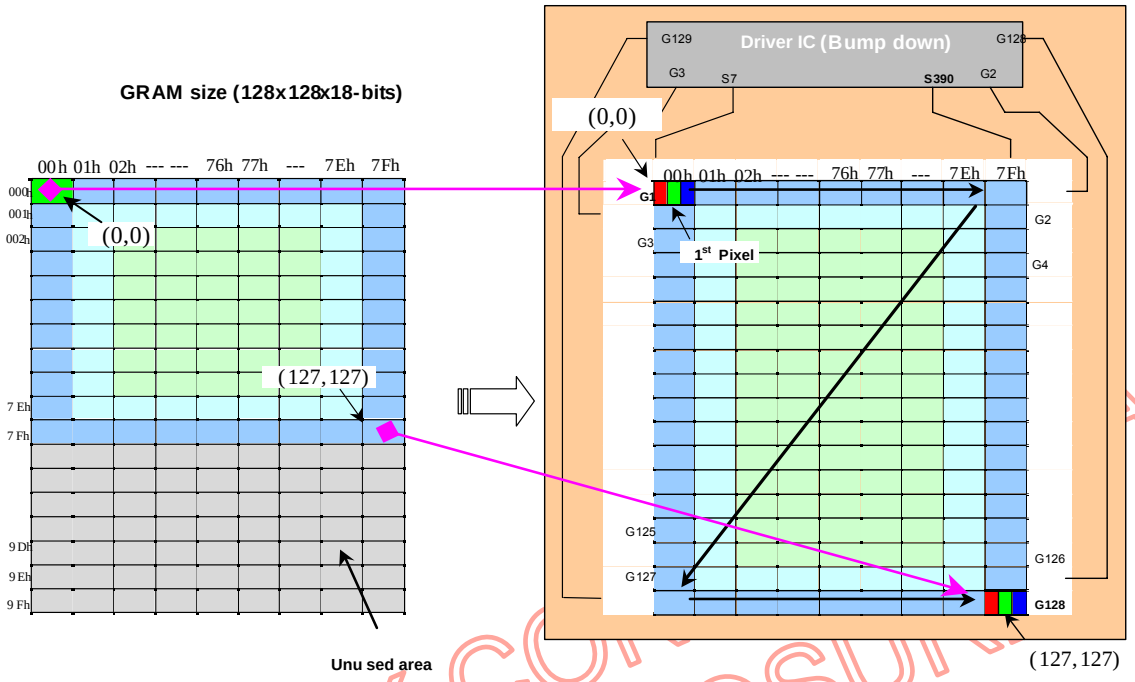


- Display direction control(S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV

- Direction default setting(H/W)
SMX = 1
SMY = 1
SRGB = 0

Case 3 of Resolution (128RGB x 128) (GM1, GM0 = “10”) RAM size=128 x 128 x 18-bits (Used)
Display size = 128RGB x 128

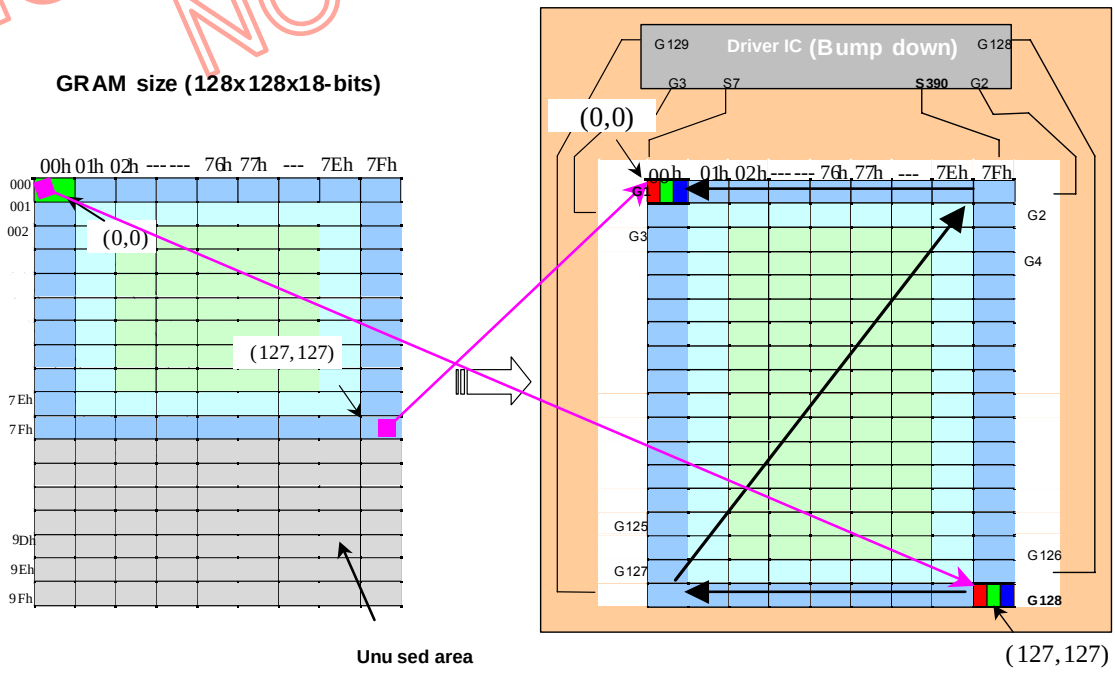
1). Example for SMX=SMY=’0’



- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

- Direction default setting (H/W)
SMX= 0
SMY= 0
SRGB= 0

2). Example for SMX=SMY=’1’

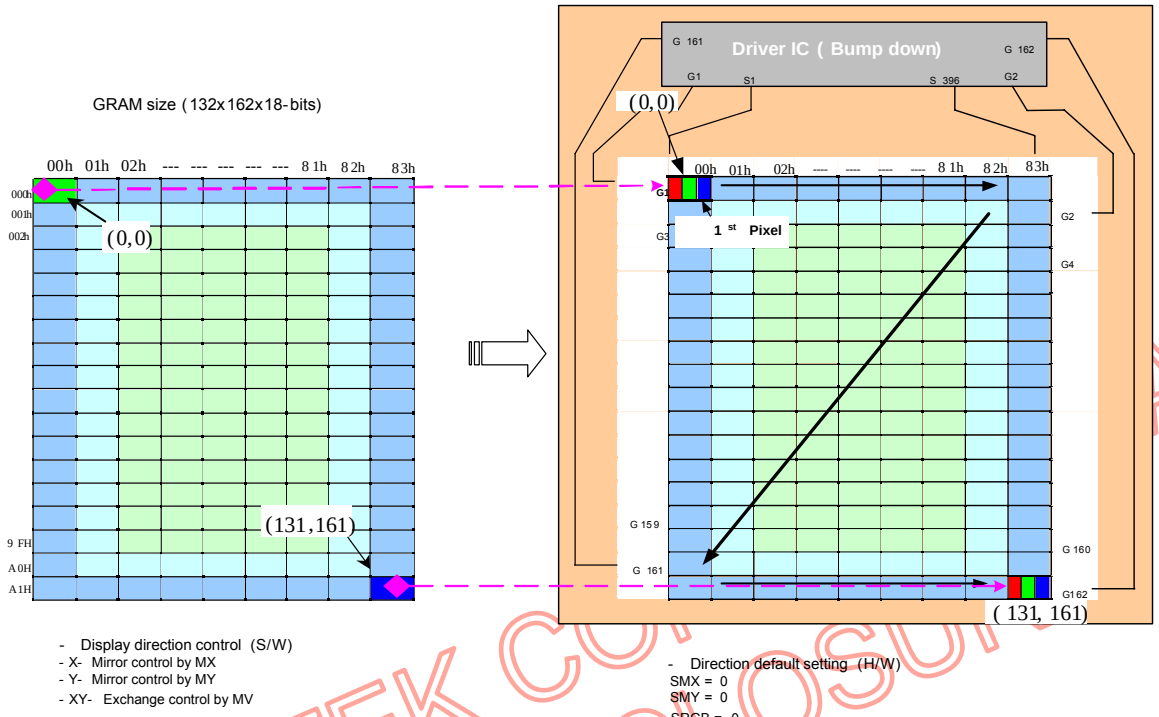


- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

- Direction default setting (H/W)
SMX= 0
SMY= 0
SRGB= 0

Case 4 of Resolution (132RGB x 162) (GM1, GM0 = “11”) RAM size=132 x 162 x 18-bits (Used)
Display size = 132RGB x 162

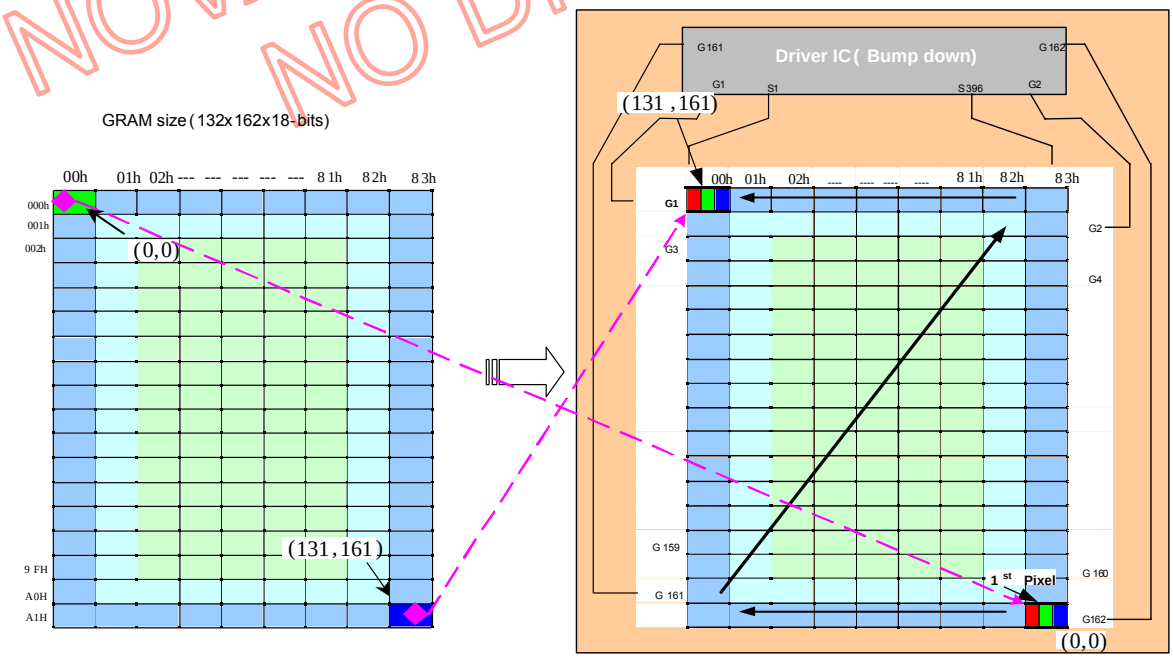
1). Example for SMX=SMY=’0’



- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV

- Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

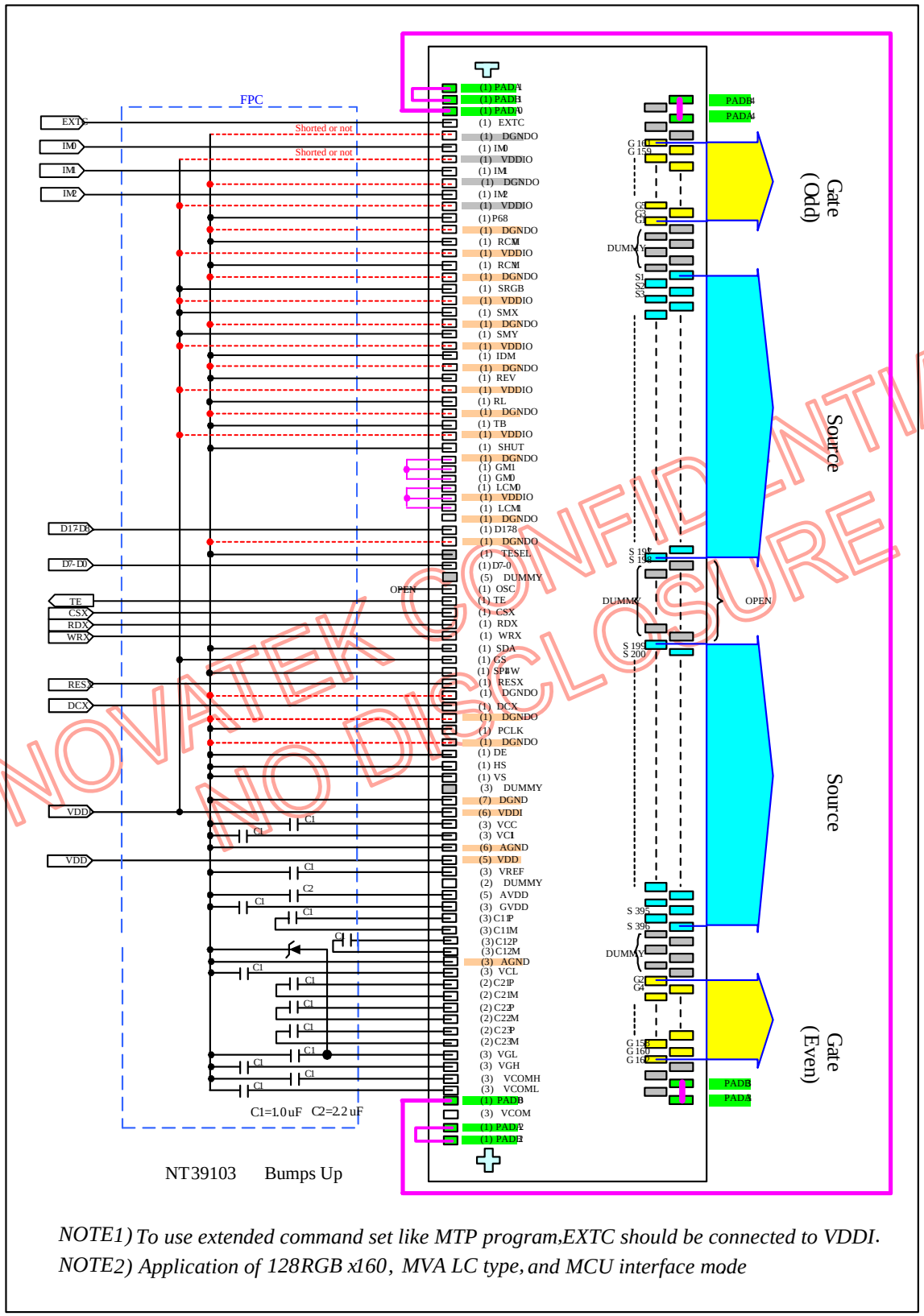
2). Example for SMX=SMY=’1’



- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV

- Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

13.3 Application of connection with NT39103 and LCM



NOTE1) To use extended command set like MTP program,EXTC should be connected to VDDI.

NOTE2) Application of 128RGB x160, MVA LC type, and MCU interface mode

13.4 INSTRUCTION SETUP FLOW

13.4.1 Initializing with the Built-in Power Supply Circuits

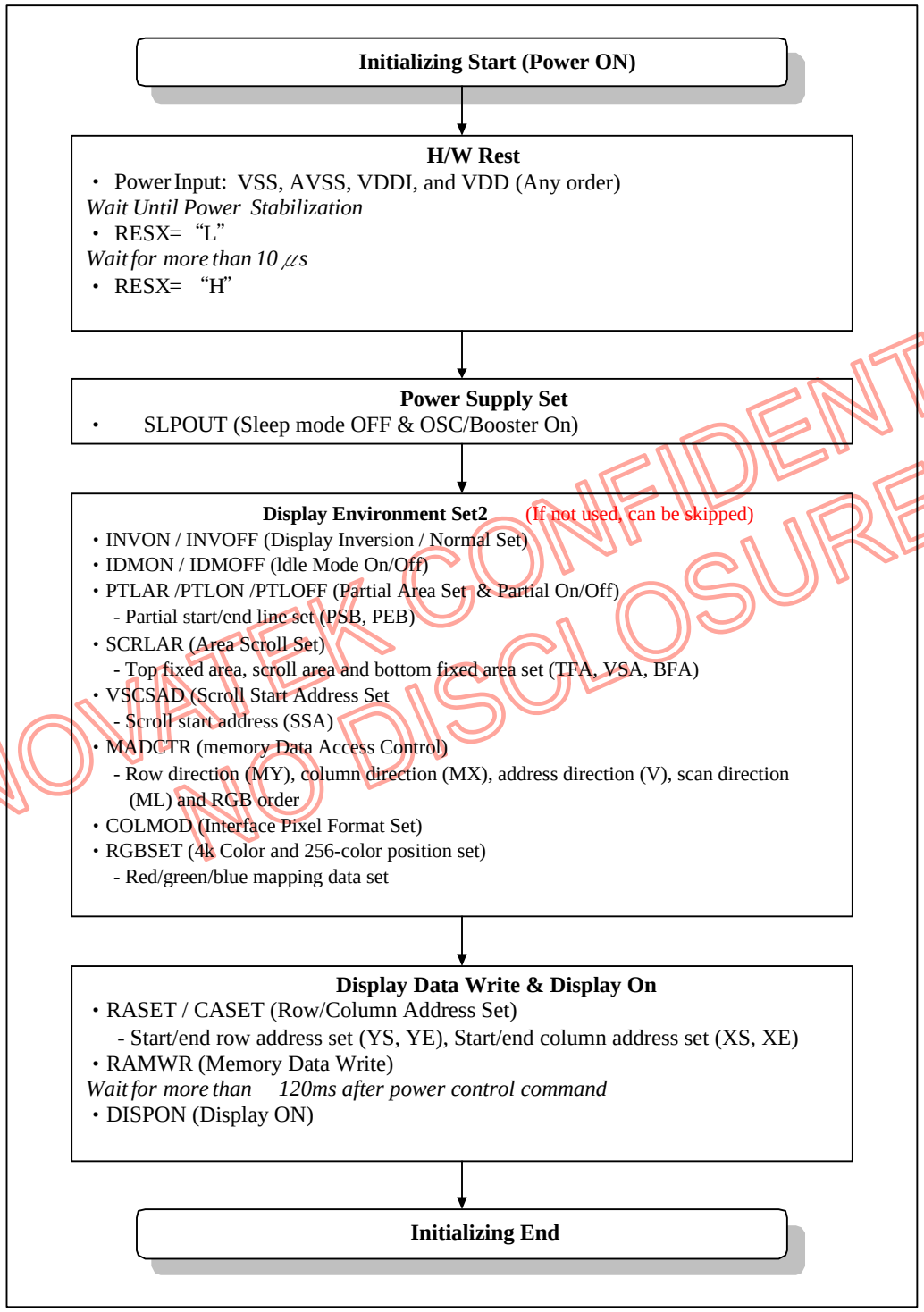


Fig. 13.4.1 Initializing with the built-in power supply circuits

The initializing sequence does not have any effect on the display. The display is in its normal background color during the initialization.

13.4.2 Power OFF Sequence

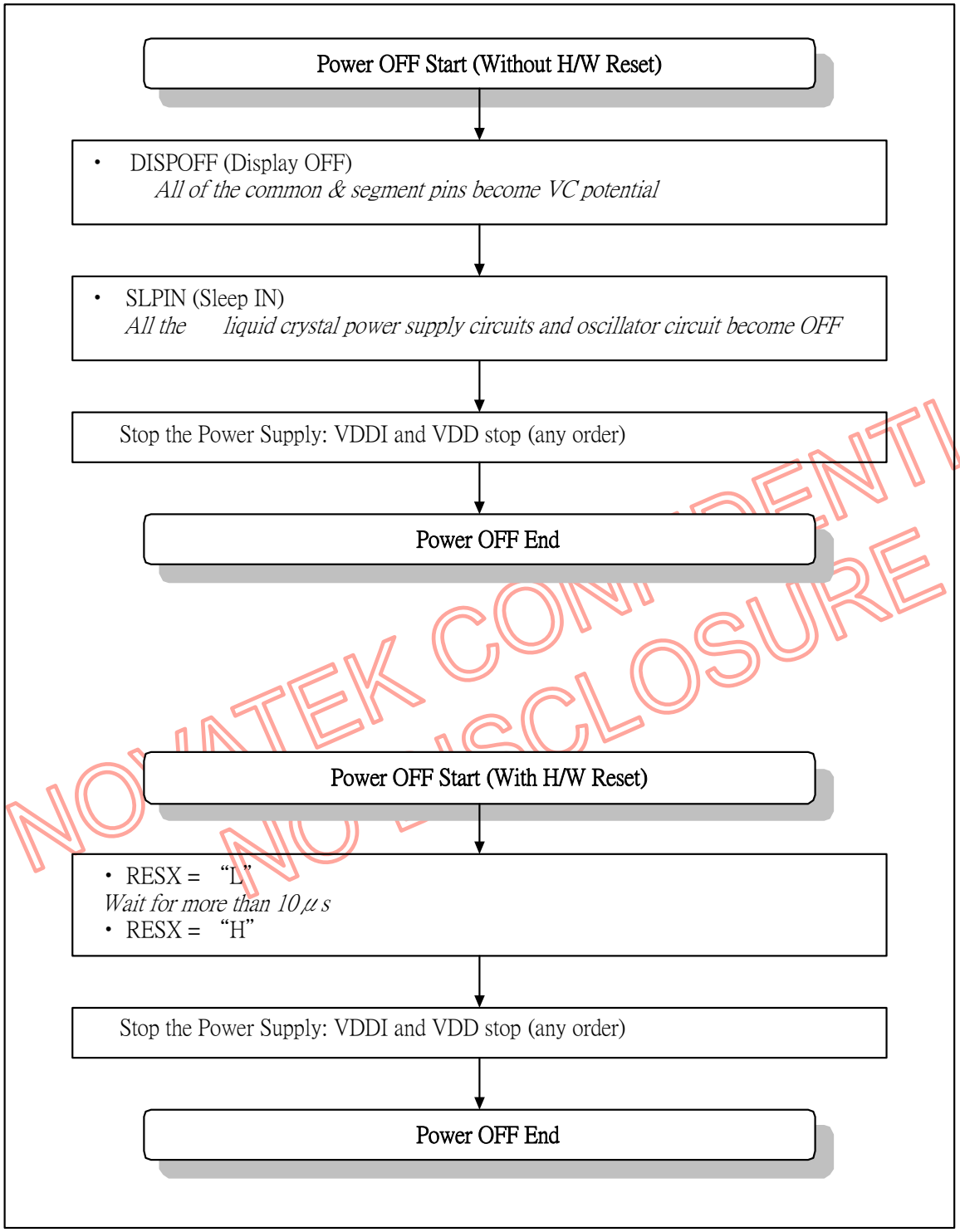


Fig. 13.4.2 Power OFF sequence

14 Chip Information

-Chip Size= 13500um x 700um *(include Scripe Lne)*

-Chip Size can shrink Y-side

-Chip Thickness = 400um (Type)

-Bump height= 15um

14.1 Bump Information

14.1.1 Output Bump Dimension (Source/ Gate /Dummy)

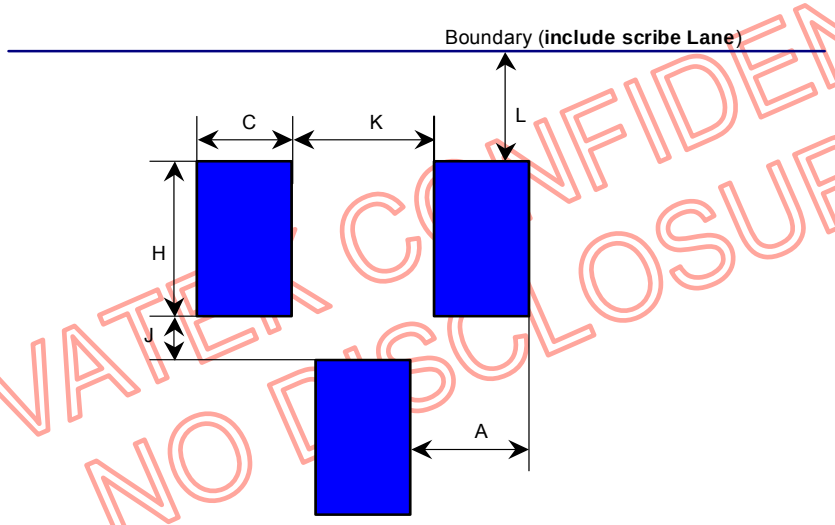


Fig. 14.1.1 Output Bump Dimension

Item	Symbol	Size
Bump pitch	A	22um
Bump width	C	21um
Bump height	H	96um
Bump gap1 (Vertical)	J	35um
Bump gap2 (Horizontal)	K	23um
Bump area	CxH	2016um2
Chip Boundary(include scribe Lane)	L	70um

14.1.2 Input Bump Dimension

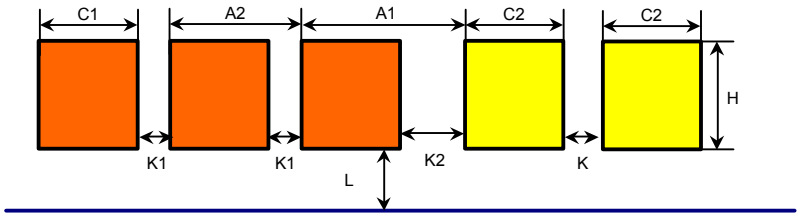


Fig. 14.1.2 Input Bump Dimension

Item	Symbol	Size
Bump pitch 1	A1	82.5um
Bump pitch 2	A2	64um
Bump width 1	C1	55um
Bump width 1	C2	50um
Bump height	H	96um
Bump gap	K	14um
Bump gap1	K1	9um
Bump gap2	K2	27.5um
Bump area 1	C1xH	5280um2
Bump area 2	C2xH	4800um2
Chip Boundary(include scribe Lane)	L	70um

14.2 Alignment Mark Information

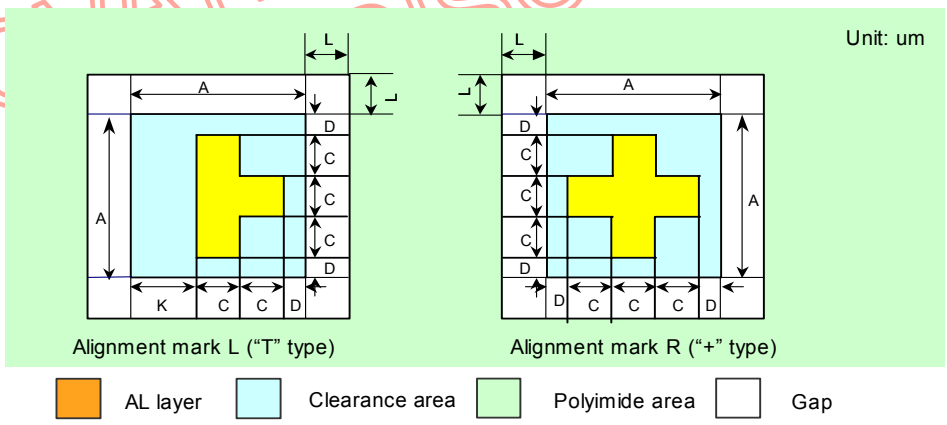
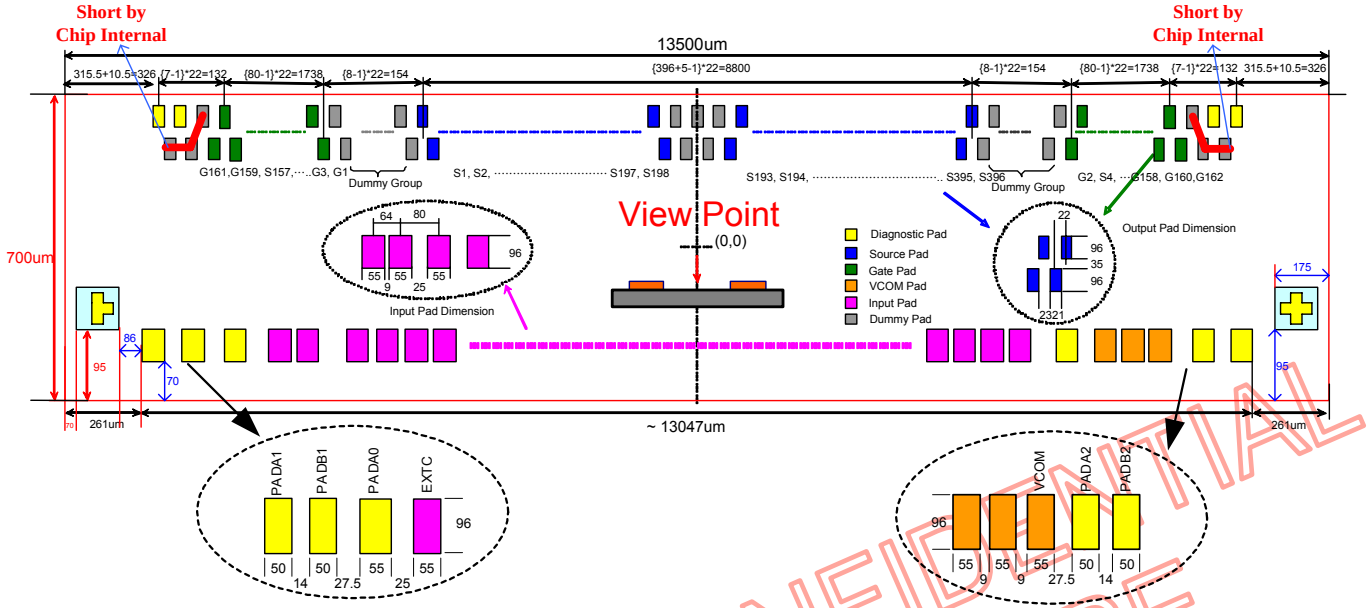


Fig. 3.1 IC Alignment Mark Dimension

Item	Symbol	Size
Alignment mark size	A	105um
Clearance gap 1	D	15um
Clearance gap 2	K	40um
Alignment mark width	C	25um
Alignment area	AxA	11025um2
Gap width	L	40~48um

14.3 Bump Location and Dimension



14.4 Pad Coordinate

Table 14.4.1 Pad Center Coordinates

No	Name	X	Y	No	Name	X	Y
1	PADA1	-6464	-232	51	TESEL	-2480	-232
2	PADB1	-6400	-232	52	D7	-2400	-232
3	PADA0	-6320	-232	53	D6	-2320	-232
4	EXTC	-6240	-232	54	D5	-2240	-232
5	DGNDO	-6160	-232	55	D4	-2160	-232
6	IM0	-6080	-232	56	D3	-2080	-232
7	VDDIO	-6000	-232	57	D2	-2000	-232
8	IM1	-5920	-232	58	D1	-1920	-232
9	DGNDO	-5840	-232	59	D0	-1840	-232
10	IM2	-5760	-232	60	TESTDA[6]	-1760	-232
11	VDDIO	-5680	-232	61	TESTDA[5]	-1680	-232
12	P68	-5600	-232	62	TESTDA[4]	-1600	-232
13	DGNDO	-5520	-232	63	TESTDA[3]	-1520	-232
14	RCM0	-5440	-232	64	TESTOSC	-1440	-232
15	VDDIO	-5360	-232	65	OSC	-1360	-232
16	RCM1	-5280	-232	66	TE	-1280	-232
17	DGNDO	-5200	-232	67	CSX	-1200	-232
18	SRGB	-5120	-232	68	RDX	-1120	-232
19	VDDIO	-5040	-232	69	WRX	-1040	-232
20	SMX	-4960	-232	70	SDA	-960	-232
21	DGNDO	-4880	-232	71	GS	-880	-232
22	SMY	-4800	-232	72	SPI4W	-800	-232
23	VDDIO	-4720	-232	73	RESX	-720	-232
24	IDM	-4640	-232	74	DGNDO	-640	-232
25	DGNDO	-4560	-232	75	DCX	-560	-232
26	REV	-4480	-232	76	DGNDO	-480	-232
27	VDDIO	-4400	-232	77	PCLK	-400	-232
28	RL	-4320	-232	78	DGNDO	-320	-232
29	DGNDO	-4240	-232	79	DE	-240	-232
30	TB	-4160	-232	80	HS	-160	-232
31	VDDIO	-4080	-232	81	VS	-80	-232
32	SHUT	-4000	-232	82	TESTDA[2]	0	-232
33	DGNDO	-3920	-232	83	TESTDA[1]	80	-232
34	GM1	-3840	-232	84	TESTDA[0]	160	-232
35	GM0	-3760	-232	85	DGND	240	-232
36	LCM0	-3680	-232	86	DGND	304	-232
37	VDDIO	-3600	-232	87	DGND	368	-232
38	LCM1	-3520	-232	88	DGND	432	-232
39	DGNDO	-3440	-232	89	DGND	496	-232
40	D17	-3360	-232	90	DGND	560	-232
41	D16	-3280	-232	91	DGND	624	-232
42	D15	-3200	-232	92	VDDI	704	-232
43	D14	-3120	-232	93	VDDI	768	-232
44	D13	-3040	-232	94	VDDI	832	-232
45	D12	-2960	-232	95	VDDI	896	-232
46	D11	-2880	-232	96	VDDI	960	-232
47	D10	-2800	-232	97	VDDI	1024	-232
48	D9	-2720	-232	98	VCC	1104	-232
49	D8	-2640	-232	99	VCC	1168	-232
50	DGNDO	-2560	-232	100	VCC	1232	-232

Table 14.4.1 Pad Center Coordinates (continued)

No	Name	X	Y	No	Name	X	Y
101	VCI1	1312	-232	151	C22P	4768	-232
102	VCI1	1376	-232	152	C22N	4848	-232
103	VCI1	1440	-232	153	C22N	4912	-232
104	AGND	1520	-232	154	C23P	4992	-232
105	AGND	1584	-232	155	C23P	5056	-232
106	AGND	1648	-232	156	C23N	5136	-232
107	AGND	1712	-232	157	C23N	5200	-232
108	AGND	1776	-232	158	VGL	5280	-232
109	AGND	1840	-232	159	VGL	5344	-232
110	VDD	1920	-232	160	VGL	5408	-232
111	VDD	1984	-232	161	VGH	5488	-232
112	VDD	2048	-232	162	VGH	5552	-232
113	VDD	2112	-232	163	VGH	5616	-232
114	VDD	2176	-232	164	VCOMH	5696	-232
115	VREF	2256	-232	165	VCOMH	5760	-232
116	VREF	2320	-232	166	VCOMH	5824	-232
117	VREF	2384	-232	167	VCOML	5904	-232
118	TEST	2464	-232	168	VCOML	5968	-232
119	VPRER_OUT	2544	-232	169	VCOML	6032	-232
120	AVDD	2624	-232	170	PADB0	6112	-232
121	AVDD	2688	-232	171	VCOM	6192	-232
122	AVDD	2752	-232	172	VCOM	6256	-232
123	AVDD	2816	-232	173	VCOM	6320	-232
124	AVDD	2880	-232	174	PADA2	6400	-232
125	GVDD	2960	-232	175	PADB2	6464	-232
126	GVDD	3024	-232	176	PADA3	6424	232
127	GVDD	3088	-232	177	Dummy4	6402	101
128	C11P	3168	-232	178	PADB3	6380	232
129	C11P	3232	-232	179	Dummy5	6358	101
130	C11P	3296	-232	180	Dummy6	6336	232
131	C11N	3376	-232	181	G162	6314	101
132	C11N	3440	-232	182	G160	6292	232
133	C11N	3504	-232	183	G158	6270	101
134	C12P	3584	-232	184	G156	6248	232
135	C12P	3648	-232	185	G154	6226	101
136	C12P	3712	-232	186	G152	6204	232
137	C12N	3792	-232	187	G150	6182	101
138	C12N	3856	-232	188	G148	6160	232
139	C12N	3920	-232	189	G146	6138	101
140	AGND	4000	-232	190	G144	6116	232
141	AGND	4064	-232	191	G142	6094	101
142	AGND	4128	-232	192	G140	6072	232
143	VCL	4208	-232	193	G138	6050	101
144	VCL	4272	-232	194	G136	6028	232
145	VCL	4336	-232	195	G134	6006	101
146	C21P	4416	-232	196	G132	5984	232
147	C21P	4480	-232	197	G130	5962	101
148	C21N	4560	-232	198	G128	5940	232
149	C21N	4624	-232	199	G126	5918	101
150	C22P	4704	-232	200	G124	5896	232

Table 14.4.1 Pad Center Coordinates (continued)

No	Name	X	Y	No	Name	X	Y
201	G122	5874	101	251	G22	4774	101
202	G120	5852	232	252	G20	4752	232
203	G118	5830	101	253	G18	4730	101
204	G116	5808	232	254	G16	4708	232
205	G114	5786	101	255	G14	4686	101
206	G112	5764	232	256	G12	4664	232
207	G110	5742	101	257	G10	4642	101
208	G108	5720	232	258	G8	4620	232
209	G106	5698	101	259	G6	4598	101
210	G104	5676	232	260	G4	4576	232
211	G102	5654	101	261	G2	4554	101
212	G100	5632	232	262	Dummy7	4532	232
213	G98	5610	101	263	Dummy8	4510	101
214	G96	5588	232	264	Dummy9	4488	232
215	G94	5566	101	265	Dummy10	4466	101
216	G92	5544	232	266	Dummy11	4444	232
217	G90	5522	101	267	Dummy12	4422	101
218	G88	5500	232	268	S396	4400	232
219	G86	5478	101	269	S395	4378	101
220	G84	5456	232	270	S394	4356	232
221	G82	5434	101	271	S393	4334	101
222	G80	5412	232	272	S392	4312	232
223	G78	5390	101	273	S391	4290	101
224	G76	5368	232	274	S390	4268	232
225	G74	5346	101	275	S389	4246	101
226	G72	5324	232	276	S388	4224	232
227	G70	5302	101	277	S387	4202	101
228	G68	5280	232	278	S386	4180	232
229	G66	5258	101	279	S385	4158	101
230	G64	5236	232	280	S384	4136	232
231	G62	5214	101	281	S383	4114	101
232	G60	5192	232	282	S382	4092	232
233	G58	5170	101	283	S381	4070	101
234	G56	5148	232	284	S380	4048	232
235	G54	5126	101	285	S379	4026	101
236	G52	5104	232	286	S378	4004	232
237	G50	5082	101	287	S377	3982	101
238	G48	5060	232	288	S376	3960	232
239	G46	5038	101	289	S375	3938	101
240	G44	5016	232	290	S374	3916	232
241	G42	4994	101	291	S373	3894	101
242	G40	4972	232	292	S372	3872	232
243	G38	4950	101	293	S371	3850	101
244	G36	4928	232	294	S370	3828	232
245	G34	4906	101	295	S369	3806	101
246	G32	4884	232	296	S368	3784	232
247	G30	4862	101	297	S367	3762	101
248	G28	4840	232	298	S366	3740	232
249	G26	4818	101	299	S365	3718	101
250	G24	4796	232	300	S364	3696	232

Table 14.4.1 Pad Center Coordinates (continued)

No	Name	X	Y	No	Name	X	Y
301	S363	3674	101	351	S313	2574	101
302	S362	3652	232	352	S312	2552	232
303	S361	3630	101	353	S311	2530	101
304	S360	3608	232	354	S310	2508	232
305	S359	3586	101	355	S309	2486	101
306	S358	3564	232	356	S308	2464	232
307	S357	3542	101	357	S307	2442	101
308	S356	3520	232	358	S306	2420	232
309	S355	3498	101	359	S305	2398	101
310	S354	3476	232	360	S304	2376	232
311	S353	3454	101	361	S303	2354	101
312	S352	3432	232	362	S302	2332	232
313	S351	3410	101	363	S301	2310	101
314	S350	3388	232	364	S300	2288	232
315	S349	3366	101	365	S299	2266	101
316	S348	3344	232	366	S298	2244	232
317	S347	3322	101	367	S297	2222	101
318	S346	3300	232	368	S296	2200	232
319	S345	3278	101	369	S295	2178	101
320	S344	3256	232	370	S294	2156	232
321	S343	3234	101	371	S293	2134	101
322	S342	3212	232	372	S292	2112	232
323	S341	3190	101	373	S291	2090	101
324	S340	3168	232	374	S290	2068	232
325	S339	3146	101	375	S289	2046	101
326	S338	3124	232	376	S288	2024	232
327	S337	3102	101	377	S287	2002	101
328	S336	3080	232	378	S286	1980	232
329	S335	3058	101	379	S285	1958	101
330	S334	3036	232	380	S284	1936	232
331	S333	3014	101	381	S283	1914	101
332	S332	2992	232	382	S282	1892	232
333	S331	2970	101	383	S281	1870	101
334	S330	2948	232	384	S280	1848	232
335	S329	2926	101	385	S279	1826	101
336	S328	2904	232	386	S278	1804	232
337	S327	2882	101	387	S277	1782	101
338	S326	2860	232	388	S276	1760	232
339	S325	2838	101	389	S275	1738	101
340	S324	2816	232	390	S274	1716	232
341	S323	2794	101	391	S273	1694	101
342	S322	2772	232	392	S272	1672	232
343	S321	2750	101	393	S271	1650	101
344	S320	2728	232	394	S270	1628	232
345	S319	2706	101	395	S269	1606	101
346	S318	2684	232	396	S268	1584	232
347	S317	2662	101	397	S267	1562	101
348	S316	2640	232	398	S266	1540	232
349	S315	2618	101	399	S265	1518	101
350	S314	2596	232	400	S264	1496	232

Table 14.4.1 Pad Center Coordinates (continued)

No	Name	X	Y	No	Name	X	Y
401	S263	1474	101	451	S213	374	101
402	S262	1452	232	452	S212	352	232
403	S261	1430	101	453	S211	330	101
404	S260	1408	232	454	S210	308	232
405	S259	1386	101	455	S209	286	101
406	S258	1364	232	456	S208	264	232
407	S257	1342	101	457	S207	242	101
408	S256	1320	232	458	S206	220	232
409	S255	1298	101	459	S205	198	101
410	S254	1276	232	460	S204	176	232
411	S253	1254	101	461	S203	154	101
412	S252	1232	232	462	S202	132	232
413	S251	1210	101	463	S201	110	101
414	S250	1188	232	464	S200	88	232
415	S249	1166	101	465	S199	66	101
416	S248	1144	232	466	Dymmy13	44	232
417	S247	1122	101	467	Dymmy14	22	101
418	S246	1100	232	468	Dymmy15	0	232
419	S245	1078	101	469	Dymmy16	-22	101
420	S244	1056	232	470	Dymmy17	-44	232
421	S243	1034	101	471	S198	-66	101
422	S242	1012	232	472	S197	-88	232
423	S241	990	101	473	S196	-110	101
424	S240	968	232	474	S195	-132	232
425	S239	946	101	475	S194	-154	101
426	S238	924	232	476	S193	-176	232
427	S237	902	101	477	S192	-198	101
428	S236	880	232	478	S191	-220	232
429	S235	858	101	479	S190	-242	101
430	S234	836	232	480	S189	-264	232
431	S233	814	101	481	S188	-286	101
432	S232	792	232	482	S187	-308	232
433	S231	770	101	483	S186	-330	101
434	S230	748	232	484	S185	-352	232
435	S229	726	101	485	S184	-374	101
436	S228	704	232	486	S183	-396	232
437	S227	682	101	487	S182	-418	101
438	S226	660	232	488	S181	-440	232
439	S225	638	101	489	S180	-462	101
440	S224	616	232	490	S179	-484	232
441	S223	594	101	491	S178	-506	101
442	S222	572	232	492	S177	-528	232
443	S221	550	101	493	S176	-550	101
444	S220	528	232	494	S175	-572	232
445	S219	506	101	495	S174	-594	101
446	S218	484	232	496	S173	-616	232
447	S217	462	101	497	S172	-638	101
448	S216	440	232	498	S171	-660	232
449	S215	418	101	499	S170	-682	101
450	S214	396	232	500	S169	-704	232

Table 14.4.1 Pad Center Coordinates (continued)

No	Name	X	Y	No	Name	X	Y
501	S168	-726	101	551	S118	-1826	101
502	S167	-748	232	552	S117	-1848	232
503	S166	-770	101	553	S116	-1870	101
504	S165	-792	232	554	S115	-1892	232
505	S164	-814	101	555	S114	-1914	101
506	S163	-836	232	556	S113	-1936	232
507	S162	-858	101	557	S112	-1958	101
508	S161	-880	232	558	S111	-1980	232
509	S160	-902	101	559	S110	-2002	101
510	S159	-924	232	560	S109	-2024	232
511	S158	-946	101	561	S108	-2046	101
512	S157	-968	232	562	S107	-2068	232
513	S156	-990	101	563	S106	-2090	101
514	S155	-1012	232	564	S105	-2112	232
515	S154	-1034	101	565	S104	-2134	101
516	S153	-1056	232	566	S103	-2156	232
517	S152	-1078	101	567	S102	-2178	101
518	S151	-1100	232	568	S101	-2200	232
519	S150	-1122	101	569	S100	-2222	101
520	S149	-1144	232	570	S99	-2244	232
521	S148	-1166	101	571	S98	-2266	101
522	S147	-1188	232	572	S97	-2288	232
523	S146	-1210	101	573	S96	-2310	101
524	S145	-1232	232	574	S95	-2332	232
525	S144	-1254	101	575	S94	-2354	101
526	S143	-1276	232	576	S93	-2376	232
527	S142	-1298	101	577	S92	-2398	101
528	S141	-1320	232	578	S91	-2420	232
529	S140	-1342	101	579	S90	-2442	101
530	S139	-1364	232	580	S89	-2464	232
531	S138	-1386	101	581	S88	-2486	101
532	S137	-1408	232	582	S87	-2508	232
533	S136	-1430	101	583	S86	-2530	101
534	S135	-1452	232	584	S85	-2552	232
535	S134	-1474	101	585	S84	-2574	101
536	S133	-1496	232	586	S83	-2596	232
537	S132	-1518	101	587	S82	-2618	101
538	S131	-1540	232	588	S81	-2640	232
539	S130	-1562	101	589	S80	-2662	101
540	S129	-1584	232	590	S79	-2684	232
541	S128	-1606	101	591	S78	-2706	101
542	S127	-1628	232	592	S77	-2728	232
543	S126	-1650	101	593	S76	-2750	101
544	S125	-1672	232	594	S75	-2772	232
545	S124	-1694	101	595	S74	-2794	101
546	S123	-1716	232	596	S73	-2816	232
547	S122	-1738	101	597	S72	-2838	101
548	S121	-1760	232	598	S71	-2860	232
549	S120	-1782	101	599	S70	-2882	101
550	S119	-1804	232	600	S69	-2904	232

Table 14.4.1 Pad Center Coordinates (continued)

No	Name	X	Y	No	Name	X	Y
601	S68	-2926	101	651	S18	-4026	101
602	S67	-2948	232	652	S17	-4048	232
603	S66	-2970	101	653	S16	-4070	101
604	S65	-2992	232	654	S15	-4092	232
605	S64	-3014	101	655	S14	-4114	101
606	S63	-3036	232	656	S13	-4136	232
607	S62	-3058	101	657	S12	-4158	101
608	S61	-3080	232	658	S11	-4180	232
609	S60	-3102	101	659	S10	-4202	101
610	S59	-3124	232	660	S9	-4224	232
611	S58	-3146	101	661	S8	-4246	101
612	S57	-3168	232	662	S7	-4268	232
613	S56	-3190	101	663	S6	-4290	101
614	S55	-3212	232	664	S5	-4312	232
615	S54	-3234	101	665	S4	-4334	101
616	S53	-3256	232	666	S3	-4356	232
617	S52	-3278	101	667	S2	-4378	101
618	S51	-3300	232	668	S1	-4400	232
619	S50	-3322	101	669	Dymmy18	-4422	101
620	S49	-3344	232	670	Dymmy19	-4444	232
621	S48	-3366	101	671	Dymmy20	-4466	101
622	S47	-3388	232	672	Dymmy21	-4488	232
623	S46	-3410	101	673	Dymmy22	-4510	101
624	S45	-3432	232	674	Dymmy23	-4532	232
625	S44	-3454	101	675	G1	-4554	101
626	S43	-3476	232	676	G3	-4576	232
627	S42	-3498	101	677	G5	-4598	101
628	S41	-3520	232	678	G7	-4620	232
629	S40	-3542	101	679	G9	-4642	101
630	S39	-3564	232	680	G11	-4664	232
631	S38	-3586	101	681	G13	-4686	101
632	S37	-3608	232	682	G15	-4708	232
633	S36	-3630	101	683	G17	-4730	101
634	S35	-3652	232	684	G19	-4752	232
635	S34	-3674	101	685	G21	-4774	101
636	S33	-3696	232	686	G23	-4796	232
637	S32	-3718	101	687	G25	-4818	101
638	S31	-3740	232	688	G27	-4840	232
639	S30	-3762	101	689	G29	-4862	101
640	S29	-3784	232	690	G31	-4884	232
641	S28	-3806	101	691	G33	-4906	101
642	S27	-3828	232	692	G35	-4928	232
643	S26	-3850	101	693	G37	-4950	101
644	S25	-3872	232	694	G39	-4972	232
645	S24	-3894	101	695	G41	-4994	101
646	S23	-3916	232	696	G43	-5016	232
647	S22	-3938	101	697	G45	-5038	101
648	S21	-3960	232	698	G47	-5060	232
649	S20	-3982	101	699	G49	-5082	101
650	S19	-4004	232	700	G51	-5104	232

Table 14.4.1 Pad Center Coordinates (continued)

No	Name	X	Y	No	Name	X	Y
701	G53	-5126	101	751	G153	-6226	101
702	G55	-5148	232	752	G155	-6248	232
703	G57	-5170	101	753	G157	-6270	101
704	G59	-5192	232	754	G159	-6292	232
705	G61	-5214	101	755	G161	-6314	101
706	G63	-5236	232	756	Dummy24	-6336	232
707	G65	-5258	101	757	Dummy25	-6358	101
708	G67	-5280	232	758	PADA4	-6380	232
709	G69	-5302	101	759	Dummy26	-6402	101
710	G71	-5324	232	760	PADB4	-6424	232
711	G73	-5346	101	761	T	-6627.5	-202.5
712	G75	-5368	232	762	+	6627.5	-202.5
713	G77	-5390	101				
714	G79	-5412	232				
715	G81	-5434	101				
716	G83	-5456	232				
717	G85	-5478	101				
718	G87	-5500	232				
719	G89	-5522	101				
720	G91	-5544	232				
721	G93	-5566	101				
722	G95	-5588	232				
723	G97	-5610	101				
724	G99	-5632	232				
725	G101	-5654	101				
726	G103	-5676	232				
727	G105	-5698	101				
728	G107	-5720	232				
729	G109	-5742	101				
730	G111	-5764	232				
731	G113	-5786	101				
732	G115	-5808	232				
733	G117	-5830	101				
734	G119	-5852	232				
735	G121	-5874	101				
736	G123	-5896	232				
737	G125	-5918	101				
738	G127	-5940	232				
739	G129	-5962	101				
740	G131	-5984	232				
741	G133	-6006	101				
742	G135	-6028	232				
743	G137	-6050	101				
744	G139	-6072	232				
745	G141	-6094	101				
746	G143	-6116	232				
747	G145	-6138	101				
748	G147	-6160	232				
749	G149	-6182	101				
750	G151	-6204	232				

REMARK

	GATE OUTPUT PIN
	SOURCE OUTPUT PIN
	TEST PIN
	DUMMY PIN
	ALIGN MARK