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ILI9327

**a-Si TFT LCD Single Chip Driver
240RGBx432 Resolution and 262K color**

**Preliminary
Datasheet**

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ILI TECHNOLOGY CORP.

8F, No. 38, Taiyuan St., Jhubei City,
Hsinchu County 302, Taiwan, R.O.C.
Tel.886-3-5600099; Fax.886-3-5600585
<http://www.ilitek.com>

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1. Introduction

ILI9327 is a 262,144-color single-chip SoC driver for a-TFT liquid crystal display with resolution of 240RGBx432 dots, comprising a 720-channel source driver, a 432-channel gate driver, 233,280 bytes GRAM for graphic data of 240RGBx432 dots, and power supply circuit.

The ILI9327 supports 18-/16-/9-/8-bit data bus interface (DBI) and serial peripheral interfaces (SPI). It also supplies 18-bit, 16-bit or 6-bit RGB interface (DPI) for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

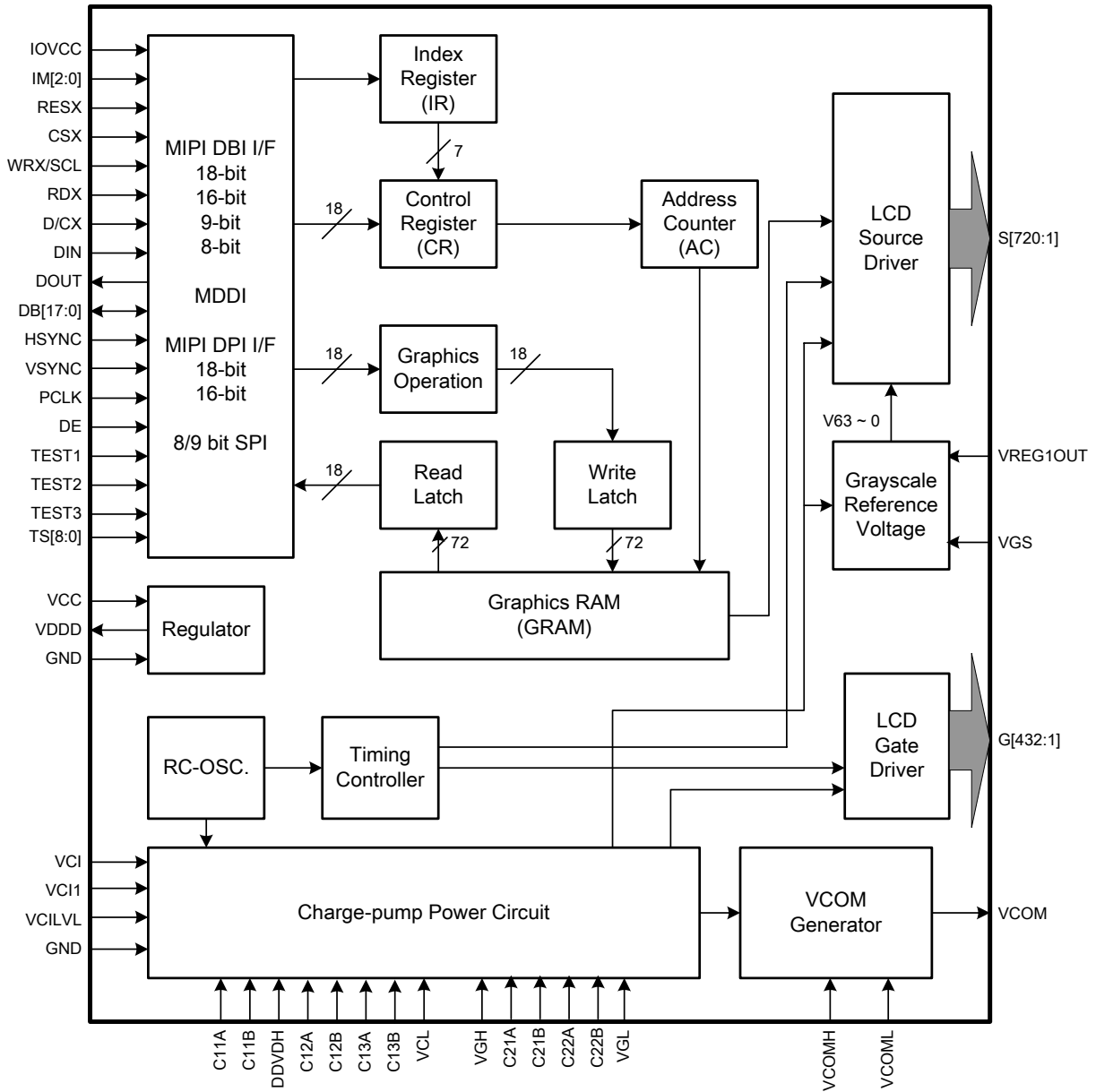
ILI9327 can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9327 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9327 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- ◆ Display resolution: [240xRGB](H) x 432(V)
- ◆ Output:
 - 720 source outputs
 - 432 gate outputs
 - Common electrode output
- ◆ a-TFT LCD driver with on-chip full display RAM: 233,280 bytes
- ◆ MCU Interface
 - MIPI DBI
 - Type B 16-/18- bit, 8-/9- bit
 - Type C 4-line 9bit (Option 1), 8bit (Option 3)
 - MIPI DPI
 - Type B 16-/18- bit
 - MIPI DCS command sets
 - MDDI high speed serial interface
- ◆ Display mode:
 - Full color mode: 262K-color
 - Separate RGB gamma
 - Reduced color mode: 8-colors (3-bits MSB bits mode)
- ◆ On chip functions:
 - VCOM generator and adjustment
 - Timing generator
 - Oscillator
 - DC/DC converter
 - Line/frame inversion
- ◆ MTP:
 - 7-bits for VCOM adjustment

- ◆ Low -power consumption architecture
 - Low operating power supplies:
 - IOVcc = 1.65V ~ 3.6V (interface I/O)
 - Vci = 2.5V ~ 3.6V (analog)
- ◆ LCD Voltage drive:
 - Source/VCOM power supply voltage
 - DDVDH - GND = 4.5V ~ 6.0V
 - VCL – GND = -2.0V ~ -3.0V
 - VCI - VCL \leq 6.0V
 - Gate driver output voltage
 - VGH - GND = 10V ~ 20V
 - VGL – GND = -5V ~ -15V
 - VGH - VGL \leq 30V
 - VCOM driver output voltage
 - VCOMH = 3.0V ~ (DDVDH-0.5)V
 - VCOML = (VCL+0.5)V ~ 0V
 - VCOMH - VCOML \leq 6.0V
- ◆ Operate temperature range: -40°C to 85°C

3. Block Diagram



4. Pin Descriptions

Pin Name	I/O	Descriptions																																																						
IM[2:0]	I (IOVCC)	Select the MPU system interface mode																																																						
		<table border="1"> <thead> <tr> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>MPU-Interface Mode</th> <th>DB Pin in use</th> <th>Colors</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>DBI Type B 18-bit</td> <td>DB[17:0]</td> <td>262K</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>DBI Type B 9-bit</td> <td>DB[8:0]</td> <td>262K</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>DBI Type B 16-bit</td> <td>DB[15:0]</td> <td>65K/262K</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>DBI Type B 8-bit</td> <td>DB[7:0]</td> <td>65K/262K</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>MDDI</td> <td>-</td> <td>65K/262K</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>DBI Type C 9-bit</td> <td>DIN, DOUT</td> <td>8/262K</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>CPU 9-bit</td> <td>DB[8:0]/DB[8:1]</td> <td>262K</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>DBI Type C 8-bit</td> <td>DIN, DOUT</td> <td>8/262K</td> </tr> </tbody> </table>	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use	Colors	0	0	0	DBI Type B 18-bit	DB[17:0]	262K	0	0	1	DBI Type B 9-bit	DB[8:0]	262K	0	1	0	DBI Type B 16-bit	DB[15:0]	65K/262K	0	1	1	DBI Type B 8-bit	DB[7:0]	65K/262K	1	0	0	MDDI	-	65K/262K	1	0	1	DBI Type C 9-bit	DIN, DOUT	8/262K	1	1	0	CPU 9-bit	DB[8:0]/DB[8:1]	262K	1	1	1	DBI Type C 8-bit	DIN, DOUT	8/262K
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1	1	1	DBI Type C 8-bit	DIN, DOUT	8/262K																																																			
RESX	I (IOVCC)	This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active																																																						
CSX	I (IOVCC)	Chip select input pin ("Low" enable). When it is not used, please fix this pin at IOVCC.																																																						
D/CX	I (IOVCC)	Display data / Command selection pin D/CX='1': Display data. D/CX='0': Command data. If not used, please fix this pin at GND level.																																																						
RDX	I (IOVCC)	Read control pin for the DBI interface. If not used, please connect this pin to IOVCC.																																																						
WRX/SCL	I (IOVCC)	Write control pin for the DBI interface. When the DBI type C is selected, this pin is used as serial clock pin. If not used, please connect this pin to IOVCC.																																																						
DB[17:9]/S_DB[8:0]	I/O (IOVCC)	These pins are data bus. In MDDI operation, DB[17:9]/S_DB[8:0] can be assigned for the sub-display interface output. <i>In MDDI mode, these pins are output, If they are not used; please let these pins as open.</i> <i>In other mode, these pins are input, If they are not used; please fix these pins as GND.</i>																																																						
DB[8:0]	I/O (IOVCC)	These pins are data bus. If not used, please connect these pins to GND.																																																						
DIN/SDA	I/O (IOVCC)	Serial data input pin and used for the DBI type C mode. If not used, please connect this pin to ground.																																																						
DOUT	O (IOVCC)	Serial data output pin and used for the DBI type C mode.																																																						
TE	O (IOVCC)	Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, please open this pin.																																																						
PCLK	I (IOVCC)	Pixel clock signal in DPI interface mode. If not used, please fix this pin at GND level.																																																						
VSYNC (S_CS)	I (IOVCC)	Vertical sync. signal in DPI interface mode.																																																						

Pin Name	I/O	Descriptions
		In MDDI operation, VSYNC is assigned for the sub-display interface output (S_CS) <i>In MDDI mode, this is an output pin, If it's not used; please let this pin as open.</i> <i>In other mode, this is an input pin, If it's not used; please fix this pin as GND.</i>
HSYNC (S_RS)	I (IOVCC)	Horizontal sync. signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_RS) <i>In MDDI mode, this is an output pin, If it's not used; please let this pin as open.</i> <i>In other mode, this is an input pin, If it's not used; please fix this pin as GND.</i>
DE (S_WR)	I (IOVCC)	Data enable signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_WR) <i>In MDDI mode, this is an output pin, If it's not used; please let this pin as open.</i> <i>In other mode, this is an input pin, If it's not used; please fix this pin as GND.</i>
Power Input Pins		
IOVCC	P	Power supply to interface pins Connect to external power supply (IOVCC= 1.65~3.6V).
Vci	P	Power supply to liquid crystal power supply analog circuit. Connect to external power supply (Vci=2.5~3.6V).
VciLVL	P	VREG1OUT reference voltage. Please connect this pin to a stable voltage.
VCC	P	Power supply Connect to external power supply (VCC=2.5~3.6V).
DGND AGND	P	Power ground pin. Make sure AGND = DGND = 0V.
LCD signals Pins		
S1 ~ S720	O	Source driver output pins.
G1 ~ G432	O	Gate driver output pins.
VDD	O	Internal logic regulator output. Used as internal logic power supply. Connect to stabilizing capacitor.
VC11	P	Reference voltage for the step-up circuit 1. Set VC11 level so that DDVDH, VGH and VGL are within the ratings.
DDVDH	P	Power supply for the source driver and VCOM.
VGH	P	Power supply to drive liquid crystal.
VGL	P	Power supply for LCD drive.
VCL	P	Power supply to drive VCOML.
C11A, C11B, C12A, C12B	P	Make sure to connect to capacitor that is used in internal step-up circuit 1.
C13A, C13B, C21A, C21B, C22A, C22B,	P	Make sure to connect to capacitor that is used in internal step-up circuit 2. Connect to capacitors according to the step-up factors in use.

Pin Name	I/O	Descriptions
VREG1OUT	P	Outputs voltage level generated from VRH VCILVL. The step-up factor applied to VRH VCILVL is set by VRH bits. Used as source driver grayscale reference voltage VREG1OUT, reference voltage to VCOMH, and Vcom amplitude reference voltage. Connect to stabilizing capacitor when in use. $VREG1OUT=4.0\sim(DDVDH-0.2)[V]$
VCOM	P	TFT display common electrode power supply. Alternates between voltage levels between VCOMH-VCOML. Registers set the alternating cycle. Registers set the alternating cycle and operate or halt VCOM.
VCOMH	P	VCOM high level. Adjust the voltage by internal electronic volume (VCM)
VCOML	P	VCOM low level. Adjust the voltage by VDV bits. $VCOML=(VCL+0.5)\sim 0[V]$
VGS	I	Reference level for grayscale generating circuit.
LED Driver pins		
LEDPWM	O (VCC)	Control signal for brightness of LED backlight. PWM signal's width is selected from 256 values between 0% (Low) and 100% (High). The amplitude of LEDPWM signal is VCC-DGND. If this pin is not used, please open this pin.
LEDON	O (VCC)	This pin is connected to external LED driver. It's a LED driver control pin which is used for turning ON/OFF of LED backlight. The amplitude of LEDPWM signal is VCC-DGND. If this pin is not used, please open this pin.
TEST pins		
TS[8:0]	-	Test pins These pins are internal pulled low. Please leave these pins as open.
TESTO[16:1]	O	Test pins These pins are internal pulled low. Please leave these pins as open.
TEST1-5	I/O	Test pins These pins are internal pulled low. Please leave these pins as open.
TEST_EN	I	Test pins (Internal pull low) Please leave these pins as open.
GNDDUM IOVCCDUM	-	The ground voltage level output. Pins to fix the electrical potentials of unused interface and test pins.
DUMMYR1~2	-	DUMMYR1 and DUMMYR4, DUMMYR2 and DUMMYR3 are short together within the chip
DUMMY	-	Dummy Pins These pins are floating.
VGLDMY1~4	O	VGL dummy pin These pins are VGL output pin. Please leave these pins as open.

Liquid crystal power supply specifications Table

No.	Item	Description	
1	TFT Source Driver	720 pins (240x RGB)	
2	TFT Gate Driver	432 pins	
3	TFT Display's Capacitor Structure	Cst structure only (Common VCOM)	
4	Liquid Crystal Drive Output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G432	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	IOVcc	1.65 ~ 3.6V
		Vci	2.50 ~ 3.6V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.0V
		VGH	10V ~ 18V
		VGL	-5V ~ -15V
		VCL	-1.0V ~ -3.0V
		VGH - VGL	Max. 30V
		Vci - VCL	Max. 6.0V
7	Internal Step-up Circuits	DDVDH	Vci1 x2
		VGH	Vci1 x4, x5, x6
		VGL	Vci1 x-3, x-4, x-5
		VCL	Vci1 x-1

5. Pad Arrangement and Coordination

Chip Size: 19030um x 840 um

Chip thickness : 280um (typ.)

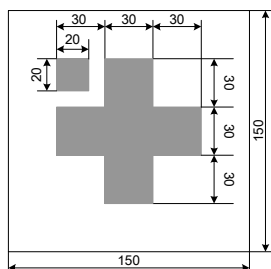
Pad Location: Pad Center.

Au bump height: 12um (typ.)

Au Bump Size:

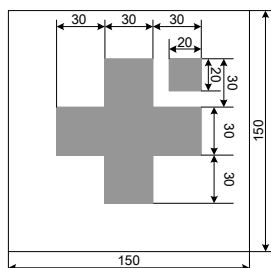
1. 15um x 100um
Gate: G1 ~ G432
Source: S1 ~ S720
2. 50um x 90um
Input Pads
Pad 1 to 262.

Alignment Marks



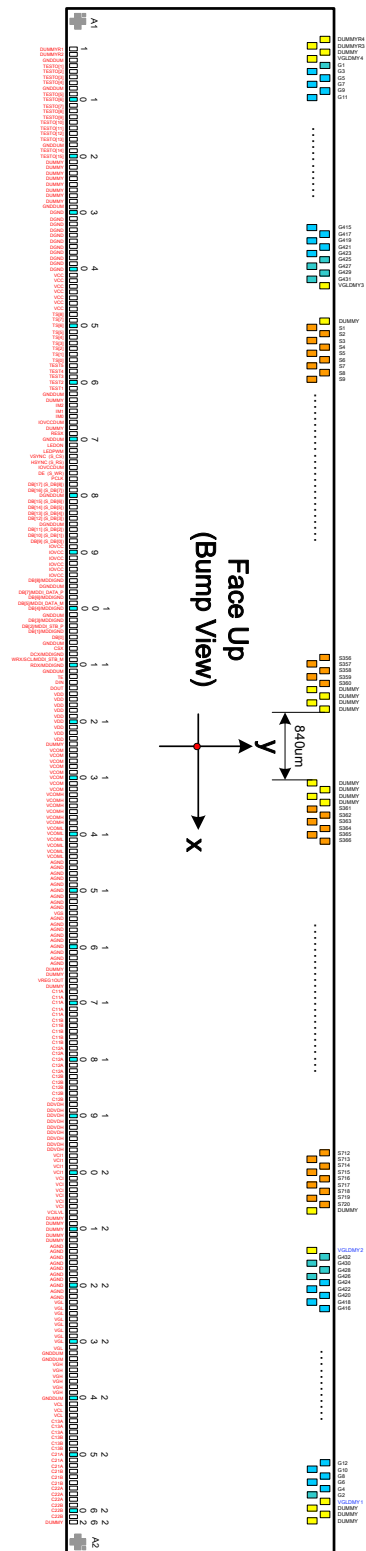
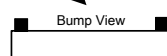
Alignment Mark: A1

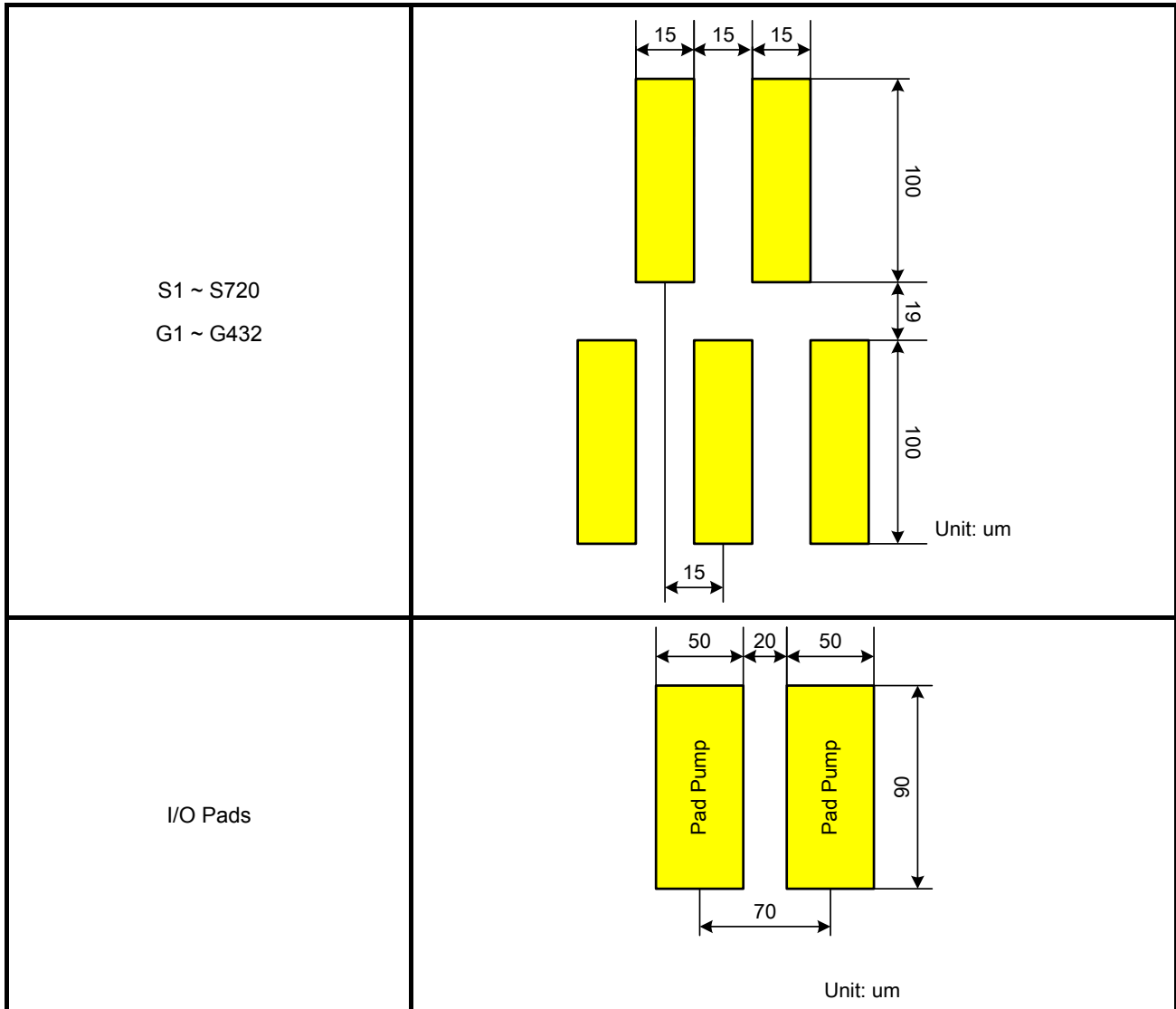
Coordination (-9381.0, -217)



Alignment Mark: A2

Coordination (9381.0, -217)





6. Block Function Description

Interface

ILI9327 supports MIPI DBI Type B (18/16/9/8bit) and MIPI DBI Type C (Option 1, 3). The interface is selected by setting IM[2:0] pin.

IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use	Colors
0	0	0	DBI Type B 18-bit	DB[17:0]	262K
0	0	1	DBI Type B 9-bit	DB[8:0]	262K
0	1	0	DBI Type B 16-bit	DB[15:0]	65K/262K
0	1	1	DBI Type B 8-bit	DB[7:0]	65K/262K
1	0	0	MDDI		65K/262K
1	0	1	DBI Type C 9-bit	DIN, DOUT	8/262K
1	1	0	CPU 9-bit	DB[8:0]/DB[8:1]	262K
1	1	1	DBI Type C 8-bit	DIN, DOUT	8/262K

Note: Set number of colors using set_pixel_format: 3Ah.

(a) MIPI DBI Type B (18-/ 16-/ 9-/ 8- bit)

ILI9327 supports MIPI DBI Type B (18/16/9/8bit) that uses command method which has 8-bit command register and 8-bit parameter registers. The ILI9327 also has the 18-bit write register (WDR) and read register (RDR). The WDR register is used to store data temporarily that is automatically written to the internal frame memory through internal operation of the chip.

The RDR is used to temporarily store the data read out from the frame memory. When reading data from the frame memory, the ILI9327 first stores the data in the RDR. For this reason, invalid data is sent to the data bus at first time read and valid data is sent as the ILI9327 reads second and subsequent data from the frame memory.

Register selection			Operation
DCX	RDX	WRX	
0	1	↑	Command
1	↑	1	Read parameter
1	1	↑	Write parameter

(b) MIPI DBI Type C (Option 1, 3)

The ILI9327 also supports MIPI DBI type C 9bit (Option 1) and 8bit (Option 3) serial interface that uses signals CSX, DCX, SCL, DIN and DOUT.

(c) Video Image Interface (TE-signal, DPI, VSYNC-I/F)

ILI9327 supports TE, DPI and VSYNC interfaces as external display interface for video image. When DBI is

selected, display data is written in synchronization with TE signal which is generated from internal clock to prevent tearing effect on the panel.

When DPI is selected, externally supplied VSYNC, HSYNC and PCLK signals drive the chip. Display data (DB[17:0]) is written in synchronization with those synchronous signals following data enable signal (DE). This enables updating image data without tearing effect on the panel.

Address Counter (AC)

Address counter (AC) gives address to GRAM. When command setting address is written to CDR, the data is transferred from CDR to AC.

When data is written/read to/from GRAM, address counter (AC) will increment by +1 or -1 automatically. ILI9327 writes data to only rectangular area that was specified by GRAM.

Graphic RAM (GRAM)

The graphic RAM (GRAM) stores 233,280 bytes pattern data using 18 bits for one pixel, enabling a maximum 240RGB x 432 dot graphic display at the maximum.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. The ILI9327 displays 262,144 colors at the maximum.

Power Supply Circuit

The power supply circuit generates supply voltages to a-TFT panel, VREG1OUT, VGH, VGL, VCOMH and VCOML.

Timing Generating

Timing generator is used to generate the timing signals for internal circuits such as the internal GRAM read/write, display control signals. The timing for display operation such as RAM read operation and the timing for internal operation such as RAM access by MPU is output separately so that they do not interfere with each other.

Oscillator

ILI9327 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

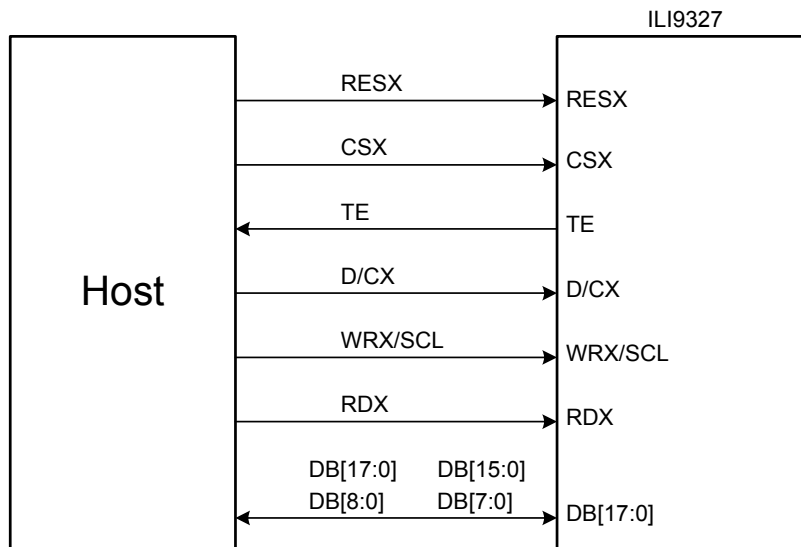
The liquid crystal display driver circuit consists of 720 source drivers (S1~S720). Display pattern data is latched when 720 pixels data is input. This latched data controls source drivers and outputs drive waveform. The gate driver consists of 432 gate drivers (G1~G432) and outputs either VGH or VGL level. The shift direction of gate driver is set by GS bit. Scan direction of gate driver can also be set by the SM bit to fit the panel gate line layout.

7. Interface Description

7.1. Display Bus Interface (DBI)

ILI9327 uses a 22-wires 18-bit parallel interface. The chip-select CSX (active low) enables and disables the DBI interface. RESX (active low) is an external reset signal. WRX is the data write, RDX is the data read and D[17:0] is parallel DBI data. The four 18/16/9/8-bit types interface is supported for the display data transfer.

The graphics controller chip reads the data at the rising edge of RDX signal. The D/CX is data/command flag. When D/CX = "1", D17 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.



DBI Type B Interface

18-bit data bus DB[17:0] interface, IM[2:0] = 000

	Set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

16-bit data bus DB[15:0] interface, IM[2:0] = 010

	Set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*																
Command/Parameter Read	*	*																

	Set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	*	*	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]	b[3]	b[2]	b[1]	b[0]
16bpp Frame Memory Read	*	*	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]	b[3]	b[2]	b[1]	b[0]

	Set_pixel_format	DFM	First Transfer				Second Transfer				Third Transfer			
			DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]
18bpp Frame Memory Write	*	0	r1[5:0]		g1[5:0]		b1[5:0]		r2[5:0]		g2[5:0]		b2[5:0]	
	*	1	r1[5:0]		g1[5:0]		b1[5:0]		r1[5:0]		g1[5:0]		b1[5:0]	

	Set_pixel_format	DFM	First Transfer				Second Transfer				Third Transfer			
			DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]
18bpp Frame Memory Read	*	0	r1[5:0]		g1[5:0]		b1[5:0]		r2[5:0]		g2[5:0]		b2[5:0]	
	*	1	r1[5:0]		g1[5:0]		b1[5:0]		r1[5:0]		g1[5:0]		b1[5:0]	

9-bit data bus DB[8:0] interface, IM[2:0] = 001

	Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*									
Command/Parameter Read	*	*									

	Set_pixel_format	DFM	First Transfer				Second Transfer													
			DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]
18 bpp Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

9-bit data bus DB[8:0] interface, IM[2:0] = 110

	Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*									
Command/Parameter Read	*	*									

	Set_pixel_format	DFM	First Transfer				Second Transfer													
			DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

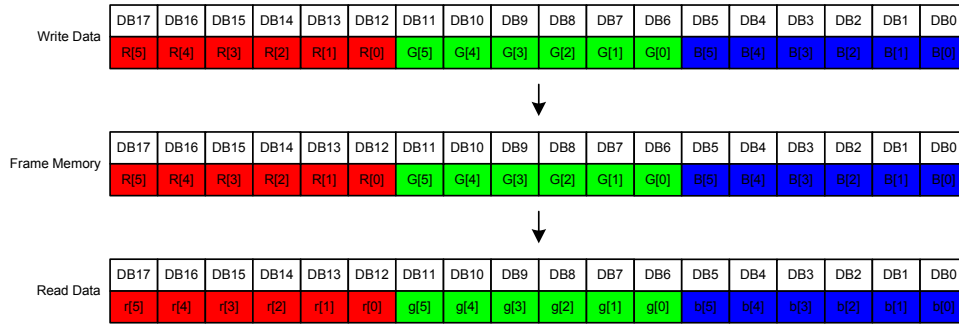
8-bit data bus DB[7:0] interface, IM[2:0] = 011

	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*								
Command/Parameter Read	*	*								

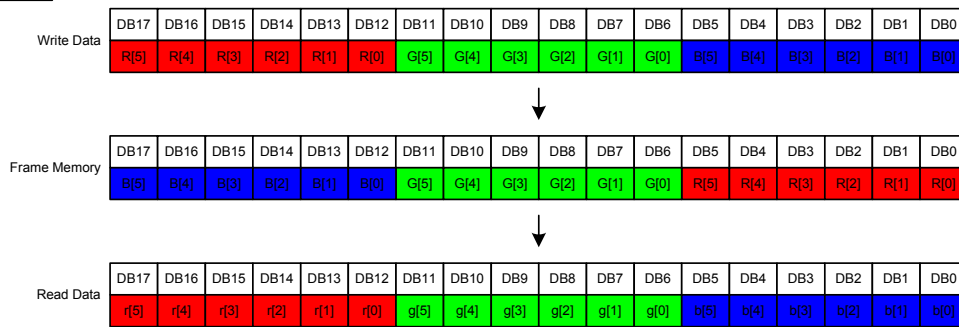
	Set_pixel_format	DFM	First Transfer				Second Transfer											
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	*	*	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]	b[3]	b[2]	b[1]	b[0]
16bpp Frame Memory Read	*	*	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]	b[3]	b[2]	b[1]	b[0]

	Set_pixel_format	DFM	First Transfer				Second Transfer				Third Transfer														
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	
18bpp Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	

BGR=0



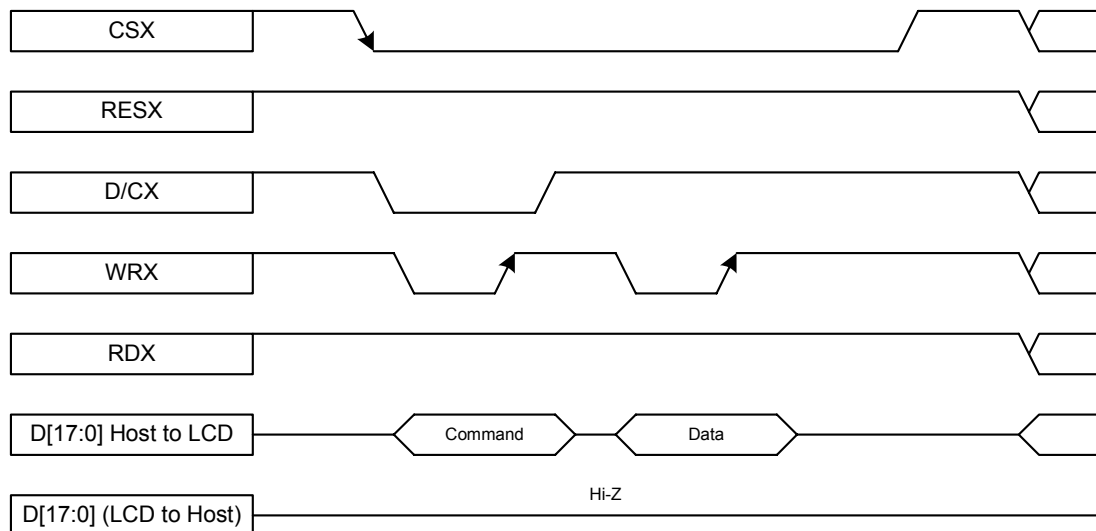
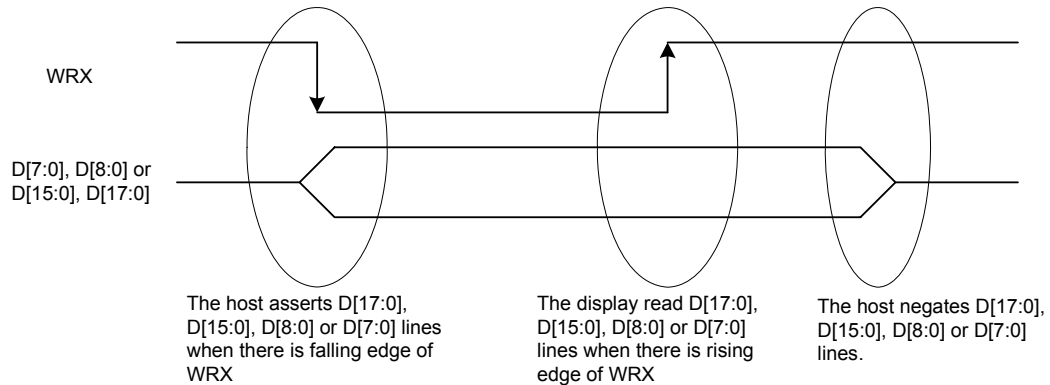
BGR=1



7.1.1. Write Cycle

During a write cycle the host processor sends data to the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]), sixteen (D[15:0]) or eighteen (D[17:0]) information signals. WRX is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of WRX. D/CX is driven low while command information is on the interface and is pulled high when data is present.

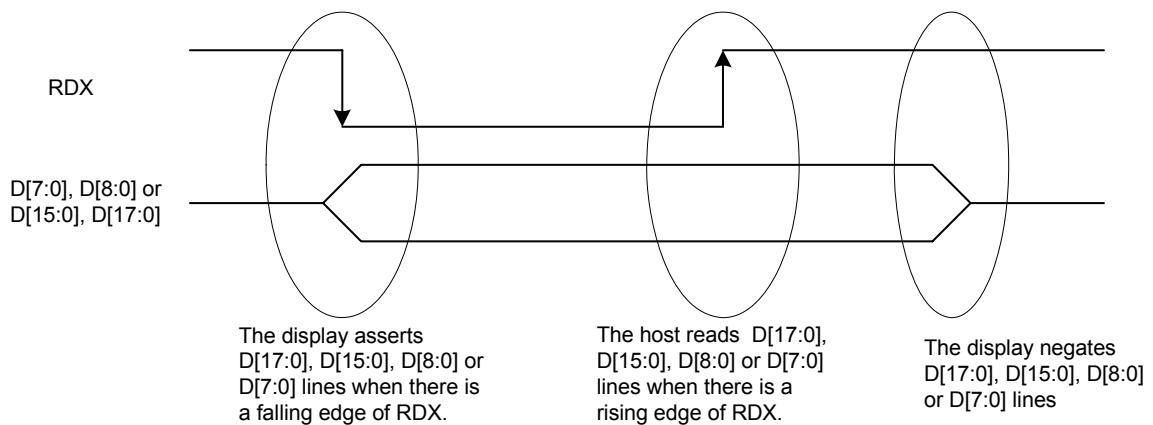
The following figure shows a write cycle for the type B interface.



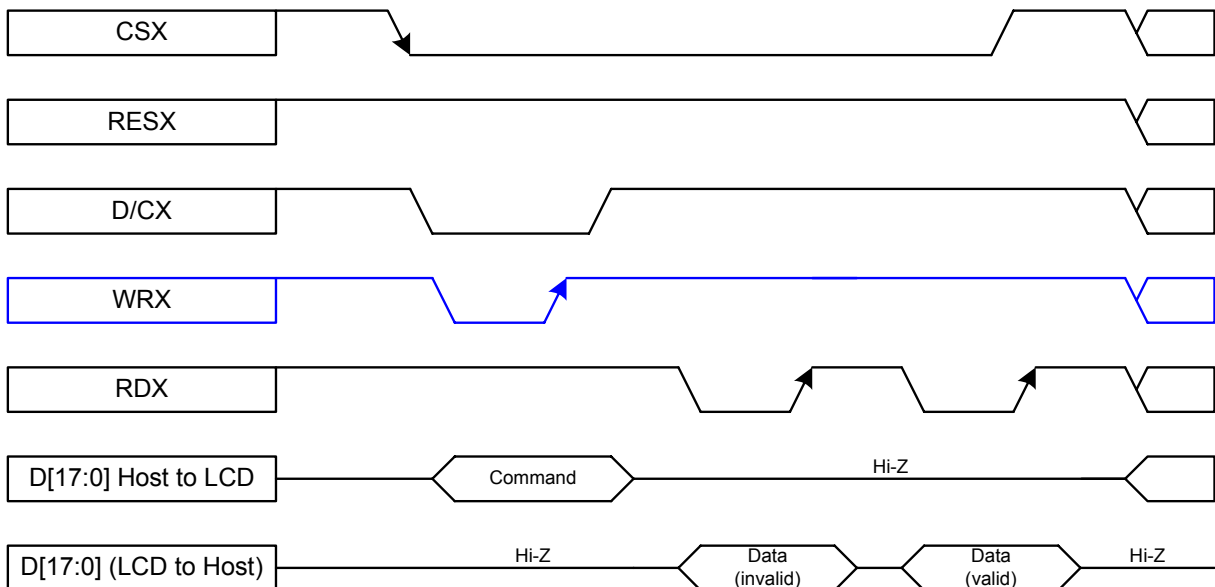
7.1.2. Read Cycle

During a read cycle the host processor reads data from the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]), sixteen (D[15:0]) or eighteen (D[17:0]) information signals. RDX is driven from high to low then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX. D/CX is driven high during the read cycle.

The following figure shows the read cycle for the type B interface.



Note: RDX is an unsynchronized signal (It can be stopped).



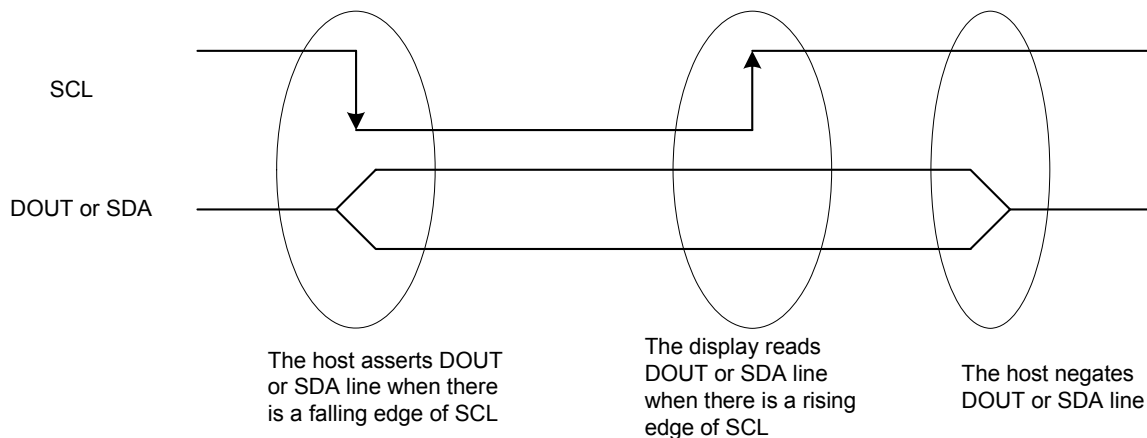
Note: Read Data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.2. Serial Interface (Type C)

7.2.1. Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The Type C interface utilizes CSX, SCL and SDA or DOUT signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

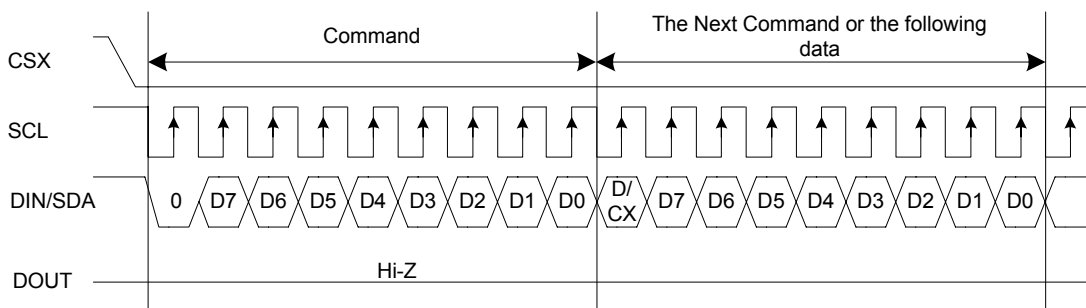
The following figure shows the write cycle for the type C interface.



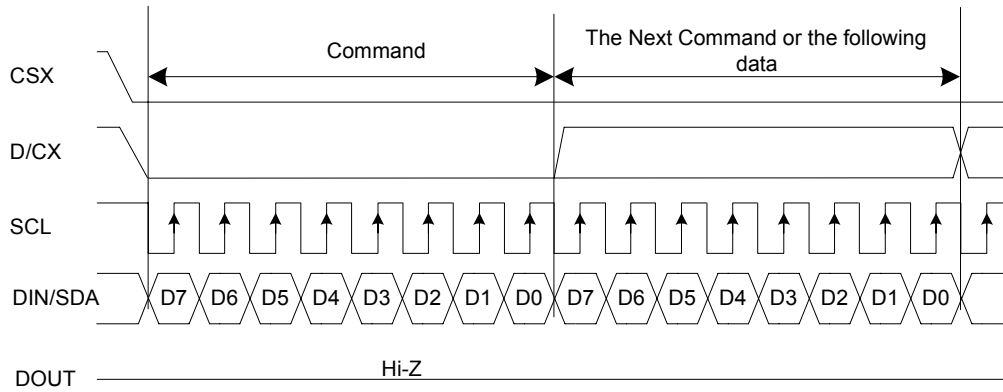
Note: SCL is an unsynchronized signal; it can be stopped.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight write cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The type C interface write sequences are described in the following Figure



DBI Type C Interface Write Sequence – Option 1



DBI Type C Interface Write Sequence - Option 3

Note:

1. D7 is MSB and D0 is LSB of byte.
2. When the Interface control register (C6h) SDA_EN is set as '1', the DIN/SDA pin is bi-direction and DOUT pin is not used.
3. When the Interface control register (C6h) SDA_EN is set as '0', the DIN/SDA pin is uni-direction and DIN and DOUT pins are used for data write and read.

DBI Type C Interface IM[2:0]=101/111

	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3bpp Frame Memory Write	3'h1	0			R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]			R3[0]	G3[0]	B3[0]	R4[0]	G4[0]	B4[0]			R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
18bpp Frame Memory Read	3'h6	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

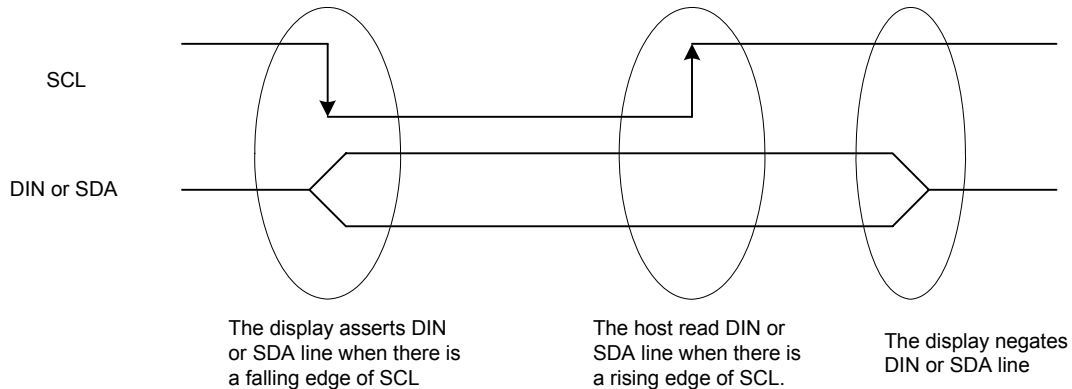
3/16-bit data extend to 18-bit

Set_pixel_format	EPF[1:0]	Frame Memory Data (18bpp)																	
		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
3bpp	*	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	G[0]	G[0]	G[0]	G[0]	G[0]	G[0]	B[0]	B[0]	B[0]	B[0]	B[0]	B[0]

7.2.2. Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The Type C interface utilizes CSX, SCL and DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL. D/CX is driven during the read cycle if it is used in option 3.

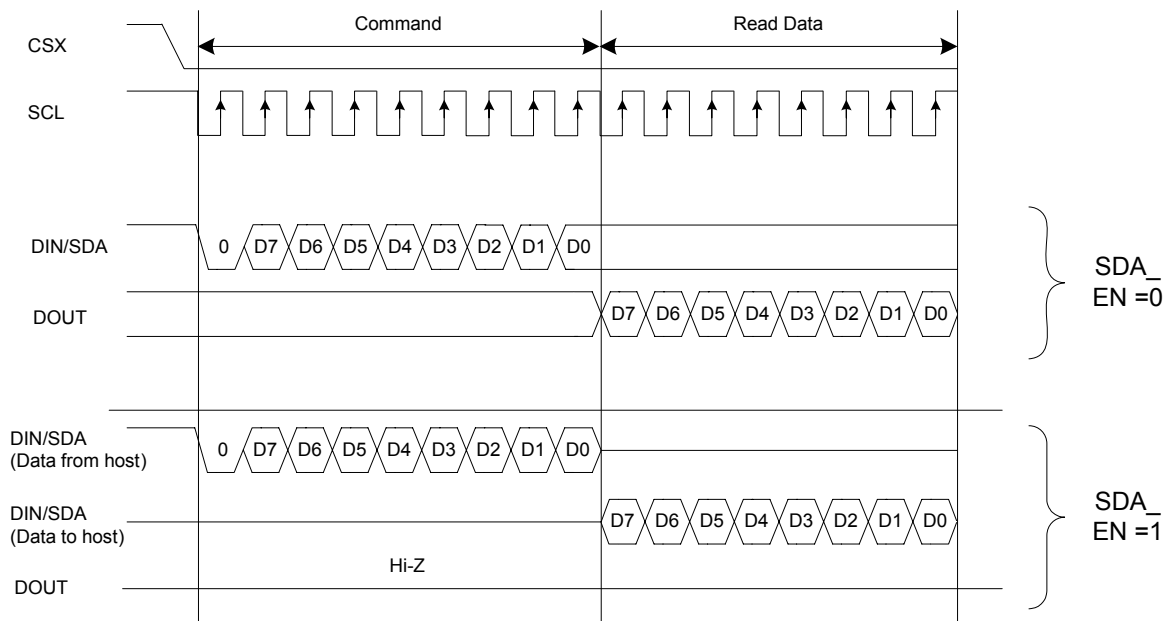
The following figure shows the read cycle for the type C interface.



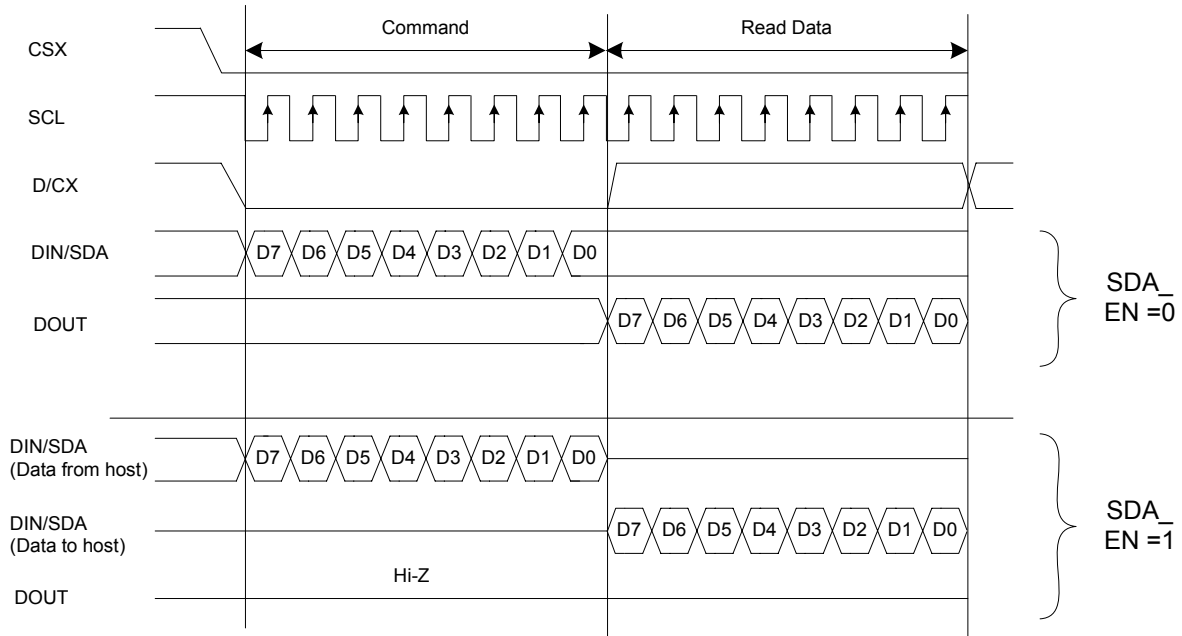
Note: SCL is an unsynchronized signal; it can be stopped.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight read cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The type C interface read sequences are shown in the following figures



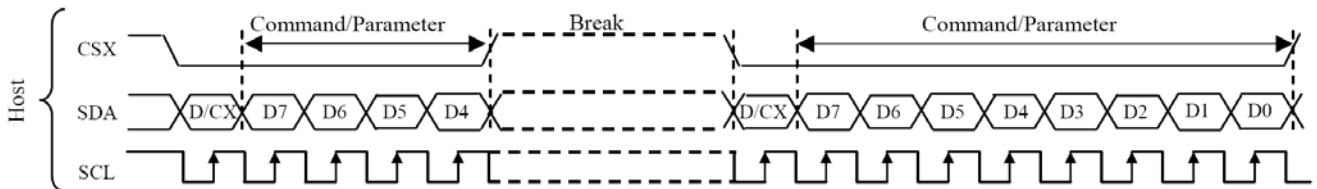
Note: D7 is MSB and D0 is LSB of byte.



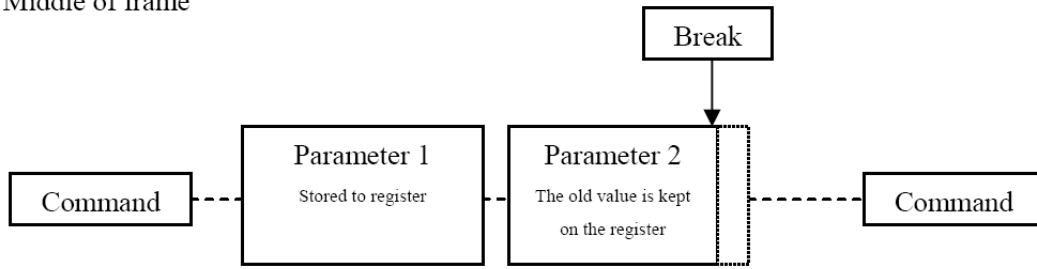
7.2.3. Break and Pause Sequences

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

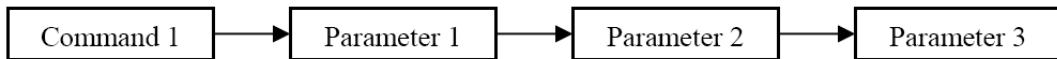


1. Middle of frame

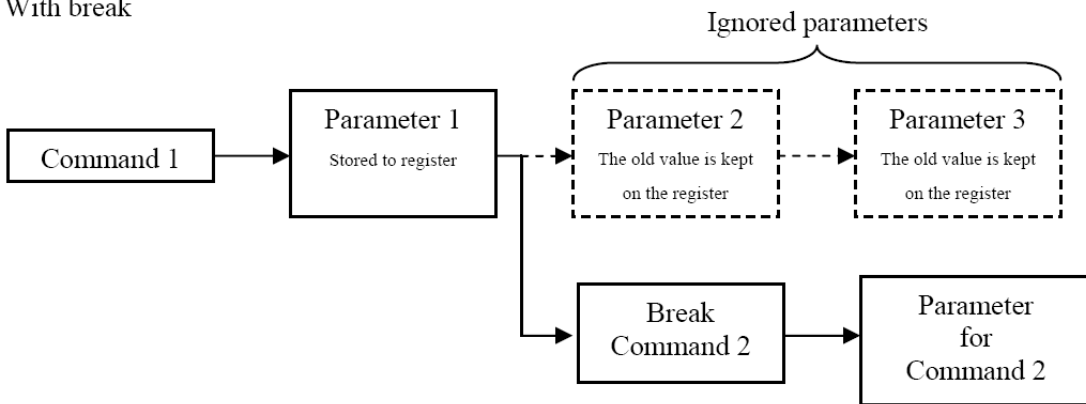


2. Between frames

Without break



With break



Break can be e.g. another command or noise pulse.

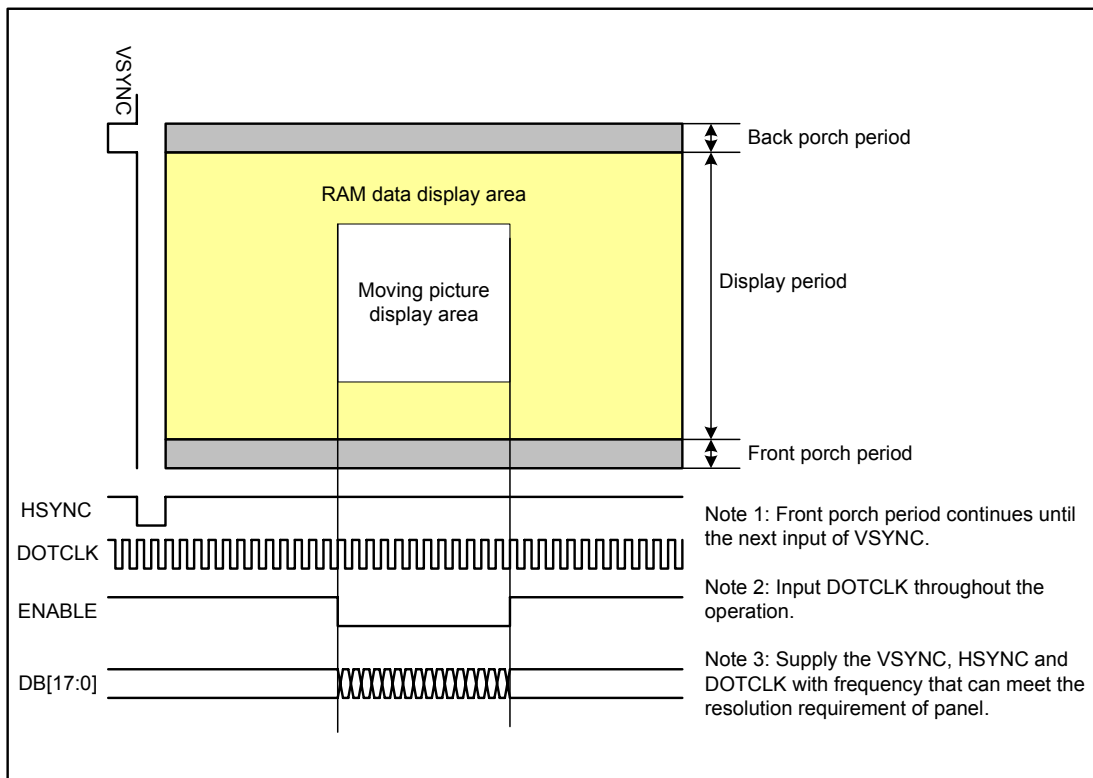
7.3. Display Pixel Interface (DPI)

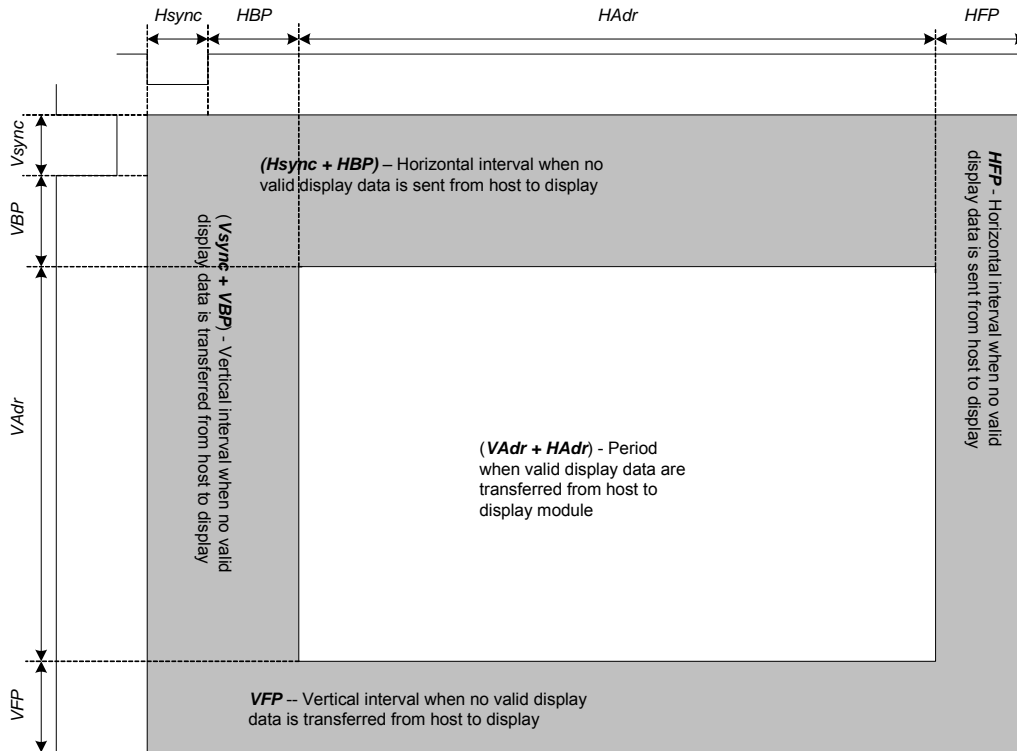
In normal operation, systems based on DPI architecture rely on the host processor to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts. The displayed image, or frame, is comprised of a rectangular array of pixels. The frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync indicates the beginning of each frame of the displayed image.

Hsync signals the beginning of each horizontal line of pixels.

Each pixel value (16 or 18-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.



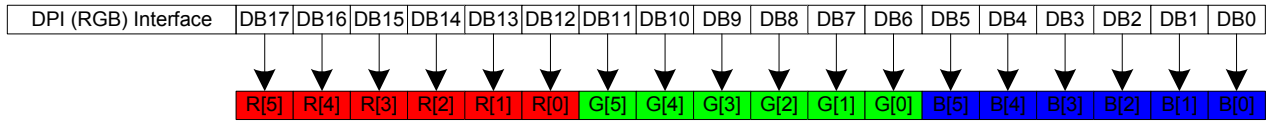


Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
PCLK Cycle	PCLK _{CYC}		-	88	-	ns
Horizontal Synchronization	Hsync		-	10	-	PCLK
Horizontal Back Porch	HBP		-	20	-	PCLK
Horizontal Address	HAdr		-	320	-	PCLK
Horizontal Front Porch	HFP		-	10	-	PCLK
Vertical Synchronization	Vsync		-	2	-	Line
Vertical Back Porch	VBP		-	2	-	Line
Vertical Address	VAdr		-	432	-	Line
Vertical Front Porch	VFP		-	4	-	Line
Vsync setup time	VSST				-	Hz
Vsync hold time	VSHT				-	Hz
Hsync setup time	HSST				-	Hz
Hsync hold time	HSHT				-	Hz
Data setup time	DST				-	Hz
Data hold time	DHT				-	Hz
Vertical Frequency(*)				60	-	Hz
Horizontal Frequency(*)			-	29.282	-	KHz
PCLK Frequency(*)			-	11.42Mhz	TBD	MHz

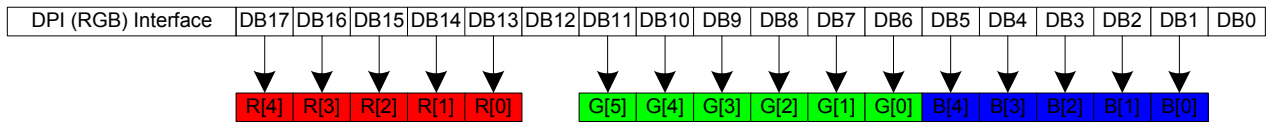
Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

18bit DPI Interface Connection: set_pixel_format D[6:4]=3'h6 : 18bpp



16bit DPI Interface Connection: set_pixel_format D[6:4]=3'h5 : 16bpp



7.4. Mobile Display Digital Interface (MDDI)

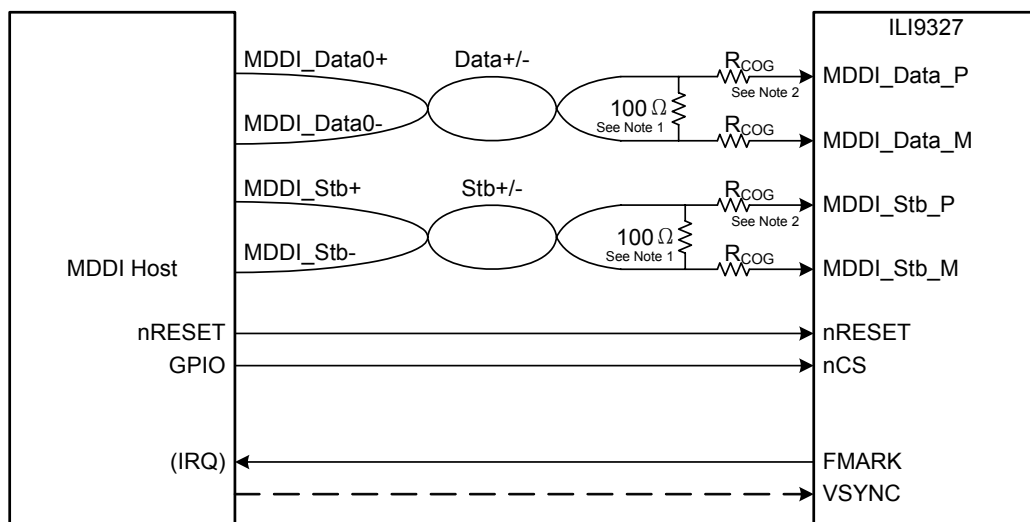
MDDI (Mobile display digital interface) is a differential small amplitude serial interface for high-speed data transfer via following 4 lines: Stb+/- (MDDI_STBP_B, MDDI_STB_M_B), Data+/- (MDDI_DATA_P_B, MDDI_DATA_M_B).

The specifications of MDDI supported by the ILI9327 are compatible to the MDDI specifications disclosed by VESA, Video Electronics Standards Association. The following are the specifications particular to the ILI9327's MDDI.

ILI9327 MDDI Specifications

- MDDI Type-I
- High-speed, differential, small-amplitude data transfer via Stb+/-, Data+/- lines
- MDDI client: the ILI9327 enables direct connection to the base band (BB) chip without bridge chip
- Cost-performance optimized interface for mobile display systems
 1. Only internal mode (one client) and Forward Link are supported
 2. Hibernation mode to save power consumption
 3. Tearing-free moving picture display via FMARK/VSYNC interface
 4. Moving picture display with low power consumption, realized by the features 2 ~ 3
 5. Shutdown mode for saving power consumption in the standby state

Incorporates an output port for sub-display interface or peripheral control providing single-chip solution for MDDI mobile display systems



Notes:

1. An external end resistor of 100 ohm is necessary between Data+ and Data- lines
2. Make the COG wiring resistances of Data+/-, Stb+/- lines as small as possible ($R_{COG} < 10$ ohm).
3. The max transmission rate is 130 Mbps!

MDDI Link Protocol (Packets Supported by the ILI9327)

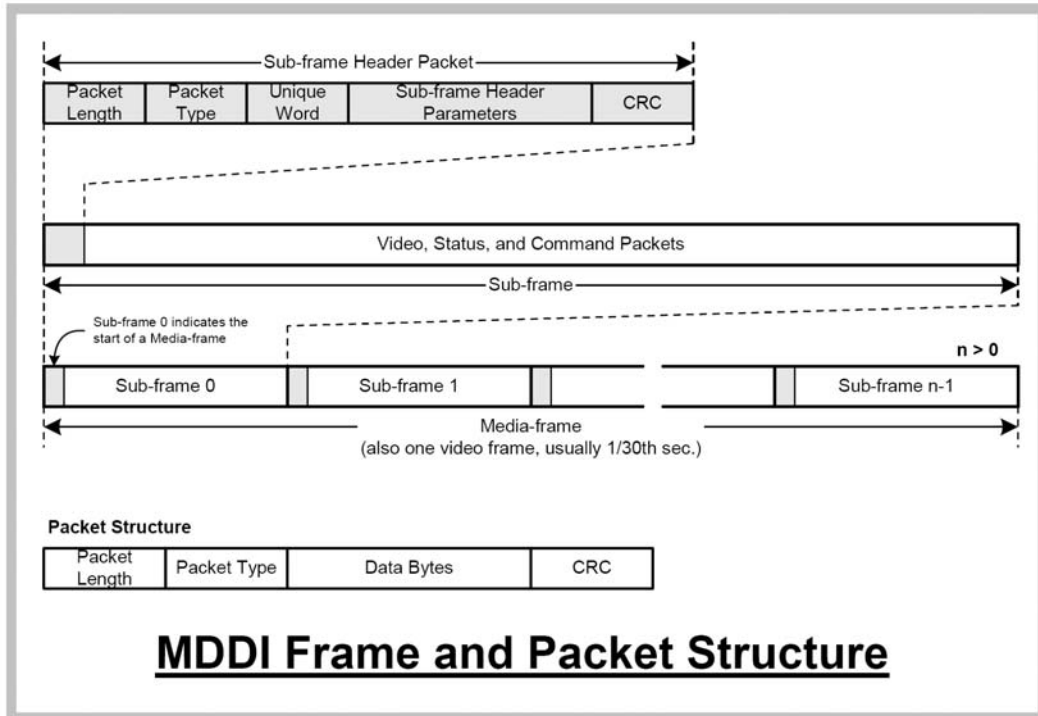
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The MDDI Link Protocol of the ILI9327 is in line with the MDDI specifications disclosed by VESA. See the MDDI specifications by VESA for details on the MDDI Link Protocol.

The MDDI packets supported by the ILI9327 are as follows. Do not send packets not supported by the ILI9327 in the system incorporating the ILI9327.

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame and some sub-frame construct media-frame together. The following table describes 9 types of packet which is supported in ILI9327.

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward



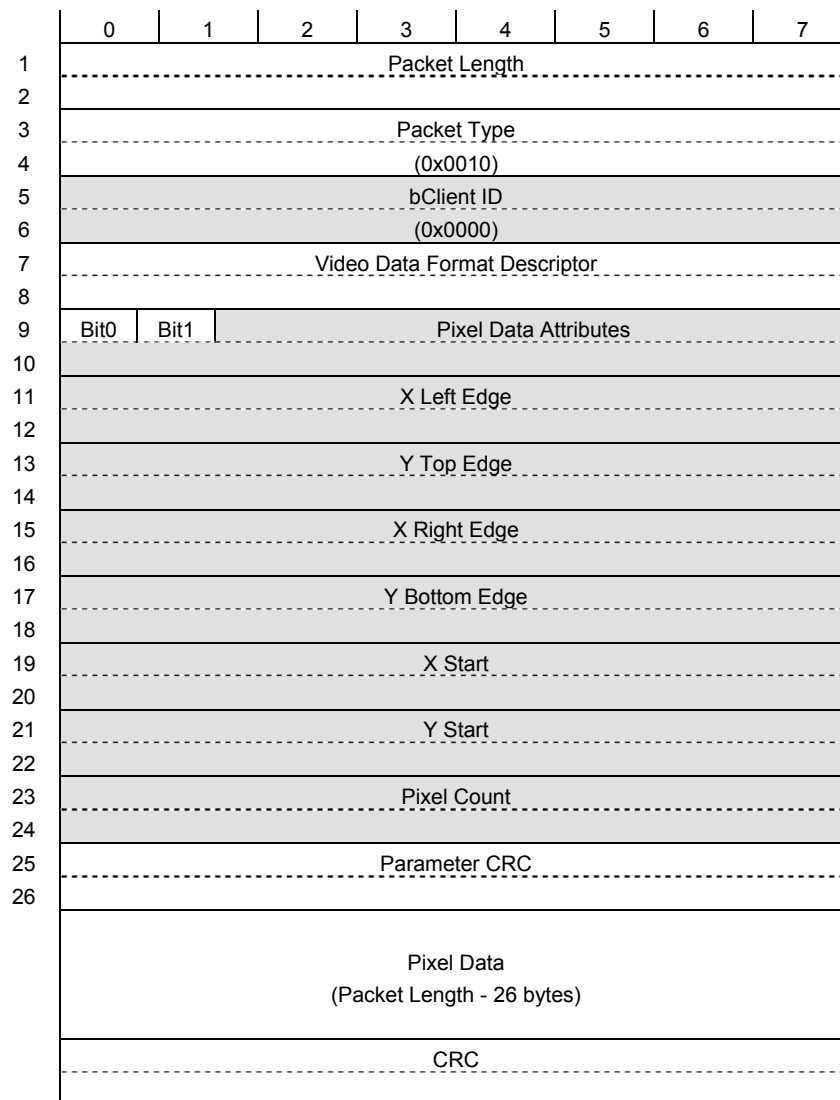
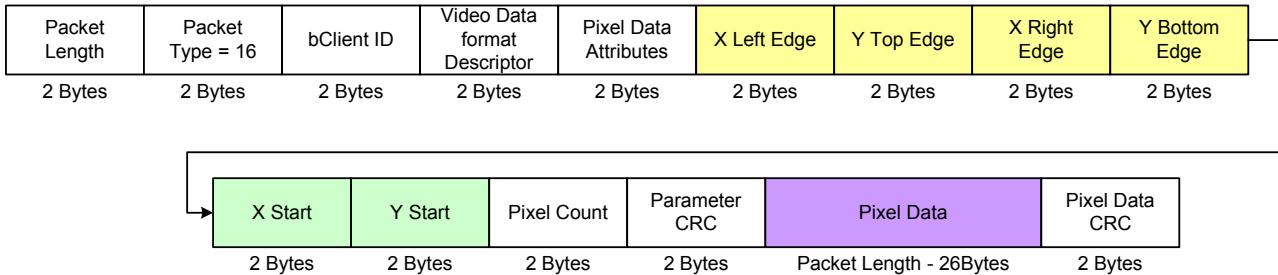
Sub-Frame Header Packet

	0	1	2	3	4	5	6	7
1	Packet Length							
2	(0x0014)							
3	Packet Type							
4	(0x3bFF)							
5	Unique Word							
6	(0x005A)							
7	Reserved 1							
8	(0x0000)							
9	Sub-Frame Length							
10								
11								
12								
13	Protocol Version							
14	(0x0000)							
15	Sub-frame Count							
16								
17	Media-frame Count							
18								
19								
20								
21	CRC							
22	(0x0000)							

Bytes ↓

Video Stream Packet

The ILI9327 writes image data to RAM via Video Stream Packet. The window and RAM addresses are set via Register Access Packet.



Note: The parameters colored in gray are not supported by the ILI9327.

Video Data Format Descriptor: sets the pixel data format. The ILI9327 supports only the following format. Set the same pixel format (bpp) as selected by DSS[1:0] in Video Data Format Descriptor.

[15:13]	[12]	[11:8]	[7:4]	[3:0]	
010	1	0x5	0x6	0x5	Packed 16bpp RGB format (R:G:B=5:6:5)
010	1	0x6	0x6	0x6	Packed 18bpp RGB format (R:G:B=6:6:6)
Others					Setting disabled

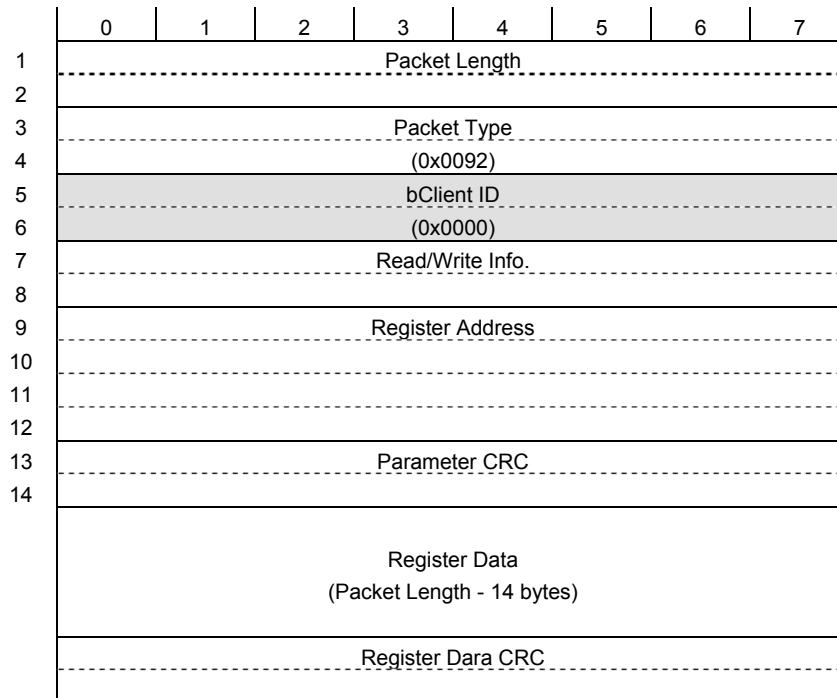
	MDDI Bytes n								MDDI Bytes (n+1)								MDDI Bytes (n+2)							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Packet 16bpp	0	1	2	3	4	0	1	2	3	4	5	0	1	2	3	4	0	1	2	3	4	0	1	2
	Pixel 1 Blue				Pixel 1 Green				Pixel 1 Red				Pixel 2 Blue				Pixel 2							
Packet 18bpp	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5
	Pixel 2 Blue				Pixel 2 Green				Pixel 2 Red				Pixel 2 Blue											

Pixel Data Attributes: the image data sent via Video Stream Packet is recognized as either the data for the main-panel or for the sub-panel according to the setting in [1:0] bits in this field.

Pixel Data Attributes	Bits[1:0]	Description
0x0000	00	The Video Stream Packet data is recognized as the sub-panel data. The Video Stream Packet data is outputted via sub-display interface and not written in the ILI9327.
0x0001	01	Setting disabled
0x0002	10	Setting disabled
0x0003	11	The Video Stream Packet data is recognized as the data written in the ILI9327. The Video Stream Packet data is written in the ILI9327 and not outputted via sub-display interface.
Others		

Register Access Packet

Register Access Packet is used when setting instruction to the ILI9327.



Note: The parameters colored in gray are not supported by the ILI9327.

Read/Write Info: Read or Write information in register access. The ILI9327 supports the following access setting.

Bits[15:14]	Bits[13:00]	Description
2'b00	0xn	Write one register by register access packet
2'b10	0xn	Read one register by register access packet
others		Setting disabled

Register Address: The index of the register to be accessed is set in Register Address area and the Register Address Packet is directed to the ILI9327 or the sub display is determined by the setting in Register Address area.

Bits[31:16]	Description
16'h0000	The Register Access Packet is directed to the ILI9327 via main-display interface.
16'h0001	The Register Access Packet is directed to the sub display via sub-display interface.
16'h0002 ~ 16'h7FFF	Setting disabled

Bits[15:0]	Description
16'h0000~FFFF	Bits [15:0] are used as index [15:0].

Register Data: The data for register access is written in Register Data. The length of Register Data will depends on the parameter length of command.

Example of Register Access Packet (e.g. write to the ILI9327)

	0	1	2	3	4	5	6	7
1	Packet Length					(0x12)		
2	(0x00)							
3	Packet Type					(0x92)		
4	(0x00)							
5	bClient ID					(0x00)		
6	(0x00)							
7	Read/Write Info.					(0x01)		
8	(0x00)							
9	Register Address					(index ID[7:0])		
10	(index ID[15:8])							
11						(0x00) → Main Panel (ILI9327)		
12						(0x01) → Sub panel		
13	(0x00)							
14	Parameter CRC							
15	Register Data List (Various Length)					1 st Parameter		
16	2 nd Parameter							
17	3 rd Parameter							
18	0x00							
19	Parameter CRC							
20								

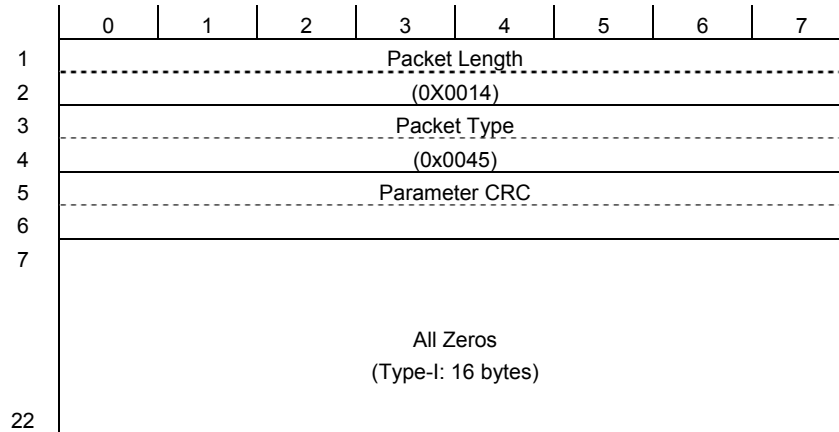
Note: The parameters colored in gray are not supported by the ILI9327.

Register Access Packet Restrictions

The ILI9327's internal RAM is accessible via Video Stream Packet. RAM access data is not included in Register Access Packet.

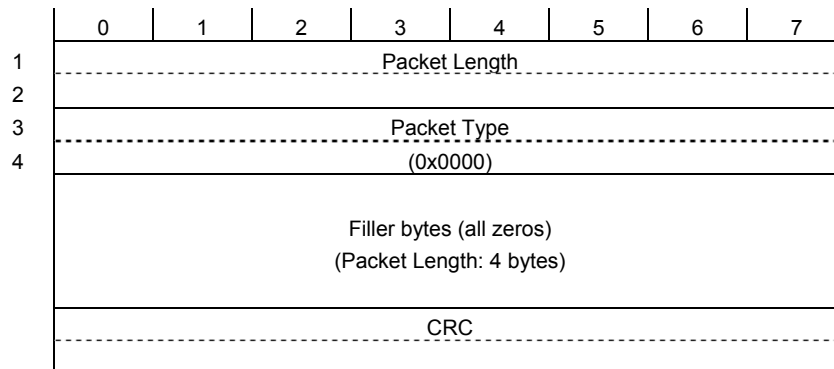
Link Shutdown Packet

This packet is used to bring Link to the Hibernation state.



Note: The parameters colored in gray are not supported by the ILI9327.

Filler Packet



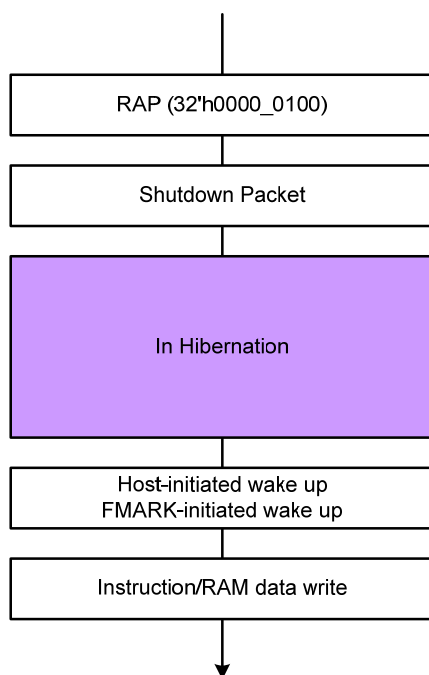
Hibernation Setting

The ILI9327's Client MDDI supports Hibernation setting. There are two ways to cancel the Hibernation setting, which can be selected according to the condition of use.

Hibernation Cancellation

Host-initiated wake up	In power-saving mode such as standby
TE-initiated wake up	Save power consumption in transferring moving picture data Host-initiated wake up triggered by the output from TE.

The Hibernation setting and cancellation sequence must be compatible with the VESA-MDDI specifications.



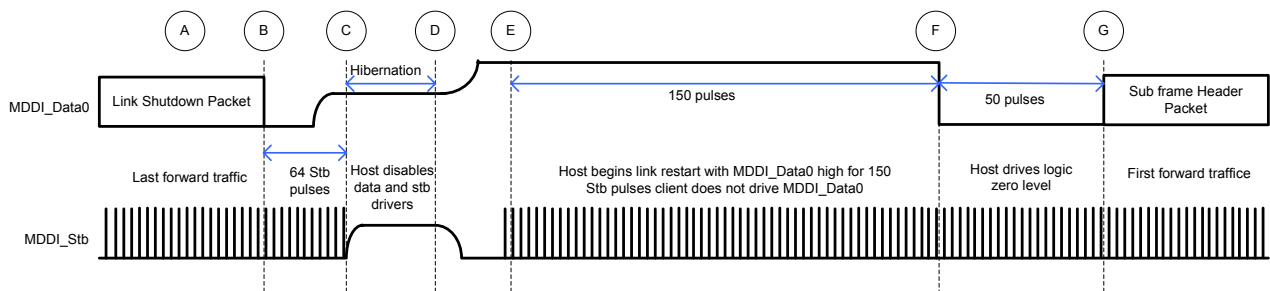
Host-Initiated Wake up from Hibernation

The host initiated wake up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the figures below!

- The host sends a Link Shutdown Packet to inform the client that the link will transition to the low power hibernation state.
- Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. During the interval the host initially sets MDDI_Data0 to a logic zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.
- The host enters the low power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low power hibernation state. It is also allowable for MDDI_Stb to be driven to a logic zero level or to continue toggling during hibernation. The client is also in the low power hibernation

state.

- D. After a while, the host begins the line restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic one level and MDDI_Stb to a logic zero level for at least 200nsec after MDDI_Data0 reaches a valid logic one level and MDDI_Stb reaches a valid logic zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high speed pulses on MDDI_Stb. The client first detects the wake up pulse using a low power differential receiver having a +125mV input offset voltage.
- E. The host drivers are fully enabled and MDDI_Data0 is being driven to a logic one level. The host begins to toggle MDDI_Stb in a manner consistent with having a logic zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.
- F. The host drives MDDI_Data0 to a logic zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub frame Header Packet after MDDI_Data0 is at a logic zero level for 40 MDDI_Stb cycles.
- G. The host begins to transmit data on the forward link by sending a Sub-frame Header packet. Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences from point G.



8. Command

8.1. Command List

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter	MIPI DCS Type1 Requirement	ILI9327 Implementation
00h	nop	C	0	Yes	Yes
01h	soft_reset	C	0	Yes	Yes
06h	get_red_channel	R	1	No	No
07h	get_green_channel	R	1	No	No
08h	get_blue_channel	R	1	No	No
0Ah	get_power_mode	R	1	Yes	Yes
0Bh	get_address_mode	R	1	Yes (Bit[7:0])	Yes (Bit[7:3]) , Only
0Ch	get_pixel_format	R	1	Yes	Yes
0Dh	get_display_mode	R	1	Yes	Yes
0Eh	get_signal_mode	R	1	Yes	Yes
0Fh	get_diagnostic_result	R	1	Bit7/6 : Yes Bit5/4 : Optional	Yes (Bit7/6 Only)
10h	enter_sleep_mode	C	0	Yes	Yes
11h	exit_sleep_mode	C	0	Yes	Yes
12h	enter_partial_mode	C	0	Yes	Yes
13h	enter_normal_mode	C	0	Yes	Yes
20h	exit_invert_mode	C	0	Yes	Yes
21h	enter_invert_mode	C	0	Yes	Yes
28h	set_display_off	C	0	Yes	Yes
29h	set_display_on	C	0	Yes	Yes
2Ah	set_column_address	W	4	Yes	Yes
2Bh	set_page_address	W	4	Yes	Yes
2Ch	write_memory_start	W	Variable	Yes	Yes
2Eh	read_memory_start	R	Variable	Yes	Yes
30h	set_partial_area	W	4	Yes	Yes
33h	set_scroll_area	W	6	Yes	Yes
34h	set_tear_off	C	0	Yes	Yes
35h	set_tear_on	W	1	Yes	Yes
36h	set_address_mode	W	1	Yes (Bit7-0)	Yes (Bit[7:3], Bit[1:0] Only)
37h	set_scroll_start	W	2	Yes	Yes
38h	exit_idle_mode	C	0	Yes	Yes
39h	enter_idle_mode	C	0	Yes	Yes
3Ah	set_pixel format	W	1	Yes	Yes
3Ch	write_memory_continue	W	Variable	Yes	Yes
3Eh	read_memory_continue	R	Variable	Yes	Yes
44h	set_tear_scanline	W	2	Yes	Yes
45h	get_scanline	R	2	Yes	Yes
51h	Write Display Brightness	W	1	-	Yes
52h	Read Display Brightness	R	1	-	Yes
53h	Write CTRL Display	W	1	-	Yes
54h	Read CTRL Display	R	1	-	Yes
55h	Write Content Adaptive Brightness Control	W	1	-	Yes
56h	Read Content Adaptive Brightness Control	R	1	-	Yes
5Eh	Write CABC Minimum Brightness	W	1	-	Yes
5Fh	Read CABC Minimum Brightness	R	1	-	Yes

A1h	read_DDB_start	R	1	Yes	Yes
B0h	Command Access Protect	R/W	1	-	Yes
B1h	Low Power Mode Control	R/W	1	-	Yes
B3h	Frame Memory Access and Interface Setting	R/W	4	-	Yes
B4h	Display Mode and Frame Memory Write Mode Setting	R/W	1	-	Yes
B5h	Sub-Panel Control Register	R/W	1	-	Yes
B8h	Backlight Control 1	R/W	1	-	Yes
B9h	Backlight Control 2	R/W	1	-	Yes
BAh	Backlight Control 3	R/W	1	-	Yes
BBh	Backlight Control 4	R/W	1	-	Yes
BCh	Backlight Control 5	R/W	1	-	Yes
BEh	Backlight Control 7	R/W	1	-	Yes
BFh	Backlight Control 8	R/W	1	-	Yes
C0h	Panel Driving Setting	R/W	6		Yes
C1h	Display_Timing_Setting for Normal/Partial Mode	R/W			Yes
C3h	Display_Timing_Setting for Idle Mode	R/W			Yes
C4h	Source/VCOM/Gate Timing Setting	R/W			Yes
C5h	Frame Rate Control	R/W			Yes
C6h	Interface Control	R/W			Yes
C8h	Gamma Setting	R/W			Yes
C9h	Gamma Setting for Red/Blue Color	R/W			Yes
D0h	Power_Setting	R/W			Yes
D1h	VCOM Control	R/W			Yes
D2h	Power_Setting for Normal Mode	R/W			Yes
D3h	Power_Setting for Partial Mode	R/W			Yes
D4h	Power_Setting for Idle Mode	R/W			Yes
E0h	NV Memory Write	R/W			Yes
E1h	NV Memory Control	R/W			Yes
E2h	NV Memory Status Read	R/W			Yes
E3h	NV Memory Protection	R/W			Yes
EAh	3-Gamma Function Control	R/W			Yes
EFh	Device Code Read	R/W			Yes

Operational Code (Hex)	Function	Command(C) Read(R)/Write(W)	Number Of Parameter
B0h	Command Access Protect	W/R	1
B1h	Low Power Mode Control	W/R	1
B3h	Frame Memory Access and Interface setting	W/R	5
B4h	Display Mode and Frame Memory Write Mode setting	W/R	1
BFh	Device code Read	R	4
C0h	Panel Driving Setting	W/R	7
C1h	Display Timing Setting for Normal Mode	W/R	3
C2h	Display Timing Setting for Partial Mode	W/R	3
C3h	Display Timing Setting for Idle Mode	W/R	3
C5h	Frame rate and Inversion Control	W/R	1
C6h	Interface Control	W/R	1
C8h	Gamma Setting	W/R	12
D0h	Power Setting	W/R	3
D1h	VCOM Control	W/R	3
D2h	Power Setting for Normal Mode	W/R	2
D3h	Power Setting for Partial Mode	W/R	2
D4h	Power Setting for Idle Mode	W/R	2
E0h	NV Memory Write	W/R	1
E1h	NV Memory Control	W/R	1
E2h	NV Memory Status	W/R	3
E3h	NV Memory Protection	W/R	2
B0~FF Except above command	LSI TEST Registers	W/R	Variable

8.2. Command Description

8.2.1. NOP (00h)

00H	NOP (No Operation)																								
	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	X	0	0	0	0	0	0	0	0	00												
Parameter	NO PARAMETER																								
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.																								
Restriction	None																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart	None																								

8.2.2. Soft_reset (01h)

01H	Soft_reset																								
	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	X	0	0	0	0	0	0	0	1	01												
Parameter	NO PARAMETER																								
Description	<p>When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)</p> <p>Note: The Frame Memory contents are affected by this command.</p> <p>X = Don't care</p>																								
Restriction	<p>Software Reset Command cannot be sent during Sleep Out sequence.</p> <p>Any new command is cannot be sent for 10-frame period until the ILI9327 enters Sleep-In mode. Do not send any command.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart	<pre> graph TD SWRESET[SWRESET] --> Display[Display whole blank screen] Display --> Set[Set Commands to S/W Default Value] Set --> Sleep[Sleep In Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: [Rectangle] Parameter: [Trapezoid] Display: [Hexagon] Action: [Hexagon] Mode: [Oval] Sequential transfer: [Oval] 																								

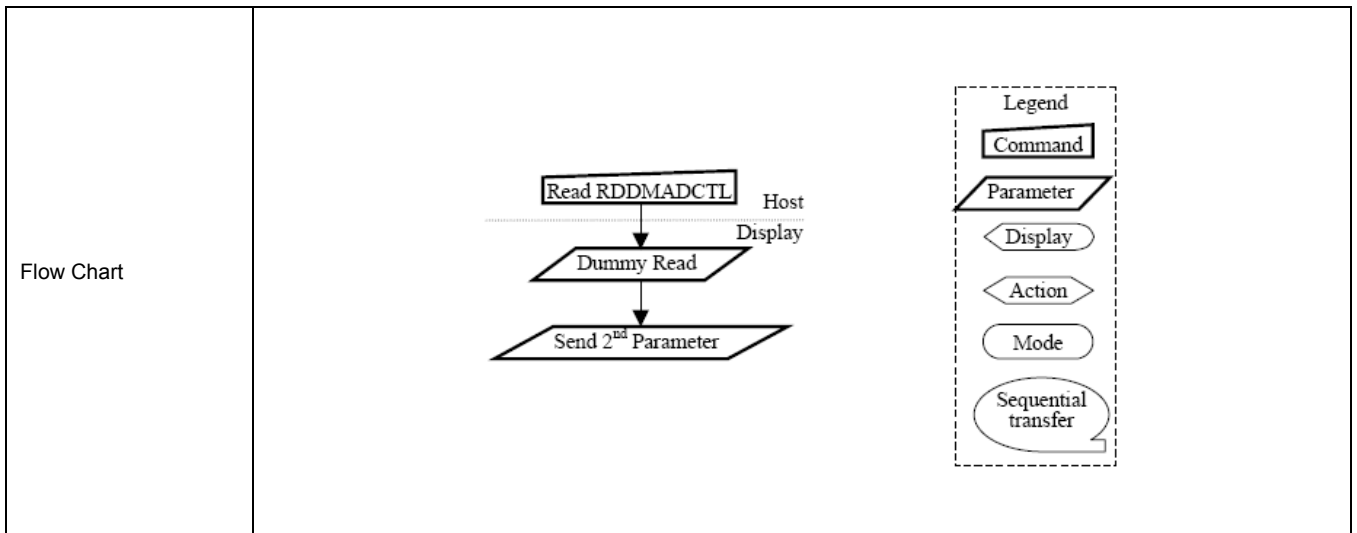
8.2.3. Get_power_mode (0Ah)

0AH	Get_power_mode																																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1	↑	x	0	0	0	0	1	0	1	0	0A																											
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	xx																											
2 nd Parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	0	0	08																											
Description	<p>This command indicates the current status of the display as described in the table below:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> <tr> <td>D6</td> <td>Idle Mode On/Off</td> <td></td> </tr> <tr> <td>D5</td> <td>Partial Mode On/Off</td> <td></td> </tr> <tr> <td>D4</td> <td>Sleep In/Out</td> <td></td> </tr> <tr> <td>D3</td> <td>Display Normal Mode On/Off</td> <td></td> </tr> <tr> <td>D2</td> <td>Display On/Off</td> <td></td> </tr> <tr> <td>D1</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> <tr> <td>D0</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> </tbody> </table>													Bit	Description	Comment	D7	Not Defined	Set to '0'	D6	Idle Mode On/Off		D5	Partial Mode On/Off		D4	Sleep In/Out		D3	Display Normal Mode On/Off		D2	Display On/Off		D1	Not Defined	Set to '0'	D0	Not Defined	Set to '0'
	Bit	Description	Comment																																					
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D3	Display Normal Mode On/Off																																							
D2	Display On/Off																																							
D1	Not Defined	Set to '0'																																						
D0	Not Defined	Set to '0'																																						
<ul style="list-style-type: none"> ◆ Bit D7 – Booster Voltage Status '0' = Booster Off or has a fault. '1' = Booster On and working OK (Meets Nokia's optical requirements). ◆ Bit D6 - Idle Mode On/Off '0' = Idle Mode Off. '1' = Idle Mode On. ◆ Bit D5 – Partial Mode On/Off '0' = Partial Mode Off. '1' = Partial Mode On. ◆ Bit D4 – Sleep In/Out '0' = Sleep In Mode. '1' = Sleep Out Mode. ◆ Bit D3 – Display Normal Mode On/Off '0' = Display Normal Mode Off. '1' = Display Normal Mode On. ◆ Bit D2 – Display On/Off '0' = Display is Off. '1' = Display is On. ◆ Bit D1 – Not Defined 'This bit is not applicable for this project, so it is set to '0' ◆ Bit D0 – Not Defined 'This bit is not applicable for this project, so it is set to '0' <p>X = Don't care</p>																																								

Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>08_{HEX}</td> </tr> <tr> <td>SW Reset</td> <td>08_{HEX}</td> </tr> <tr> <td>HW Reset</td> <td>08_{HEX}</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	08 _{HEX}	SW Reset	08 _{HEX}	HW Reset	08 _{HEX}				
Status	Default Value												
Power On Sequence	08 _{HEX}												
SW Reset	08 _{HEX}												
HW Reset	08 _{HEX}												
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD subgraph Host A[Read RDDPM] --> B[/Dummy Read/] B --> C[/Send 2nd Parameter/] end </pre> </div> <div style="flex: 0.5; border: 1px dashed black; padding: 5px; margin-left: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>												

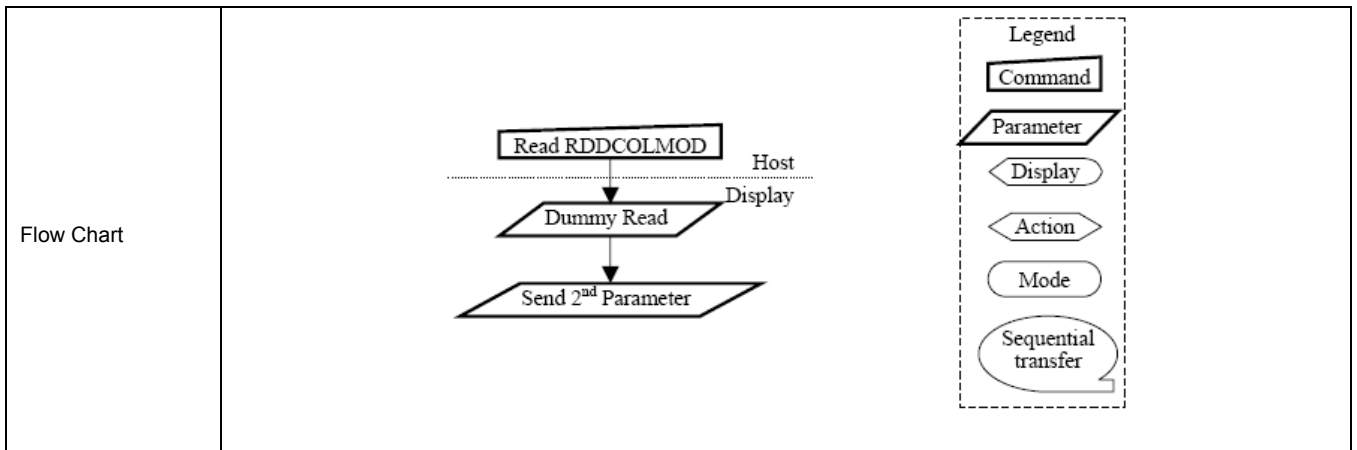
8.2.4. Get_address_mode (0Bh)

0BH	Get_address_mode																																						
	D/CX	RDX	WRX	D17-0	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command	0	1	↑	x	0	0	0	0	1	0	1	1	0B																										
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																										
2 nd Parameter	1	↑	1	x	D7	D6	D5	D4	D3	0	0	0	xx																										
Description	This command indicates the current status of the display as described in the table below:																																						
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Page Address Order</td> <td></td> </tr> <tr> <td>D6</td> <td>Column Address Order</td> <td></td> </tr> <tr> <td>D5</td> <td>Page/Column Order</td> <td></td> </tr> <tr> <td>D4</td> <td>Line Address Order</td> <td></td> </tr> <tr> <td>D3</td> <td>RGB/BGR Order</td> <td></td> </tr> <tr> <td>D2</td> <td>Reserved</td> <td>Set to '0'</td> </tr> <tr> <td>D1</td> <td>Reserved</td> <td>Set to '0'</td> </tr> <tr> <td>D0</td> <td>Reserved</td> <td>Set to '0'</td> </tr> </tbody> </table> <ul style="list-style-type: none"> ◆ Bit D7 – Page Address Order ‘0’ = Top to Bottom ‘1’ = Bottom to Top ◆ Bit D6 – Column Address Order ‘0’ = Left to Right ‘1’ = Right to Left ◆ Bit D5 - Page/Column Order ‘0’ = Normal Mode ‘1’ = Reverse Mode Note: For Bits D7 to D5, also refer to Section 8.2.3 MCU to memory write/read direction. ◆ Bit D4 – Line Address Order ‘0’ = LCD Refresh Top to Bottom ‘1’ = LCD Refresh Bottom to Top ◆ Bit D3 – RGB/BGR Order ‘0’ = RGB ‘1’ = BGR 													Bit	Description	Comment	D7	Page Address Order		D6	Column Address Order		D5	Page/Column Order		D4	Line Address Order		D3	RGB/BGR Order		D2	Reserved	Set to '0'	D1	Reserved	Set to '0'	D0	Reserved
Bit	Description	Comment																																					
D7	Page Address Order																																						
D6	Column Address Order																																						
D5	Page/Column Order																																						
D4	Line Address Order																																						
D3	RGB/BGR Order																																						
D2	Reserved	Set to '0'																																					
D1	Reserved	Set to '0'																																					
D0	Reserved	Set to '0'																																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes														
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Status	Default Value																																						
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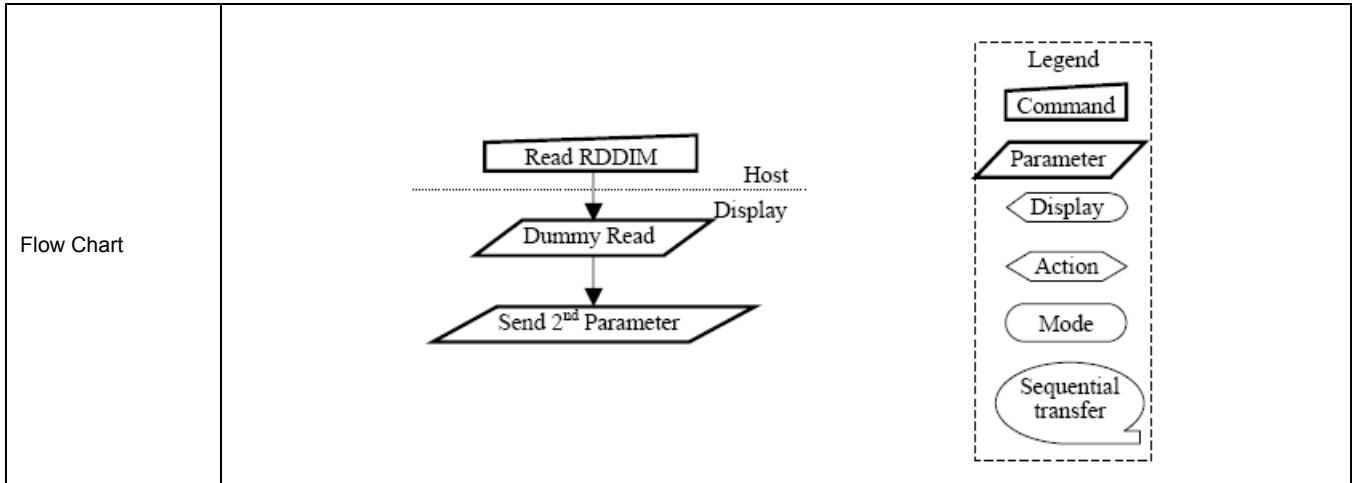
8.2.5. Get_pixel_format (0Ch)

0CH	Get_pixel_format																																																											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																															
Command	0	1	↑	x	0	0	0	0	1	1	0	0	0C																																															
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																																															
2 nd Parameter	1	↑	1	x	0	D6	D5	D4	0	D2	D1	D0	66																																															
Description	This command indicates the current status of the display as described in the table below:																																																											
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td rowspan="4">DPI Pixel Format (RGB Interface Color Format)</td> </tr> <tr> <td>D6</td> </tr> <tr> <td>D5</td> </tr> <tr> <td>D4</td> </tr> <tr> <td>D3</td> <td rowspan="4">DBI Pixel Format (Control Interface Color Format)</td> </tr> <tr> <td>D2</td> </tr> <tr> <td>D1</td> </tr> <tr> <td>D0</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Pixel Format</th> <th>D6/D2</th> <th>D5/D1</th> <th>D4/D0</th> </tr> </thead> <tbody> <tr> <td>Reserved</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>3 bits / pixel</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Reserved</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Reserved</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Reserved</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>16 bits / pixel</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>18 bits / pixel</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>Reserved</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>													Bit	Description	D7	DPI Pixel Format (RGB Interface Color Format)	D6	D5	D4	D3	DBI Pixel Format (Control Interface Color Format)	D2	D1	D0	Pixel Format	D6/D2	D5/D1	D4/D0	Reserved	0	0	0	3 bits / pixel	0	0	1	Reserved	0	1	0	Reserved	0	1	1	Reserved	1	0	0	16 bits / pixel	1	0	1	18 bits / pixel	1	1	0	Reserved	1	1
Bit	Description																																																											
D7	DPI Pixel Format (RGB Interface Color Format)																																																											
D6																																																												
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D2																																																												
D1																																																												
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Pixel Format	D6/D2	D5/D1	D4/D0																																																									
Reserved	0	0	0																																																									
3 bits / pixel	0	0	1																																																									
Reserved	0	1	0																																																									
Reserved	0	1	1																																																									
Reserved	1	0	0																																																									
16 bits / pixel	1	0	1																																																									
18 bits / pixel	1	1	0																																																									
Reserved	1	1	1																																																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																			
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Default value	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>66_{HEX}</td> </tr> <tr> <td>SW Reset</td> <td>66_{HEX}</td> </tr> <tr> <td>HW Reset</td> <td>66_{HEX}</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	66 _{HEX}	SW Reset	66 _{HEX}	HW Reset	66 _{HEX}																																							
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Power On Sequence	66 _{HEX}																																																											
SW Reset	66 _{HEX}																																																											
HW Reset	66 _{HEX}																																																											



8.2.6. Get_display_mode (0Dh)

0DH	Get_display_mode																																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command	0	1	↑	x	0	0	0	0	1	1	0	1	0D																										
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																										
2 nd Parameter	1	↑	1	x	0	0	0	0	0	0	0	0	00																										
Description	The display module returns the Display Image Mode status.																																						
	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Symbol</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Vertical Scrolling Status</td> <td>VSSON</td> </tr> <tr> <td>D6</td> <td>Reserved</td> <td></td> </tr> <tr> <td>D5</td> <td>Inversion On/Off</td> <td>DSPINVON</td> </tr> <tr> <td>D4</td> <td>Reserved</td> <td></td> </tr> <tr> <td>D3</td> <td>Reserved</td> <td></td> </tr> <tr> <td>D2</td> <td>Gamma Curve Selection</td> <td></td> </tr> <tr> <td>D1</td> <td>Gamma Curve Selection</td> <td></td> </tr> <tr> <td>D0</td> <td>Gamma Curve Selection</td> <td></td> </tr> </tbody> </table> <p>This command indicates the current status of the display as described in the table below:</p> <ul style="list-style-type: none"> ◆ Bit D7 – Vertical Scrolling On/Off <ul style="list-style-type: none"> '0' = Vertical Scrolling is Off. '1' = Vertical Scrolling is On. ◆ Bit D6 – Reserved ◆ Bit D5 – Inversion On/Off <ul style="list-style-type: none"> '0' = Inversion is Off. '1' = Inversion is On. ◆ Bit D4 – Reserved ◆ Bit D3 – Reserved ◆ Bits D2, D1, D0 – Gamma Curve Selection <ul style="list-style-type: none"> These bits are not applicable for this project, so they are set to '000' 													Bit	Description	Symbol	D7	Vertical Scrolling Status	VSSON	D6	Reserved		D5	Inversion On/Off	DSPINVON	D4	Reserved		D3	Reserved		D2	Gamma Curve Selection		D1	Gamma Curve Selection		D0	Gamma Curve Selection
Bit	Description	Symbol																																					
D7	Vertical Scrolling Status	VSSON																																					
D6	Reserved																																						
D5	Inversion On/Off	DSPINVON																																					
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D2	Gamma Curve Selection																																						
D1	Gamma Curve Selection																																						
D0	Gamma Curve Selection																																						
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes														
Status	Availability																																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																						
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Status	Default Value																																						
Power On Sequence	00 _{HEX}																																						
SW Reset	00 _{HEX}																																						
HW Reset	00 _{HEX}																																						



8.2.7. Get_signal_mode (0Eh)

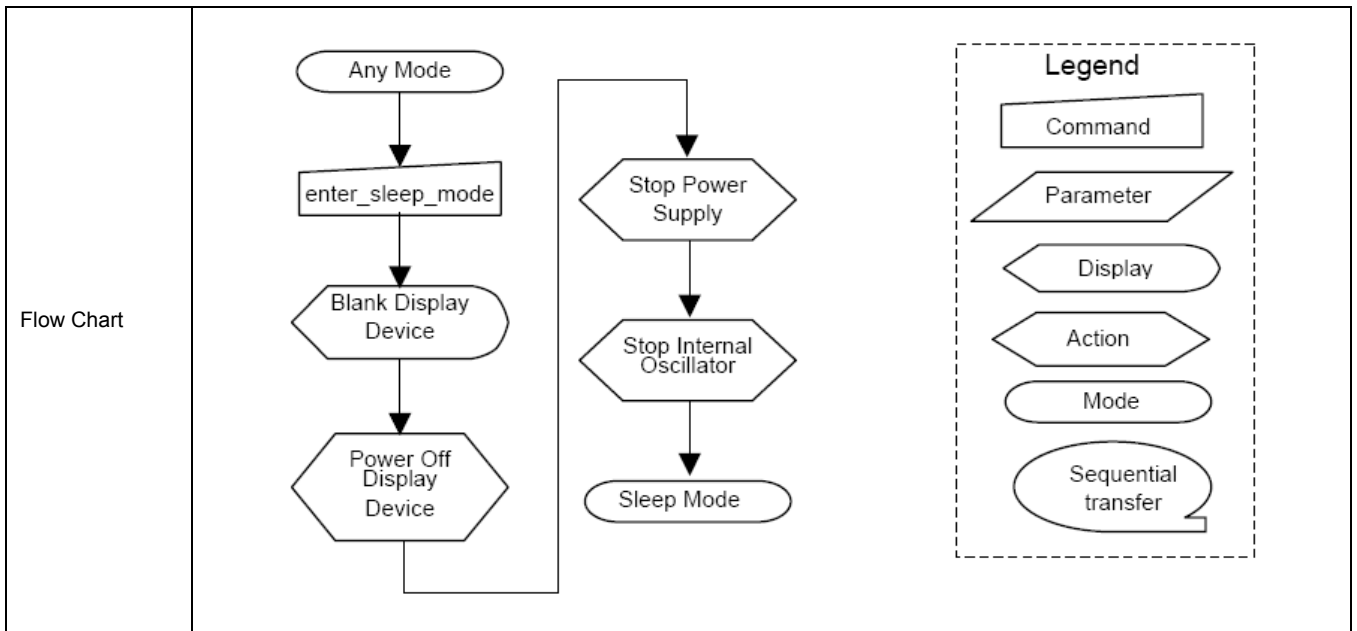
0EH	Get_signal_mode																																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command	0	1	↑	x	0	0	0	0	1	1	1	0	0E																										
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																										
2 nd Parameter	1	↑	1	x	D7	D6	0	0	0	0	0	0	00																										
Description	The display module returns the Display Signal Mode.																																						
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Symbol</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Tearing Effect Line On/Off</td> <td>TEON</td> </tr> <tr> <td>D6</td> <td>Tearing Effect Line Output Mode</td> <td>TELOM</td> </tr> <tr> <td>D5</td> <td>Reserved</td> <td></td> </tr> <tr> <td>D4</td> <td>Reserved</td> <td></td> </tr> <tr> <td>D3</td> <td>Reserved</td> <td></td> </tr> <tr> <td>D2</td> <td>Reserved</td> <td></td> </tr> <tr> <td>D1</td> <td>Reserved</td> <td></td> </tr> <tr> <td>D0</td> <td>Reserved</td> <td></td> </tr> </tbody> </table> <p>This command indicates the current status of the display as described in the table below:</p> <ul style="list-style-type: none"> ◆ Bit D7 – Tearing Effect Line On/Off '0' = Tearing Effect Line Off. '1' = Tearing Effect On. ◆ Bit D6 – Tearing Effect Line Output Mode, see section 8.3 for mode definitions. '0' = Mode 1. '1' = Mode 2. ◆ Bit D[5:0] – Reserved 													Bit	Description	Symbol	D7	Tearing Effect Line On/Off	TEON	D6	Tearing Effect Line Output Mode	TELOM	D5	Reserved		D4	Reserved		D3	Reserved		D2	Reserved		D1	Reserved		D0	Reserved
Bit	Description	Symbol																																					
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D6	Tearing Effect Line Output Mode	TELOM																																					
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D4	Reserved																																						
D3	Reserved																																						
D2	Reserved																																						
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Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes														
Status	Availability																																						
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Status	Default Value																																						
Power On Sequence	00 _{HEX}																																						
SW Reset	00 _{HEX}																																						
HW Reset	00 _{HEX}																																						
Flow Chart	<pre> graph TD subgraph Host A[Read RDDIM] end subgraph Display B[/Dummy Read/] C[/Send 2nd Parameter/] end A --> B B --> C </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Trapezoid Action: Diamond Mode: Circle Sequential transfer: Dashed line 																																						

8.2.8. Get_diagnostic_result (0Fh)

0FH	Get_diagnostic_result																																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command	0	1	↑	x	0	0	0	0	1	1	1	1	0F																										
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																										
2 nd Parameter	1	↑	1	x	D7	D6	0	0	0	0	0	0	00																										
Description	The display module returns the self-diagnostic results following a Sleep Out command.																																						
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Symbol</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Register Loading Detection</td> <td>SDR</td> </tr> <tr> <td>D6</td> <td>Functionality Detection</td> <td>FUNCD</td> </tr> <tr> <td>D5</td> <td>Chip attachment Detection</td> <td>Set '0'</td> </tr> <tr> <td>D4</td> <td>Display Glass Break Detection</td> <td>Set '0'</td> </tr> <tr> <td>D3</td> <td>Reserved</td> <td>Set '0'</td> </tr> <tr> <td>D2</td> <td>Reserved</td> <td>Set '0'</td> </tr> <tr> <td>D1</td> <td>Reserved</td> <td>Set '0'</td> </tr> <tr> <td>D0</td> <td>Reserved</td> <td>Set '0'</td> </tr> </tbody> </table> <p>Bit D7 – Register Loading Detection</p> <p>Bit D6 – Functionality Detection</p> <p>Bit D5 – Chip Attachment Detection Set to '0' if feature unimplemented.</p> <p>Bit D4 – Display Glass Break Detection Set to '0' if feature unimplemented.</p> <p>Bits D[3:0] – Reserved Set to '0'.</p>													Bit	Description	Symbol	D7	Register Loading Detection	SDR	D6	Functionality Detection	FUNCD	D5	Chip attachment Detection	Set '0'	D4	Display Glass Break Detection	Set '0'	D3	Reserved	Set '0'	D2	Reserved	Set '0'	D1	Reserved	Set '0'	D0	Reserved
Bit	Description	Symbol																																					
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Status	Availability																																						
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Normal Mode On, Idle Mode On, Sleep Out	Yes																																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																																						
Sleep In	Yes																																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00_{HEX}</td> </tr> <tr> <td>SW Reset</td> <td>00_{HEX}</td> </tr> <tr> <td>HW Reset</td> <td>00_{HEX}</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	00 _{HEX}	SW Reset	00 _{HEX}	HW Reset	00 _{HEX}																		
Status	Default Value																																						
Power On Sequence	00 _{HEX}																																						
SW Reset	00 _{HEX}																																						
HW Reset	00 _{HEX}																																						
Flow Chart	<pre> graph TD subgraph Host A[Read RDDIM] end subgraph Display B[/Dummy Read/] C[/Send 2nd Parameter/] end A --> B B --> C </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Trapezoid Action: Diamond Mode: Oval Sequential transfer: Curved arrow 																																						

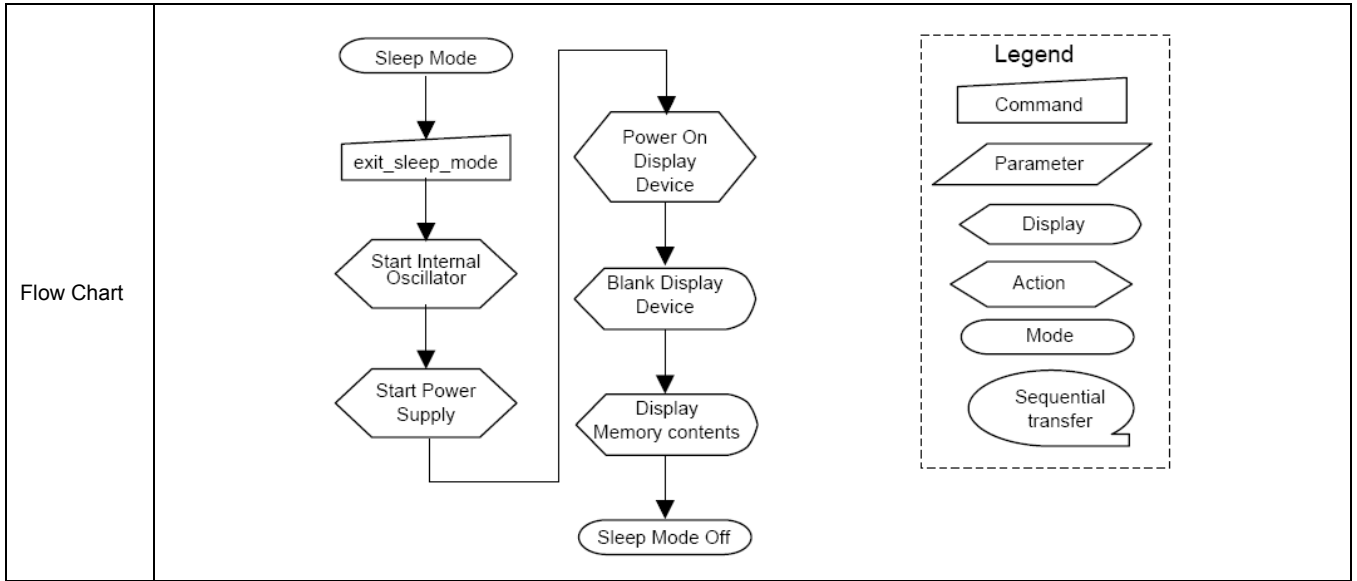
8.2.9. Enter_sleep_mode (10h)

10H	Enter_sleep_mode																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	0	1	0	0	0	0	10												
Parameter	No Parameter																								
Description	<p>This command causes the display module to enter the Sleep mode.</p> <p>This command causes the LCD module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop.</p> <p>DBI or DSI Command Mode remains operational and the frame memory maintains its contents. The host processor continues to send PCLK, HS and VS information to Type 2 and Type 3 display modules for two frames after this command is sent when the display module is in Normal mode.</p>																								
Restriction	<p>This command has no effect when the display module is already in Sleep mode.</p> <p>The host processor must wait five milliseconds before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize.</p> <p>The host processor must wait 120 milliseconds after sending an exit_sleep_mode command before sending an enter_sleep_mode command.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>SW Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>HW Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode				
Status	Default Value																								
Power On Sequence	Sleep In Mode																								
SW Reset	Sleep In Mode																								
HW Reset	Sleep In Mode																								



8.2.10. Exit_sleep_mode (11h)

11H	Exit_sleep_mode																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	0	1	0	0	0	1	11												
Parameter	No Parameter																								
Description	This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to Type 2 and Type 3 display modules two frames before this command is sent when the display module is in Normal Mode.																								
Restriction	<p>This command shall not cause any visible effect on the display device when the display module is not in Sleep mode.</p> <p>The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize.</p> <p>The host processor must wait 120 milliseconds after sending an exit_sleep_mode command before sending an enter_sleep_mode command.</p> <p>The display module loads the display module's default values to the registers when exiting the Sleep mode.</p> <p>There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode.</p> <p>The display module runs the self-diagnostic functions after this command is received. See section 5.3 for a description of the self-diagnostic functions.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>SW Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>HW Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode				
Status	Default Value																								
Power On Sequence	Sleep In Mode																								
SW Reset	Sleep In Mode																								
HW Reset	Sleep In Mode																								



8.2.11. Enter_Partial_mode (12h)

12H	Enter_Partial_mode																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	0	1	0	0	1	0	12												
Parameter	No Parameter																								
Description	<p>This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the set_partial_area (30h) command.</p> <p>To leave Partial Display Mode, the enter_normal_mode (13h) command should be written.</p> <p>The host processor continues to send PCLK, HS and VS information to Type 2 display modules for two frames after this command is sent when the display module is in Normal Display Mode.</p>																								
Restriction	This command has no effect when Partial Display Mode is already active.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
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Status	Default Value																								
Power On Sequence	Normal Display Mode On																								
SW Reset	Normal Display Mode On																								
HW Reset	Normal Display Mode On																								
Flow Chart	Refer to Partial Area (30h)																								

8.2.12. Enter_normal_mode (13h)

13H	Enter_normal_mode																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	0	1	0	0	1	1	13												
Parameter	No Parameter																								
Description	<p>This command causes the display module to enter the Normal mode.</p> <p>Normal Mode is defined as Partial Display mode and Scroll mode are off.</p> <p>The host processor sends PCLK, HS and VS information to Type 2 display modules two frames before this command is sent when the display module is in Partial Display Mode.</p>																								
Restriction	This command has no effect when Normal Display mode is already active.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display Mode On</td> </tr> <tr> <td>SW Reset</td> <td>Normal Display Mode On</td> </tr> <tr> <td>HW Reset</td> <td>Normal Display Mode On</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Normal Display Mode On	SW Reset	Normal Display Mode On	HW Reset	Normal Display Mode On				
Status	Default Value																								
Power On Sequence	Normal Display Mode On																								
SW Reset	Normal Display Mode On																								
HW Reset	Normal Display Mode On																								
Flow Chart	Refer to the description of set_partial_area(30h) and set_scroll_area(33h)																								

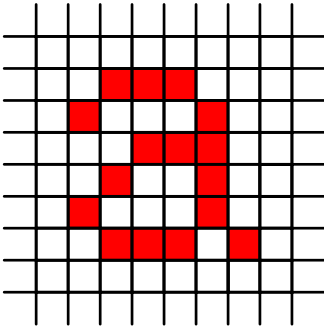
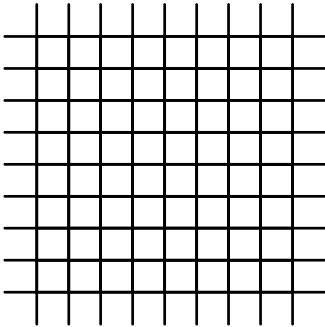
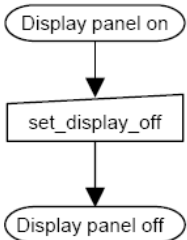
8.2.13. Exit_invert_mode (20h)

20H	Exit_invert_mode																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	0	0	0	0	20												
Parameter	No Parameter																								
Description	<p>This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p> </div> <div style="font-size: 2em; margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display Panel</p> </div> </div>																								
Restriction	This command has no effect when the display module is not inverting the display image.																								
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
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Status	Default Value																								
Power On Sequence	Display Inversion Off																								
SW Reset	Display Inversion Off																								
HW Reset	Display Inversion Off																								
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A([Invert mode on]) --> B[exit_invert_mode] B --> C([Invert mode off]) </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command: [] Parameter: /> Display: > Action: > Mode: > Sequential transfer: > </div> </div>																								

8.2.14. Enter_invert_mode (21h)

21H	Enter_invert_mode																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	0	0	0	1	21												
Parameter	No Parameter																								
Description	<p>This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. No status bits are changed.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p> </div> <div style="font-size: 2em; margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display Panel</p> </div> </div>																								
Restriction	This command has no effect when module is already in inversion on mode.																								
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Inversion Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Inversion Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Inversion Off	SW Reset	Display Inversion Off	HW Reset	Display Inversion Off				
Status	Default Value																								
Power On Sequence	Display Inversion Off																								
SW Reset	Display Inversion Off																								
HW Reset	Display Inversion Off																								
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A([Invert mode off]) --> B[enter_invert_mode] B --> C([Invert mode on]) </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command: [Rectangle] Parameter: [Parallelogram] Display: [Rounded rectangle] Action: [Arrow-shaped rectangle] Mode: [Oval] Sequential transfer: [Speech bubble] </div> </div>																								

8.2.15. Set_display_off (28h)

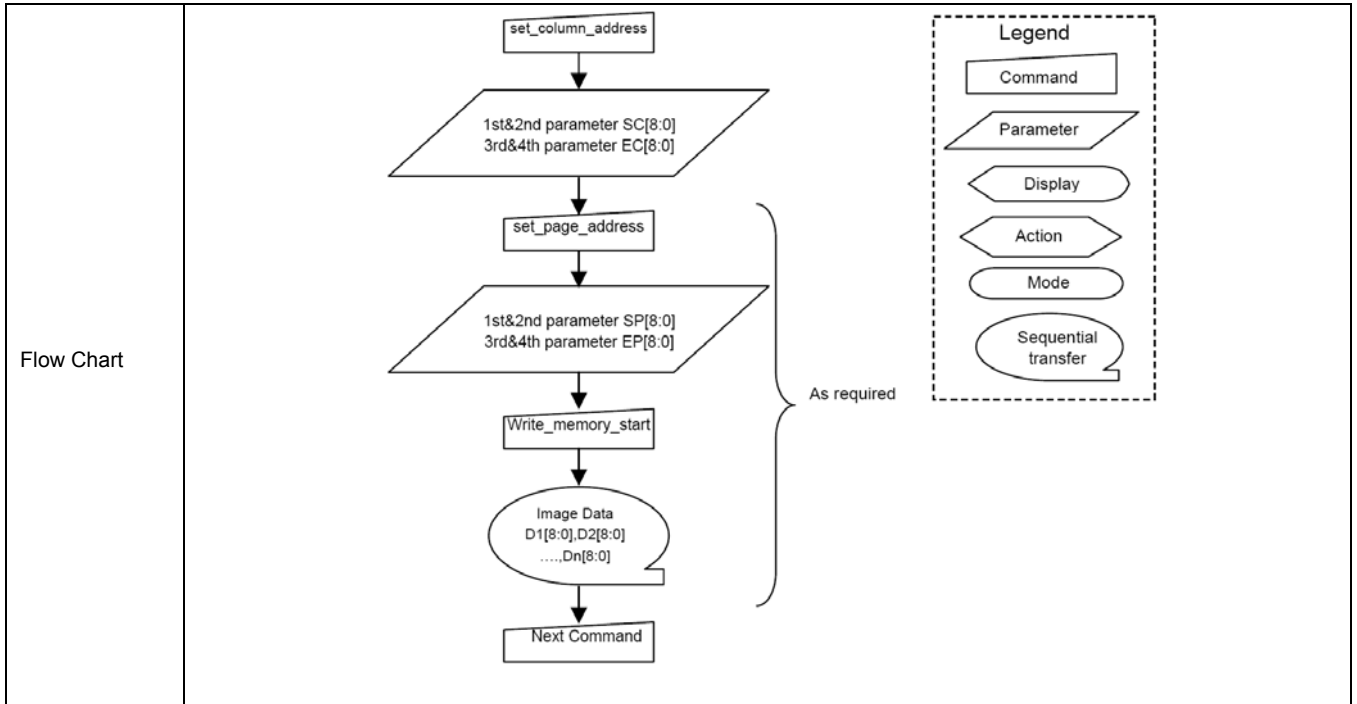
28H	Set_display_off																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	1	0	0	0	28												
Parameter	No Parameter																								
Description	<p>This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p>  </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display Panel</p>  </div> </div>																								
Restriction	This command has no effect when module is already in display off mode.																								
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off				
Status	Default Value																								
Power On Sequence	Display Off																								
SW Reset	Display Off																								
HW Reset	Display Off																								
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;">  </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command: [Rectangle] Parameter: [Parallelogram] Display: [Oval] Action: [Hexagon] Mode: [Rounded Rectangle] Sequential transfer: [Speech bubble] </div> </div>																								

8.2.16. Set_display_on (29h)

29H	Set_display_on																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	1	0	0	1	29												
Parameter	No Parameter																								
Description	<p>This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p> </div> <div style="font-size: 2em; margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display Panel</p> </div> </div>																								
Restriction	This command has no effect when module is already in display on mode.																								
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off				
Status	Default Value																								
Power On Sequence	Display Off																								
SW Reset	Display Off																								
HW Reset	Display Off																								
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A([Display panel off]) --> B[set_display_on] B --> C([Display panel on]) </pre> </div> <div style="border: 1px dashed black; padding: 10px; margin-left: 20px;"> <p>Legend</p> <ul style="list-style-type: none"> Command: [] Parameter: /> Display: > Action: > Mode: > Sequential transfer: > </div> </div>																								

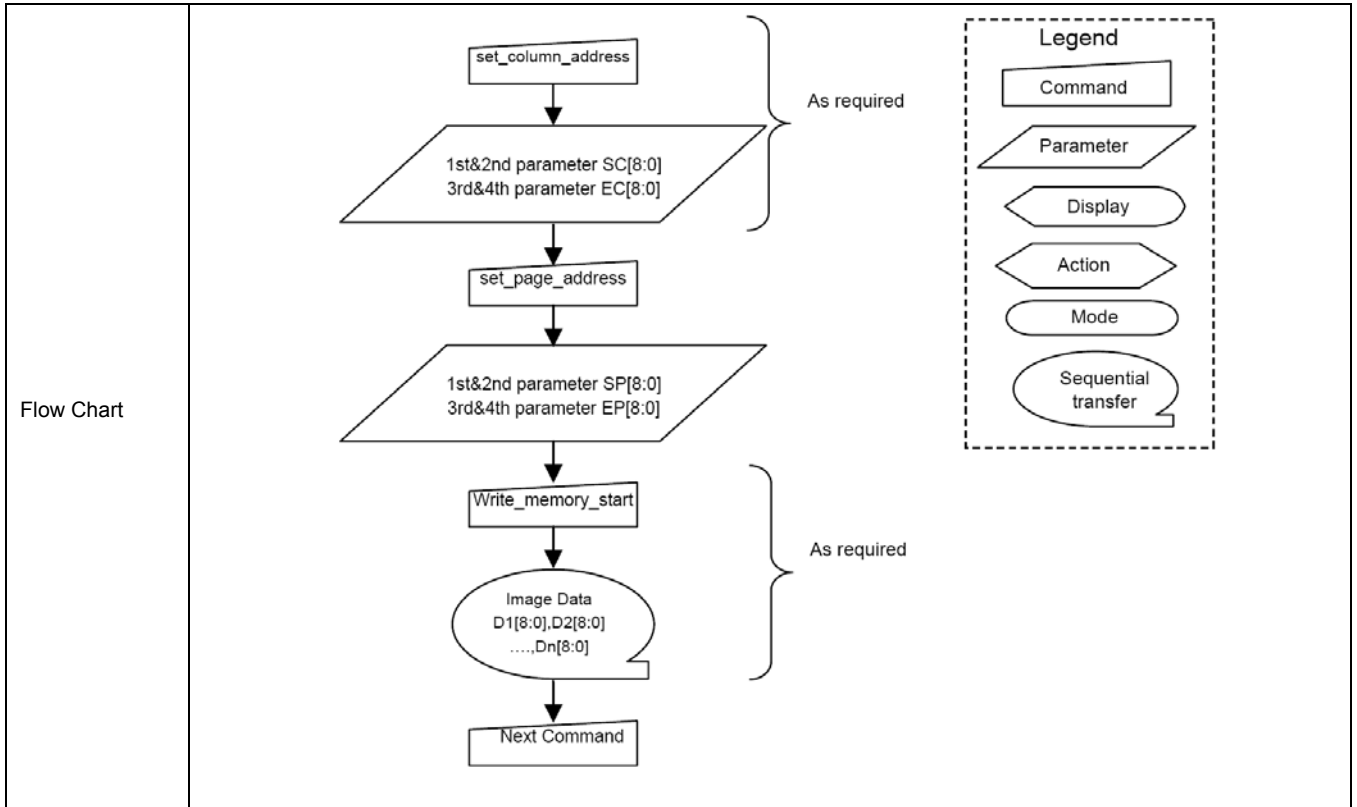
8.2.17. Set_column_address (2Ah)

2AH	Set_column_address																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	1	0	1	0	2A												
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SC8	Note												
2 nd Parameter	1	1	↑	x	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	1												
3 rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	EC8	Note												
4 th Parameter	1	1	↑	x	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	2												
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status.</p> <p>Each value represents one column line in the Frame</p> <div style="text-align: center;"> </div> <p>Memory.</p>																								
	Restriction	<p>SC [8:0] always must be equal to or less than EC[8:0]. If SC[8:0] or EC[8:0] is greater than the available frame memory then the parameter is not updated.</p>																							
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Status</th> <th colspan="2" style="width: 80%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SC[8:0]=0000_{HEX}</td> <td>SE[8:0]=0EF_{HEX}</td> </tr> <tr> <td>SW Reset</td> <td>SC[8:0]=0000_{HEX}</td> <td>If Set_address_mode(36h) B5=0 : EC[8:0]=0EF_{HEX} If Set_address_mode(36h) B5=1 : EC[8:0]=1AF_{HEX}</td> </tr> <tr> <td>HW Reset</td> <td>SC[8:0]=0000_{HEX}</td> <td>SE[8:0]=0EF_{HEX}</td> </tr> </tbody> </table>													Status	Default Value		Power On Sequence	SC[8:0]=0000 _{HEX}	SE[8:0]=0EF _{HEX}	SW Reset	SC[8:0]=0000 _{HEX}	If Set_address_mode(36h) B5=0 : EC[8:0]=0EF _{HEX} If Set_address_mode(36h) B5=1 : EC[8:0]=1AF _{HEX}	HW Reset	SC[8:0]=0000 _{HEX}	SE[8:0]=0EF _{HEX}
Status	Default Value																								
Power On Sequence	SC[8:0]=0000 _{HEX}	SE[8:0]=0EF _{HEX}																							
SW Reset	SC[8:0]=0000 _{HEX}	If Set_address_mode(36h) B5=0 : EC[8:0]=0EF _{HEX} If Set_address_mode(36h) B5=1 : EC[8:0]=1AF _{HEX}																							
HW Reset	SC[8:0]=0000 _{HEX}	SE[8:0]=0EF _{HEX}																							



8.2.18. Set_page_address (2Bh)

2BH	Set_page_address																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	1	0	1	1	2B												
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SP8	xxx												
2 nd Parameter	1	1	↑	x	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0													
3 rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	EP8	xxx												
4 th Parameter	1	1	↑	x	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0													
Description	<p>This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. No status bits are changed.</p> <div style="text-align: center;"> </div>																								
Restriction	<p>SP [8:0] always must be equal to or less than EP [8:0].</p> <p>If SP[8:0] or EP[8:0] is greater than the available frame memory then the parameter is not updated.</p>																								
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SP[8:0]=0000_{HEX}</td> <td>EP[8:0]=1AF_{HEX}</td> </tr> <tr> <td>SW Reset</td> <td>SP[8:0]=0000_{HEX}</td> <td>If Set_address_mode(36h) B5=0 : EP[8:0]=1AF_{HEX} If Set_address_mode(36h) B5=1 : EP[8:0]=0EF_{HEX}</td> </tr> <tr> <td>HW Reset</td> <td>SP8:0]=0000_{HEX}</td> <td>EP[8:0]=1AF_{HEX}</td> </tr> </tbody> </table>													Status	Default Value		Power On Sequence	SP[8:0]=0000 _{HEX}	EP[8:0]=1AF _{HEX}	SW Reset	SP[8:0]=0000 _{HEX}	If Set_address_mode(36h) B5=0 : EP[8:0]=1AF _{HEX} If Set_address_mode(36h) B5=1 : EP[8:0]=0EF _{HEX}	HW Reset	SP8:0]=0000 _{HEX}	EP[8:0]=1AF _{HEX}
Status	Default Value																								
Power On Sequence	SP[8:0]=0000 _{HEX}	EP[8:0]=1AF _{HEX}																							
SW Reset	SP[8:0]=0000 _{HEX}	If Set_address_mode(36h) B5=0 : EP[8:0]=1AF _{HEX} If Set_address_mode(36h) B5=1 : EP[8:0]=0EF _{HEX}																							
HW Reset	SP8:0]=0000 _{HEX}	EP[8:0]=1AF _{HEX}																							



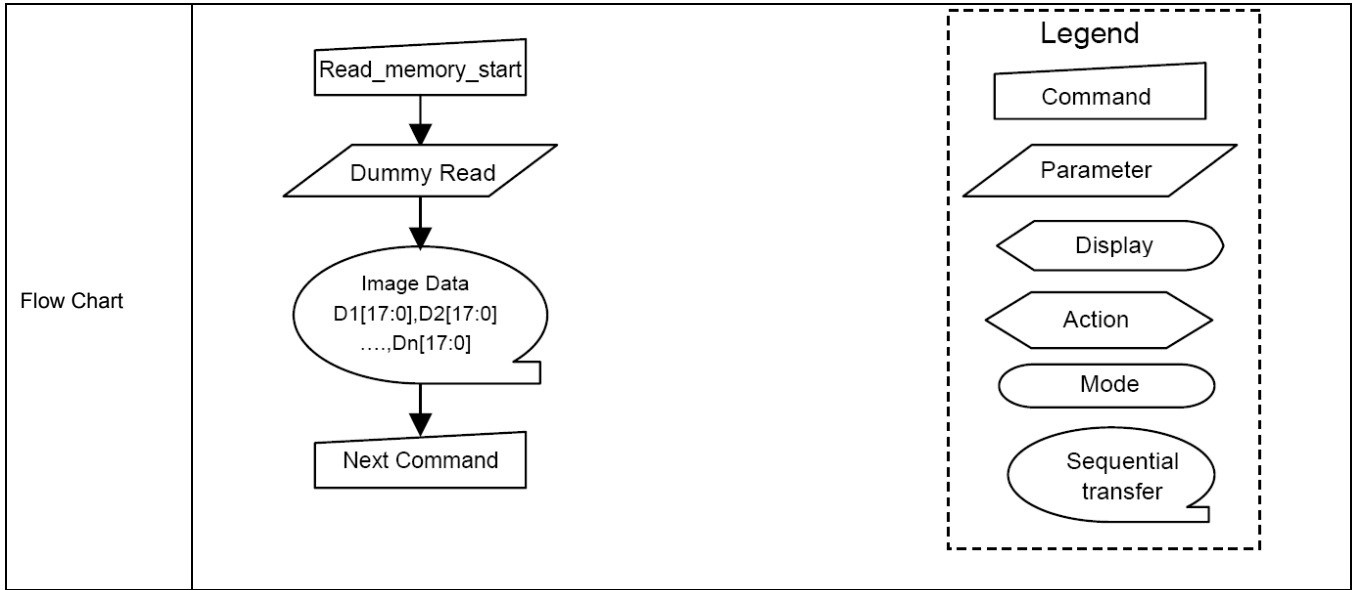
8.2.19. Write_memory_start (2Ch)

2CH	Write_memory_start												HEX												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0													
Command	0	1	↑	xx	0	0	1	0	1	1	0	0	2C												
1 st pixel data	1	1	↑	D1 [17..8]	D1 7	D1 6	D1 5	D1 4	D1 3	D1 2	D1 1	D1 0	00000..3FFF												
:	1	1	↑	Dx [17..8]	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	00000..3FFF												
N TH pixel data	1	1	↑	Dn [17..8]	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	00000..3FFF												
Description	<p>This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding set_column_address (2Ah) and set_page_address (2Bh) commands.</p> <p>When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.</p> <p>If set_address_mode (36h) B5 = 0:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.</p> <p>If set_address_mode (36h) B5 = 1:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.</p>																								
Restriction	<p>A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write location. Otherwise, data written with write_memory_start and any following write_memory_continue commands is written to undefined locations..</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>SW Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>HW Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is not cleared	HW Reset	Contents of memory is not cleared
Status	Default Value								
Power On Sequence	Contents of memory is set randomly								
SW Reset	Contents of memory is not cleared								
HW Reset	Contents of memory is not cleared								
Flow Chart	<pre> graph TD A[Write_memory_start] --> B(Image Data D1[17:0],D2[17:0],Dn[17:0]) B --> C[Next Command] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Rounded rectangle Action: Arrow Mode: Oval Sequential transfer: Oval with tail 								

8.2.20. Read_memory_start (2Eh)

2EH	RAMRD (Memory Read)												HEX												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0													
Command	0	1	↑	x	0	0	1	0	1	1	1	0	2E												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x												
2 nd Parameter	1	↑	1	D1 [17..8]	D1 7	D1 6	D1 5	D1 4	D1 3	D1 2	D1 1	D1 0	0000..3FF												
:	1	↑	1	Dx [17..8]	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	0000..3FF												
(N+1) TH Parameter	1	↑	1	Dn [17..8]	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	0000..3FF												
Description	<p>This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.</p> <p>If set_address_mode B5 = 0:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.</p> <p>If set_address_mode B5 = 1:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.</p>																								
Restriction	Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Sleep In	Yes																								
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Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
SW Reset	Contents of memory is not cleared																								
HW Reset	Contents of memory is not cleared																								

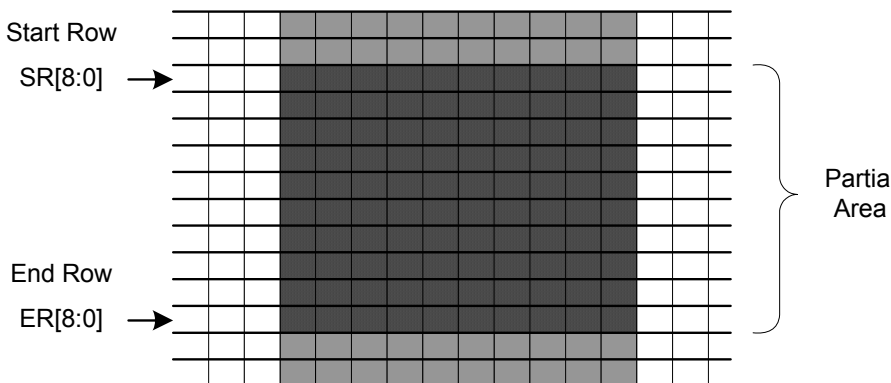


8.2.21. Set_partial_area (30h)

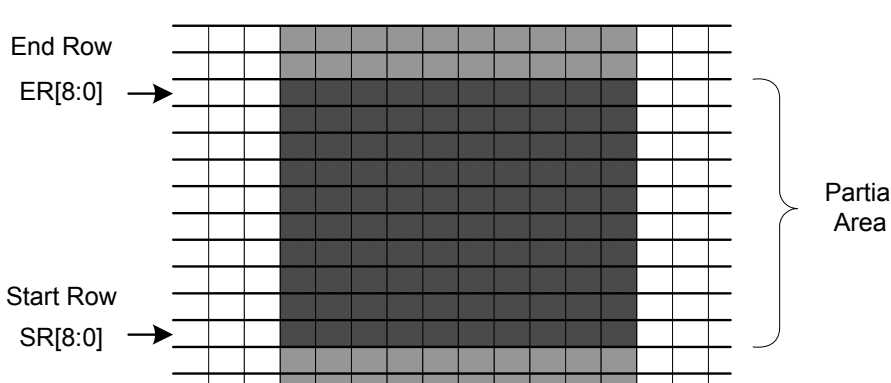
30H	Set_partial_area												HEX
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	1	↑	x	0	0	1	1	0	0	0	0	30
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SR8	000..1DFh
2 nd Parameter	1	1	↑	x	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
3 rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	ER8	000..1DFh
4 th Parameter	1	1	↑	x	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	

This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory

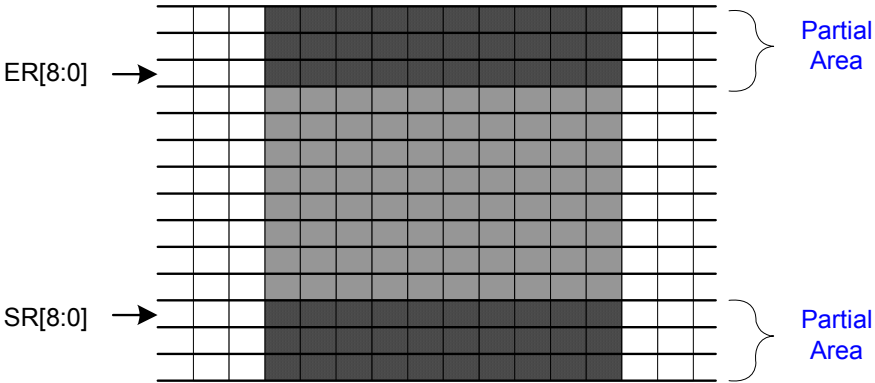
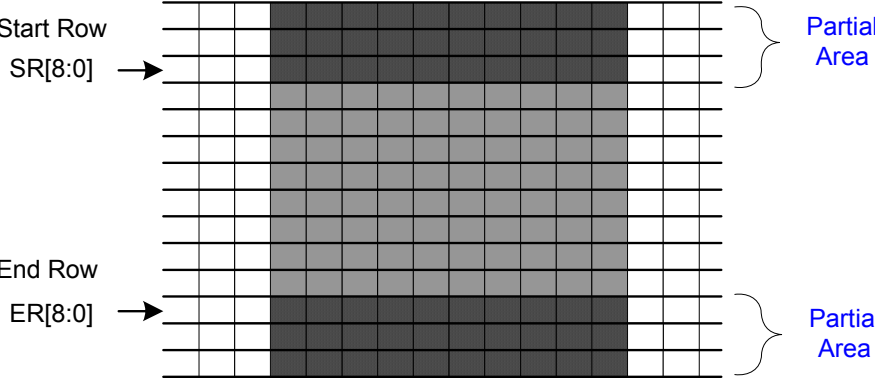
If End Row > Start Row and set_address_mode B4 = 0:

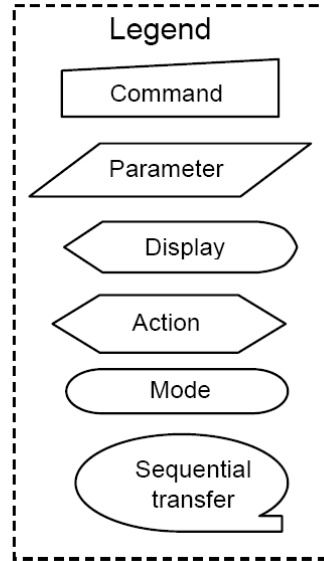
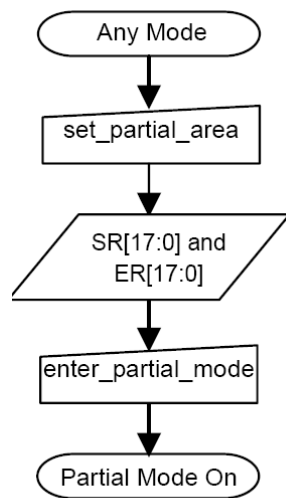


If End Row > Start Row and set_address_mode B4 = 1:

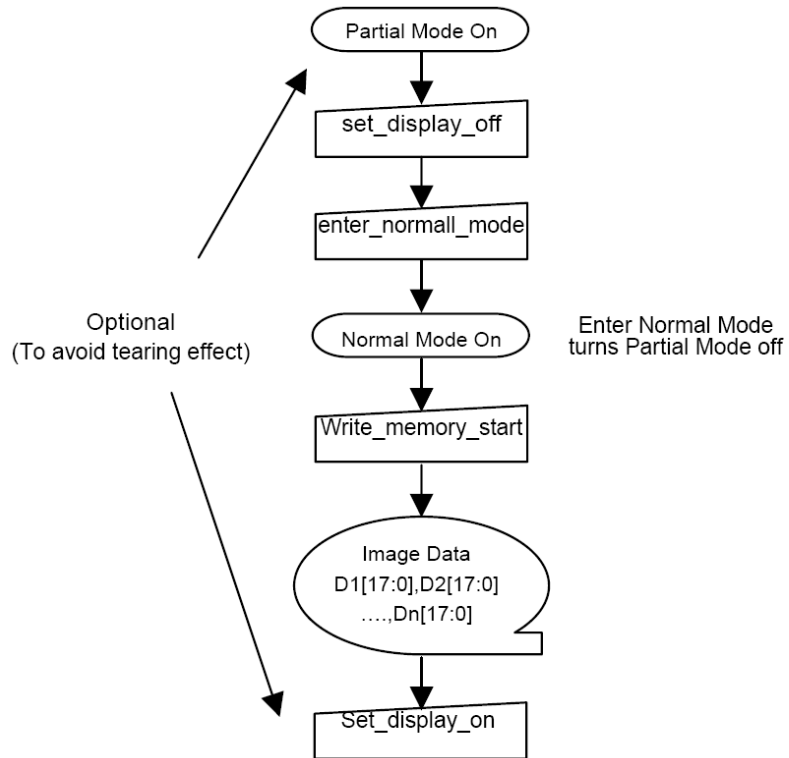


Description

	<p>End Row < Start Row (set_address_mode(36h) B4=0)</p>  <p>End Row < Start Row (set_address_mode(36h) B4=1)</p>  <p>If End Row = Start Row then the Partial Area will be one row deep.</p>												
Restriction	SR[15:0] and ER[15:0] cannot be 0000h nor exceed the last vertical line number (01DFh).												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SR[8:0]=0000_{HEX}</td> <td>ER[8:0]=1AF_{HEX}</td> </tr> <tr> <td>SW Reset</td> <td>SR[8:0]=0000_{HEX}</td> <td>ER[8:0]=1AF_{HEX}</td> </tr> <tr> <td>HW Reset</td> <td>SR[8:0]=0000_{HEX}</td> <td>ER[8:0]=1AF_{HEX}</td> </tr> </tbody> </table>	Status	Default Value		Power On Sequence	SR[8:0]=0000 _{HEX}	ER[8:0]=1AF _{HEX}	SW Reset	SR[8:0]=0000 _{HEX}	ER[8:0]=1AF _{HEX}	HW Reset	SR[8:0]=0000 _{HEX}	ER[8:0]=1AF _{HEX}
Status	Default Value												
Power On Sequence	SR[8:0]=0000 _{HEX}	ER[8:0]=1AF _{HEX}											
SW Reset	SR[8:0]=0000 _{HEX}	ER[8:0]=1AF _{HEX}											
HW Reset	SR[8:0]=0000 _{HEX}	ER[8:0]=1AF _{HEX}											
Flow Chart	1. To Enter Partial Mode												



2. To Leave Partial Mode



8.2.22. Set_scroll_area (33h)

33H	Set_scroll_area												HEX
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	1	↑	x	0	0	1	1	0	0	1	1	33
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	TFA [8]	0000
2 nd Parameter	1	1	↑	x	TFA [7]	TFA [6]	TFA [5]	TFA [4]	TFA [3]	TFA [2]	TFA [1]	TFA [0]	... 01E0
3 rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	VSA [8]	0000
4 th Parameter	1	1	↑	x	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]	... 01E0
5 th Parameter	1	1	↑	x	0	0	0	0	0	0	0	BFA [8]	0000
6 th Parameter	1	1	↑	x	BFA [7]	BFA [6]	BFA [5]	BFA [4]	BFA [3]	BFA [2]	BFA [1]	BFA [0]	... 01E0

This command defines the display vertical scrolling area.

set_address_mode (36h) B4 = 0:

The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



set_scroll_area set_address_mode B4 = 0 Example

set_address_mode (36h) B4 = 1:

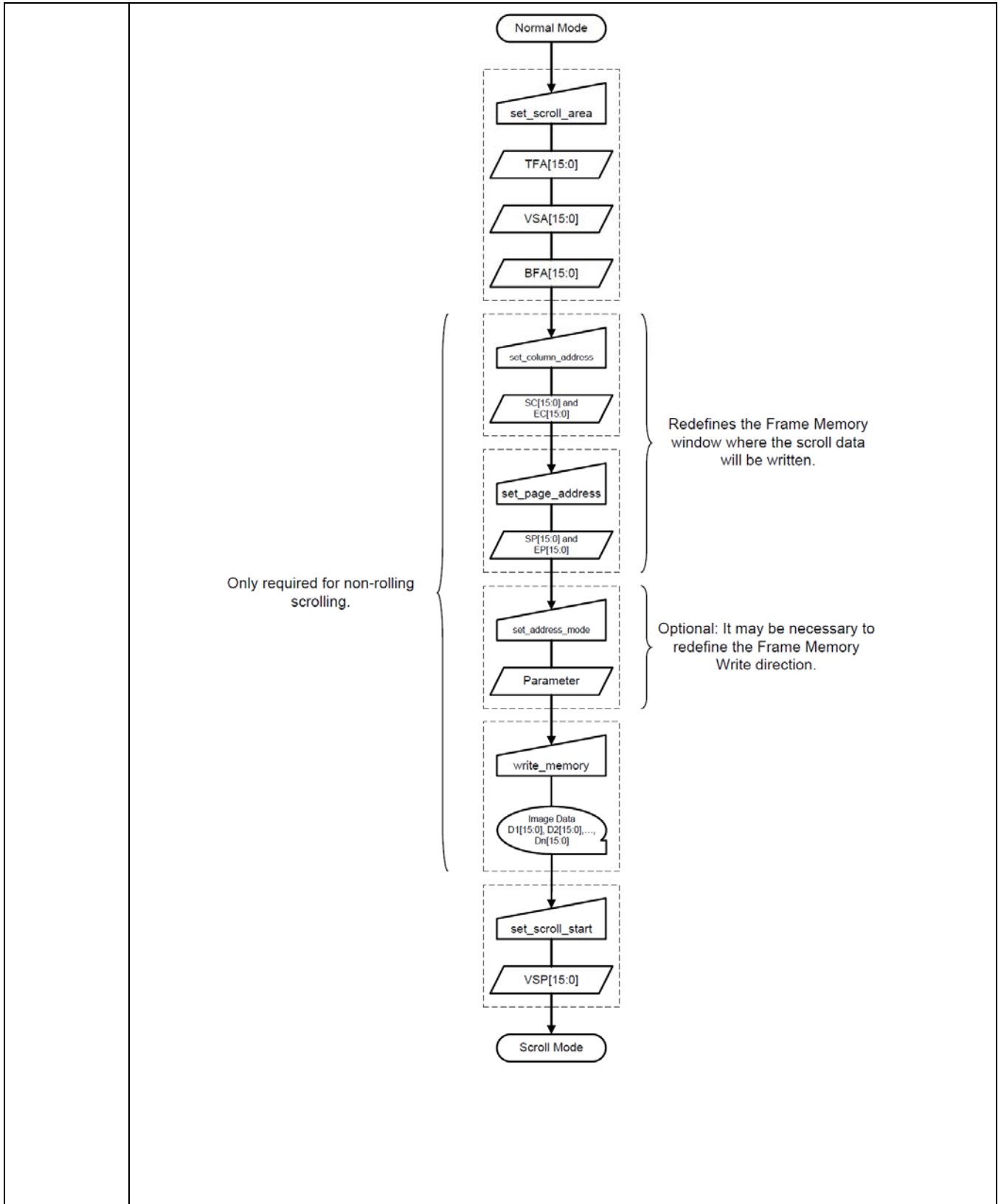
The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.

	<p style="text-align: center;">set_scroll_area set_address_mode B4 = 1 Example</p>																
Restriction	<p>The sum of TFA, VSA and BFA must equal the number of the display device's horizontal lines (pages), otherwise Scrolling mode is undefined. In Vertical Scroll Mode, set_address_mode B5 should be set to '0' – this only affects the Frame Memory Write.</p>																
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
Status	Availability																
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Sleep In	Yes																
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th colspan="3">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>TFA[8:0]=0000_{HEX}</td> <td>VSA[8:0]=01B0_{HEX}</td> <td>BFA[8:0]=0000_{HEX}</td> </tr> <tr> <td>SW Reset</td> <td>TFA [8:0]=0000_{HEX}</td> <td>VSA[8:0]=01B0_{HEX}</td> <td>BFA[8:0]=0000_{HEX}</td> </tr> <tr> <td>HW Reset</td> <td>TFA [8:0]=0000_{HEX}</td> <td>VSA[8:0]=01B0_{HEX}</td> <td>BFA[8:0]=0000_{HEX}</td> </tr> </tbody> </table>	Status	Default Value			Power On Sequence	TFA[8:0]=0000 _{HEX}	VSA[8:0]=01B0 _{HEX}	BFA[8:0]=0000 _{HEX}	SW Reset	TFA [8:0]=0000 _{HEX}	VSA[8:0]=01B0 _{HEX}	BFA[8:0]=0000 _{HEX}	HW Reset	TFA [8:0]=0000 _{HEX}	VSA[8:0]=01B0 _{HEX}	BFA[8:0]=0000 _{HEX}
Status	Default Value																
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SW Reset	TFA [8:0]=0000 _{HEX}	VSA[8:0]=01B0 _{HEX}	BFA[8:0]=0000 _{HEX}														
HW Reset	TFA [8:0]=0000 _{HEX}	VSA[8:0]=01B0 _{HEX}	BFA[8:0]=0000 _{HEX}														
Flow Chart	<p>1. To enter Vertical Scroll Mode:</p>																

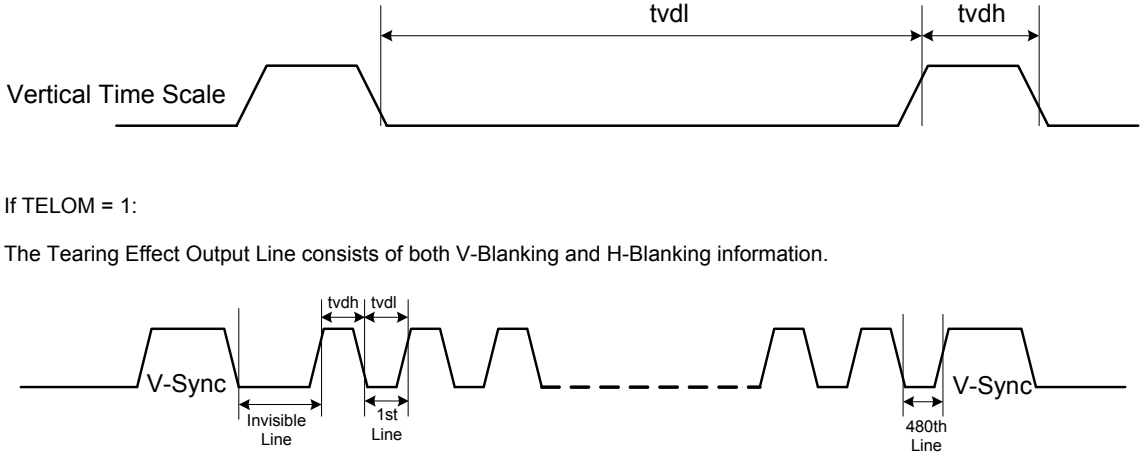
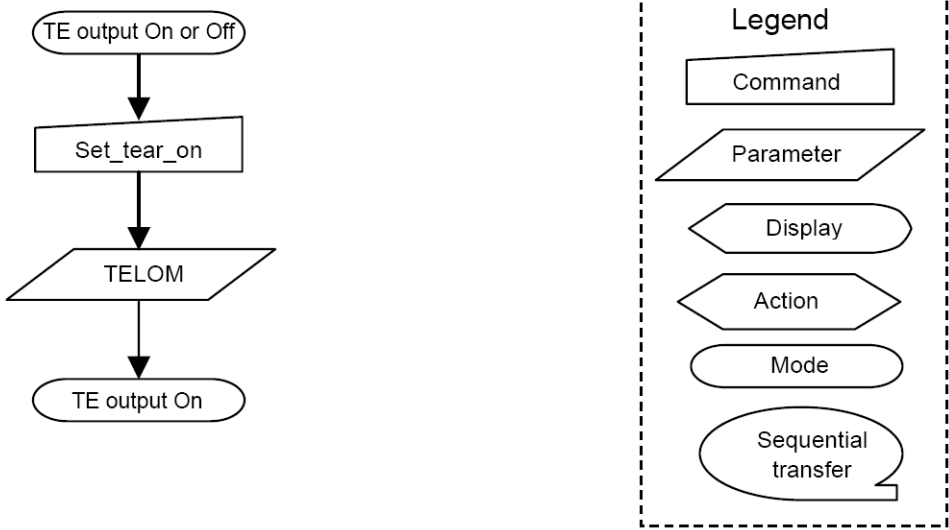


8.2.23. Set_tear_off (34h)

34H	Set_tear_off																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	0	1	0	0	34												
Parameter	NO PARAMETER																								
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.																								
Restriction	This command has no effect when the Tearing Effect output is already off.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	OFF																								
SW Reset	OFF																								
HW Reset	OFF																								
Flow Chart	<pre> graph TD A([TE output On or Off]) --> B[Set_tear_off] B --> C([TE output off]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Rounded rectangle Action: Pointed rectangle Mode: Oval Sequential transfer: Oval with tail 																								

8.2.24. Set_tear_on (35h)

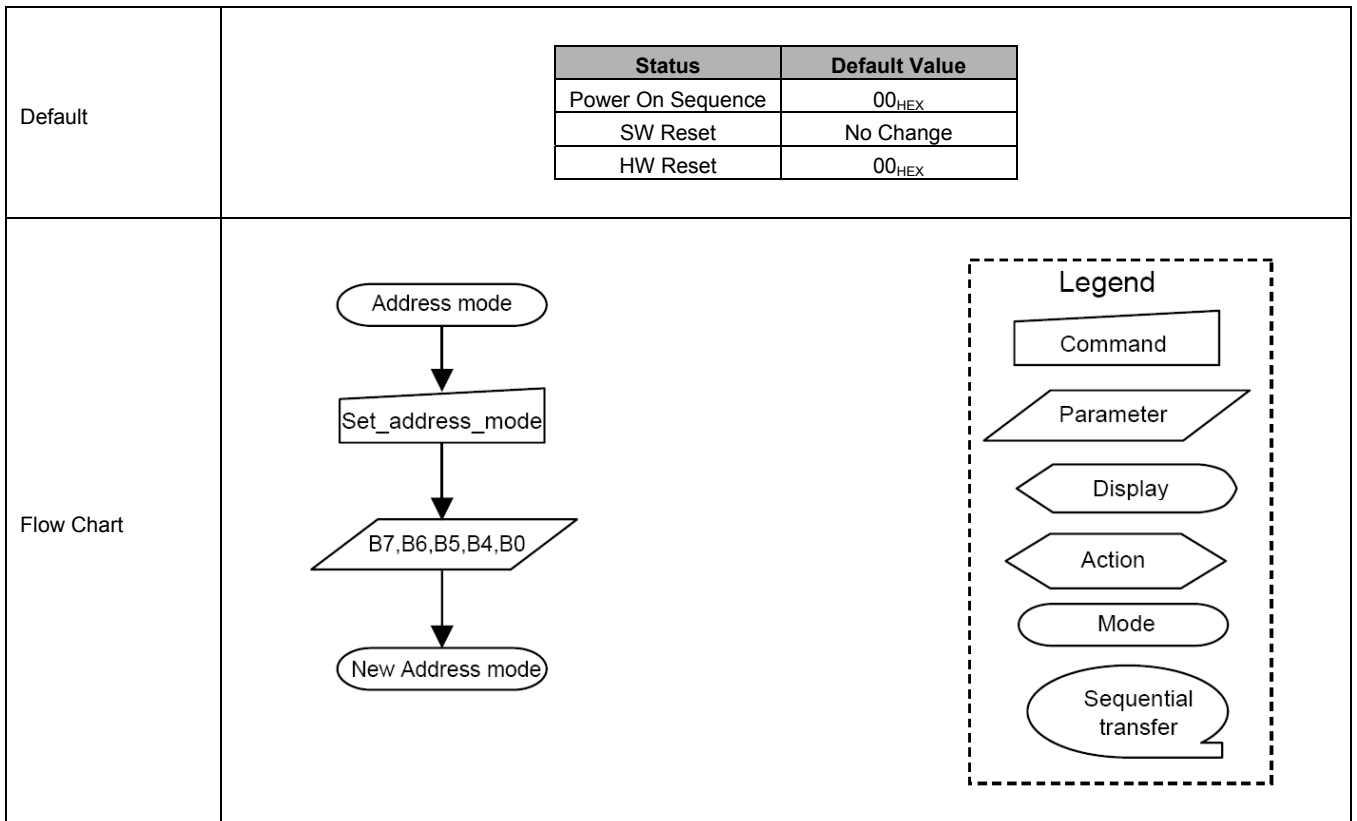
35H	Set_tear_on												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	0	1	35
1 st Parameter	1	1	↑	x	x	x	x	x	x	x	x	TELOM	xx
Description	<p>This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing set_address_mode (36h) bit B4 (Line Address Order).</p> <p>The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.</p> <p>If TELOM = 0: The Tearing Effect Output line consists of V-Blanking information only.</p>												

<p>Vertical Time Scale</p>	 <p>If TELOM = 1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.</p> <p>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p>												
<p>Restriction</p>	<p>This command has no effect when Tearing Effect output is already ON.</p>												
<p>Register Availability</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Sleep In	Yes												
<p>Default</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OFF</td> </tr> <tr> <td>SW Reset</td> <td>OFF</td> </tr> <tr> <td>HW Reset</td> <td>OFF</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF				
Status	Default Value												
Power On Sequence	OFF												
SW Reset	OFF												
HW Reset	OFF												
<p>Flow Chart</p>													

8.2.25. Set_address_mode (36h)

36H	Set_address_mode																																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command	0	1	↑	x	0	0	1	1	0	1	1	0	36																										
1 st Parameter	1	1	↑	x	B7	B6	B5	B4	B3	0	B1	B0	xx																										
Description	<p>This command defines read/write scanning direction of frame memory.</p> <p>This command makes no change on the other driver status.</p>																																						
	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>B7</td> <td>Page Address Order</td> <td></td> </tr> <tr> <td>B6</td> <td>Column Address Order</td> <td></td> </tr> <tr> <td>B5</td> <td>Page/Column Selection</td> <td></td> </tr> <tr> <td>B4</td> <td>Vertical Order</td> <td></td> </tr> <tr> <td>B3</td> <td>RGB/BGR Order</td> <td></td> </tr> <tr> <td>B2</td> <td>Display data latch data order</td> <td>Set to '0'</td> </tr> <tr> <td>B1</td> <td>Horizontal Flip</td> <td></td> </tr> <tr> <td>B0</td> <td>Vertical Flip</td> <td></td> </tr> </tbody> </table> <ul style="list-style-type: none"> • Bit B7 – Page Address Order <ul style="list-style-type: none"> '0' = Top to Bottom '1' = Bottom to Top • Bit B6 – Column Address Order <ul style="list-style-type: none"> '0' = Left to Right '1' = Right to Left • Bit B5 – Page/Column Order <ul style="list-style-type: none"> '0' = Normal Mode '1' = Reverse Mode • Bit B4 –Line Address Order <ul style="list-style-type: none"> '0' = LCD Refresh Top to Bottom '1' = LCD Refresh Bottom to Top • Bit B3 – RGB/BGR Order <ul style="list-style-type: none"> '0' = Pixels sent in RGB order '1' = Pixels sent in BGR order • Bit B2 –Display Data Latch Data Order <ul style="list-style-type: none"> This bit is not applicable for this project, so it is set to '0'. (Not supported) • Bit B1 – Horizontal Flip <ul style="list-style-type: none"> '0' = Normal display '1' = Flipped display • Bit B0 – Vertical Flip <ul style="list-style-type: none"> '0' = Normal display '1' = Flipped display <p>X = Don't care</p>													Bit	Description	Comment	B7	Page Address Order		B6	Column Address Order		B5	Page/Column Selection		B4	Vertical Order		B3	RGB/BGR Order		B2	Display data latch data order	Set to '0'	B1	Horizontal Flip		B0	Vertical Flip
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B4	Vertical Order																																						
B3	RGB/BGR Order																																						
B2	Display data latch data order	Set to '0'																																					
B1	Horizontal Flip																																						
B0	Vertical Flip																																						

	<table border="1"> <tr> <td>B5</td> <td>B6</td> <td>B7</td> <td>Image in Frame Memory</td> <td>B5</td> <td>B6</td> <td>B7</td> <td>Image in Frame Memory</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td></td> <td>1</td> <td>0</td> <td>0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td></td> <td>1</td> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td></td> <td>1</td> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td></td> <td>1</td> <td>1</td> <td>1</td> <td></td> </tr> </table>	B5	B6	B7	Image in Frame Memory	B5	B6	B7	Image in Frame Memory	0	0	0		1	0	0		0	0	1		1	0	1		0	1	0		1	1	0		0	1	1		1	1	1	
B5	B6	B7	Image in Frame Memory	B5	B6	B7	Image in Frame Memory																																		
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0	0	1		1	0	1																																			
0	1	0		1	1	0																																			
0	1	1		1	1	1																																			
	<p style="text-align: center;">B3 = 0</p> <p style="text-align: center;"> Memory Sent RGB Display Panel → </p> <p style="text-align: center;">B3 = 1</p> <p style="text-align: center;"> Memory Sent BGR Display Panel → </p>																																								
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Sleep In	Yes																																								



8.2.26. Set_scroll_start (37h)

37H	Set_scroll_start												HEX
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	1	↑	x	0	0	1	1	0	1	1	1	37
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	VSP [8]	xx
2 nd Parameter	1	1	↑	x	VSP [7]	VSP [6]	VSP [5]	VSP [4]	VSP [3]	VSP [2]	VSP [1]	VSP [0]	xx
Description	<p>This command sets the start of the vertical scrolling area in the frame memory. The vertical scrolling area is fully defined when this command is used with the set_scroll_area command</p> <p>The set_scroll_start command has one parameter, the Vertical Scroll Pointer. The VSP defines the line in the frame memory that is written to the display device as the first line of the vertical scroll area.</p> <p>The displayed image also depends on the setting of the Line Address Order bit, B4, in the set_address_mode register. See the examples below.</p> <p>If set_address_mode (R36h) B4 = 0:</p> <p>Example: When Top Fixed Area = Bottom Fixed Area = 0, Vertical Scrolling Area = 432 and VSP = 3.</p> <p>If set_address_mode (R36h) B4 = 1:</p> <p>Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 432 and VSP='3'.</p> <p>Note: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.</p>												
	Restriction	<p>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.</p>											

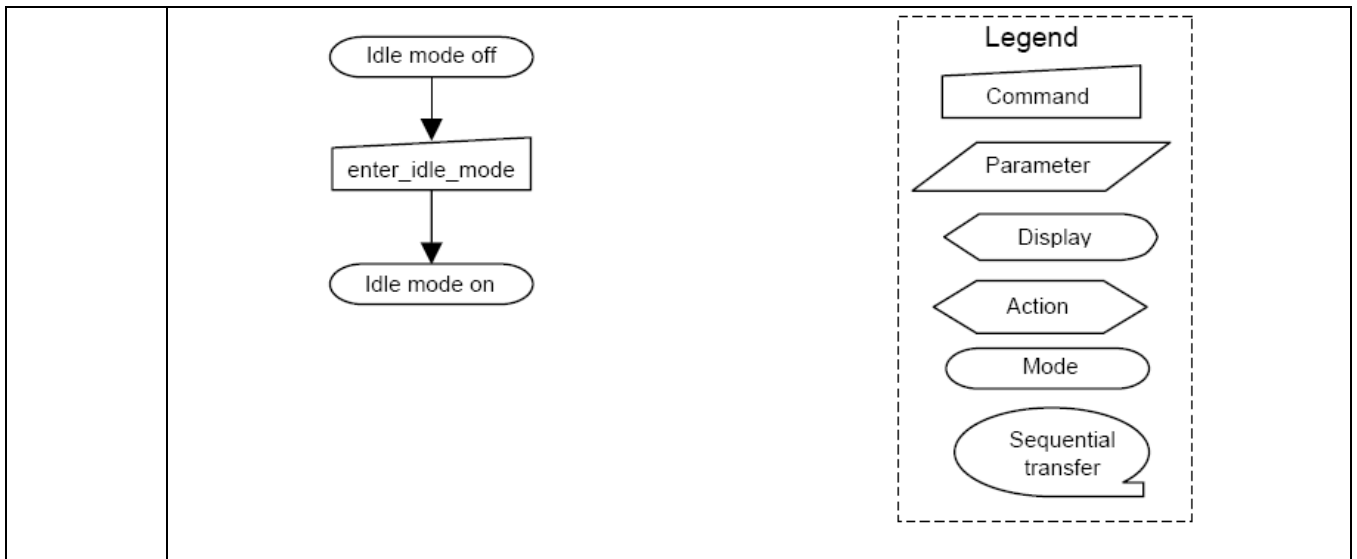
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>No</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>No</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
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	Status	Default Value												
	Power On Sequence	0000 _{HEX}												
	SW Reset	0000 _{HEX}												
HW Reset	0000 _{HEX}													
Flow Chart	Refer to the description set_scroll_area (33h)													

8.2.27. Exit_idle_mode (38h)

38H	Exit_idle_mode																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	1	0	0	0	38												
Parameter	NO PARAMETER																								
Description	This command causes the display module to exit Idle mode.																								
Restriction	This command has no effect when the display module is not in Idle mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	Idle Mode Off																								
SW Reset	Idle Mode Off																								
HW Reset	Idle Mode Off																								
Flow Chart	<pre> graph TD A([Idle mode on]) --> B[/Exit_idle_mode/] B --> C([Idle mode off]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Trapezoid Parameter: Parallelogram Display: Rounded rectangle Action: Pointed rectangle Mode: Oval Sequential transfer: Oval with tail 																								

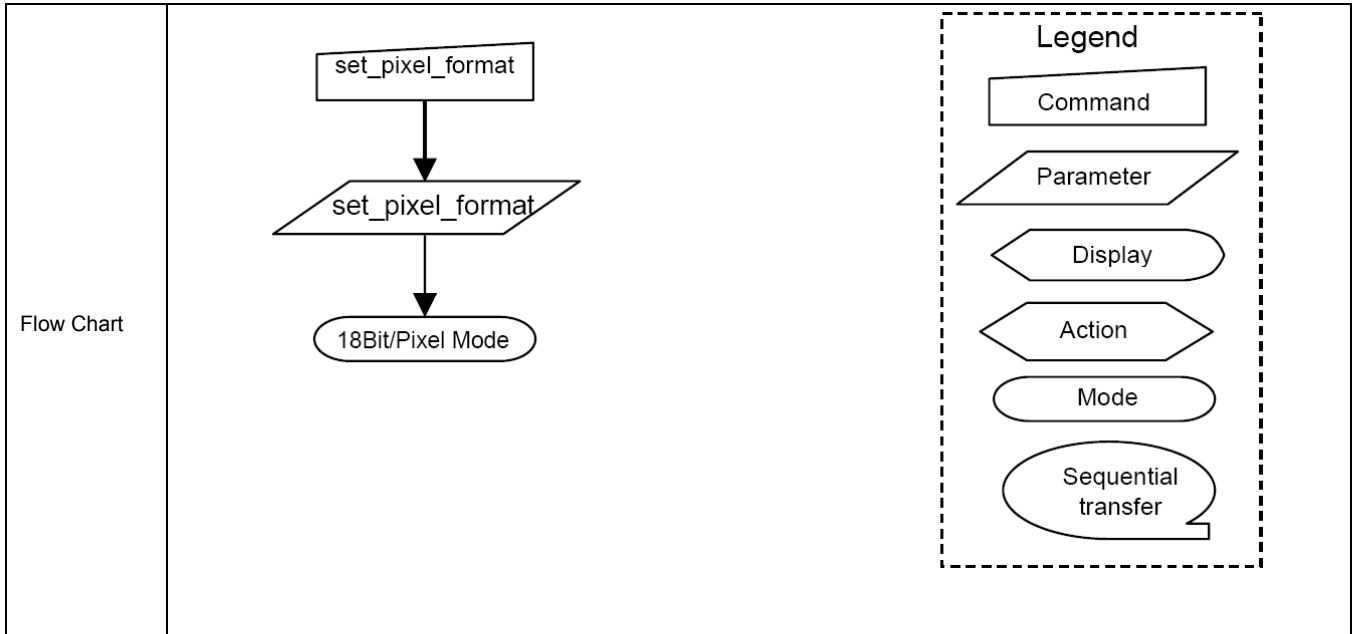
8.2.28. Enter_idle_mode (39h)

39H	Enter_idle_mode																																																
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	1	↑	x	0	0	1	1	1	0	0	1	39																																				
Parameter	NO PARAMETER																																																
Description	<p>This command causes the display module to enter Idle Mode.</p> <p>In Idle Mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the frame memory.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p> </div> <div style="font-size: 2em; margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Panel Display</p> </div> </div> <table border="1" style="margin-top: 10px; width: 100%; text-align: center;"> <thead> <tr> <th></th> <th>R5 R4 R3 R2 R1 R0</th> <th>G5 G4 G3 G2 G1 G0</th> <th>B5 B4 B3 B2 B1 B0</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Red</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Magenta</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Green</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>White</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> </tbody> </table>														R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0	Black	0XXXXX	0XXXXX	0XXXXX	Blue	0XXXXX	0XXXXX	1XXXXX	Red	1XXXXX	0XXXXX	0XXXXX	Magenta	1XXXXX	0XXXXX	1XXXXX	Green	0XXXXX	1XXXXX	0XXXXX	Cyan	0XXXXX	1XXXXX	1XXXXX	Yellow	1XXXXX	1XXXXX	0XXXXX	White	1XXXXX	1XXXXX	1XXXXX
		R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0																																													
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Blue	0XXXXX	0XXXXX	1XXXXX																																														
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Green	0XXXXX	1XXXXX	0XXXXX																																														
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Yellow	1XXXXX	1XXXXX	0XXXXX																																														
White	1XXXXX	1XXXXX	1XXXXX																																														
Restriction	This command has no effect when module is already in idle on mode.																																																
Register Availability	<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
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Status	Default Value																																																
Power On Sequence	Idle Mode Off																																																
SW Reset	Idle Mode Off																																																
HW Reset	Idle Mode Off																																																
Flow Chart																																																	



8.2.29. Set_pixel_format (3Ah)

3AH	Set_pixel_format																																															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
Command	0	1	↑	x	0	0	1	1	1	0	1	0	3A																																			
1 st Parameter	1	1	↑	x	x	D6	D5	D4	x	D2	D1	D0	66																																			
Description	<p>This command sets the pixel format for the RGB image data used by the interface.</p> <p>Bits D[6:4] – DPI Pixel Format Definition</p> <p>Bits D[2:0] – DBI Pixel Format Definition</p> <p>Bits D7 and D3 are not used.</p> <p>If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter are ignored.</p>																																															
	<table border="1"> <thead> <tr> <th>Control Interface Color Format</th> <th>D6/D2</th> <th>D5/D1</th> <th>D4/D0</th> </tr> </thead> <tbody> <tr> <td>Not defined</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>3bit/pixel (8 color)</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Not defined</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Not defined</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Not defined</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>16bit/pixel (65,536 colors)</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>18bit/pixel (262,144 colors)</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>Not defined</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>													Control Interface Color Format	D6/D2	D5/D1	D4/D0	Not defined	0	0	0	3bit/pixel (8 color)	0	0	1	Not defined	0	1	0	Not defined	0	1	1	Not defined	1	0	0	16bit/pixel (65,536 colors)	1	0	1	18bit/pixel (262,144 colors)	1	1	0	Not defined	1	1
Control Interface Color Format	D6/D2	D5/D1	D4/D0																																													
Not defined	0	0	0																																													
3bit/pixel (8 color)	0	0	1																																													
Not defined	0	1	0																																													
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16bit/pixel (65,536 colors)	1	0	1																																													
18bit/pixel (262,144 colors)	1	1	0																																													
Not defined	1	1	1																																													
Restriction	There is no visible effect until the Frame Memory is written to.																																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																							
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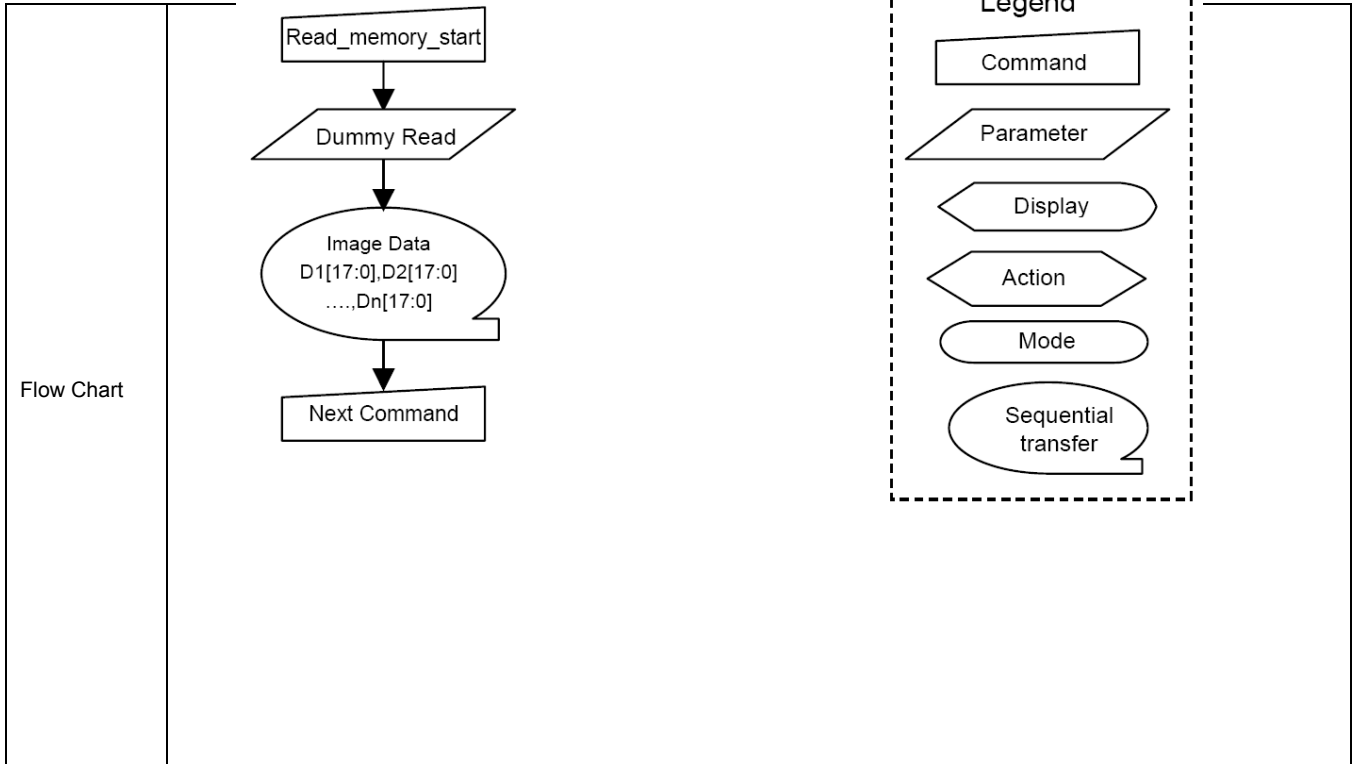
8.2.30. Write_Memory_Continue (3Ch)

3CH	Write_Memory_Continue												HEX
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	1	↑	x	0	0	1	1	1	1	0	0	3C
1 st Parameter	1	1	↑	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF
x st Parameter	1	1	↑	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF
N st Parameter	1	1	↑	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF
Description	<p>This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.</p> <p>If set_address_mode B5 = 0:</p> <p>Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds $(EC - SC + 1) * (EP - SP + 1)$ the extra pixels are ignored.</p> <p>If set_address_mode B5 = 1:</p> <p>Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds $(EC - SC + 1) * (EP - SP + 1)$ the extra pixels are ignored.</p> <p>Sending any other command can stop frame Write.</p> <p>Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds $(EC-SC+1)*(EP-SP+1)$, the exceeding data will be ignored.</p> <p>Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds $(EC-SC+1)*(EP-SP+1)$, the column and page number will be reset, and the exceeding data will be written into the following column and page.</p>												
Restriction	<p>A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.</p>												

Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>No</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	No												
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Status	Default Value												
Power On Sequence	Random value												
SW Reset	No change												
HW Reset	No change												
Flow Chart	<pre> graph TD A[Write_memory_continue] --> B((Image Data D1[17:0],D2[17:0],Dn[17:0])) B --> C[Next Command] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Pointed rectangle Action: Pointed rectangle Mode: Rounded rectangle Sequential transfer: Oval with tail 												

8.2.31. Read_Memory_Continue (3Eh)

3EH	Read_Memory_Continue																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	1	1	1	0	3E												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x												
2 nd Parameter	1	↑	1	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF												
x st Parameter	1	↑	1	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF												
N st Parameter	1	↑	1	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF												
Description	<p>This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue (3Eh) or read_memory_start (2Eh) command.</p> <p>If set_address_mode B5 = 0:</p> <p>Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command.</p> <p>If set_address_mode B5 = 1:</p> <p>Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command.</p> <p>This command makes no change to the other driver status.</p>																								
Restriction	A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	Random data																								
SW Reset	No change																								
HW Reset	No change																								



8.2.32. Set_Tear_Scanline (44h)

44H	Set_Tear_Scanline												HEX												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0													
Command	0	1	↑	x	0	1	0	0	0	1	0	0	44												
1 st Parameter	1	1	↑	xx	0	0	0	0	0	0	0	STS [8]	0x												
2 nd Parameter	1	1	↑	xx	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	xx												
Description	<p>This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.</p> <p>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p>																								
Restriction	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
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Status	Default Value								
Power On Sequence	00 _{HEX}								
SW Reset	00 _{HEX}								
HW Reset	00 _{HEX}								
Flow Chart	<pre> graph TD Start([TE Output On or Off]) --> Command[set_tear_scanline] Command --> Param1[/Send 1st parameter STS[8]/] Param1 --> Param2[/Send 2nd parameter STS[7:0]/] Param2 --> End([TE Output On the Nth line]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

8.2.33. Get_Scanline (45h)

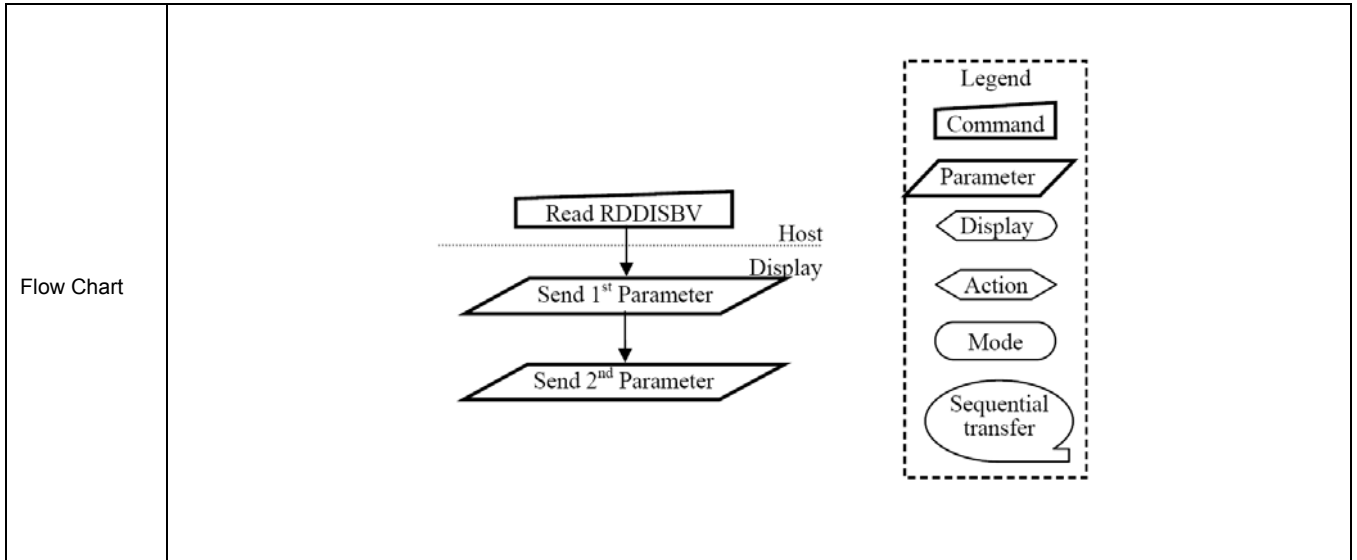
45H	Get_Scanline																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	1	0	0	0	1	0	1	45												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x												
2 nd Parameter	1	↑	1	xx	0	0	0	0	0	0	0	GTS [8]	0x												
3 rd Parameter	1	↑	1	xx	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	xx												
Description	<p>The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.</p> <p>When in Sleep Mode, the value returned by get_scanline is undefined.</p>																								
Restriction	None																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	00 _{HEX}																								
SW Reset	00 _{HEX}																								
HW Reset	00 _{HEX}																								
Flow Chart	<pre> graph TD A[get_scanline] --> B[/Wait 3us/] B --> C[/Dummy Read/] C --> D[/Send 1st parameter GTS[9:8]/] D --> E[/Send 2nd parameter GTS[7:0]/] </pre>																								

8.2.34. Write Display Brightness (51h)

51H	WRDISBV (Write Display Brightness)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	1	0	1	0	0	0	1	51												
1 st Parameter	1	↑	1	xx	DBV [7]	DBV [6]	DBV [5]	DBV [4]	DBV [3]	DBV [2]	DBV [1]	DBV [0]	00 .. FF												
Description	<p>This command is used to adjust the brightness value of the display.</p> <p>It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification.</p> <p>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p>																								
Restriction	None																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	00 _{HEX}																								
SW Reset	00 _{HEX}																								
HW Reset	00 _{HEX}																								
Flow Chart	<pre> graph TD A[WRDISBV] --> B[/DBV[7..0]/] B --> C{{New Display Brightness Value Loaded}} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Hexagon Action: Pentagon Mode: Oval Sequential transfer: Dashed line 																								

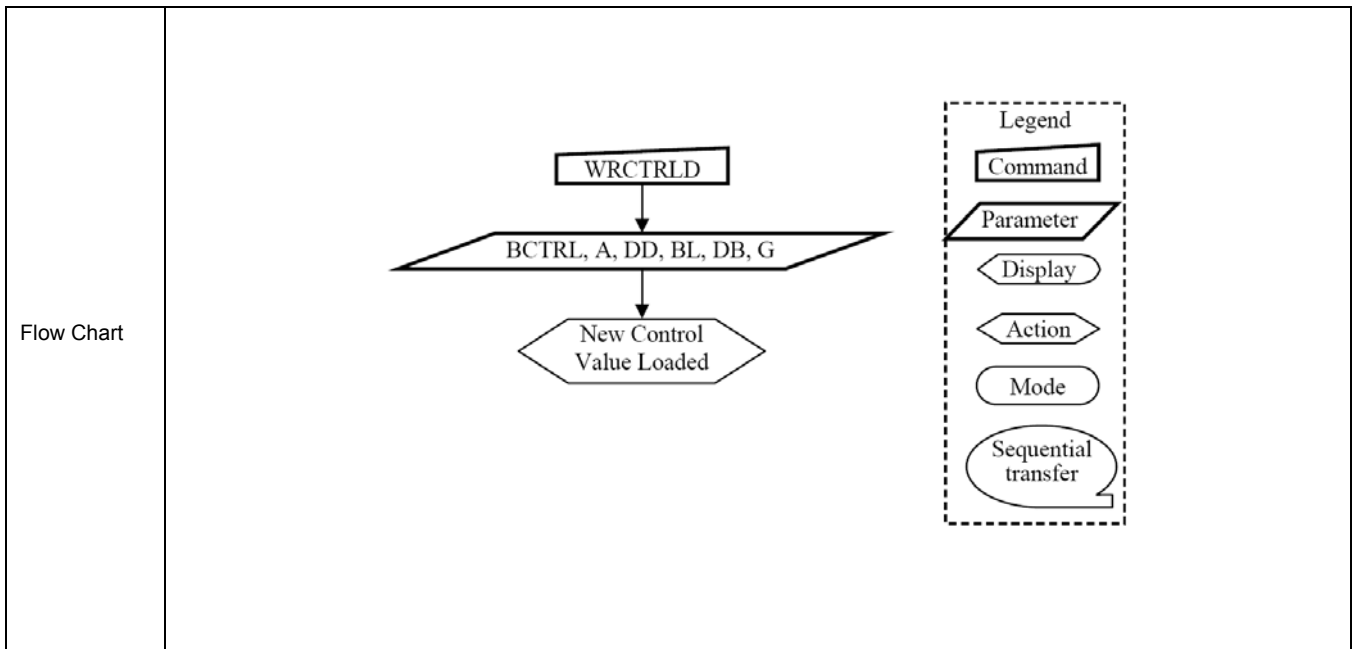
8.2.35. Read Display Brightness (52h)

52H	RDISBV (Read Display Brightness Value)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	1	0	1	0	0	1	0	52												
1 st Parameter	1	↑	1	xx	x	x	x	x	x	x	x	x	x												
2 nd Parameter	1	↑	1	xx	DBV [7]	DBV [6]	DBV [5]	DBV [4]	DBV [3]	DBV [2]	DBV [1]	DBV [0]	xx												
Description	<p>This command returns the brightness value of the display.</p> <p>It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>This command can be used to read the brightness value of the display also when Display brightness control is in automatic mode.</p> <p>Write CTRL Display (53h)" bit DB = '1'.</p> <p>DBV[7:0] is reset when display is in sleep-in mode.</p> <p>DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (53h)" command is '0'.</p> <p>DBV[7:0] is manual set brightness specified with "Write CTRL Display (53h)" command when bit BCTRL is '1' and bit A of "Write CTRL Display (53h)" command is '0'.</p>																								
Restriction	<p>The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI Mode.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																								
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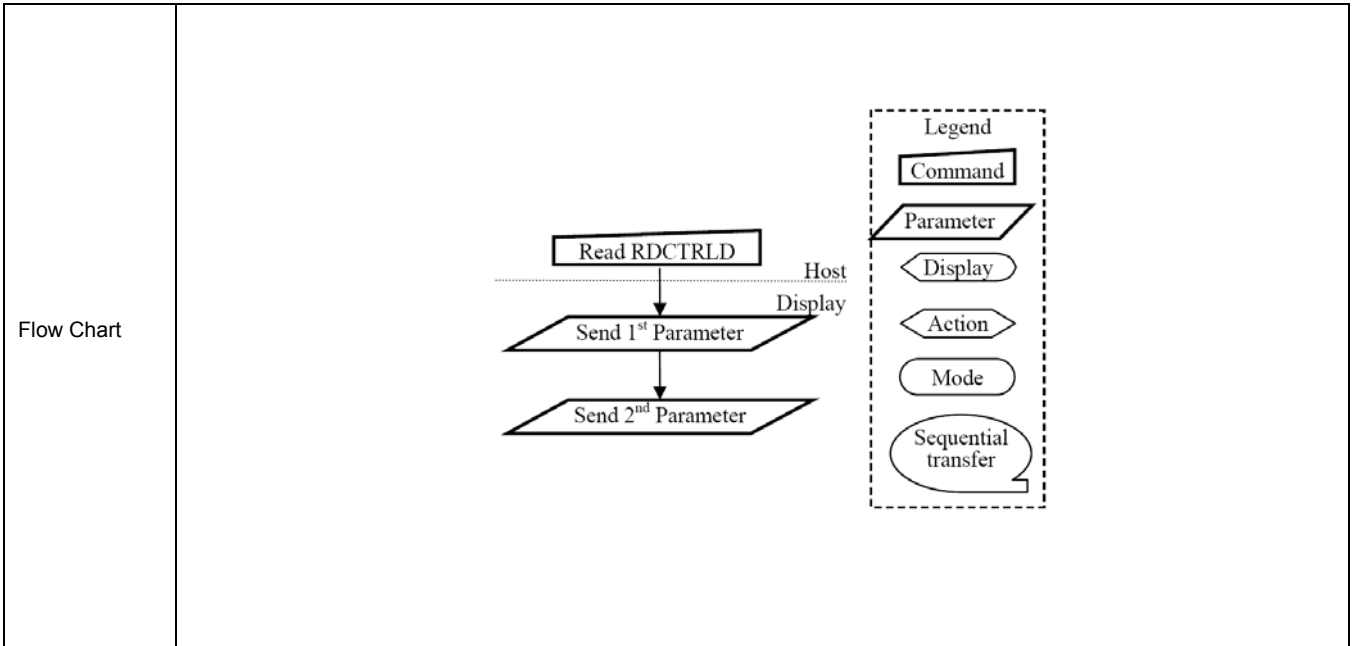
8.2.36. Write CTRL Display (53h)

53H	WRCTRLD (Write Control Display)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	1	0	1	0	0	1	1	53												
1 st Parameter	1	↑	1	xx	0	0	BCTRL	0	DD	BL	0	0	xx												
Description	<p>This command is used to control display brightness.</p> <p>BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.</p> <p>0 = Off (Brightness registers are 00h, DBV[7..0])</p> <p>1 = On (Brightness registers are active, according to the other parameters.)</p> <p>Display Dimming (DD): (Only for manual brightness setting)</p> <p>DD = 0: Display Dimming is off</p> <p>DD = 1: Display Dimming is on</p> <p>BL: Backlight Control On/Off</p> <p>0 = Off (Completely turn off backlight circuit. Control lines must be low.)</p> <p>1 = On</p> <p>Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 → 1 or 1 → 0.</p> <p>When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.</p>																								
Restriction	None																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	BCTRL=0, DD=0, BL=0																								
SW Reset	BCTRL=0, DD=0, BL=0																								
HW Reset	BCTRL=0, DD=0, BL=0																								



8.2.37. Read CTRL Display (54h)

54H	RDCTRLD (Read Control Display)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	1	0	1	0	1	0	0	54												
1 st Parameter	1	↑	1	xx	x	x	x	x	x	x	x	x	xx												
2 nd Parameter	1	↑	1	xx	0	0	BCTRL	0	DD	BL	0	0	xx												
Description	<p>This command is used to return brightness setting.</p> <p>BCTRL: Brightness Control Block On/Off, '0' = Off (Brightness registers are 00h) '1' = On (Brightness registers are active, according to the DBV[7..0] parameters.)</p> <p>DD: Display Dimming '0' = Display Dimming is off '1' = Display Dimming is on</p> <p>BL: Backlight On/Off '0' = Off (Completely turn off backlight circuit. Control lines must be low.) '1' = On</p>																								
Restriction	<p>The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	BCTRL=0, DD=0, BL=0, DB=0																								
SW Reset	BCTRL=0, DD=0, BL=0, DB=0																								
HW Reset	BCTRL=0, DD=0, BL=0, DB=0																								



8.2.38. Write Content Adaptive Brightness Control (55h)

55H	WRCABC (Write Content Adaptive Brightness Control)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	1	0	1	0	1	0	1	55												
1 st Parameter	1	↑	1	xx	0	0	0	0	0	0	C[1]	C[0]	xx												
Description	<p>This command is used to set parameters for image content based adaptive brightness control functionality.</p> <p>There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>C[1:0]</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>2'b00</td> <td>Off</td> </tr> <tr> <td>2'b01</td> <td>User Interface Image</td> </tr> <tr> <td>2'b10</td> <td>Still Picture</td> </tr> <tr> <td>2'b11</td> <td>Moving Image</td> </tr> </tbody> </table>													C[1:0]	Default Value	2'b00	Off	2'b01	User Interface Image	2'b10	Still Picture	2'b11	Moving Image		
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2'b11	Moving Image																								
Restriction	None																								
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Power On Sequence	C[1:0]=00 _{HEX}																								
SW Reset	C[1:0]=00 _{HEX}																								
HW Reset	C[1:0]=00 _{HEX}																								
Flow Chart	<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;"> <pre> graph TD WRCABC[WRCABC] --> Param[/1st parameter: C[1:0]/] Param --> Mode{{New Adaptive Image Mode}} </pre> </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command: [] Parameter: / / Display: < > Action: < > Mode: () Sequential transfer: () </div> </div>																								

8.2.39. Read Content Adaptive Brightness Control (56h)

56H	RDCABC (Read Content Adaptive Brightness Control)												HEX												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0													
Command	0	1	↑	x	0	1	0	1	0	1	1	0	56												
1 st Parameter	1	↑	1	xx	x	x	x	x	x	x	x	x	xx												
2 nd Parameter	1	↑	1	xx	0	0	0	0	0	0	C[1]	C[0]	xx												
Description	<p>This command is used to read the settings for image content based adaptive brightness control functionality.</p> <p>It is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>C[1:0]</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>2'b00</td> <td>Off</td> </tr> <tr> <td>2'b01</td> <td>User Interface Image</td> </tr> <tr> <td>2'b10</td> <td>Still Picture</td> </tr> <tr> <td>2'b11</td> <td>Moving Image</td> </tr> </tbody> </table>													C[1:0]	Default Value	2'b00	Off	2'b01	User Interface Image	2'b10	Still Picture	2'b11	Moving Image		
C[1:0]	Default Value																								
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2'b01	User Interface Image																								
2'b10	Still Picture																								
2'b11	Moving Image																								
Restriction	<p>The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																								
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Power On Sequence	C[1:0]=00 _{HEX}																								
SW Reset	C[1:0]=00 _{HEX}																								
HW Reset	C[1:0]=00 _{HEX}																								
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD subgraph Host A[Read RDCABC] end subgraph Display B[/Send 1st Parameter/] C[/Send 2nd Parameter/] end A --> B B --> C </pre> </div> <div style="flex: 0.5; border: 1px dashed black; padding: 5px; margin-left: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																								

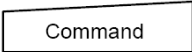
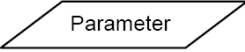
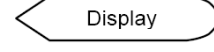
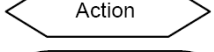
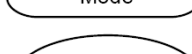
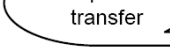
8.2.40. Write CABC Minimum Brightness (5Eh)

B8H	Backlight Control 1												HEX												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0													
Command	0	1	↑	xx	1	0	1	1	1	1	0	0	0	B8											
1 st parameter	0	↑	1	xx	CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1]	CMB[0]	CMB[7]	FF											
Description	<p>This command is used to set the minimum brightness value of the display for CABC function.</p> <p>CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.</p> <p>When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness cannot be changed.</p> <p>This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.</p> <p>When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is ignored.</p> <p>In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	00h																								
SW Reset	No Change																								
HW Reset	00h																								

8.2.41. Read CABC Minimum Brightness (5Fh)

B8H	Backlight Control 1																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	xx	1	0	1	1	1	0	0	0	B8												
1 st parameter	0	↑	1	xx	CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1]	CMB[0]	FF												
Description	<p>This command returns the minimum brightness value of CABC function.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (5Eh)" command. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	00h																								
SW Reset	No Change																								
HW Reset	00h																								

8.2.42. Read_DDB_Start (A1h)

A1H	Read_DDB_Start																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	0	1	0	0	0	0	1	A1												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x												
2 nd Parameter	1	↑	1	xx	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	xx												
3 rd Parameter	1	↑	1	xx	1	1	1	1	1	1	1	1	FF												
Description	This 1 st parameter: Dummy read 2 nd parameter: ID code[7:0] 3 th parameter: Exit code (FFh).																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Flow Chart	<div style="border: 1px dashed black; padding: 10px; text-align: center;"> <p>Legend</p> <p>Command: </p> <p>Parameter: </p> <p>Display: </p> <p>Action: </p> <p>Mode: </p> <p>Sequential transfer: </p> </div>																								

8.2.43. Command Access Protect (B0h)

B0H	Command Access Protect																																															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
Command	0	1	↑	xx	1	0	1	1	0	0	0	0	B0																																			
1 st parameter	0	1	↑	xx	0	0	0	0	0	0	MCAP[1]	MCAP[0]	00																																			
Description	<table border="1"> <thead> <tr> <th rowspan="2">MCAP[1:0]</th> <th>User Command</th> <th>Protect command</th> <th colspan="3">Manufacturer Command</th> </tr> <tr> <th>00h ~ AFh</th> <th>B0h</th> <th>B1h ~ DFh</th> <th>E0h~EFh</th> <th>F0h~FFh</th> </tr> </thead> <tbody> <tr> <td>2'b00</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> </tr> <tr> <td>2'b01</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> <td>No</td> </tr> <tr> <td>2'b10</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> <td>No</td> <td>No</td> </tr> <tr> <td>2'b11</td> <td>Yes</td> <td>Yes</td> <td>No</td> <td>No</td> <td>No</td> </tr> </tbody> </table>													MCAP[1:0]	User Command	Protect command	Manufacturer Command			00h ~ AFh	B0h	B1h ~ DFh	E0h~EFh	F0h~FFh	2'b00	Yes	Yes	Yes	Yes	Yes	2'b01	Yes	Yes	Yes	Yes	No	2'b10	Yes	Yes	Yes	No	No	2'b11	Yes	Yes	No	No	No
	MCAP[1:0]	User Command	Protect command	Manufacturer Command																																												
		00h ~ AFh	B0h	B1h ~ DFh	E0h~EFh	F0h~FFh																																										
	2'b00	Yes	Yes	Yes	Yes	Yes																																										
	2'b01	Yes	Yes	Yes	Yes	No																																										
	2'b10	Yes	Yes	Yes	No	No																																										
2'b11	Yes	Yes	No	No	No																																											
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Flow Chart	<pre> graph TD A([Sleep Mode]) --> B[Low Power Mode Control] B --> C[/DSTB=1/] C --> D([Deepstandby Mode]) </pre>																																															

8.2.44. Low Power Mode Control (B1h)

B1H	Low Power Mode Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	0	0	0	1	B1
1 st parameter	0	1	↑	xx	0	0	0	0	0	0	0	DSTB	0

DSTB

The driver enters the deep standby mode when DSTB=1. Internal logic power supply circuit is turned down enabling low power consumption. In the deep standby mode, data stored in the Frame Memory and the Instructions are not retained. Re-write them after the deep standby mode is necessary.

There are two ways to wake up deep standby mode,

1. Reset the ILI9327 and re-write the initial code
2. Toggle CSX pin High → Low → High 6 times to quit the deep standby mode.

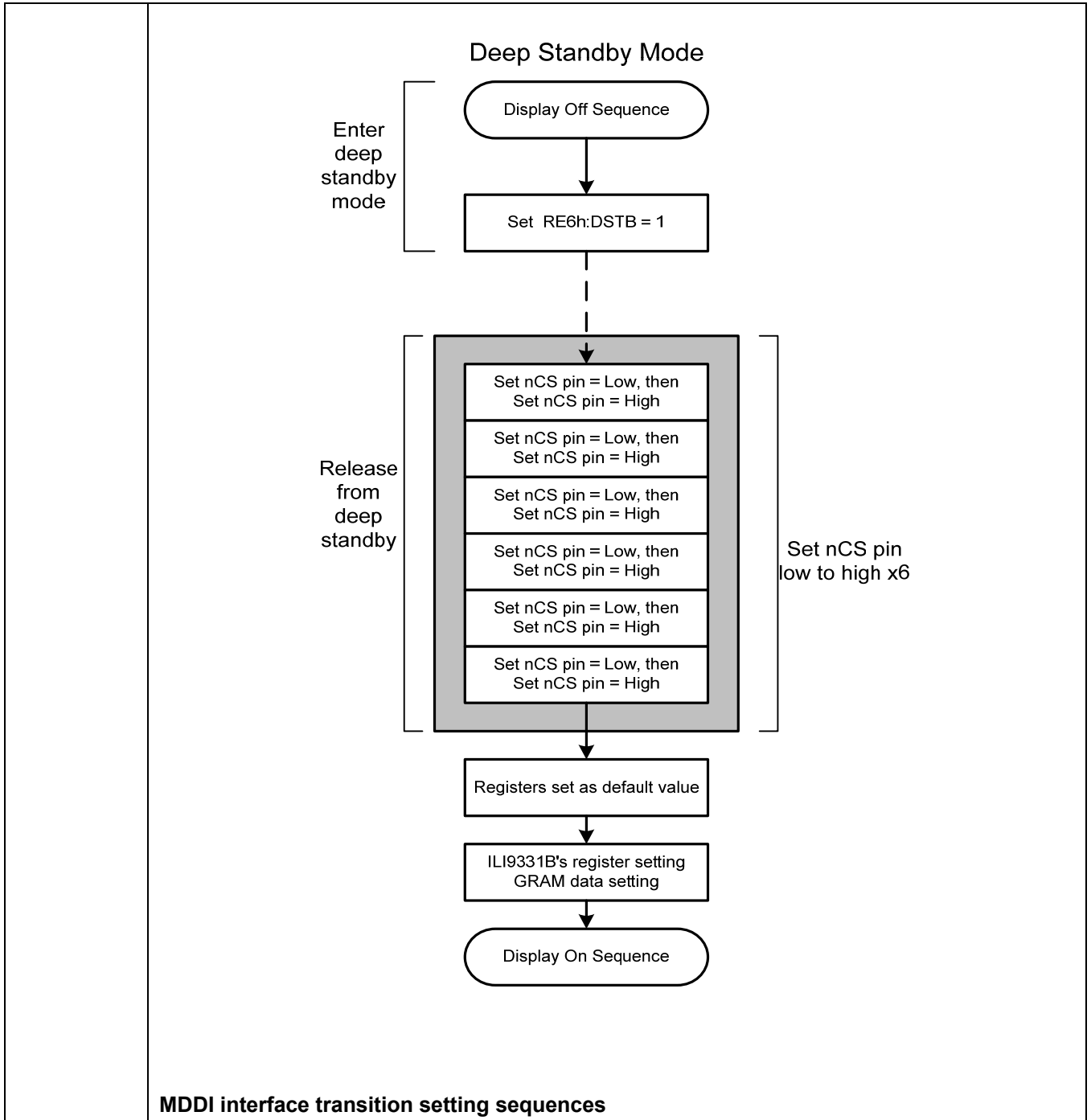
Basic operation

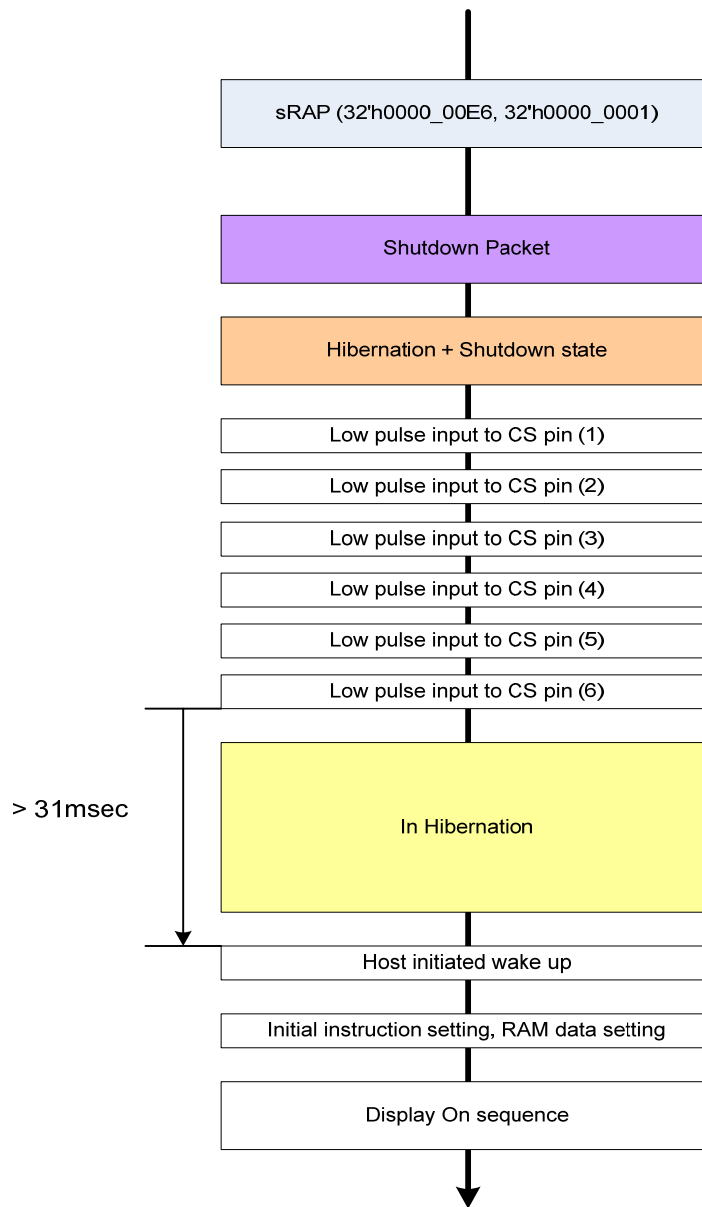
The basic operation modes of 9327 are as shown in the following diagram.

```

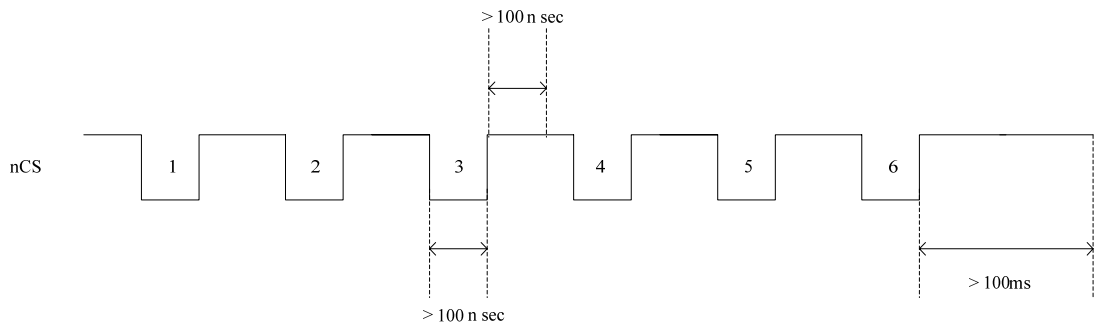
graph TD
    DisplayOn[Display On] --> DisplayOff[Display Off]
    DisplayOff --> DisplayOn
    DisplayOff -- DSTBY --> DeepStandby[Deep Standby]
    DeepStandby -- Exit --> Reset[Reset]
    Reset -- Initial --> DisplayOff
    RESET --> Reset
  
```

CPU interface transition setting sequences





The timing requirement of the pulse is shown as below.



Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value												
Power On Sequence	DSTB=1'b0												
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HW Reset	DSTB=1'b0												
Flow Chart	<pre> graph TD A([Sleep Mode]) --> B[Low Power Mode Control] B --> C[/DSTB=1/] C --> D([Deepstandby Mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Rounded rectangle Action: Pointed rectangle Mode: Oval Sequential transfer: Oval with tail 												

8.2.45. Frame Memory Access and Interface Setting (B3h)

B3H	Frame Memory Access and Interface Setting																																																
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	1	↑	xx	1	0	1	1	0	0	1	1	B3																																				
1 st parameter	0	1	↑	xx	0	0	0	0	0	0	WEMODE	0	02																																				
1 st parameter	0	1	↑	xx	0	0	0	0	0	TEI[2]	TEI[10]	TEI[0]	00																																				
2 nd parameter	0	1	↑	xx	0	0	0	0	0	DENC[2]	DENC[1]	DENC[0]	00																																				
4 th parameter	0	1	↑	xx	0	0	EPF[1]	EPF[0]	0	0	0	DFM	20																																				
Description	<p>WEMODE: Memory write control</p> <p>WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.</p> <p>WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.</p> <p>TEI[2:0]: ILI9327 starts to output TE signal in the output interval set by TEI[2:0] bits.</p> <table border="1"> <thead> <tr> <th>TEI[2:0]</th> <th>Output Interval</th> </tr> </thead> <tbody> <tr> <td>3'b000</td> <td>1 frame</td> </tr> <tr> <td>3'b001</td> <td>2 frame</td> </tr> <tr> <td>3'b011</td> <td>4 frame</td> </tr> <tr> <td>3'b101</td> <td>6 frame</td> </tr> <tr> <td>Others</td> <td>Setting Prohibited</td> </tr> </tbody> </table> <p>DENC[2:0]: Set the GRAM write cycle through the RGB interface</p> <table border="1"> <thead> <tr> <th>DENC[2:0]</th> <th>GRAM Write Cycle (Frame periods)</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>1 Frame</td> </tr> <tr> <td>001</td> <td>2 Frames</td> </tr> <tr> <td>010</td> <td>3 Frames</td> </tr> <tr> <td>011</td> <td>4 Frames</td> </tr> <tr> <td>100</td> <td>5 Frames</td> </tr> <tr> <td>101</td> <td>6 Frames</td> </tr> <tr> <td>110</td> <td>7 Frames</td> </tr> <tr> <td>111</td> <td>8 Frames</td> </tr> </tbody> </table> <p>DFM: The bit is used to define image data write/read format to the Frame Memory in DBI Type B (16bit bus interface) and DBI Type C serial interface operation.</p> <p>EPF[1:0] Set the data format when 16bbp (R,G,B) to 18 bbp (r, g, b) is stored in the internal GRAM.</p> <table border="1"> <thead> <tr> <th>EPF[1:0]</th> <th>Expand 16bbp (R,G,B) to 18 bbp (R, G, B)</th> </tr> </thead> <tbody> <tr> <td>00</td> <td> "0" is inputted to LSB $r[5:0] = \{R[4:0], 0\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], 0\}$ Exception: $R[4:0], B[4:0]=5'h1F \rightarrow r[5:0], b[5:0] = 6'h3F$ </td> </tr> <tr> <td>01</td> <td> "1" is inputted to LSB $r[5:0] = \{R[4:0], 1\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], 1\}$ </td> </tr> </tbody> </table>													TEI[2:0]	Output Interval	3'b000	1 frame	3'b001	2 frame	3'b011	4 frame	3'b101	6 frame	Others	Setting Prohibited	DENC[2:0]	GRAM Write Cycle (Frame periods)	000	1 Frame	001	2 Frames	010	3 Frames	011	4 Frames	100	5 Frames	101	6 Frames	110	7 Frames	111	8 Frames	EPF[1:0]	Expand 16bbp (R,G,B) to 18 bbp (R, G, B)	00	"0" is inputted to LSB $r[5:0] = \{R[4:0], 0\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], 0\}$ Exception: $R[4:0], B[4:0]=5'h1F \rightarrow r[5:0], b[5:0] = 6'h3F$	01	"1" is inputted to LSB $r[5:0] = \{R[4:0], 1\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], 1\}$
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		Exception: R[4:0], B[4:0]=5'h00 → r[5:0], b[5:0] = 6'h00												
	10	MSB is inputted to LSB r[5:0] = {R[4:0], R[4]} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], B[4]}												
	11	Compare R[4:0], G[5:1], B[4:0] case: Case 1: R=G=B → r[5:0] = {R[4:0], G[0]}, g[5:0] = {G[5:0]}, b[5:0] = {B[4:0], G[0]} Case 2: R=B≠G → r[5:0] = {R[4:0], R[4]}, g[5:0] = {G[5:0]}, b[5:0] = {B[4:0], B[4]} Case 3: R=G≠B → r[5:0] = {R[4:0], G[0]}, g[5:0] = {G[5:0]}, b[5:0] = {B[4:0], B[4]} Case 4: B=G≠R → r[5:0] = {R[4:0], R[4]}, g[5:0] = {G[5:0]}, b[5:0] = {B[4:0], G[0]}												
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SW Reset	No change													
HW Reset	WEMODE=1, TEI[2:0]=3'h0, DENC[2:0]=3'h0, DFM=1'h0, EPF[1:0]=2'h2													

8.2.46. Display Mode and Frame Memory Write Mode Setting (B4h)

B4H	Display Mode and Frame Memory Write Mode Setting																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	xx	1	0	1	1	0	1	0	0	B4												
1 st parameter	0	1	↑	xx	0	0	0	RM	0	0	0	DM	00												
Description	<p>DM Select the display operation mode.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DM0</th> <th>Display Interface</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Internal system clock</td> </tr> <tr> <td>1</td> <td>DPI (RGB) interface</td> </tr> </tbody> </table> <p>The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode.</p> <p>RM Select the interface to access the GRAM.</p> <p>Set RM to "1" when writing display data by the RGB interface.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>RM</th> <th>Interface for RAM Access</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DBI Interface (CPU)</td> </tr> <tr> <td>1</td> <td>DPI Interface (RGB)</td> </tr> </tbody> </table>													DM0	Display Interface	0	Internal system clock	1	DPI (RGB) interface	RM	Interface for RAM Access	0	DBI Interface (CPU)	1	DPI Interface (RGB)
	DM0	Display Interface																							
0	Internal system clock																								
1	DPI (RGB) interface																								
RM	Interface for RAM Access																								
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Status	Default Value																								
Power On Sequence	DM=0, RM=0																								
SW Reset	No change																								
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8.2.47. Sub-Panel Control Register (B5h)

B5H	Sub-Panel Control Register																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	xx	1	0	1	1	0	1	0	1	B5												
1 st parameter	0	1	↑	xx	0	0	0	STN_EN	0	0	0	Sub_IM[0]	00												
Description	Sub_IM[1:0]: Sub-panel interface selection. <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>Sub_IM</th> <th>Display Interface</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>8-bit interface (default)</td> </tr> <tr> <td>1</td> <td>9-bit interface</td> </tr> </tbody> </table>													Sub_IM	Display Interface	0	8-bit interface (default)	1	9-bit interface						
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	STN_EN[1:0]: panel type selection. <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>STN_EN</th> <th>Display Interface</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TFT Type sub-panel</td> </tr> <tr> <td>1</td> <td>STN Type sub-panel</td> </tr> </tbody> </table>													STN_EN	Display Interface	0	TFT Type sub-panel	1	STN Type sub-panel						
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Status	Default Value																								
Power On Sequence	Sub_IM=0, STN_EN=0																								
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8.2.48. Backlight Control 1 (B8h)

B8H	Backlight Control 1																																														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																		
Command	0	1	↑	xx	1	0	1	1	1	0	0	0	B8																																		
2 nd parameter	0	↑	1	xx	0	0	0	0	TH_UI[3]	TH_UI[2]	TH_UI[1]	TH_UI[0]	04																																		
Description	<p>TH_UI[3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the user interface (UI) mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.</p>																																														
	<table border="1"> <thead> <tr> <th>TH_UI[3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>4'0h</td><td>99%</td></tr> <tr><td>4'1h</td><td>98%</td></tr> <tr><td>4'2h</td><td>96%</td></tr> <tr><td>4'3h</td><td>94%</td></tr> <tr><td>4'4h</td><td>92%</td></tr> <tr><td>4'5h</td><td>90%</td></tr> <tr><td>4'6h</td><td>88%</td></tr> <tr><td>4'7h</td><td>86%</td></tr> </tbody> </table>						TH_UI[3:0]	Description	4'0h	99%	4'1h	98%	4'2h	96%	4'3h	94%	4'4h	92%	4'5h	90%	4'6h	88%	4'7h	86%	<table border="1"> <thead> <tr> <th>TH_UI[3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>4'8h</td><td>84%</td></tr> <tr><td>4'9h</td><td>82%</td></tr> <tr><td>4'Ah</td><td>80%</td></tr> <tr><td>4'Bh</td><td>78%</td></tr> <tr><td>4'Ch</td><td>76%</td></tr> <tr><td>4'Dh</td><td>74%</td></tr> <tr><td>4'Eh</td><td>72%</td></tr> <tr><td>4'Fh</td><td>70%</td></tr> </tbody> </table>						TH_UI[3:0]	Description	4'8h	84%	4'9h	82%	4'Ah	80%	4'Bh	78%	4'Ch	76%	4'Dh	74%	4'Eh	72%	4'Fh
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8.2.49. Backlight Control 2 (B9h)

B8H	Backlight Control 2												HEX																																				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0																																					
Command	0	1	↑	xx	1	0	1	1	1	0	0	1	B9																																				
2 nd parameter	0	↑	1	xx	TH_MV [3]	TH_MV [2]	TH_MV [1]	TH_MV [0]	TH_ST [3]	TH_ST [2]	TH_ST [1]	TH_ST [0]	B8																																				
Description	<p>TH_ST[3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>TH_ST[3:0]</th> <th>Description</th> <th>TH_ST[3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>4'0h</td><td>99%</td><td>4'8h</td><td>84%</td></tr> <tr><td>4'1h</td><td>98%</td><td>4'9h</td><td>82%</td></tr> <tr><td>4'2h</td><td>96%</td><td>4'Ah</td><td>80%</td></tr> <tr><td>4'3h</td><td>94%</td><td>4'Bh</td><td>78%</td></tr> <tr><td>4'4h</td><td>92%</td><td>4'Ch</td><td>76%</td></tr> <tr><td>4'5h</td><td>90%</td><td>4'Dh</td><td>74%</td></tr> <tr><td>4'6h</td><td>88%</td><td>4'Eh</td><td>72%</td></tr> <tr><td>4'7h</td><td>86%</td><td>4'Fh</td><td>70%</td></tr> </tbody> </table>													TH_ST[3:0]	Description	TH_ST[3:0]	Description	4'0h	99%	4'8h	84%	4'1h	98%	4'9h	82%	4'2h	96%	4'Ah	80%	4'3h	94%	4'Bh	78%	4'4h	92%	4'Ch	76%	4'5h	90%	4'Dh	74%	4'6h	88%	4'Eh	72%	4'7h	86%	4'Fh	70%
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<p>TH_MV[3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the moving image mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>TH_MV[3:0]</th> <th>Description</th> <th>TH_MV[3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>4'0h</td><td>99%</td><td>4'8h</td><td>84%</td></tr> <tr><td>4'1h</td><td>98%</td><td>4'9h</td><td>82%</td></tr> <tr><td>4'2h</td><td>96%</td><td>4'Ah</td><td>80%</td></tr> <tr><td>4'3h</td><td>94%</td><td>4'Bh</td><td>78%</td></tr> <tr><td>4'4h</td><td>92%</td><td>4'Ch</td><td>76%</td></tr> <tr><td>4'5h</td><td>90%</td><td>4'Dh</td><td>74%</td></tr> <tr><td>4'6h</td><td>88%</td><td>4'Eh</td><td>72%</td></tr> <tr><td>4'7h</td><td>86%</td><td>4'Fh</td><td>70%</td></tr> </tbody> </table>													TH_MV[3:0]	Description	TH_MV[3:0]	Description	4'0h	99%	4'8h	84%	4'1h	98%	4'9h	82%	4'2h	96%	4'Ah	80%	4'3h	94%	4'Bh	78%	4'4h	92%	4'Ch	76%	4'5h	90%	4'Dh	74%	4'6h	88%	4'Eh	72%	4'7h	86%	4'Fh	70%	
TH_MV[3:0]	Description	TH_MV[3:0]	Description																																														
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	<p>Histogram</p> <p>100%</p> <p>TH_MV[3:0] TH_ST[3:0] TH_UI[3:0]</p> <p>Dth</p> <p>255</p> <p>Gray Scales</p>												
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Status	Availability												
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Status	Default Value												
Power On Sequence	TH_MV[3:0]=4'h0B, TH_ST[3:0]=4'h08												
SW Reset	No change												
HW Reset	TH_MV[3:0]=4'h0B, TH_ST[3:0]=4'h08												

8.2.50. Backlight Control 3 (BAh)

B8H	Backlight Control 3																																										
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																														
Command	0	1	↑	xx	1	0	1	1	1	0	1	0	BA																														
2 nd parameter	0	↑	1	xx	0	0	0	0	DTH_UI[3]	DTH_UI[2]	DTH_UI[1]	DTH_UI[0]	04																														
Description	<p>DTH_UI[3:0]: This parameter is used set the minimum limitation of grayscale threshold value in User Icon (UI) image mode.</p> <p>This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.</p>																																										
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SW Reset	No change																																										
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8.2.51. Backlight Control 4 (BBh)

B8H	Backlight Control 4												HEX																															
Command	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	BB																															
0	1	↑	xx	1	0	1	1	1	1	0	1	1																																
2 nd parameter	0	↑	1	xx	DTH_MV [3]	DTH_MV [2]	DTH_MV [1]	DTH_MV [0]	DTH_ST [3]	DTH_ST [2]	DTH_ST [1]	DTH_ST [0]	C9																															
Description	<p>DTH_ST[3:0]/DTH_MV[3:0]: This parameter is used set the minimum limitation of grayscale threshold value. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.</p>																																											
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	Status	Default Value												
	Power On Sequence	DTH_MV[3:0]=4'h0C, DTH_ST[3:0]=4'h09												
	SW Reset	No change												
HW Reset	DTH_MV[3:0]=4'h0C, DTH_ST[3:0]=4'h09													

8.2.52. Backlight Control 5 (BCh)

B8H	Backlight Control 5												HEX																			
Command	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	BC																			
2 nd parameter	0	1	↑	xx	1	0	1	1	1	1	0	0	44																			
	0	↑	1	xx	DIM2[3]	DIM2[2]	DIM2[1]	DIM2[0]	0	DIM1[2]	DIM1[1]	DIM1[0]																				
Description	<p>DIM1[2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision.</p> <table border="1"> <thead> <tr> <th>DIM1[2:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>3'0h</td><td>1 frame</td></tr> <tr><td>3'1h</td><td>1 frame</td></tr> <tr><td>3'2h</td><td>2 frames</td></tr> <tr><td>3'3h</td><td>4 frames</td></tr> <tr><td>3'4h</td><td>8 frames</td></tr> <tr><td>3'5h</td><td>16 frames</td></tr> <tr><td>3'6h</td><td>32 frames</td></tr> <tr><td>3'7h</td><td>64 frames</td></tr> </tbody> </table> <p>DIM2[3:0]: This parameter is used to set the threshold of brightness change. When the brightness transition difference is smaller than DIM2[3:0], the brightness transition will be ignored. For example: If $\text{brightness B} - \text{brightness A} < \text{DIM2[2:0]}$, the brightness transition will be ignored and keep the brightness A.</p>													DIM1[2:0]	Description	3'0h	1 frame	3'1h	1 frame	3'2h	2 frames	3'3h	4 frames	3'4h	8 frames	3'5h	16 frames	3'6h	32 frames	3'7h	64 frames	
	DIM1[2:0]	Description																														
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Default									
	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>DIM2[3:0]=4'h04, DIM1[2:0]=4'h04</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>DIM2[3:0]=4'h04, DIM1[2:0]=4'h04</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	DIM2[3:0]=4'h04, DIM1[2:0]=4'h04	SW Reset	No change	HW Reset	DIM2[3:0]=4'h04, DIM1[2:0]=4'h04
	Status	Default Value							
	Power On Sequence	DIM2[3:0]=4'h04, DIM1[2:0]=4'h04							
SW Reset	No change								
HW Reset	DIM2[3:0]=4'h04, DIM1[2:0]=4'h04								

8.2.53. Backlight Control 7 (BEh)

B9H	Backlight Control 7																																				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
Command	0	1	↑	xx	1	0	1	1	1	1	1	0	BE																								
1 st parameter	0	↑	1	xx	PWM_ DIV[7]	PWM_ DIV[6]	PWM_ DIV[5]	PWM_ DIV[4]	PWM_ DIV[3]	PWM_ DIV[2]	PWM_ DIV[1]	PWM_ DIV[0]	0F																								
Description	<p>PWM_DIV[7:0]: PWM_OUT output frequency control. This command is used to adjust the PWM waveform frequency of PWM_OUT. The PWM frequency can be calculated by using the following equation.</p> $f_{pwm_out} = \frac{8MHz}{(PWM_DIV[7:0]+1) \times 255}$ <table border="1"> <thead> <tr> <th>PWM_DIV[7:0]</th> <th>f_{PWM_OUT}</th> </tr> </thead> <tbody> <tr><td>8'h0</td><td>31.37 KHz</td></tr> <tr><td>8'h1</td><td>15.69 KHz</td></tr> <tr><td>8'h2</td><td>10.46KHz</td></tr> <tr><td>8'h3</td><td>7.843 KHz</td></tr> <tr><td>8'h4</td><td>6.27 KHz</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>8'hFB</td><td>124.49Hz</td></tr> <tr><td>8'hFC</td><td>124Hz</td></tr> <tr><td>8'hFD</td><td>123.51Hz</td></tr> <tr><td>8'hFE</td><td>123.03Hz</td></tr> <tr><td>8'hFF</td><td>122.55Hz</td></tr> </tbody> </table> <p>Note: The output frequency tolerance of internal frequency divider in CABC is ±10%</p>													PWM_DIV[7:0]	f _{PWM_OUT}	8'h0	31.37 KHz	8'h1	15.69 KHz	8'h2	10.46KHz	8'h3	7.843 KHz	8'h4	6.27 KHz	8'hFB	124.49Hz	8'hFC	124Hz	8'hFD	123.51Hz	8'hFE	123.03Hz	8'hFF	122.55Hz
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8.2.54. Backlight Control 8 (BFh)

B9H	Backlight Control 2																											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	↑	xx	1	0	1	1	1	1	1	1	BF															
1 st parameter	0	↑	1	xx	0	0	0	0	0	LEDONR	LEDONPOL	LEDPWMPOL	00															
Description	LEDPWMPOL: The bit is used to define polarity of LEDPWM signal.																											
	<table border="1"> <thead> <tr> <th>BL</th> <th>LEDPWMPOL</th> <th>LEDPWM pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>Original polarity of PWM signal</td> </tr> <tr> <td>1</td> <td>1</td> <td>Inversed polarity of PWM signal</td> </tr> </tbody> </table>													BL	LEDPWMPOL	LEDPWM pin	0	0	0	0	1	1	1	0	Original polarity of PWM signal	1	1	Inversed polarity of PWM signal
	BL	LEDPWMPOL	LEDPWM pin																									
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0	1	1																										
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LEDONPOL: This bit is used to control LEDON pin.																												
<table border="1"> <thead> <tr> <th>BL</th> <th>LEDONPOL</th> <th>LEDON pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>LEDONR</td> </tr> <tr> <td>1</td> <td>1</td> <td>Inversed LEDONR</td> </tr> </tbody> </table>													BL	LEDONPOL	LEDON pin	0	0	0	0	1	1	1	0	LEDONR	1	1	Inversed LEDONR	
BL	LEDONPOL	LEDON pin																										
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0	1	1																										
1	0	LEDONR																										
1	1	Inversed LEDONR																										
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	Status	Default Value																										
	Power On Sequence	LEDPWMPOL=0, LEDONPOL=0, LEDONR=0																										
	SW Reset	No change																										
HW Reset	LEDPWMPOL=0, LEDONPOL=0, LEDONR=0																											

8.2.55. Panel Driving Setting (C0h)

C0H	Panel Driving Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	0	0	C0
1 st Parameter	1	1	↑	0	0	0	0	REV	SM	GS	BGR	SS	00
2 nd Parameter	1	1	↑	0	0	0	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	35
3 rd Parameter	1	1	↑	0	0	SCN [6]	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	00
4 th Parameter	1	1	↑	0	0	0	0	0	0	0	PTS [1]	PTS [0]	00
5 th Parameter	1	1	↑	0	0	0	0	PTG	ISC [3]	ISC [2]	ISC [1]	ISC [0]	01
6 th Parameter	1	1	↑	0	0	0	0	0	0	0	DIVE [1]	DIVE [0]	02

Description	<p>SS</p> <p>The bit is used to select the shifting direction of the source driver output.</p> <p>SS=0: S1 to S720 (Default)</p> <p>SS=1: S720 to S1</p>																										
	<p>BGR</p> <p>The bit is used to reverse 18-bit write data in the Frame Memory from RGB to BGR. Set in accordance with arrangement of color filters.</p> <p>BGR=0: Display data is in RGB sequence. (Default)</p> <p>BGR=1: Display data is in BGR sequence.</p>																										
	<p>REV: Enables the grayscale inversion of the image by setting REV=1.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">REV</th> <th rowspan="2">GRAM Data</th> <th colspan="2">Source Output in Display Area</th> </tr> <tr> <th>Positive polarity</th> <th>negative polarity</th> </tr> </thead> <tbody> <tr> <td rowspan="3">0</td> <td>18'h00000</td> <td>V63</td> <td>V0</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>18'h3FFFF</td> <td>V0</td> <td>V63</td> </tr> <tr> <td rowspan="3">1</td> <td>18'h00000</td> <td>V0</td> <td>V63</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>18'h3FFFF</td> <td>V63</td> <td>V0</td> </tr> </tbody> </table>	REV	GRAM Data	Source Output in Display Area		Positive polarity	negative polarity	0	18'h00000	V63	V0	:	:	:	18'h3FFFF	V0	V63	1	18'h00000	V0	V63	:	:	:	18'h3FFFF	V63	V0
REV	GRAM Data			Source Output in Display Area																							
		Positive polarity	negative polarity																								
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	:	:	:																								
	18'h3FFFF	V0	V63																								
1	18'h00000	V0	V63																								
	:	:	:																								
	18'h3FFFF	V63	V0																								
	<p>SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.</p>																										

SM	GS	Scan Direction	Gate Output Sequence
0	0		<p>G1, G2, G3, G4, ..., G428 G429, G430, G431, G432</p>
0	1		<p>G432, G431, G430, ..., G9 G7, G5, G4, G3, G2, G1</p>
1	0		<p>G1, G3, G5, G7, ..., G423 G425, G427, G429, G431 G2, G4, G6, G8, ..., G424 G426, G428, G430, G432</p>
1	1		<p>G432, G430, G428, ..., G14 G12, G10, G8, G6, G4, G2 G431, G429, G427, ..., G13 G11, G9, G7, G5, G3, G1</p>

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h00 ~ 6'h35	8 * (NL5:0)+1) lines
Others	Setting inhibited

SCN[6:0]: Specifies the gate line where the gate driver starts scan

SCN[6:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h ~ 35h	G[1+SCN[6:0]*4]	G[432 - SCN[6:0]*4]	G[1+SCN[6:0]*8]	G[432 - SCN[6:0]*8]
36h ~ 6Bh	G[1+SCN[6:0]*4]	G[432 - SCN[6:0]*4]	G[2+(SCN[6:0]-36h)*8]	G[431 - (SCN[6:0]-36h)*8]
Others	Setting disabled	Setting disabled	Setting disabled	Setting disabled

PTG: Sets the scan mode in non-display area. Select frame-inversion when interval-scan is selected.

PTG	Scan Mode in non-display area
0	Normal Scan
1	Interval Scan

ISC[3:0]: Set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

ISC[3:0]	Scan cycle	(f _{FRAME})=60Hz
4'h0	Setting inhibited	-
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

PTS[2:0]:

Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

PTS[1:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Positive polarity	Negative polarity		
00	V63	V0	V63 and V0	Register Setting(DC1, DC0)
01	V0	V63	-	-
10	GND	GND	V63 and V0	Register Setting(DC1, DC0)
11	Hi-Z	Hi-Z	V63 and V0	Register Setting(DC1, DC0)

DIVE[1:0]: DIVE[1:0] is used to set division ratio of PCLK clock frequency when the DPI interface is selected.

The divided PCLK will be used as internal clock for the source driver pre-charge, VCOM equalizing, etc.

		DIVE[1:0]	Division Ratio												
		2'h0	1/1												
		2'h1	1/2												
		2'h2	1/4												
		2'h3	1/8												
Restriction	-														
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
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Sleep In	Yes														
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SS=0, BGR=0, GS=0, SM=0, REV=0, NL[5:0]=6'h35, SCN[6:0]=7'h0, PTS[2:0]=3'h0, ISC[3:0]=4'h1, PTG=0, DIVE[1:0]=2'h2</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>SS=0, BGR=0, GS=0, SM=0, REV=0, NL[5:0]=6'h35, SCN[6:0]=7'h0, PTS[2:0]=3'h0, ISC[3:0]=4'h1, PTG=0, DIVE[1:0]=2'h2</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	SS=0, BGR=0, GS=0, SM=0, REV=0, NL[5:0]=6'h35, SCN[6:0]=7'h0, PTS[2:0]=3'h0, ISC[3:0]=4'h1, PTG=0, DIVE[1:0]=2'h2	SW Reset	No change	HW Reset	SS=0, BGR=0, GS=0, SM=0, REV=0, NL[5:0]=6'h35, SCN[6:0]=7'h0, PTS[2:0]=3'h0, ISC[3:0]=4'h1, PTG=0, DIVE[1:0]=2'h2					
Status	Default Value														
Power On Sequence	SS=0, BGR=0, GS=0, SM=0, REV=0, NL[5:0]=6'h35, SCN[6:0]=7'h0, PTS[2:0]=3'h0, ISC[3:0]=4'h1, PTG=0, DIVE[1:0]=2'h2														
SW Reset	No change														
HW Reset	SS=0, BGR=0, GS=0, SM=0, REV=0, NL[5:0]=6'h35, SCN[6:0]=7'h0, PTS[2:0]=3'h0, ISC[3:0]=4'h1, PTG=0, DIVE[1:0]=2'h2														

8.2.56. Display_Timing_Setting for Normal/Partial Mode (C1h)

C1H	Display_Timing_Setting for Normal/Partial Mode																																																																
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																				
Command	0	1	↑	x	1	1	0	0	0	0	0	1	C1																																																				
1 st Parameter	1	1	↑	0	0	0	0	BC0	0	0	DIV0[1]	DIV0[0]	10																																																				
2 nd Parameter	1	1	↑	0	0	0	0	RTN0[4]	RTN0[3]	RTN0[2]	RTN0[1]	RTN0[0]	10																																																				
3 rd Parameter	1	1	↑	0	BP0[7]	BP0[6]	BP0[5]	BP0[4]	BP0[3]	BP0[2]	BP0[1]	BP0[0]	02																																																				
4 th Parameter	1	1	↑	0	FP0[7]	FP0[6]	FP0[5]	FP0[4]	FP0[3]	FP0[2]	FP0[1]	FP0[0]	02																																																				
Description	<p>BC0: BC0 is used to select VCOM liquid crystal drive waveform.</p> <p>BC0 = 0: Frame inversion waveform is selected.</p> <p>BC0 = 1: Line inversion waveform is selected.</p> <p>DIV0[1:0]: DIV0[1:0] is used to set division ratio of internal clock frequency.</p> <p>The internal operation is synchronized with the frequency divided internal clock. When DIV0 setting is changed, the width of the reference clock for liquid crystal control signals is changed.</p> <p>The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DIV0[1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>2'h0</td> <td>1/1</td> </tr> <tr> <td>2'h1</td> <td>1/2</td> </tr> <tr> <td>2'h2</td> <td>1/4</td> </tr> <tr> <td>2'h3</td> <td>1/8</td> </tr> </tbody> </table> <p>Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)]</p> <p>fosc. : internal oscillator frequency</p> <p>clocks per line : RTNn setting</p> <p>division ratio: DIVn setting</p> <p>Line: total driving line number</p> <p>BP: back porch line number</p> <p>FP: front porch line number</p> <p>RTN0[4:0]: RTN0[4:0] is used to set 1H (line) period.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>RTN[4:0]</th> <th>Clocks per line</th> <th>RTN[4:0]</th> <th>Clocks per line</th> <th>RTN[4:0]</th> <th>Clocks per line</th> </tr> </thead> <tbody> <tr> <td>5'h00~0F</td> <td>Setting prohibited</td> <td>5'h15</td> <td>21 clocks</td> <td>5'h1B</td> <td>27 clocks</td> </tr> <tr> <td>5'h10</td> <td>16 clocks</td> <td>5'h16</td> <td>22 clocks</td> <td>5'h1C</td> <td>28 clocks</td> </tr> <tr> <td>5'h11</td> <td>17 clocks</td> <td>5'h17</td> <td>23 clocks</td> <td>5'h1D</td> <td>29 clocks</td> </tr> <tr> <td>5'h12</td> <td>18 clocks</td> <td>5'h18</td> <td>24 clocks</td> <td>5'h1E</td> <td>30 clocks</td> </tr> <tr> <td>5'h13</td> <td>19 clocks</td> <td>5'h19</td> <td>25 clocks</td> <td>5'h1F</td> <td>31 clocks</td> </tr> <tr> <td>5'h14</td> <td>20 clocks</td> <td>5'h1A</td> <td>26 clocks</td> <td></td> <td></td> </tr> </tbody> </table>													DIV0[1:0]	Division Ratio	2'h0	1/1	2'h1	1/2	2'h2	1/4	2'h3	1/8	RTN[4:0]	Clocks per line	RTN[4:0]	Clocks per line	RTN[4:0]	Clocks per line	5'h00~0F	Setting prohibited	5'h15	21 clocks	5'h1B	27 clocks	5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks	5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks	5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks	5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks	5'h14	20 clocks	5'h1A	26 clocks		
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	<p>FP0[7:0], BP0[7:0]</p> <p>FP0[7:0] is used to set the number of lines for a front porch period (a blank period following the end of display).</p> <p>BP0[7:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of display).</p> <table border="1"> <thead> <tr> <th>FP0[7:0] BP0[7:0]</th> <th>Front and back porch period (line period)</th> </tr> </thead> <tbody> <tr><td>8'h0</td><td>Setting prohibited</td></tr> <tr><td>8'h1</td><td>Setting prohibited</td></tr> <tr><td>8'h2</td><td>2 lines</td></tr> <tr><td>8'h3</td><td>3 lines</td></tr> <tr><td>8'h4</td><td>4 lines</td></tr> <tr><td>8'h5</td><td>5 lines</td></tr> <tr><td>8'h6</td><td>6 lines</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>8'h7E</td><td>126 lines</td></tr> <tr><td>8'h7F</td><td>127 lines</td></tr> <tr><td>8'h80</td><td>128 lines</td></tr> <tr><td>Others</td><td>Setting Prohibited</td></tr> </tbody> </table> <p>Note to Setting BP0 and FP0</p> <p>The condition in setting BP0 and FP0 bits are: $BP0 \geq 2$ lines and $FP0 \geq 2$ lines, $FP0+BP0 \leq 256$ lines</p>	FP0[7:0] BP0[7:0]	Front and back porch period (line period)	8'h0	Setting prohibited	8'h1	Setting prohibited	8'h2	2 lines	8'h3	3 lines	8'h4	4 lines	8'h5	5 lines	8'h6	6 lines	8'h7E	126 lines	8'h7F	127 lines	8'h80	128 lines	Others	Setting Prohibited
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Partial Mode On, Idle Mode On, Sleep Out	Yes																										
Sleep In	Yes																										
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=8'h2, BP=8'h2</td></tr> <tr><td>SW Reset</td><td>No change</td></tr> <tr><td>HW Reset</td><td>BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=8'h2, BP0=8'h2</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=8'h2, BP=8'h2	SW Reset	No change	HW Reset	BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=8'h2, BP0=8'h2																		
Status	Default Value																										
Power On Sequence	BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=8'h2, BP=8'h2																										
SW Reset	No change																										
HW Reset	BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=8'h2, BP0=8'h2																										

8.2.57. Display_Timing_Setting for Idle Mode (C3h)

C3H	Display_Timing_Setting for Idle Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	1	1	C3
1 st Parameter	1	1	↑	0	0	0	0	BC2	0	0	DIV2[1]	DIV2[0]	00
2 nd Parameter	1	1	↑	0	0	0	0	RTN2 [4]	RTN2 [3]	RTN2 [2]	RTN2 [1]	RTN2 [0]	10
3 rd Parameter	1	1	↑	0	BP2 [7]	BP2 [6]	BP2 [5]	BP2 [4]	BP2 [3]	BP2 [2]	BP2 [1]	BP2 [0]	02
4 th Parameter	1	1	↑	0	FP2 [7]	FP2 [6]	FP2 [5]	FP2 [4]	FP2 [3]	FP2 [2]	FP0 [1]	FP2 [0]	02

Description	<p>BC2: BC2 is used to select VCOM liquid crystal drive waveform.</p> <p>BC2 = 0: Frame inversion waveform is selected.</p> <p>BC2 = 1: Line inversion waveform is selected.</p>																																										
	<p>DIV2[1:0]: DIV2[1:0] is used to set division ratio of internal clock frequency.</p> <p>The internal operation is synchronized with the frequency divided internal clock. When DIV2 setting is changed, the width of the reference clock for liquid crystal control signals is changed.</p> <p>The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DIV2[1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>2'h0</td> <td>1/1</td> </tr> <tr> <td>2'h1</td> <td>1/2</td> </tr> <tr> <td>2'h2</td> <td>1/4</td> </tr> <tr> <td>2'h3</td> <td>1/8</td> </tr> </tbody> </table> <p>Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)]</p> <p>fosc. : internal oscillator frequency</p> <p>clocks per line : RTNn setting</p> <p>division ratio: DIVn setting</p> <p>Line: total driving line number</p> <p>BP: back porch line number</p> <p>FP: front porch line number</p>	DIV2[1:0]	Division Ratio	2'h0	1/1	2'h1	1/2	2'h2	1/4	2'h3	1/8																																
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	<p>RTN2[4:0]: RTN2[4:0] is used to set 1H (line) period.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>RTN2[4:0]</th> <th>Clocks per line</th> <th>RTN2[4:0]</th> <th>Clocks per line</th> <th>RTN2[4:0]</th> <th>Clocks per line</th> </tr> </thead> <tbody> <tr> <td>5'h00~0F</td> <td>Setting prohibited</td> <td>5'h15</td> <td>21 clocks</td> <td>5'h1B</td> <td>27 clocks</td> </tr> <tr> <td>5'h10</td> <td>16 clocks</td> <td>5'h16</td> <td>22 clocks</td> <td>5'h1C</td> <td>28 clocks</td> </tr> <tr> <td>5'h11</td> <td>17 clocks</td> <td>5'h17</td> <td>23 clocks</td> <td>5'h1D</td> <td>29 clocks</td> </tr> <tr> <td>5'h12</td> <td>18 clocks</td> <td>5'h18</td> <td>24 clocks</td> <td>5'h1E</td> <td>30 clocks</td> </tr> <tr> <td>5'h13</td> <td>19 clocks</td> <td>5'h19</td> <td>25 clocks</td> <td>5'h1F</td> <td>31 clocks</td> </tr> <tr> <td>5'h14</td> <td>20 clocks</td> <td>5'h1A</td> <td>26 clocks</td> <td></td> <td></td> </tr> </tbody> </table>	RTN2[4:0]	Clocks per line	RTN2[4:0]	Clocks per line	RTN2[4:0]	Clocks per line	5'h00~0F	Setting prohibited	5'h15	21 clocks	5'h1B	27 clocks	5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks	5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks	5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks	5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks	5'h14	20 clocks	5'h1A	26 clocks		
RTN2[4:0]	Clocks per line	RTN2[4:0]	Clocks per line	RTN2[4:0]	Clocks per line																																						
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	<p>FP2[7:0], BP2[7:0]</p> <p>FP2[7:0] is used to set the number of lines for a front porch period (a blank period following the end of display).</p> <p>BP2[7:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of display).</p> <table border="1"> <thead> <tr> <th>FP2[7:0] BP2[7:0]</th> <th>Front and back porch period (line period)</th> </tr> </thead> <tbody> <tr><td>8'h0</td><td>Setting prohibited</td></tr> <tr><td>8'h1</td><td>Setting prohibited</td></tr> <tr><td>8'h2</td><td>2 lines</td></tr> <tr><td>8'h3</td><td>3 lines</td></tr> <tr><td>8'h4</td><td>4 lines</td></tr> <tr><td>8'h5</td><td>5 lines</td></tr> <tr><td>8'h6</td><td>6 lines</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>8'h7E</td><td>126 lines</td></tr> <tr><td>8'h7F</td><td>127 lines</td></tr> <tr><td>8'h80</td><td>128 lines</td></tr> <tr><td>Others</td><td>Setting Prohibited</td></tr> </tbody> </table> <p>Note to Setting BP2 and FP2</p> <p>The condition in setting BP2 and FP2 bits are: $BP2 \geq 2$ lines and $FP2 \geq 2$ lines, $FP2+BP2 \leq 256$ lines</p>	FP2[7:0] BP2[7:0]	Front and back porch period (line period)	8'h0	Setting prohibited	8'h1	Setting prohibited	8'h2	2 lines	8'h3	3 lines	8'h4	4 lines	8'h5	5 lines	8'h6	6 lines	8'h7E	126 lines	8'h7F	127 lines	8'h80	128 lines	Others	Setting Prohibited
FP2[7:0] BP2[7:0]	Front and back porch period (line period)																										
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Sleep In	Yes																										
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>BC2=1'h1, DIV2=2'h0, RTN2=5'h10, FP2=4'h2, BP2=4'h2</td></tr> <tr><td>SW Reset</td><td>No change</td></tr> <tr><td>HW Reset</td><td>BC2=1'h1, DIV2=2'h0, RTN2=5'h10, FP2=4'h2, BP2=4'h2</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	BC2=1'h1, DIV2=2'h0, RTN2=5'h10, FP2=4'h2, BP2=4'h2	SW Reset	No change	HW Reset	BC2=1'h1, DIV2=2'h0, RTN2=5'h10, FP2=4'h2, BP2=4'h2																		
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SW Reset	No change																										
HW Reset	BC2=1'h1, DIV2=2'h0, RTN2=5'h10, FP2=4'h2, BP2=4'h2																										

8.2.58. Source/VCOM/Gate Timing Setting (C4h)

C4H	Frame Rate Control																														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	1	1	1	0	0	0	1	0	0	C4																		
1 st Parameter	1	1	↑	0	0	SDT[2]	SDT[1]	SDT[0]	0	NOW[2]	NOW[1]	NOW[0]	06																		
Description	<p>SDT[2:0]</p> <p>The bit is used to set the source output alternating position in 1H period.</p> <table border="1"> <thead> <tr> <th>SDT[2:0]</th> <th>Source Output Position</th> </tr> </thead> <tbody> <tr><td>000</td><td>1 clock</td></tr> <tr><td>001</td><td>2 clocks</td></tr> <tr><td>010</td><td>3 clocks</td></tr> <tr><td>011</td><td>4 clocks</td></tr> <tr><td>100</td><td>5 clocks</td></tr> <tr><td>101</td><td>6 clocks</td></tr> <tr><td>110</td><td>7 clocks</td></tr> <tr><td>111</td><td>8 clocks</td></tr> </tbody> </table> <p>Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h, and C3h).</p>													SDT[2:0]	Source Output Position	000	1 clock	001	2 clocks	010	3 clocks	011	4 clocks	100	5 clocks	101	6 clocks	110	7 clocks	111	8 clocks
	SDT[2:0]	Source Output Position																													
000	1 clock																														
001	2 clocks																														
010	3 clocks																														
011	4 clocks																														
100	5 clocks																														
101	6 clocks																														
110	7 clocks																														
111	8 clocks																														
<p>NOW[2:0]</p> <p>These bits set the gate output start position (non-overlap period).</p> <table border="1"> <thead> <tr> <th>NOW[2:0]</th> <th>Gate Output Start Position</th> </tr> </thead> <tbody> <tr><td>000</td><td>Setting prohibited</td></tr> <tr><td>001</td><td>1 clock</td></tr> <tr><td>010</td><td>2 clocks</td></tr> <tr><td>011</td><td>3 clocks</td></tr> <tr><td>100</td><td>4 clocks</td></tr> <tr><td>101</td><td>5 clocks</td></tr> <tr><td>110</td><td>6 clocks</td></tr> <tr><td>111</td><td>7 clocks</td></tr> </tbody> </table> <p>Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h, and C3h).</p>													NOW[2:0]	Gate Output Start Position	000	Setting prohibited	001	1 clock	010	2 clocks	011	3 clocks	100	4 clocks	101	5 clocks	110	6 clocks	111	7 clocks	
NOW[2:0]	Gate Output Start Position																														
000	Setting prohibited																														
001	1 clock																														
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101	5 clocks																														
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Restriction																															
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Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
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Sleep In	Yes																														
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>NOW[2:0]=3'h6, SDT[2:0]=3'h0</td></tr> <tr><td>SW Reset</td><td>No change</td></tr> <tr><td>HW Reset</td><td>NOW[2:0]=3'h6, SDT[2:0]=3'h0</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence	NOW[2:0]=3'h6, SDT[2:0]=3'h0	SW Reset	No change	HW Reset	NOW[2:0]=3'h6, SDT[2:0]=3'h0										
Status	Default Value																														
Power On Sequence	NOW[2:0]=3'h6, SDT[2:0]=3'h0																														
SW Reset	No change																														
HW Reset	NOW[2:0]=3'h6, SDT[2:0]=3'h0																														

8.2.59. Frame Rate Control (C5h)

C5H	Frame Rate Control																													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																	
Command	0	1	↑	1	1	1	0	0	0	1	0	1	C5																	
1 st Parameter	1	1	↑	0	0	0	0	0	0	FRA[2]	FRA[1]	FRA[0]	04																	
Description	Set the frame frequency of display.																													
	<p>Frame Rate= $\frac{16\text{MHz}}{\text{RTN}[4:0] \times (\text{Display Line} + \text{Back porch} + \text{Front Porch}) \times (\text{FRA}[2:0] + 12) \times 2}$</p> <table border="1"> <thead> <tr> <th>FRA[2:0]</th> <th>Frame Rate (Hz)</th> </tr> </thead> <tbody> <tr> <td>3'h0</td> <td>96</td> </tr> <tr> <td>3'h1</td> <td>88</td> </tr> <tr> <td>3'h2</td> <td>82</td> </tr> <tr> <td>3'h3</td> <td>76</td> </tr> <tr> <td>3'h4</td> <td>72 (default)</td> </tr> <tr> <td>3'h5</td> <td>67</td> </tr> <tr> <td>3'h6</td> <td>64</td> </tr> <tr> <td>3'h7</td> <td>60</td> </tr> </tbody> </table> <p><i>The above table is based on back/front porch equal to 2 lines and 16 clocks per display line and the total display lines are 432. When any parameter is changed, the frame rate will also be changed.</i></p>													FRA[2:0]	Frame Rate (Hz)	3'h0	96	3'h1	88	3'h2	82	3'h3	76	3'h4	72 (default)	3'h5	67	3'h6	64	3'h7
FRA[2:0]	Frame Rate (Hz)																													
3'h0	96																													
3'h1	88																													
3'h2	82																													
3'h3	76																													
3'h4	72 (default)																													
3'h5	67																													
3'h6	64																													
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Sleep In	Yes																													
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Status	Default Value																													
Power On Sequence	FRA=3'h4																													
SW Reset	No change																													
HW Reset	FRA=3'h4																													

8.2.60. Interface Control (C6h)

C6H	Interface Control																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	0	0	0	1	1	0	C6												
1 st Parameter	1	1	↑	x	SDA_EN	0	0	VSPL	HSPL	0	EPL	DPL	02												
Description	<p>DPL: Sets the signal polarity of the PCLK pin. DPL = "0" The data is input on the rising edge of PCLK. DPL = "1" The data is input on the falling edge of PCLK.</p> <p>EPL: Sets the signal polarity of the ENABLE pin. EPL = "0" The data DB[17:0] is written when ENABLE = "0". EPL = "1" The data DB[17:0] is written when ENABLE = "1".</p> <p>HSPL: Sets the signal polarity of the HSYNC pin. HSPL = "0" Low active HSPL = "1" High active</p> <p>VSPL: Sets the signal polarity of the VSYNC pin. VSPL = "0" Low active VSPL = "1" High active</p> <p>SDA_EN: DBI type C interface selection SDA_EN = "0", DIN and DOUT pins are used for DBI type C interface mode. SDA_EN = "1", DIN/SDA pin is used for DBI type C interface mode and DOUT pin is not used.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	DPL=1'h0, EPL=1'h1, VSPL=1'h0, HSPL=:1'h0,SDA_EN=1'h0																								
SW Reset	No change																								
HW Reset	DPL=1'h0, EPL=1'h1, VSPL=1'h0, HSPL=:1'h0,SDA_EN=1'h0																								

8.2.61. Gamma Setting (C8h)

C8H	Gamma Setting																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	0	0	1	0	0	0	C8												
1 st Parameter	1	1	↑	x	0	KP1 [2]	KP1 [1]	KP1 [0]	0	KP0 [2]	KP0 [1]	KP0 [0]	44												
2 nd Parameter	1	1	↑	x	0	KP3 [2]	KP3 [1]	KP3 [0]	0	KP2 [2]	KP2 [1]	KP2 [0]	44												
3 rd Parameter	1	1	↑	x	0	KP5 [2]	KP5 [1]	KP5 [0]	0	KP4 [2]	KP4 [1]	KP4 [0]	44												
4 th Parameter	1	1	↑	x	0	RP1 [2]	RP1 [1]	RP1 [0]	0	RP0 [2]	RP0 [1]	RP0 [0]	44												
5 th Parameter	1	1	↑	x	0	0	0	0	VRP0 [3]	VRP0 [2]	VRP0 [1]	VRP0 [0]	08												
6 th Parameter	1	1	↑	x	0	0	0	VRP1 [4]	VRP1 [3]	VRP1 [2]	VRP1 [1]	VRP1 [0]	10												
7 th Parameter	1	1	↑	x	0	KN1 [2]	KN1 [1]	KN1 [0]	0	KN0 [2]	KN0 [1]	KN0 [0]	44												
8 th Parameter	1	1	↑	x	0	KN3 [2]	KN3 [1]	KN3 [0]	0	KN2 [2]	KN2 [1]	KN2 [0]	44												
9 th Parameter	1	1	↑	x	0	KN5 [2]	KN5 [1]	KN5 [0]	0	KN4 [2]	KN4 [1]	KN4 [0]	44												
10 th Parameter	1	1	↑	x	0	RN1 [2]	RN1 [1]	RN1 [0]	0	RN0 [2]	RN0 [1]	RN0 [0]	44												
11 th Parameter	1	1	↑	x	0	0	0	0	VRN0 [3]	VRN0 [2]	VRN0 [1]	VRN0 [0]	08												
12 th Parameter	1	1	↑	x	0	0	0	VRN1 [4]	VRN1 [3]	VRN1 [2]	VRN1 [1]	VRN1 [0]	10												
13 th Parameter	1	1	↑	x	VREP1 [3]	VREP1 [2]	VREP1 [1]	VREP1 [0]	VREP0 [3]	VREP0 [2]	VREP0 [1]	VREP0 [0]	88												
14 th Parameter	1	1	↑	x	VREN0 [3]	VREN0 [2]	VREN0 [1]	VREN0 [0]	VREP2 [3]	VREP2 [2]	VREP2 [1]	VREP2 [0]	88												
15 th Parameter	1	1	↑	x	VREN2 [3]	VREN2 [2]	VREN2 [1]	VREN2 [0]	VREN1 [3]	VREN1 [2]	VREN1 [1]	VREN1 [0]	88												
Description	KP5-0[2:0] : γ fine adjustment register for positive polarity RP1-0[2:0] : γ gradient adjustment register for positive polarity VRP1-0[4:0] : γ amplitude adjustment register for positive polarity KN5-0[2:0] : γ fine adjustment register for negative polarity RN1-0[2:0] : γ gradient adjustment register for negative polarity VRN1-0[4:0] : γ amplitude adjustment register for negative polarity																								
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

Default Value	Status	Default Value
	Power On Sequence	KPx/KNx[2:0]=3'h4, RPx/RNx[2:0]=3'h4, VRP0/VRN0[3:0]=4'h8, VRP1/VRN1[4:0]=5'h10, VREP0/VREP1/VREP2=4'h8, VREN0/VREN1/VREN2=4'h8,
	SW Reset	No Change
	HW Reset	KPx/KNx[2:0]=3'h4, RPx/RNx[2:0]=3'h4, VRP0/VRN0[3:0]=4'h8, VRP1/VRN1[4:0]=5'h10 VREP0/VREP1/VREP2=4'h8, VREN0/VREN1/VREN2=4'h8,

8.2.62. Gamma Setting for Red/Blue Color (C9h)

C9h	Gamma Setting for Red/Blue Color													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	x	1	1	0	0	1	0	0	1	C9	
1 st Parameter	1	1	↑	x	0	0	0	0	RV0[3]	RV0[2]	RV0[1]	RV0[0]	00	
2 nd Parameter	1	1	↑	x	0	0	0	0	RV1[3]	RV1[2]	RV1[1]	RV1[0]	00	
3 rd Parameter	1	1	↑	x	0	0	0	0	RV2[3]	RV2[2]	RV2[1]	RV2[0]	00	
4 th Parameter	1	1	↑	x	0	0	0	0	RV3[3]	RV3[2]	RV3[1]	RV3[0]	00	
...	
61 th Parameter	1	1	↑	x	0	0	0	0	RV60[3]	RV60[2]	RV60[1]	RV60[0]	00	
62 th Parameter	1	1	↑	x	0	0	0	0	RV61[3]	RV61[2]	RV61[1]	RV61[0]	00	
63 th Parameter	1	1	↑	x	0	0	0	0	RV62[3]	RV62[2]	RV62[1]	RV62[0]	00	
64 th Parameter	1	1	↑	x	0	0	0	0	RV63[3]	RV63[2]	RV63[1]	RV63[0]	00	
65 th Parameter	1	1	↑	x	0	0	0	0	BV0[3]	BV0[2]	BV0[1]	BV0[0]	00	
66 th Parameter	1	1	↑	x	0	0	0	0	BV1[3]	BV1[2]	BV1[1]	BV1[0]	00	
67 th Parameter	1	1	↑	x	0	0	0	0	BV2[3]	BV2[2]	BV2[1]	BV2[0]	00	
68 th Parameter	1	1	↑	x	0	0	0	0	BV3[3]	BV3[2]	BV3[1]	BV3[0]	00	
...	
125 th Parameter	1	1	↑	x	0	0	0	0	BV60[3]	BV60[2]	BV60[1]	BV60[0]	00	
126 th Parameter	1	1	↑	x	0	0	0	0	BV61[3]	BV61[2]	BV61[1]	BV61[0]	00	
127 th Parameter	1	1	↑	x	0	0	0	0	BV62[3]	BV62[2]	BV62[1]	BV62[0]	00	
128 th Parameter	1	1	↑	x	0	0	0	0	BV63[3]	BV63[2]	BV63[1]	BV63[0]	00	
Description	This register is used to fine tune the red/blue color gamma mapping.													
	Note: Please disable the 3-gamma function (EAh register) before setting this gamma table.													
	RVn[3:0] n=0~63		Red color gamma level (relative to green color)						BVn[3:0] n=0~63		Blue color gamma level (relative to green color)			
	4'h0		+0						4'h0		+0			
	4'h1		+1						4'h1		+1			
	4'h2		+2						4'h2		+2			
	4'h3		+3						4'h3		+3			
	4'h4		+4						4'h4		+4			
	4'h5		+5						4'h5		+5			
	4'h6		+6						4'h6		+6			
	4'h7		+7						4'h7		+7			
	4'h8		-8						4'h8		-8			
	4'h9		-7						4'h9		-7			
	4'hA		-6						4'hA		-6			
	4'hB		-5						4'hB		-5			
	4'hC		-4						4'hC		-4			
	4'hD		-3						4'hD		-3			
	4'hE		-2						4'hE		-2			
	4'hF		-1						4'hF		-1			
	Register Availability	Status						Availability						
Normal Mode On, Idle Mode Off, Sleep Out						Yes								
Normal Mode On, Idle Mode On, Sleep Out						Yes								
Partial Mode On, Idle Mode Off, Sleep Out						Yes								
Partial Mode On, Idle Mode On, Sleep Out						Yes								
Sleep In						Yes								

Default									
	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>All the parameters are 00h</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>All the parameters are 00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	All the parameters are 00h	SW Reset	No change	HW Reset	All the parameters are 00h
	Status	Default Value							
	Power On Sequence	All the parameters are 00h							
SW Reset	No change								
HW Reset	All the parameters are 00h								

8.2.63. Power_Setting (D0h)

D0H	Power_Setting																																																																																																																		
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																						
Command	0	1	↑	x	1	1	0	1	0	0	0	0	D0																																																																																																						
1 st Parameter	1	1	↑	x	0	0	0	0	0	VC[2]	VC[1]	VC[0]	07																																																																																																						
2 nd Parameter	1	1	↑	x	0	0	0	0	0	BT[2]	BT[1]	BT[0]	04																																																																																																						
3 rd Parameter	1	1	↑	x	VCIRE	0	0	VRH[4]	VRH[3]	VRH[2]	VRH[1]	VRH[0]	8C																																																																																																						
Description	<p>VC[2:0] Sets the ratio factor of Vci to generate the reference voltages Vci1.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VC[2:0]</th> <th>Vci1 voltage</th> </tr> </thead> <tbody> <tr><td>3'h0</td><td>0.95 x Vci</td></tr> <tr><td>3'h1</td><td>0.90 x Vci</td></tr> <tr><td>3'h2</td><td>0.85 x Vci</td></tr> <tr><td>3'h3</td><td>0.80 x Vci</td></tr> <tr><td>3'h4</td><td>0.75 x Vci</td></tr> <tr><td>3'h5</td><td>0.70 x Vci</td></tr> <tr><td>3'h6</td><td>Setting Prohibited</td></tr> <tr><td>3'h7</td><td>1.0 x Vci</td></tr> </tbody> </table> <p>BT[2:0] Sets the Step up factor and output voltage level from the reference voltages Vci1.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BT[2:0]</th> <th>DDVDH</th> <th>VCL</th> <th>VGH</th> <th>VGL</th> </tr> </thead> <tbody> <tr> <td>3'h0</td> <td>Vci1 x 2</td> <td>- Vci1</td> <td rowspan="3">Vci1 x 6</td> <td>- Vci1 x 5</td> </tr> <tr> <td>3'h1</td> <td rowspan="2">Vci1 x 2</td> <td rowspan="2">- Vci1</td> <td>- Vci1 x 4</td> </tr> <tr> <td>3'h2</td> <td>- Vci1 x 3</td> </tr> <tr> <td>3'h3</td> <td rowspan="3">Vci1 x 2</td> <td rowspan="3">- Vci1</td> <td rowspan="3">Vci1 x 5</td> <td>- Vci1 x 5</td> </tr> <tr> <td>3'h4</td> <td>- Vci1 x 4</td> </tr> <tr> <td>3'h5</td> <td>- Vci1 x 3</td> </tr> <tr> <td>3'h6</td> <td rowspan="2">Vci1 x 2</td> <td rowspan="2">- Vci1</td> <td rowspan="2">Vci1 x 4</td> <td>- Vci1 x 4</td> </tr> <tr> <td>3'h7</td> <td>- Vci1 x 3</td> </tr> </tbody> </table> <p>Note 1: Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages. Note 2: Set following voltages within the respective ranges: DDVDH = 6.0V (max) VGH = 18.0V (max) VGL = -15.0V (max) VCL = -3.0V (max).</p> <p>VCIRE: Select the external reference voltage VciLVL or internal reference voltage VCIR.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>VCIRE=0</td> <td>External reference voltage VciLVL</td> </tr> <tr> <td>VCIRE = 1</td> <td>Internal reference voltage 2.5V (default)</td> </tr> </table> <p>VRH[4:0]: Sets the factor to generate VREG1OUT from VCI</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VRH[4:0]</th> <th>VREG1OUT</th> <th>VRH[4:0]</th> <th>VREG1OUT</th> </tr> </thead> <tbody> <tr><td>5'h0</td><td>VciLVL x 1.600</td><td>5'h0</td><td>2.5 x 1.600 = 4.0000</td></tr> <tr><td>5'h1</td><td>VciLVL x 1.625</td><td>5'h1</td><td>2.5 x 1.625 = 4.0625</td></tr> <tr><td>5'h2</td><td>VciLVL x 1.650</td><td>5'h2</td><td>2.5 x 1.650 = 4.1250</td></tr> <tr><td>5'h3</td><td>VciLVL x 1.675</td><td>5'h3</td><td>2.5 x 1.675 = 4.1875</td></tr> <tr><td>5'h4</td><td>VciLVL x 1.700</td><td>5'h4</td><td>2.5 x 1.700 = 4.2500</td></tr> <tr><td>5'h5</td><td>VciLVL x 1.725</td><td>5'h5</td><td>2.5 x 1.725 = 4.3125</td></tr> <tr><td>5'h6</td><td>VciLVL x 1.750</td><td>5'h6</td><td>2.5 x 1.750 = 4.3750</td></tr> <tr><td>5'h7</td><td>VciLVL x 1.775</td><td>5'h7</td><td>2.5 x 1.775 = 4.4375</td></tr> <tr><td>5'h8</td><td>VciLVL x 1.800</td><td>5'h8</td><td>2.5 x 1.800 = 4.5000</td></tr> <tr><td>5'h9</td><td>VciLVL x 1.825</td><td>5'h9</td><td>2.5 x 1.825 = 4.5625</td></tr> <tr><td>5'hA</td><td>VciLVL x 1.850</td><td>5'hA</td><td>2.5 x 1.850 = 4.6250</td></tr> </tbody> </table>													VC[2:0]	Vci1 voltage	3'h0	0.95 x Vci	3'h1	0.90 x Vci	3'h2	0.85 x Vci	3'h3	0.80 x Vci	3'h4	0.75 x Vci	3'h5	0.70 x Vci	3'h6	Setting Prohibited	3'h7	1.0 x Vci	BT[2:0]	DDVDH	VCL	VGH	VGL	3'h0	Vci1 x 2	- Vci1	Vci1 x 6	- Vci1 x 5	3'h1	Vci1 x 2	- Vci1	- Vci1 x 4	3'h2	- Vci1 x 3	3'h3	Vci1 x 2	- Vci1	Vci1 x 5	- Vci1 x 5	3'h4	- Vci1 x 4	3'h5	- Vci1 x 3	3'h6	Vci1 x 2	- Vci1	Vci1 x 4	- Vci1 x 4	3'h7	- Vci1 x 3	VCIRE=0	External reference voltage VciLVL	VCIRE = 1	Internal reference voltage 2.5V (default)	VRH[4:0]	VREG1OUT	VRH[4:0]	VREG1OUT	5'h0	VciLVL x 1.600	5'h0	2.5 x 1.600 = 4.0000	5'h1	VciLVL x 1.625	5'h1	2.5 x 1.625 = 4.0625	5'h2	VciLVL x 1.650	5'h2	2.5 x 1.650 = 4.1250	5'h3	VciLVL x 1.675	5'h3	2.5 x 1.675 = 4.1875	5'h4	VciLVL x 1.700	5'h4	2.5 x 1.700 = 4.2500	5'h5	VciLVL x 1.725	5'h5	2.5 x 1.725 = 4.3125	5'h6	VciLVL x 1.750	5'h6	2.5 x 1.750 = 4.3750	5'h7	VciLVL x 1.775	5'h7	2.5 x 1.775 = 4.4375	5'h8	VciLVL x 1.800	5'h8	2.5 x 1.800 = 4.5000	5'h9	VciLVL x 1.825	5'h9	2.5 x 1.825 = 4.5625	5'hA	VciLVL x 1.850	5'hA	2.5 x 1.850 = 4.6250
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		<p>When VCI<2.5V, Internal reference voltage will be same as VCI.</p> <p>Make sure that VC[2:0] and VRH[3:0] setting restriction: $VREG1OUT \leq (DDVDH - 0.2)V$.</p>																																																																													
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8.2.64. VCOM Control (D1h)

D1H	VCOM Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	1	D1
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SEL VCM	00
2 nd Parameter	1	1	↑	x	0	VCM[6]	VCM[5]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]	40
3 rd Parameter	1	1	↑	x	0	0	0	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	0F

SELVCM: Selection the VCM setting. When the NV memory is programmed, the SELVCM will be set as '1' automatically.

SELVCM =0	Register D1h for VCM setting
SELVCM =1	NV Memory selected for VCM setting

VCM [6:0] is used to set factor to generate VCOMH voltage from the reference voltage VREG1OUT.

Note: VCOMH must be set as higher than Vci.

VCM[6:0]	VCOMH	VCM[6:0]	VCOMH
7'h00	VREG1OUT x 0.492	7'h40	VREG1OUT x 0.748
7'h01	VREG1OUT x 0.496	7'h41	VREG1OUT x 0.752
7'h02	VREG1OUT x 0.500	7'h42	VREG1OUT x 0.756
7'h03	VREG1OUT x 0.504	7'h43	VREG1OUT x 0.760
7'h04	VREG1OUT x 0.508	7'h44	VREG1OUT x 0.764
7'h05	VREG1OUT x 0.512	7'h45	VREG1OUT x 0.768
7'h06	VREG1OUT x 0.516	7'h46	VREG1OUT x 0.772
7'h07	VREG1OUT x 0.520	7'h47	VREG1OUT x 0.776
7'h08	VREG1OUT x 0.524	7'h48	VREG1OUT x 0.780
7'h09	VREG1OUT x 0.528	7'h49	VREG1OUT x 0.784
7'h0A	VREG1OUT x 0.532	7'h4A	VREG1OUT x 0.788
7'h0B	VREG1OUT x 0.536	7'h4B	VREG1OUT x 0.792
7'h0C	VREG1OUT x 0.540	7'h4C	VREG1OUT x 0.796
7'h0D	VREG1OUT x 0.544	7'h4D	VREG1OUT x 0.800
7'h0E	VREG1OUT x 0.548	7'h4E	VREG1OUT x 0.804
7'h0F	VREG1OUT x 0.552	7'h4F	VREG1OUT x 0.808
7'h10	VREG1OUT x 0.556	7'h50	VREG1OUT x 0.812
7'h11	VREG1OUT x 0.560	7'h51	VREG1OUT x 0.816
7'h12	VREG1OUT x 0.564	7'h52	VREG1OUT x 0.820
7'h13	VREG1OUT x 0.568	7'h53	VREG1OUT x 0.824
7'h14	VREG1OUT x 0.572	7'h54	VREG1OUT x 0.828
7'h15	VREG1OUT x 0.576	7'h55	VREG1OUT x 0.832
7'h16	VREG1OUT x 0.580	7'h56	VREG1OUT x 0.836
7'h17	VREG1OUT x 0.584	7'h57	VREG1OUT x 0.840
7'h18	VREG1OUT x 0.588	7'h58	VREG1OUT x 0.844
7'h19	VREG1OUT x 0.592	7'h59	VREG1OUT x 0.848
7'h1A	VREG1OUT x 0.596	7'h5A	VREG1OUT x 0.852
7'h1B	VREG1OUT x 0.600	7'h5B	VREG1OUT x 0.856
7'h1C	VREG1OUT x 0.604	7'h5C	VREG1OUT x 0.860
7'h1D	VREG1OUT x 0.608	7'h5D	VREG1OUT x 0.864
7'h1E	VREG1OUT x 0.612	7'h5E	VREG1OUT x 0.868
7'h1F	VREG1OUT x 0.616	7'h5F	VREG1OUT x 0.872
7'h20	VREG1OUT x 0.620	7'h60	VREG1OUT x 0.876
7'h21	VREG1OUT x 0.624	7'h61	VREG1OUT x 0.880
7'h22	VREG1OUT x 0.628	7'h62	VREG1OUT x 0.884
7'h23	VREG1OUT x 0.632	7'h63	VREG1OUT x 0.888
7'h24	VREG1OUT x 0.636	7'h64	VREG1OUT x 0.892
7'h25	VREG1OUT x 0.640	7'h65	VREG1OUT x 0.896

Description

7'h26	VREG1OUT x 0.644	7'h66	VREG1OUT x 0.900
7'h27	VREG1OUT x 0.648	7'h67	VREG1OUT x 0.904
7'h28	VREG1OUT x 0.652	7'h68	VREG1OUT x 0.908
7'h29	VREG1OUT x 0.656	7'h69	VREG1OUT x 0.912
7'h2A	VREG1OUT x 0.660	7'h6A	VREG1OUT x 0.916
7'h2B	VREG1OUT x 0.664	7'h6B	VREG1OUT x 0.920
7'h2C	VREG1OUT x 0.668	7'h6C	VREG1OUT x 0.924
7'h2D	VREG1OUT x 0.672	7'h6D	VREG1OUT x 0.928
7'h2E	VREG1OUT x 0.676	7'h6E	VREG1OUT x 0.932
7'h2F	VREG1OUT x 0.680	7'h6F	VREG1OUT x 0.936
7'h30	VREG1OUT x 0.684	7'h70	VREG1OUT x 0.940
7'h31	VREG1OUT x 0.688	7'h71	VREG1OUT x 0.944
7'h32	VREG1OUT x 0.692	7'h72	VREG1OUT x 0.948
7'h33	VREG1OUT x 0.696	7'h73	VREG1OUT x 0.952
7'h34	VREG1OUT x 0.700	7'h74	VREG1OUT x 0.956
7'h35	VREG1OUT x 0.704	7'h75	VREG1OUT x 0.960
7'h36	VREG1OUT x 0.708	7'h76	VREG1OUT x 0.964
7'h37	VREG1OUT x 0.712	7'h77	VREG1OUT x 0.968
7'h38	VREG1OUT x 0.716	7'h78	VREG1OUT x 0.972
7'h39	VREG1OUT x 0.720	7'h79	VREG1OUT x 0.976
7'h3A	VREG1OUT x 0.724	7'h7A	VREG1OUT x 0.980
7'h3B	VREG1OUT x 0.728	7'h7B	VREG1OUT x 0.984
7'h3C	VREG1OUT x 0.732	7'h7C	VREG1OUT x 0.988
7'h3D	VREG1OUT x 0.736	7'h7D	VREG1OUT x 0.992
7'h3E	VREG1OUT x 0.740	7'h7E	VREG1OUT x 0.996
7'h3F	VREG1OUT x 0.744	7'h7F	VREG1OUT x 1.000

VDV[4:0] is used to set the VCOM alternating amplitude in the range of VREG1OUT x 0.70 to VREG1OUT x 1.32.

VDV[4:0]	VCOM amplitude	VDV[4:0]	VCOM amplitude
5'h00	VREG1OUT x 0.70	5'h10	VREG1OUT x 1.02
5'h01	VREG1OUT x 0.72	5'h11	VREG1OUT x 1.04
5'h02	VREG1OUT x 0.74	5'h12	VREG1OUT x 1.06
5'h03	VREG1OUT x 0.76	5'h13	VREG1OUT x 1.08
5'h04	VREG1OUT x 0.78	5'h14	VREG1OUT x 1.10
5'h05	VREG1OUT x 0.80	5'h15	VREG1OUT x 1.12
5'h06	VREG1OUT x 0.82	5'h16	VREG1OUT x 1.14
5'h07	VREG1OUT x 0.84	5'h17	VREG1OUT x 1.16
5'h08	VREG1OUT x 0.86	5'h18	VREG1OUT x 1.18
5'h09	VREG1OUT x 0.88	5'h19	VREG1OUT x 1.20
5'h0A	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.22
5'h0B	VREG1OUT x 0.92	5'h1B	VREG1OUT x 1.24
5'h0C	VREG1OUT x 0.94	5'h1C	VREG1OUT x 1.26
5'h0D	VREG1OUT x 0.96	5'h1D	VREG1OUT x 1.28
5'h0E	VREG1OUT x 0.98	5'h1E	VREG1OUT x 1.30
5'h0F	VREG1OUT x 1.00	5'h1F	VREG1OUT x 1.32

Set VDV[4:0] to let VCOM amplitude less than 6V.

Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>VCM[5:0]=6'h40, VDV[4:0]=5'h0F, SELVCM=1'h0</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>VCM[5:0]=6'h40, VDV[4:0]=5'h0F, SELVCM=1'h0</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	VCM[5:0]=6'h40, VDV[4:0]=5'h0F, SELVCM=1'h0	SW Reset	No change	HW Reset	VCM[5:0]=6'h40, VDV[4:0]=5'h0F, SELVCM=1'h0				
Status	Default Value												
Power On Sequence	VCM[5:0]=6'h40, VDV[4:0]=5'h0F, SELVCM=1'h0												
SW Reset	No change												
HW Reset	VCM[5:0]=6'h40, VDV[4:0]=5'h0F, SELVCM=1'h0												

8.2.65. Power_Setting for Normal Mode (D2h)

D2H	Power_Setting for Normal Mode																																																																											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																															
Command	0	1	↑	x	1	1	0	1	0	0	1	0	D2																																																															
1 st Parameter	1	1	↑	x	0	0	0	0	0	AP0[2]	AP0[1]	AP0[0]	01																																																															
2 nd Parameter	1	1	↑	x	0	DC10[2]	DC10[1]	DC10[0]	0	DC00[2]	DC00[1]	DC00[0]	44																																																															
Description	<p>AP0[2:0]</p> <p>AP0 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.</p> <table border="1"> <thead> <tr> <th>AP0[2:0]</th> <th>Gamma Driver Amplifier</th> <th>Source Driver Amplifier</th> </tr> </thead> <tbody> <tr><td>3'h0</td><td>Halt operation</td><td>Halt operation</td></tr> <tr><td>3'h1</td><td>1.00</td><td>1.00</td></tr> <tr><td>3'h2</td><td>1.00</td><td>0.75</td></tr> <tr><td>3'h3</td><td>1.00</td><td>0.50</td></tr> <tr><td>3'h4</td><td>0.75</td><td>1.00</td></tr> <tr><td>3'h5</td><td>0.75</td><td>0.75</td></tr> <tr><td>3'h6</td><td>0.75</td><td>0.50</td></tr> <tr><td>3'h7</td><td>0.50</td><td>0.50</td></tr> </tbody> </table> <p>DC00[2:0], DC10[2:0]</p> <p>DC00/DC10 are used to select the charge-pump frequency of circuit and circuit2.</p> <table border="1"> <thead> <tr> <th>DC00[1:0]</th> <th>Step-up circuit 1 clock frequency (fDCDC1)</th> </tr> </thead> <tbody> <tr><td>2'h0</td><td>Fosc</td></tr> <tr><td>2'h1</td><td>Fosc / 2</td></tr> <tr><td>2'h2</td><td>Fosc / 4</td></tr> <tr><td>2'h3</td><td>Fosc / 8</td></tr> <tr><td>2'h4</td><td>Fosc / 16</td></tr> <tr><td>2'h5</td><td>Fosc / 32</td></tr> <tr><td>2'h6</td><td>Fosc / 64</td></tr> <tr><td>2'h7</td><td>Setting inhibited</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>DC10[1:0]</th> <th>Step-up circuit 2 clock frequency (fDCDC2)</th> </tr> </thead> <tbody> <tr><td>2'h0</td><td>Fosc / 16</td></tr> <tr><td>2'h1</td><td>Fosc / 32</td></tr> <tr><td>2'h2</td><td>Fosc / 64</td></tr> <tr><td>2'h3</td><td>Fosc / 128</td></tr> <tr><td>2'h4</td><td>Fosc / 256</td></tr> <tr><td>2'h5</td><td>Fosc / 512</td></tr> <tr><td>2'h6</td><td>Setting inhibited</td></tr> <tr><td>2'h7</td><td>Setting inhibited</td></tr> </tbody> </table>													AP0[2:0]	Gamma Driver Amplifier	Source Driver Amplifier	3'h0	Halt operation	Halt operation	3'h1	1.00	1.00	3'h2	1.00	0.75	3'h3	1.00	0.50	3'h4	0.75	1.00	3'h5	0.75	0.75	3'h6	0.75	0.50	3'h7	0.50	0.50	DC00[1:0]	Step-up circuit 1 clock frequency (fDCDC1)	2'h0	Fosc	2'h1	Fosc / 2	2'h2	Fosc / 4	2'h3	Fosc / 8	2'h4	Fosc / 16	2'h5	Fosc / 32	2'h6	Fosc / 64	2'h7	Setting inhibited	DC10[1:0]	Step-up circuit 2 clock frequency (fDCDC2)	2'h0	Fosc / 16	2'h1	Fosc / 32	2'h2	Fosc / 64	2'h3	Fosc / 128	2'h4	Fosc / 256	2'h5	Fosc / 512	2'h6	Setting inhibited	2'h7	Setting inhibited
	AP0[2:0]	Gamma Driver Amplifier	Source Driver Amplifier																																																																									
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DC10[1:0]	Step-up circuit 2 clock frequency (fDCDC2)																																																																											
2'h0	Fosc / 16																																																																											
2'h1	Fosc / 32																																																																											
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Default	Status		Default Value	
	Power On Sequence	AP0[2:0]=3'h1, DC10[2:0]=3'h4, DC00[2:0]=3'h4		
	SW Reset	No change		
	HW Reset	AP0[2:0]=3'h1, DC10[2:0]=3'h4, DC00[2:0]=3'h4		

8.2.66. Power_Setting for Partial Mode (D3h)

D3H	Power_Setting for Partial Mode																																																																											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																															
Command	0	1	↑	x	1	1	0	1	0	0	1	1	D3																																																															
1 st Parameter	1	1	↑	x	0	0	0	0	0	AP1[2]	AP1[1]	AP1[0]	01																																																															
2 nd Parameter	1	1	↑	x	0	DC11[2]	DC11[1]	DC11[0]	0	DC01[2]	DC01[1]	DC01[0]	44																																																															
Description	<p>AP1[2:0]</p> <p>AP1 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP1=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.</p> <table border="1"> <thead> <tr> <th>AP1[2:0]</th> <th>Gamma Driver Amplifier</th> <th>Source Driver Amplifier</th> </tr> </thead> <tbody> <tr><td>3'h0</td><td>Halt operation</td><td>Halt operation</td></tr> <tr><td>3'h1</td><td>1.00</td><td>1.00</td></tr> <tr><td>3'h2</td><td>1.00</td><td>0.75</td></tr> <tr><td>3'h3</td><td>1.00</td><td>0.50</td></tr> <tr><td>3'h4</td><td>0.75</td><td>1.00</td></tr> <tr><td>3'h5</td><td>0.75</td><td>0.75</td></tr> <tr><td>3'h6</td><td>0.75</td><td>0.50</td></tr> <tr><td>3'h7</td><td>0.50</td><td>0.50</td></tr> </tbody> </table> <p>DC01[2:0], DC11[2:0]</p> <p>DC01/DC11 are used to select the charge-pump frequency of circuit and circuit2.</p> <table border="1"> <thead> <tr> <th>DC01[1:0]</th> <th>Step-up circuit 1 clock frequency (fDCDC1)</th> </tr> </thead> <tbody> <tr><td>2'h0</td><td>Fosc</td></tr> <tr><td>2'h1</td><td>Fosc / 2</td></tr> <tr><td>2'h2</td><td>Fosc / 4</td></tr> <tr><td>2'h3</td><td>Fosc / 8</td></tr> <tr><td>2'h4</td><td>Fosc / 16</td></tr> <tr><td>2'h5</td><td>Fosc / 32</td></tr> <tr><td>2'h6</td><td>Fosc / 64</td></tr> <tr><td>2'h7</td><td>Setting inhibited</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>DC11[1:0]</th> <th>Step-up circuit 2 clock frequency (fDCDC2)</th> </tr> </thead> <tbody> <tr><td>2'h0</td><td>Fosc / 16</td></tr> <tr><td>2'h1</td><td>Fosc / 32</td></tr> <tr><td>2'h2</td><td>Fosc / 64</td></tr> <tr><td>2'h3</td><td>Fosc / 128</td></tr> <tr><td>2'h4</td><td>Fosc / 256</td></tr> <tr><td>2'h5</td><td>Fosc / 512</td></tr> <tr><td>2'h6</td><td>Setting inhibited</td></tr> <tr><td>2'h7</td><td>Setting inhibited</td></tr> </tbody> </table>													AP1[2:0]	Gamma Driver Amplifier	Source Driver Amplifier	3'h0	Halt operation	Halt operation	3'h1	1.00	1.00	3'h2	1.00	0.75	3'h3	1.00	0.50	3'h4	0.75	1.00	3'h5	0.75	0.75	3'h6	0.75	0.50	3'h7	0.50	0.50	DC01[1:0]	Step-up circuit 1 clock frequency (fDCDC1)	2'h0	Fosc	2'h1	Fosc / 2	2'h2	Fosc / 4	2'h3	Fosc / 8	2'h4	Fosc / 16	2'h5	Fosc / 32	2'h6	Fosc / 64	2'h7	Setting inhibited	DC11[1:0]	Step-up circuit 2 clock frequency (fDCDC2)	2'h0	Fosc / 16	2'h1	Fosc / 32	2'h2	Fosc / 64	2'h3	Fosc / 128	2'h4	Fosc / 256	2'h5	Fosc / 512	2'h6	Setting inhibited	2'h7	Setting inhibited
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DC11[1:0]	Step-up circuit 2 clock frequency (fDCDC2)																																																																											
2'h0	Fosc / 16																																																																											
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>AP1[2:0]=3'h1, DC11[2:0]=3'h4, DC01[2:0]=3'h4</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>AP1[2:0]=3'h1, DC11[2:0]=3'h4, DC01[2:0]=3'h4</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	AP1[2:0]=3'h1, DC11[2:0]=3'h4, DC01[2:0]=3'h4	SW Reset	No change	HW Reset	AP1[2:0]=3'h1, DC11[2:0]=3'h4, DC01[2:0]=3'h4
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	Power On Sequence	AP1[2:0]=3'h1, DC11[2:0]=3'h4, DC01[2:0]=3'h4								
	SW Reset	No change								
HW Reset	AP1[2:0]=3'h1, DC11[2:0]=3'h4, DC01[2:0]=3'h4									

8.2.67. Power_Setting for Idle Mode (D4h)

D4H	Power_Setting for Idle Mode																																																																											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																															
Command	0	1	↑	x	1	1	0	1	0	1	0	0	D4																																																															
1 st Parameter	1	1	↑	x	0	0	0	0	0	AP2[2]	AP2[1]	AP2[0]	01																																																															
2 nd Parameter	1	1	↑	x	0	DC12[2]	DC12[1]	DC12[0]	0	DC02[2]	DC02[1]	DC02[0]	44																																																															
Description	<p>AP2[2:0]</p> <p>AP2 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP2=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.</p> <table border="1"> <thead> <tr> <th>AP2[2:0]</th> <th>Gamma Driver Amplifier</th> <th>Source Driver Amplifier</th> </tr> </thead> <tbody> <tr><td>3'h0</td><td>Halt operation</td><td>Halt operation</td></tr> <tr><td>3'h1</td><td>1.00</td><td>1.00</td></tr> <tr><td>3'h2</td><td>1.00</td><td>0.75</td></tr> <tr><td>3'h3</td><td>1.00</td><td>0.50</td></tr> <tr><td>3'h4</td><td>0.75</td><td>1.00</td></tr> <tr><td>3'h5</td><td>0.75</td><td>0.75</td></tr> <tr><td>3'h6</td><td>0.75</td><td>0.50</td></tr> <tr><td>3'h7</td><td>0.50</td><td>0.50</td></tr> </tbody> </table> <p>DC02[2:0], DC12[2:0]</p> <p>DC01/DC11 are used to select the charge-pump frequency of circuit and circuit2.</p> <table border="1"> <thead> <tr> <th>DC02[1:0]</th> <th>Step-up circuit 1 clock frequency (fDCDC1)</th> </tr> </thead> <tbody> <tr><td>2'h0</td><td>Fosc</td></tr> <tr><td>2'h1</td><td>Fosc / 2</td></tr> <tr><td>2'h2</td><td>Fosc / 4</td></tr> <tr><td>2'h3</td><td>Fosc / 8</td></tr> <tr><td>2'h4</td><td>Fosc / 16</td></tr> <tr><td>2'h5</td><td>Fosc / 32</td></tr> <tr><td>2'h6</td><td>Fosc / 64</td></tr> <tr><td>2'h7</td><td>Setting inhibited</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>DC12[1:0]</th> <th>Step-up circuit 2 clock frequency (fDCDC2)</th> </tr> </thead> <tbody> <tr><td>2'h0</td><td>Fosc / 16</td></tr> <tr><td>2'h1</td><td>Fosc / 32</td></tr> <tr><td>2'h2</td><td>Fosc / 64</td></tr> <tr><td>2'h3</td><td>Fosc / 128</td></tr> <tr><td>2'h4</td><td>Fosc / 256</td></tr> <tr><td>2'h5</td><td>Fosc / 512</td></tr> <tr><td>2'h6</td><td>Setting inhibited</td></tr> <tr><td>2'h7</td><td>Setting inhibited</td></tr> </tbody> </table>													AP2[2:0]	Gamma Driver Amplifier	Source Driver Amplifier	3'h0	Halt operation	Halt operation	3'h1	1.00	1.00	3'h2	1.00	0.75	3'h3	1.00	0.50	3'h4	0.75	1.00	3'h5	0.75	0.75	3'h6	0.75	0.50	3'h7	0.50	0.50	DC02[1:0]	Step-up circuit 1 clock frequency (fDCDC1)	2'h0	Fosc	2'h1	Fosc / 2	2'h2	Fosc / 4	2'h3	Fosc / 8	2'h4	Fosc / 16	2'h5	Fosc / 32	2'h6	Fosc / 64	2'h7	Setting inhibited	DC12[1:0]	Step-up circuit 2 clock frequency (fDCDC2)	2'h0	Fosc / 16	2'h1	Fosc / 32	2'h2	Fosc / 64	2'h3	Fosc / 128	2'h4	Fosc / 256	2'h5	Fosc / 512	2'h6	Setting inhibited	2'h7	Setting inhibited
	AP2[2:0]	Gamma Driver Amplifier	Source Driver Amplifier																																																																									
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	Partial Mode On, Idle Mode On, Sleep Out	Yes																																																																										
Sleep In	Yes																																																																											

Default		
	Status	Default Value
	Power On Sequence	AP2[2:0]=3'h1, DC12[2:0]=3'h4, DC02[2:0]=3'h4
	SW Reset	No change
	HW Reset	AP2[2:0]=3'h1, DC11[2:0]=3'h4, DC02[2:0]=3'h4

8.2.68. NV Memory Write (E0h)

E0h	NV Memory Write																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	1	0	0	0	0	0	E0												
1 st Parameter	1	1	↑	x	VM_D [7]	VM_D [6]	VM_D [5]	VM_D [4]	VM_D [3]	VM_D [2]	VM_D [1]	VM_D [0]	00												
Description	<p>This command is used to program the NV memory data.</p> <p>VM_D[7:0]: Use to write the data (including VCM and ID code) into the NV memory data.</p>																								
Restriction																									
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	VM_D[7:0]=8'h00																								
SW Reset	No change																								
HW Reset	VM_D[7:0]=8'h00																								

8.2.69. NV Memory Control (E1h)

E1H	NV Memory Control																											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	↑	x	1	1	1	0	0	0	0	1	E1															
1 st Parameter	1	1	↑	x	0	0	ID_PGM_EN	VCM_PGM_EN	0	0	0	0	00															
Description	<p>This command is used to control the NV memory programming.</p> <p>VCM_PGM_EN: VCM OTP programming enable. When writing the VCOMH NV memory, the bit must be set as '1'.</p> <p><i>When the VCOMH NV memory is programmed, the SELVCM bit of RD1h register will be set as '1' automatically.</i></p> <p><i>Note that: VCM OTP can be written 3 times.</i></p> <p>ID_PGM_EN: ID OTP programming enable. When writing the ID code NV memory, the bit must be set as '1'.</p> <p><i>Note that: ID OTP can be only written 1 time.</i></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>ID_PGM_EN</th> <th>VCM_PGM_EN</th> <th>OTP Programming Selection</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>NV Memory programming disabled</td> </tr> <tr> <td>0</td> <td>1</td> <td>VCM (VCOMH) NV Memory programming enable</td> </tr> <tr> <td>1</td> <td>0</td> <td>ID code NV Memory programming enable</td> </tr> <tr> <td>1</td> <td>1</td> <td>Setting Prohibited</td> </tr> </tbody> </table>													ID_PGM_EN	VCM_PGM_EN	OTP Programming Selection	0	0	NV Memory programming disabled	0	1	VCM (VCOMH) NV Memory programming enable	1	0	ID code NV Memory programming enable	1	1	Setting Prohibited
ID_PGM_EN	VCM_PGM_EN	OTP Programming Selection																										
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Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0	SW Reset	No change	HW Reset	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0							
Status	Default Value																											
Power On Sequence	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0																											
SW Reset	No change																											
HW Reset	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0																											

8.2.70. NV Memory Status Read (E2h)

E2H	NV Memory Status Read																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	1	0	0	0	1	0	E2												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x												
2 nd Parameter	1	↑	1	x	0	0	0	0	0	0	PGM_CNT1	PGM_CNT0	00												
3 rd Parameter	1	↑	1	x	0	NV_VCM[6]	NV_VCM[5]	NV_VCM[4]	NV_VCM[3]	NV_VCM[2]	NV_VCM[1]	NV_VCM[0]	00												
Description	<p>PGM_CNT[1:0]: NV memory programmed record. The bit will increase “+1” automatically when writing the NV_VCM [5:0].</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>PGM_CNT[1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>NV Memory clean</td> </tr> <tr> <td>01</td> <td>NV Memory programmed 1 time</td> </tr> <tr> <td>10</td> <td>NV Memory programmed 2 times</td> </tr> <tr> <td>11</td> <td>NV Memory programmed 3 times</td> </tr> </tbody> </table> <p style="text-align: center;">These bits are read only.</p> <p>NV_VCM [6:0]: NV memory VCM data read value. These bits are read only.</p>													PGM_CNT[1:0]	Description	00	NV Memory clean	01	NV Memory programmed 1 time	10	NV Memory programmed 2 times	11	NV Memory programmed 3 times		
	PGM_CNT[1:0]	Description																							
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	Status	Availability																							
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
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Sleep In	Yes																								
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>PGM_CNT[1:0]=2'h0, NV_VCM[6:0]=7'h0</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>PGM_CNT[1:0]=2'h0, NV_VCM[6:0]=7'h0</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	PGM_CNT[1:0]=2'h0, NV_VCM[6:0]=7'h0	SW Reset	No change	HW Reset	PGM_CNT[1:0]=2'h0, NV_VCM[6:0]=7'h0				
	Status	Default Value																							
	Power On Sequence	PGM_CNT[1:0]=2'h0, NV_VCM[6:0]=7'h0																							
	SW Reset	No change																							
HW Reset	PGM_CNT[1:0]=2'h0, NV_VCM[6:0]=7'h0																								

8.2.71. NV Memory Protection (E3h)

E3H	NV Memory Protection																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	--	1	1	1	0	0	0	1	1	E3												
1 st Parameter	1	1	↑	--	KEY [15]	KEY [14]	KEY [13]	KEY [12]	KEY [11]	KEY [10]	KEY [9]	KEY [8]	00												
2 nd Parameter	1	1	↑	--	KEY [7]	KEY [6]	KEY [5]	KEY [4]	KEY [3]	KEY [2]	KEY [1]	KEY [0]	00												
Description	<p>KEY[15:0]: NV memory programming protection key. When writing OTP data C8h, this register must be set as 0xAA55 to enable OTP programming. If C8h register is not written with 0xAA55, NV Memory programming will fail.</p>																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>KEY[15:0]=16'h0000</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>KEY[15:0]=16'h0000</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	KEY[15:0]=16'h0000	SW Reset	No change	HW Reset	KEY[15:0]=16'h0000				
Status	Default Value																								
Power On Sequence	KEY[15:0]=16'h0000																								
SW Reset	No change																								
HW Reset	KEY[15:0]=16'h0000																								

8.2.72. 3-Gamma Function Control (EAh)

EAH	3-gamma function control																																	
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
Command	0	1	↑	--	1	1	1	0	1	0	1	0	EA																					
1 st Parameter	1	1	↑	--	3_GAM_EN	reserved							00																					
1 st Parameter	1	1	↑	--	GON	DTE	NW[5:0]					C0																						
Description	<p>3_GAM_EN: This bit is used to control the digital 3-gamma function.</p> <table border="1"> <thead> <tr> <th>3_GAM_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>3 gamma function is disabled</td> </tr> <tr> <td>1</td> <td>3 gamma function is enabled</td> </tr> </tbody> </table> <p>NW[5:0]: Set "n" for the number of lines for the VCOM inverting. n=(NW[5:0]+1);</p> <p>DTE, GON: control the gate output level from G1 to G432 as follows.</p> <table border="1"> <thead> <tr> <th>GON</th> <th>DTE</th> <th>Gate Output Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>VGH</td> </tr> <tr> <td>0</td> <td>1</td> <td>VGH</td> </tr> <tr> <td>1</td> <td>0</td> <td>VGL</td> </tr> <tr> <td>1</td> <td>1</td> <td>VGH/VGL</td> </tr> </tbody> </table>													3_GAM_EN	Description	0	3 gamma function is disabled	1	3 gamma function is enabled	GON	DTE	Gate Output Level	0	0	VGH	0	1	VGH	1	0	VGL	1	1	VGH/VGL
	3_GAM_EN	Description																																
	0	3 gamma function is disabled																																
	1	3 gamma function is enabled																																
GON	DTE	Gate Output Level																																
0	0	VGH																																
0	1	VGH																																
1	0	VGL																																
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Restriction																																		
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Partial Mode On, Idle Mode On, Sleep Out	Yes																																	
Sleep In	Yes																																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>3_GAM_EN=1'b0, DTE=1'b1, GON=1'b1</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>3_GAM_EN=1'b0, DTE=1'b1, GON=1'b1</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	3_GAM_EN=1'b0, DTE=1'b1, GON=1'b1	SW Reset	No change	HW Reset	3_GAM_EN=1'b0, DTE=1'b1, GON=1'b1														
	Status	Default Value																																
	Power On Sequence	3_GAM_EN=1'b0, DTE=1'b1, GON=1'b1																																
	SW Reset	No change																																
HW Reset	3_GAM_EN=1'b0, DTE=1'b1, GON=1'b1																																	

8.2.73. Device Code Read (EFh)

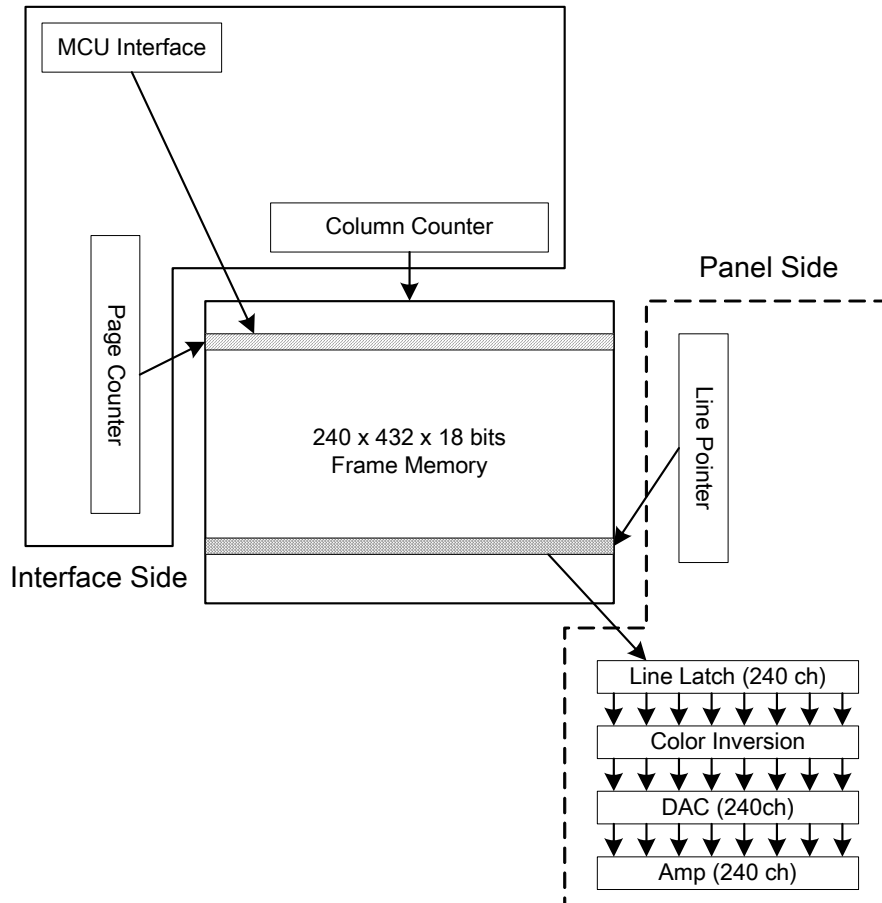
BFH	Device Code Read																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	xx	1	1	1	0	1	1	1	1	EF												
1 st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x												
2 nd parameter	1	↑	1	xx	0	0	0	0	0	0	1	0	02												
3 rd parameter	1	↑	1	xx	0	0	0	0	0	1	0	0	04												
4 th parameter	1	↑	1	xx	1	0	0	1	0	1	0	0	93												
5 th parameter	1	↑	1	xx	1	0	0	0	0	0	0	1	27												
6 th parameter	1	↑	1	xx	1	1	1	1	1	1	1	1	FF												
Description	1 st parameter : dummy read 2 nd parameter : MIPI Alliance code 3 rd parameter : MIPI Alliance code 4 th parameter : Device ID code of ILI9327 5 th parameter : Device ID code of ILI9327 6 th parameter : Exit code (FFh)																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

9. Display Data RAM

9.1. Configuration

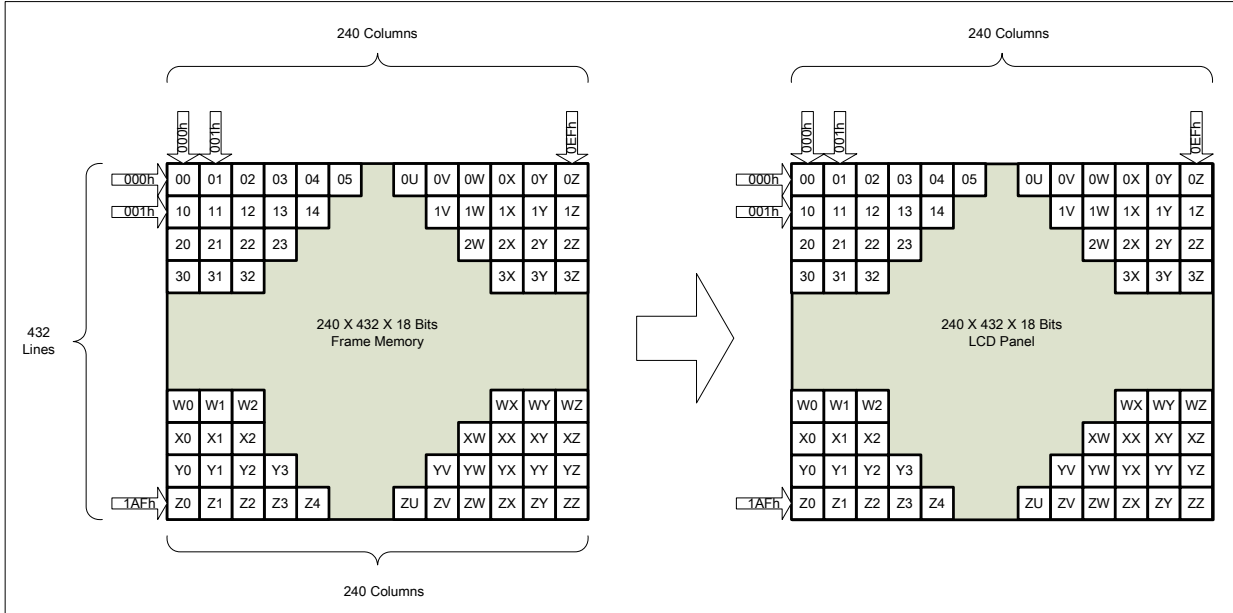
The display data RAM stores display dots and consists of 1,866,240bits (240 x 18 x 432 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC.

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the frame memory.



9.2. Memory to Display Address Mapping

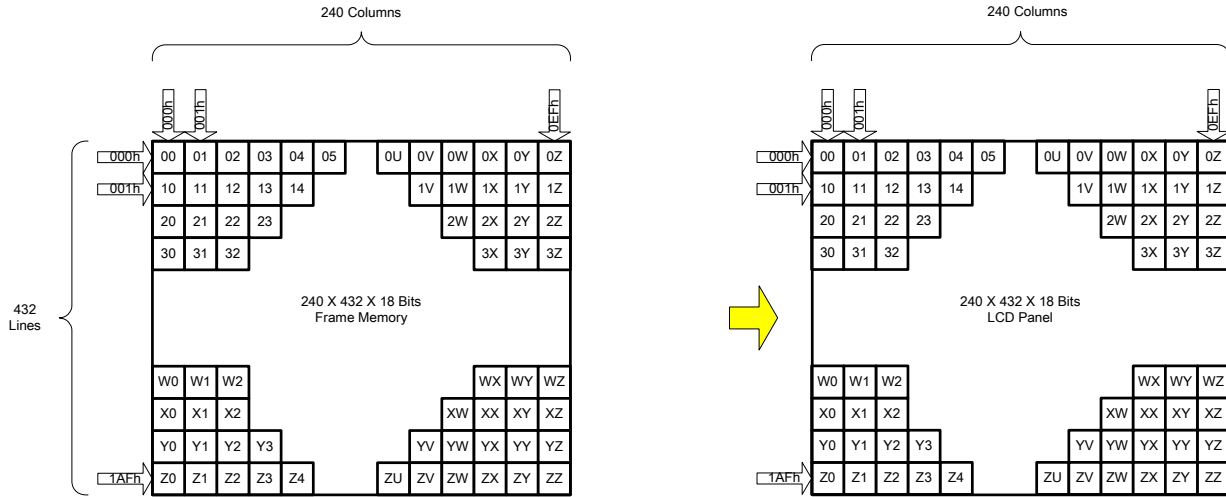
In this mode, content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer 0000h to 01DFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).



9.3. Vertical Scroll Mode

There is a vertical scrolling mode, which is described by the commands “set_scroll_area”(33h) and “set_scroll_start”(37h).

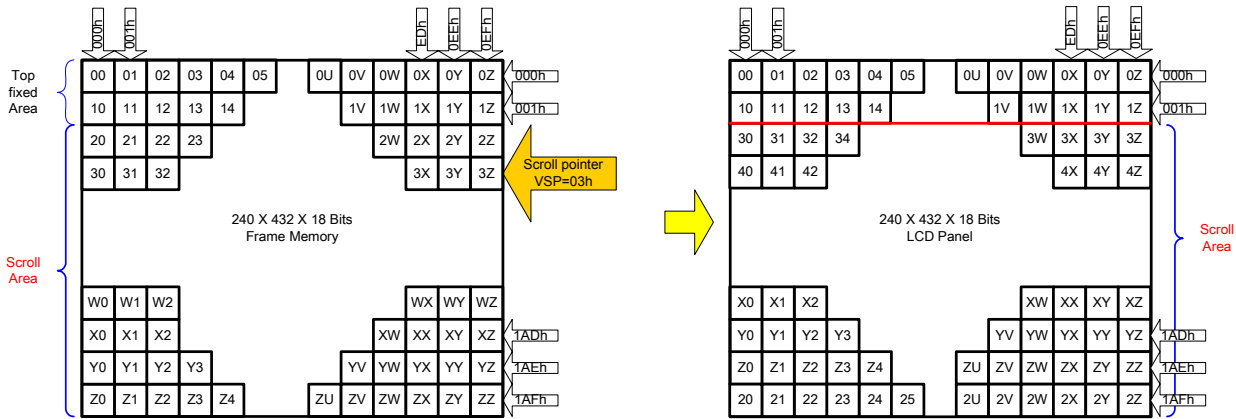
(1) Normal Display On or Partial Mode On, Vertical Scroll Off



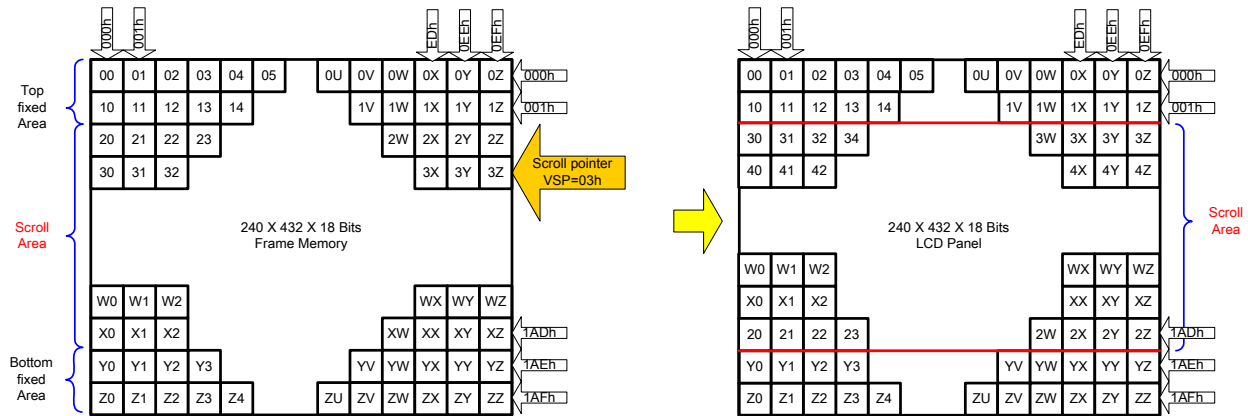
(2) Vertical Scroll Mode

“set_scroll_area(33h)” and “set_scroll_start(37h)” setting define the scroll area.

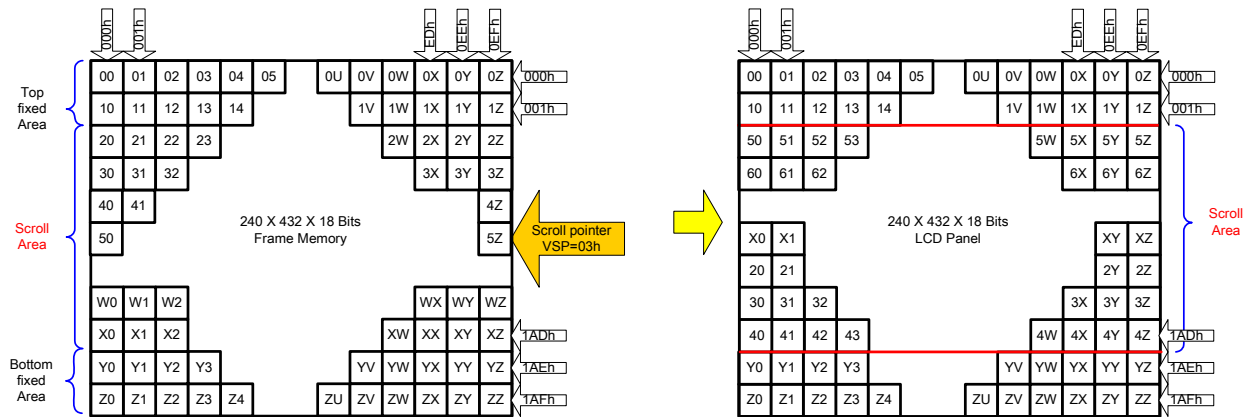
Example1: TFA=2, VSA=430, BFA=0 (set_address_mode(36h) B4=0), VSP=3



Example2: TFA=2,VSA=428,BFA=2 (set_address_mode(36h) B4=0), VSP=3



Example3: TFA=2,VSA=428,BFA=2 (set_address_mode(36h) B4=0), VSP=5



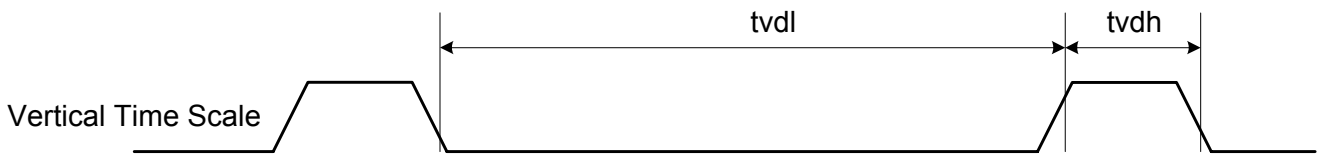
10. Tearing Effect Output

The tearing effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the `set_tear_off` (34h) and `set_tear_on` (35h) commands. The mode of the tearing effect signal is defined by the parameter of the `set_tear_on` (35h) and `set_tear_scanline` (44h) commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

10.1. Tearing Effect Line Modes

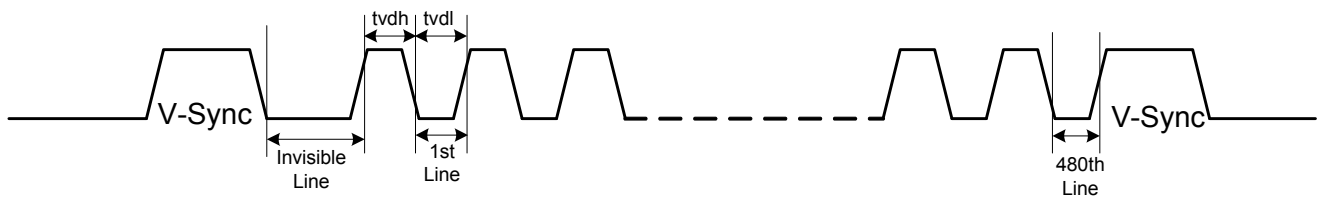
Mode 1 (`set_tear_on`, `TELOM=0`), the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

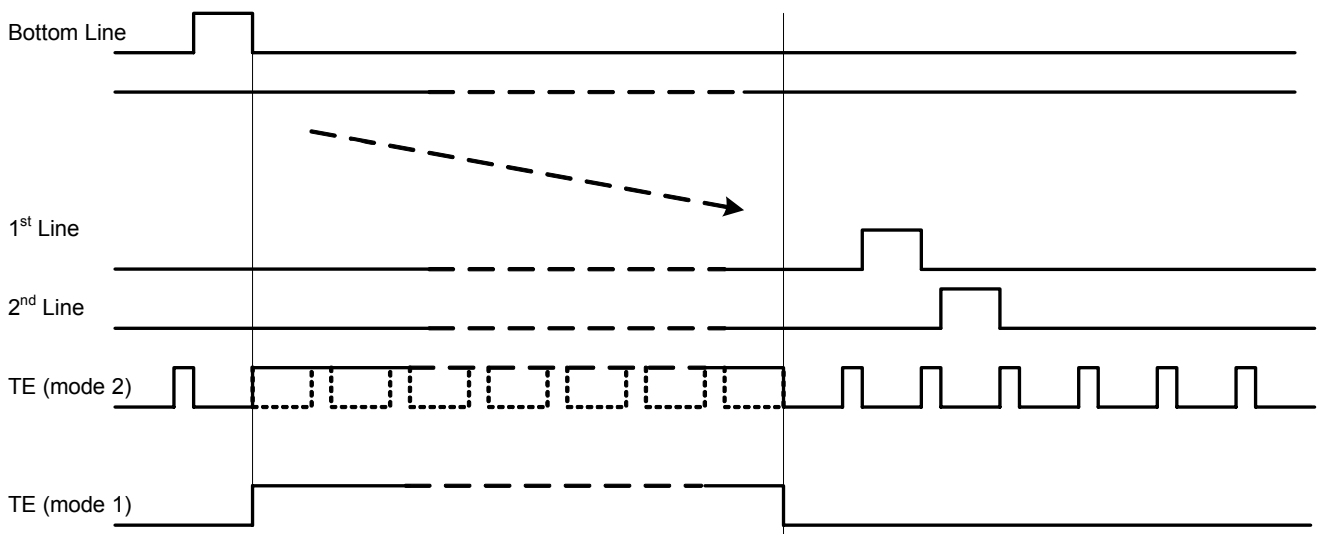
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2 (`set_tear_on`, `TELOM=1`), the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 432 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

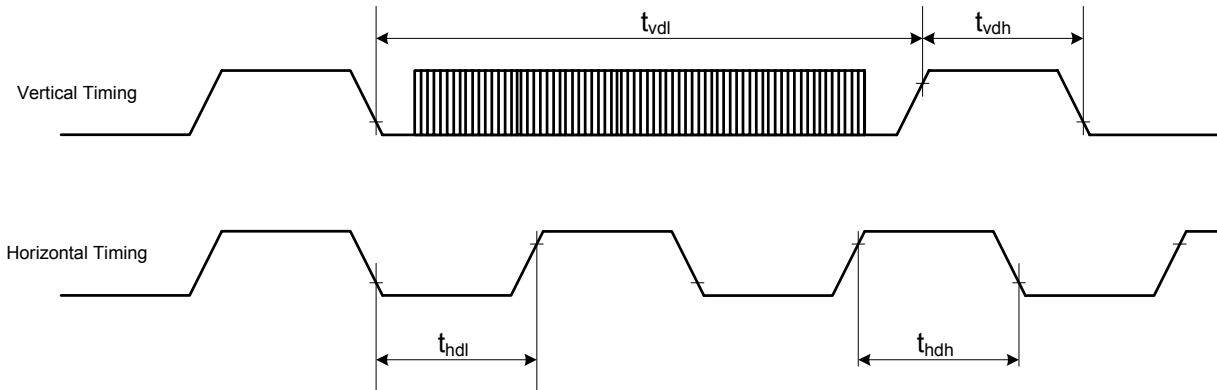
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

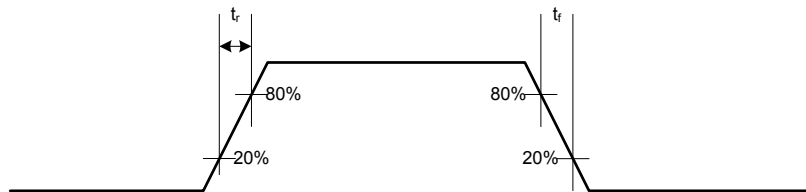


AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	TBD		ms	
t_{vdh}	Vertical timing high duration	TBD		us	
t_{hdl}	Horizontal timing low duration	TBD		us	
t_{hdh}	Horizontal timing high duration	TBD		us	

Notes:

1. The timings in Table 8.3.1 apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid Tearing Effect:

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the `set_tear_off(34h)`, `set_tear_on(35h)` commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

TEON (35h)	TELOM (35h, 1 st bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

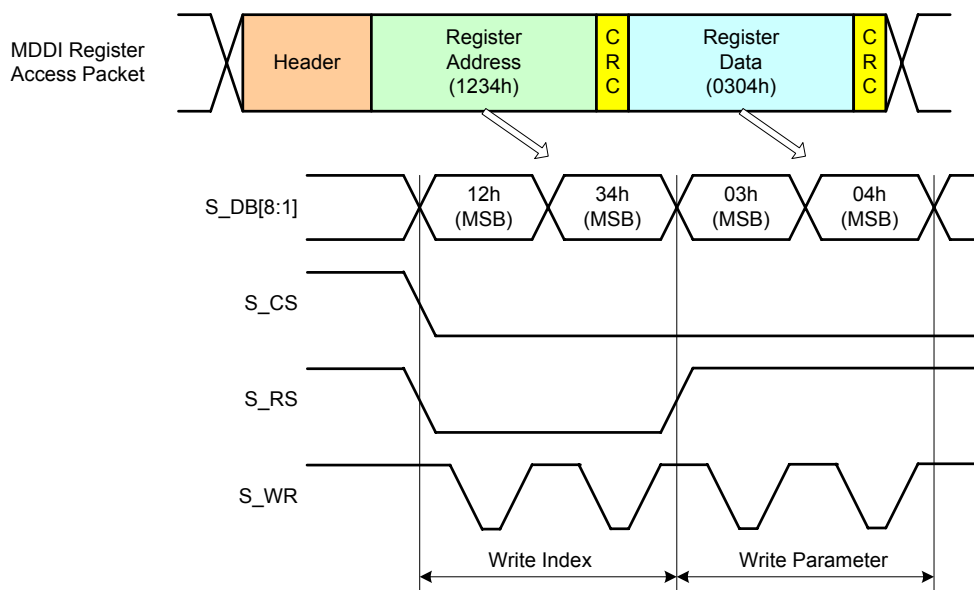
11. Sub-panel Control

TFT type sub panel timing

A. Register data transfer timing

If TFT type sub panel is selected (STN_EN=0), register setting is executed like below figure. Register data is transferred through S_DB[8:0] in 9/8 bit type. Please refer to the MDDI section for the register address direction to sub panel.

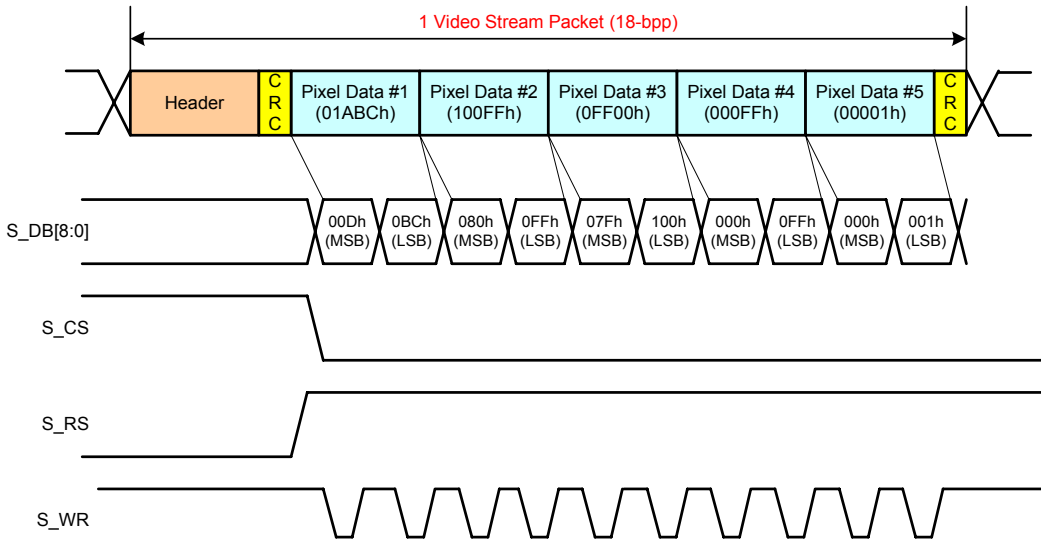
In this mode, data is transferred at two times. First transfer is MSB 8bit and second transfer is LSB 8bit.



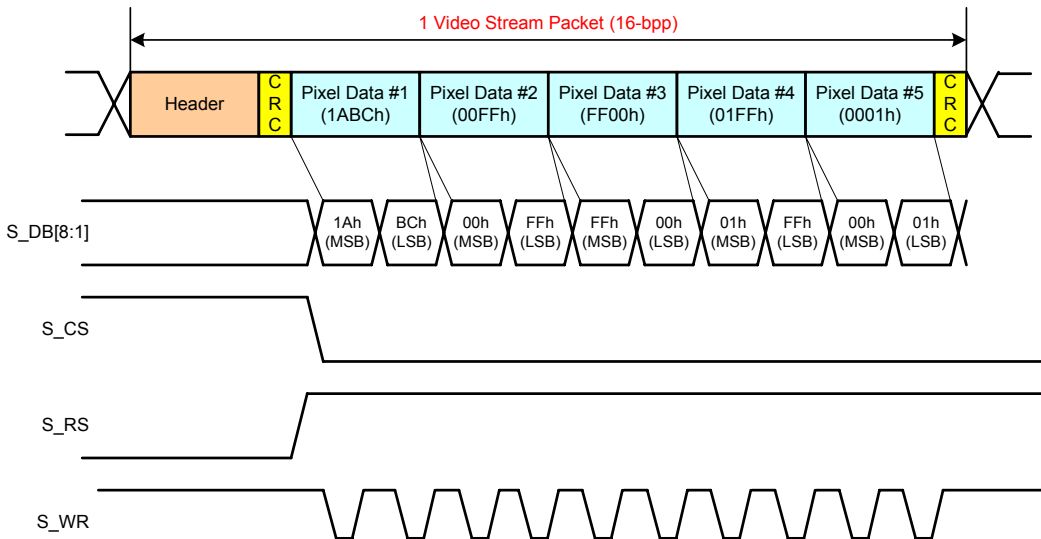
B. Video data transfer timing

In TFT type sub panel, the 9/8-bit mode is selected as setting SUB_IM register.

This figure shows 9-bit sub-panel data bus with 18-bpp video data transfer.



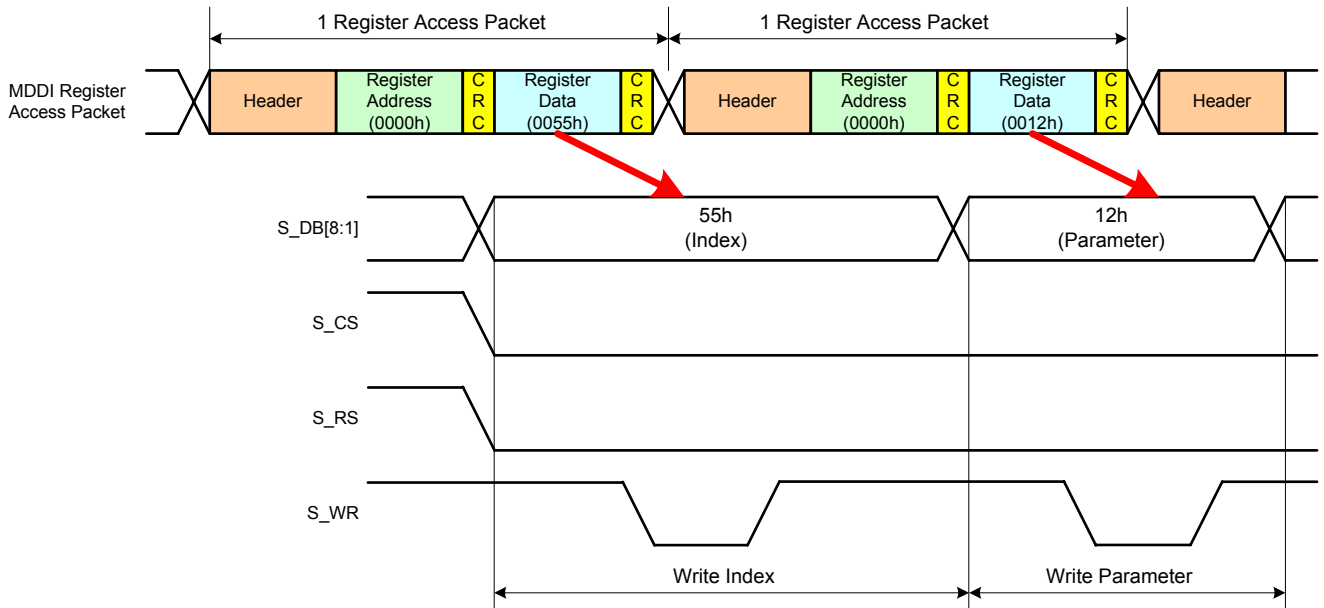
This figure shows 8-bit sub-panel data bus with 16-bpp video data transfer.



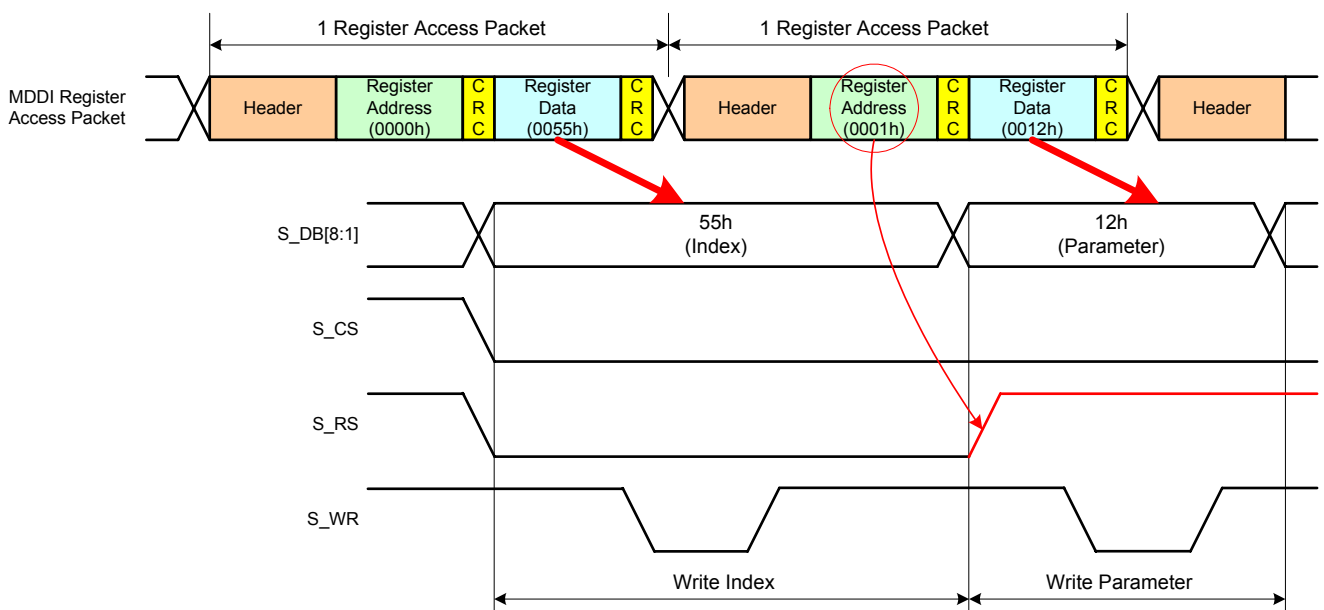
STN type sub panel timing

A. Register data transfer timing

This figure shows conventional type STN mode register data setting. Conventional type does not include parameter. Instruction type is only 8bit. To use STN type, STN_EN is set to "1". In STN type, ILI9327 controls S_RS pin using register address[0] in register access packet. Register address[0] is "0", then S_RS is set to "0", and register address[0] is "1", S_RS is set to "1".



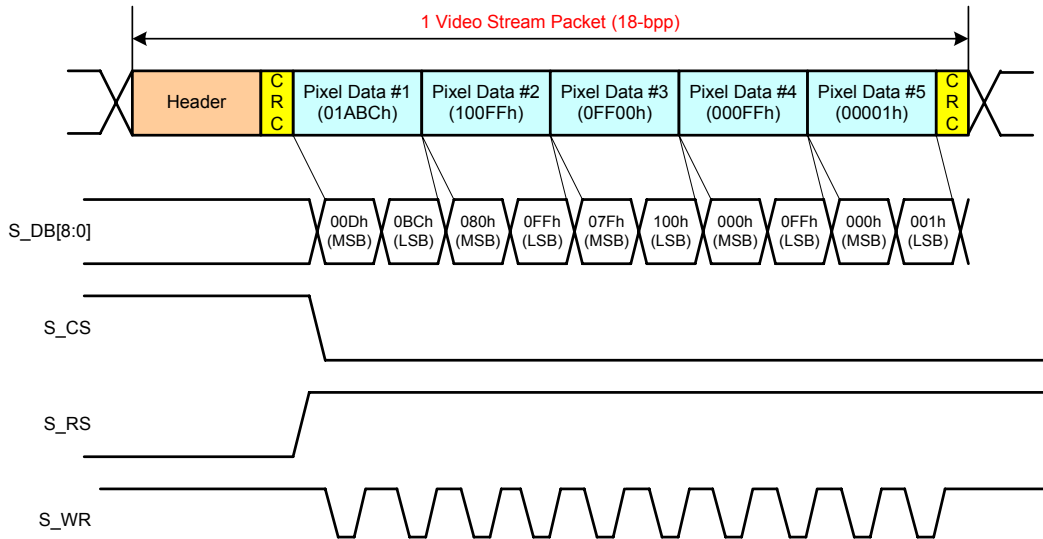
This type is used to include parameter. When instruction is transferred, S_RS is zero, and when parameter is transferred, S_RS is "1". S_RS is controlled using register address[0] of register access packet.



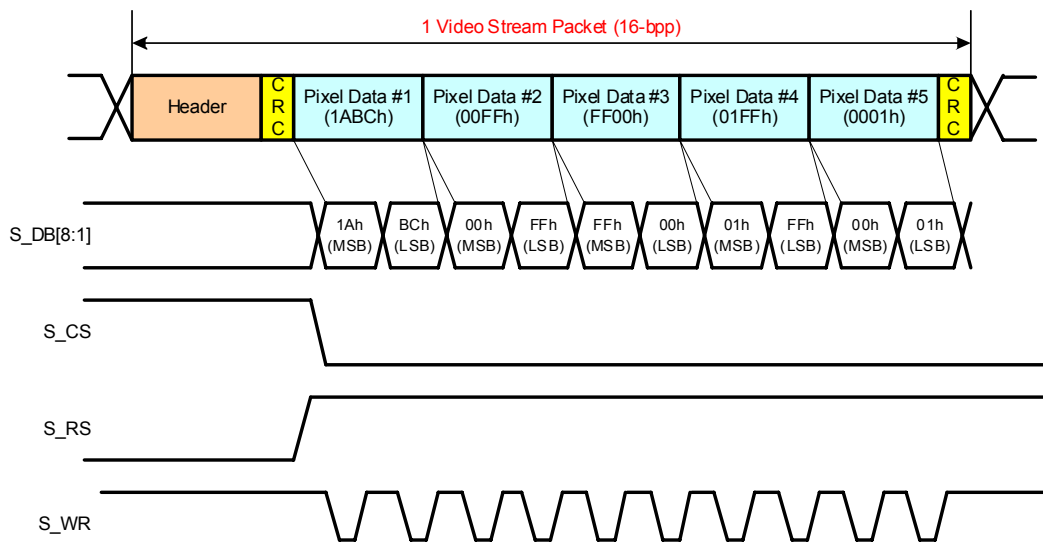
B. Video data transfer timing

In STN mode, video data start register (like 22H in TFT mode) generally is not necessary. But some STN type needs video data start register. If that type STN DDI is used, user has to set the register index.

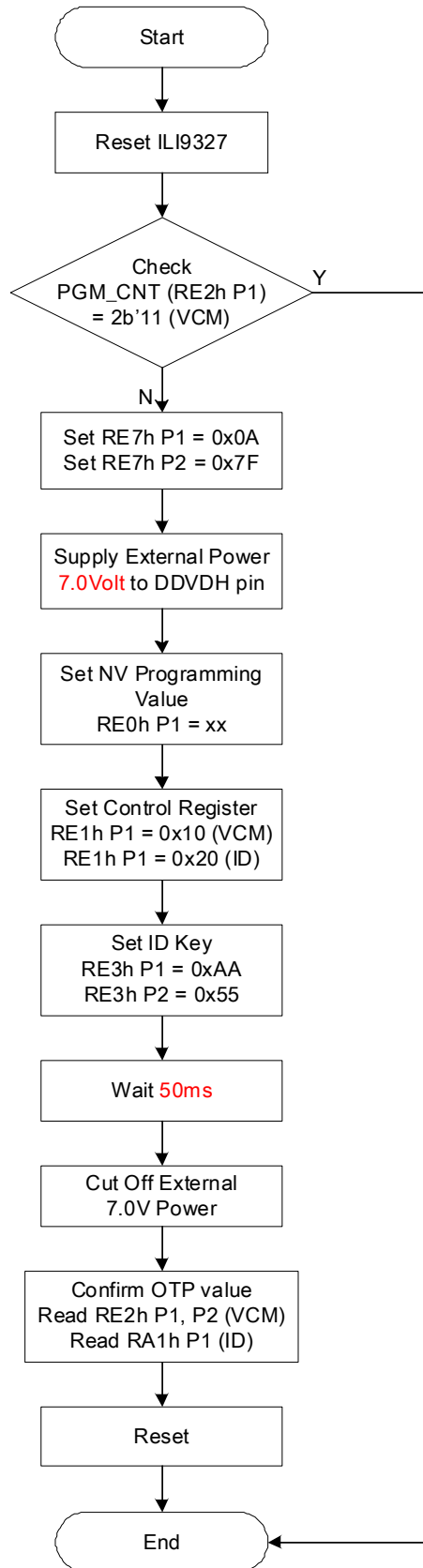
This figure shows STN 9 bit mode video data transfer.



This figure shows STN 8bit mode video data transfer. If STN video data is 16bit mode, data transfer is executed during 2 times. First transfer is MSB 8bits, and second is LSB 8bits.



12. NV Memory Programming Flow



13. Gamma Correction

ILI9327 incorporates the γ -correction function to display 262,144 colors for the LCD panel. The γ -correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9327 available with liquid crystal panels of various characteristics.

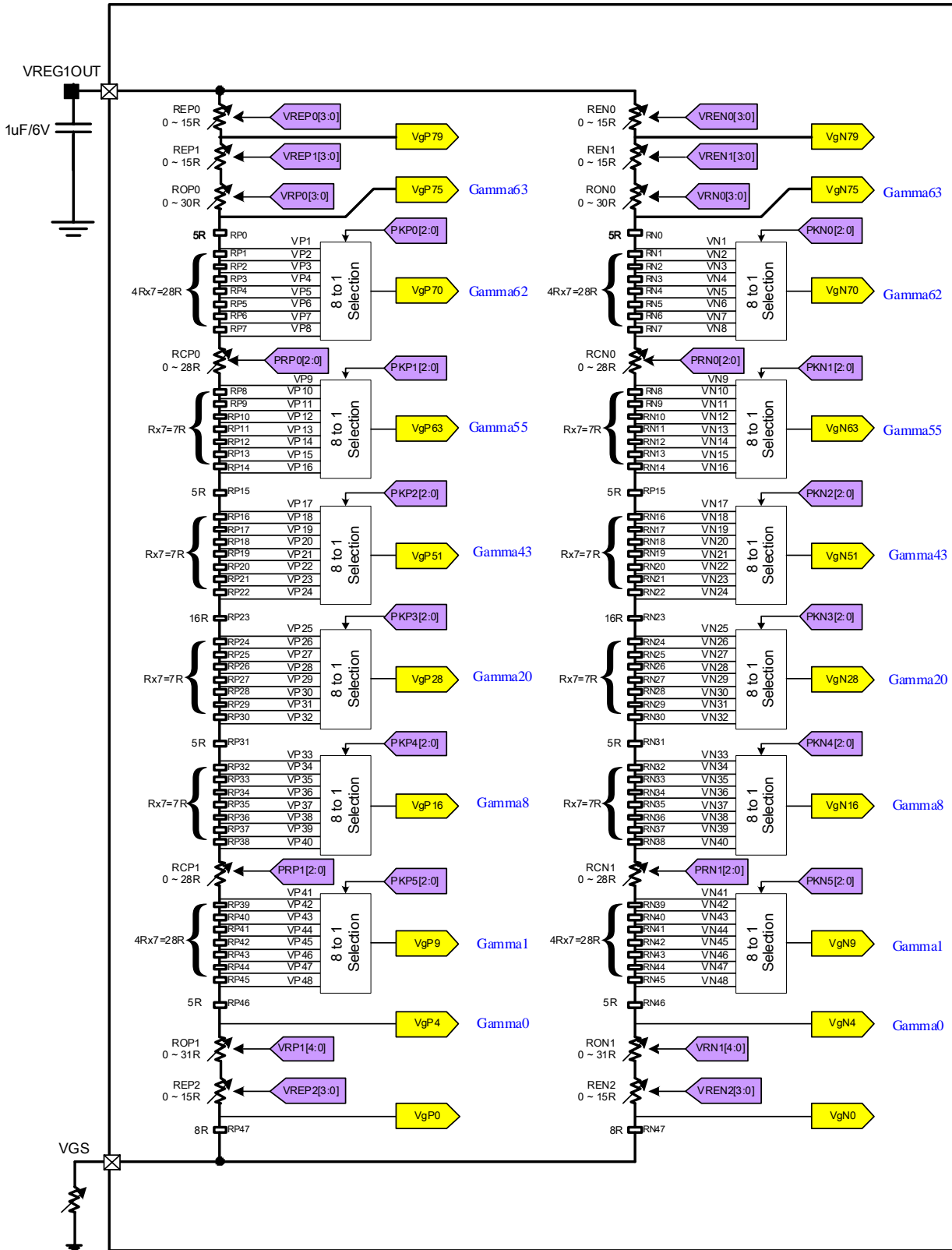
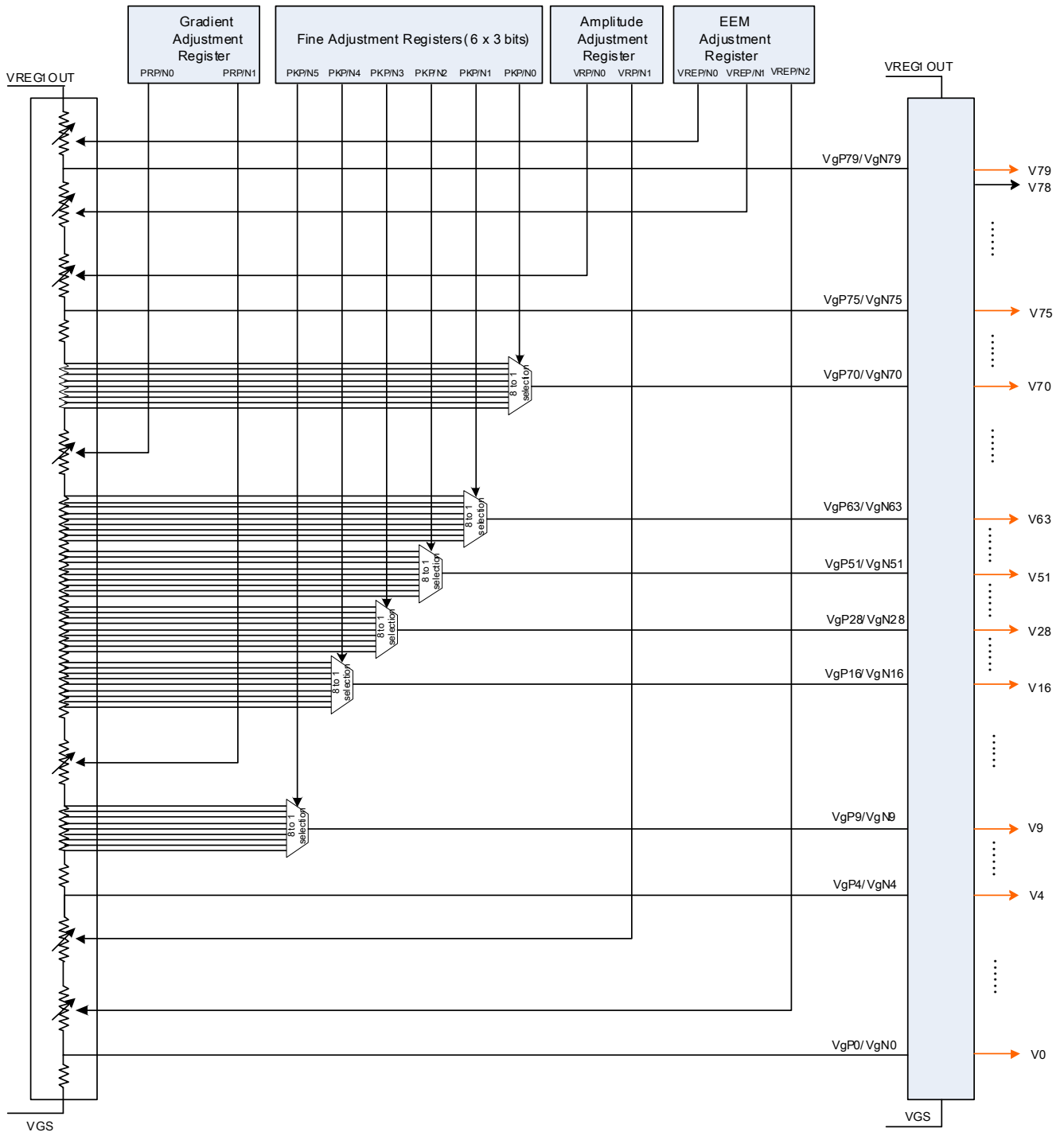


Figure 1 Grayscale Voltage Adjustment



1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers PRP0[2:0]/PRN0[2:0], PRP1[2:0]/PRN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[3:0]/VRN0[3:0], VRP1[4:0]/VRN1[4:0], are used to adjust the

amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

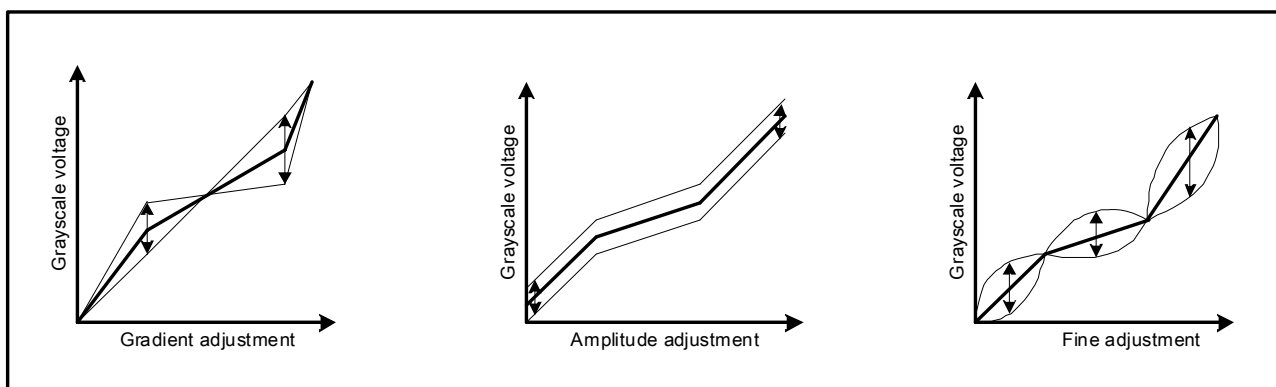


Figure 2 Gamma Curve Adjustment

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 [2:0]	PRN0 [2:0]	Variable resistor VRCP0, VRCN0
	PRP1 [2:0]	PRN1 [2:0]	Variable resistor VRCP1, VRCN1
Amplitude adjustment	VRP0 [3:0]	VRN0 [3:0]	Variable resistor VROP0, VRON0
	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VROP1, VRON1
Fine adjustment	KP0 [2:0]	KN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	KP1 [2:0]	KN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	KP2 [2:0]	KN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	KP3 [2:0]	KN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	KP4 [2:0]	KN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	KP5 [2:0]	KN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ -correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable resistors

ILI9327 uses variable resistors of the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of

these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment	
PRP(N)0/1[2:0] Register	VRCP(N)0/1 Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Amplitude adjustment (1)	
VRP(N)0[3:0] Register	VROP(N)0 Resistance
0000	0R
0001	2R
0010	4R
:	:
:	:
1101	26R
1111	28R
1111	30R

Amplitude adjustment (2)	
VRP(N)1[4:0] Register	VROP(N)1 Resistance
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6).

The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine adjustment registers and selected voltage						
Register	Selected Voltage					
KP(N)[2:0]	VgP(N)1	VgP(N)8	VgP(N)20	VgP(N)43	VgP(N)55	VgP(N)62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Fine adjustment registers and selected resistor						
Register	Selected Resistor					
KP(N)[2:0]	RMP(N)0	RMP(N)1	RMP(N)2	RMP(N)3	RMP(N)4	RMP(N)5
000	0R	0R	0R	0R	0R	0R
001	4R	1R	1R	1R	1R	4R
010	8R	2R	2R	2R	2R	8R
011	12R	3R	3R	3R	3R	12R
100	16R	4R	4R	4R	4R	16R
101	20R	5R	5R	5R	5R	20R
110	24R	6R	6R	6R	6R	24R
111	28R	7R	7R	7R	7R	28R

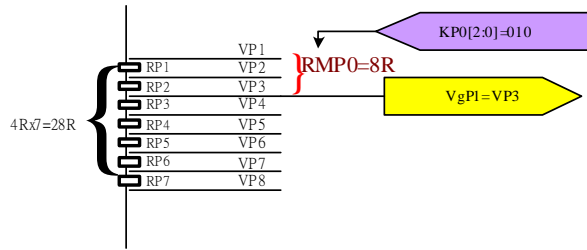


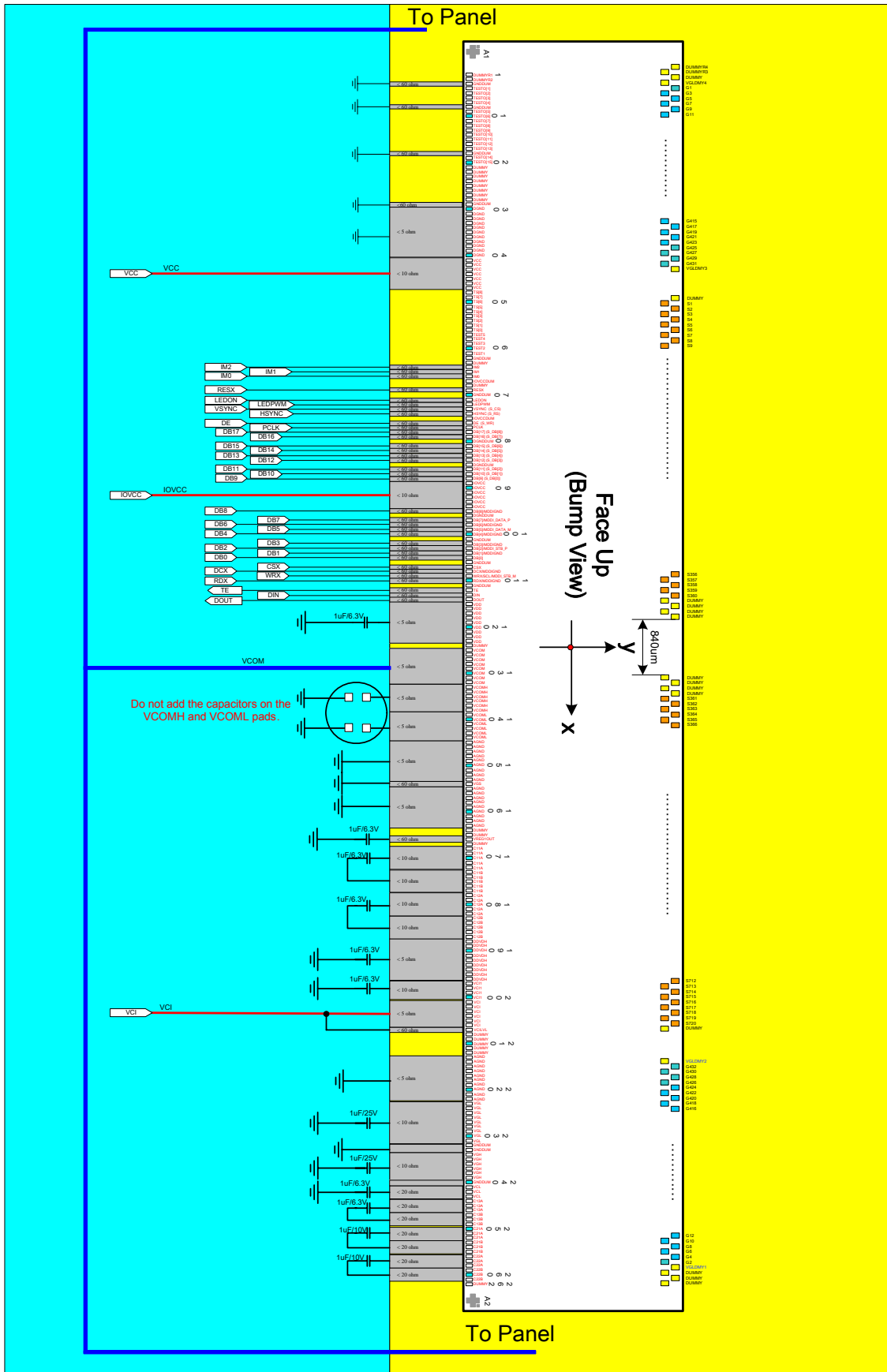
Figure 3 Example of RMP(N)0~5 definition

Code	Positive polarity output voltage		Negative polarity output voltage	
4Fh	VP79	(VgP79)	VN79	(VgN79)
4Eh	VP78	(VP75+(VP79-VP75)*(48/64))	VN78	(VN75+(VN79-VN75)*(48/64))
4Dh	VP77	(VP75+(VP79-VP75)*(32/64))	VN77	(VN75+(VN79-VN75)*(32/64))
4Ch	VP76	(VP75+(VP79-VP75)*(16/64))	VN76	(VN75+(VN79-VN75)*(16/64))
4Bh	VP75	(VgP75)	VN75	(VgN75)
4Ah	VP74	(VP70+(VP75-VP70)*(36/45))	VN74	(VN70+(VN75-VN70)*(36/45))
49h	VP73	(VP70+(VP75-VP70)*(27/45))	VN73	(VN70+(VN75-VN70)*(27/45))
48h	VP72	(VP70+(VP75-VP70)*(18/45))	VN72	(VN70+(VN75-VN70)*(18/45))
47h	VP71	(VP70+(VP75-VP70)*(9/45))	VN71	(VN70+(VN75-VN70)*(9/45))
46h	VP70	(VgP70)	VN70	(VgN70)
45h	VP69	(VP63+(VP70-VP63)*(30/48))	VN69	(VN63+(VN70-VN63)*(30/48))
44h	VP68	(VP63+(VP70-VP63)*(23/48))	VN68	(VN63+(VN70-VN63)*(23/48))
43h	VP67	(VP63+(VP70-VP63)*(16/48))	VN67	(VN63+(VN70-VN63)*(16/48))
42h	VP66	(VP63+(VP70-VP63)*(12/48))	VN66	(VN63+(VN70-VN63)*(12/48))
41h	VP65	(VP63+(VP70-VP63)*(8/48))	VN65	(VN63+(VN70-VN63)*(8/48))
40h	VP64	(VP63+(VP70-VP63)*(4/48))	VN64	(VN63+(VN70-VN63)*(4/48))
3Fh	VP63	(VgP63)	VN63	(VgN63)
3Eh	VP62	(VP51+(VP63-VP51)*(22/24))	VN62	(VN51+(VN63-VN51)*(22/24))
3Dh	VP61	(VP51+(VP63-VP51)*(20/24))	VN61	(VN51+(VN63-VN51)*(20/24))
3Ch	VP60	(VP51+(VP63-VP51)*(18/24))	VN60	(VN51+(VN63-VN51)*(18/24))
3Bh	VP59	(VP51+(VP63-VP51)*(16/24))	VN59	(VN51+(VN63-VN51)*(16/24))
3Ah	VP58	(VP51+(VP63-VP51)*(14/24))	VN58	(VN51+(VN63-VN51)*(14/24))
39h	VP57	(VP51+(VP63-VP51)*(12/24))	VN57	(VN51+(VN63-VN51)*(12/24))
38h	VP56	(VP51+(VP63-VP51)*(10/24))	VN56	(VN51+(VN63-VN51)*(10/24))
37h	VP55	(VP51+(VP63-VP51)*(8/24))	VN55	(VN51+(VN63-VN51)*(8/24))
36h	VP54	(VP51+(VP63-VP51)*(6/24))	VN54	(VN51+(VN63-VN51)*(6/24))
35h	VP53	(VP51+(VP63-VP51)*(4/24))	VN53	(VN51+(VN63-VN51)*(4/24))
34h	VP52	(VP51+(VP63-VP51)*(2/24))	VN52	(VN51+(VN63-VN51)*(2/24))
33h	VP51	(VgP51)	VN51	(VgN51)
32h	VP50	(VP28+(VP51-VP28)*(22/23))	VN50	(VN28+(VN51-VN28)*(22/23))
31h	VP49	(VP28+(VP51-VP28)*(21/23))	VN49	(VN28+(VN51-VN28)*(21/23))
30h	VP48	(VP28+(VP51-VP28)*(20/23))	VN48	(VN28+(VN51-VN28)*(20/23))
2Fh	VP47	(VP28+(VP51-VP28)*(19/23))	VN47	(VN28+(VN51-VN28)*(19/23))
2Eh	VP46	(VP28+(VP51-VP28)*(18/23))	VN46	(VN28+(VN51-VN28)*(18/23))
2Dh	VP45	(VP28+(VP51-VP28)*(17/23))	VN45	(VN28+(VN51-VN28)*(17/23))
2Ch	VP44	(VP28+(VP51-VP28)*(16/23))	VN44	(VN28+(VN51-VN28)*(16/23))
2Bh	VP43	(VP28+(VP51-VP28)*(15/23))	VN43	(VN28+(VN51-VN28)*(15/23))
2Ah	VP42	(VP28+(VP51-VP28)*(14/23))	VN42	(VN28+(VN51-VN28)*(14/23))
29h	VP41	(VP28+(VP51-VP28)*(13/23))	VN41	(VN28+(VN51-VN28)*(13/23))
28h	VP40	(VP28+(VP51-VP28)*(12/23))	VN40	(VN28+(VN51-VN28)*(12/23))
27h	VP39	(VP28+(VP51-VP28)*(11/23))	VN39	(VN28+(VN51-VN28)*(11/23))
26h	VP38	(VP28+(VP51-VP28)*(10/23))	VN38	(VN28+(VN51-VN28)*(10/23))
25h	VP37	(VP28+(VP51-VP28)*(9/23))	VN37	(VN28+(VN51-VN28)*(9/23))

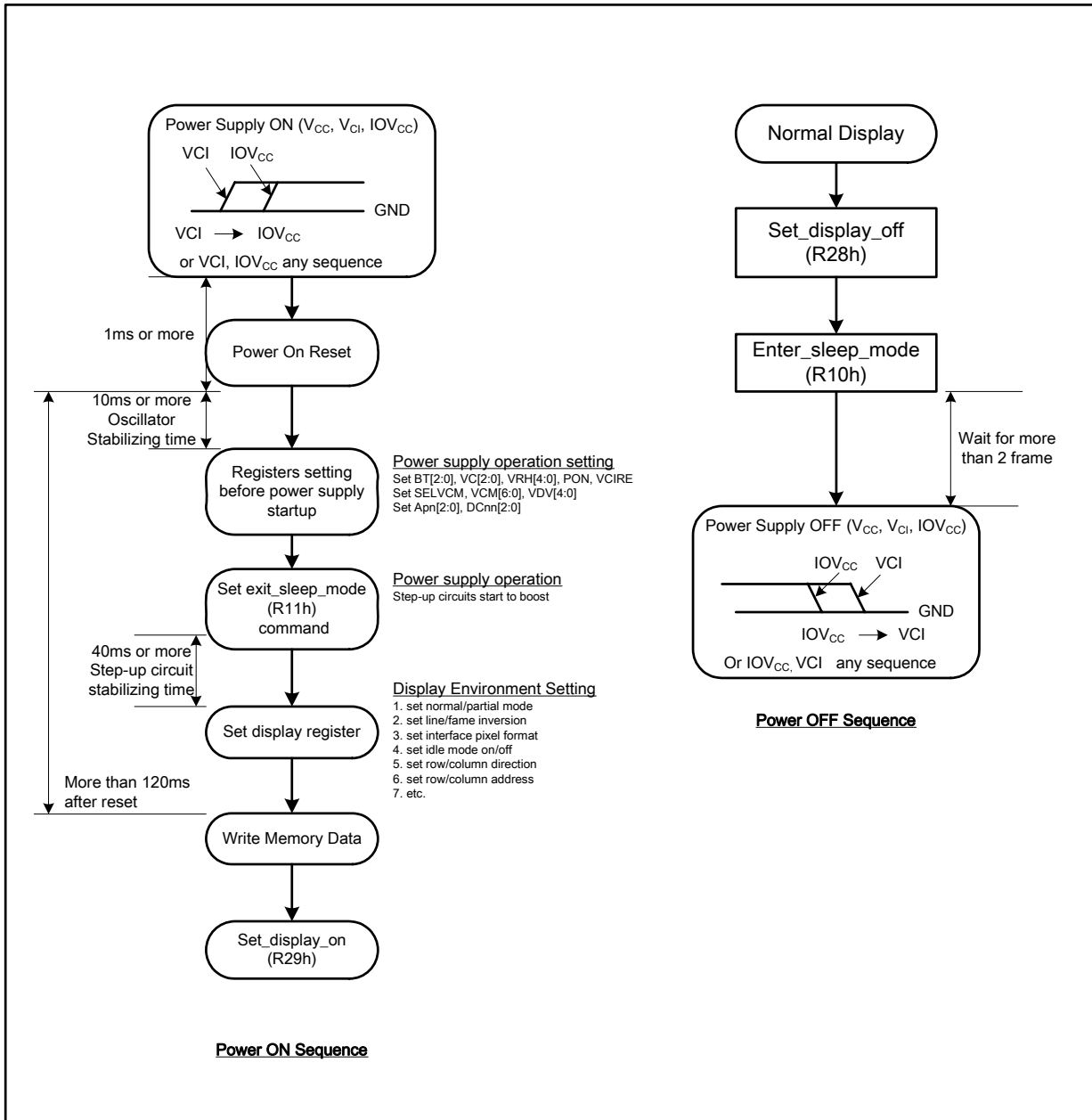
24h	VP36	(VP28+(VP51-VP28)*(8/23))	VN36	(VN28+(VN51-VN28)*(8/23))
23h	VP35	(VP28+(VP51-VP28)*(7/23))	VN35	(VN28+(VN51-VN28)*(7/23))
22h	VP34	(VP28+(VP51-VP28)*(6/23))	VN34	(VN28+(VN51-VN28)*(6/23))
21h	VP33	(VP28+(VP51-VP28)*(5/23))	VN33	(VN28+(VN51-VN28)*(5/23))
20h	VP32	(VP28+(VP51-VP28)*(4/23))	VN32	(VN28+(VN51-VN28)*(4/23))
1Fh	VP31	(VP28+(VP51-VP28)*(3/23))	VN31	(VN28+(VN51-VN28)*(3/23))
1Eh	VP30	(VP28+(VP51-VP28)*(2/23))	VN30	(VN28+(VN51-VN28)*(2/23))
1Dh	VP29	(VP28+(VP51-VP28)*(1/23))	VN29	(VN28+(VN51-VN28)*(1/23))
1Ch	VP28	(VgP28)	VN28	(VgN28)
1Bh	VP27	(VP16+(VP28-VP16)*(22/24))	VN27	(VN16+(VN28-VN16)*(22/24))
1Ah	VP26	(VP16+(VP28-VP16)*(20/24))	VN26	(VN16+(VN28-VN16)*(20/24))
19h	VP25	(VP16+(VP28-VP16)*(18/24))	VN25	(VN16+(VN28-VN16)*(18/24))
18h	VP24	(VP16+(VP28-VP16)*(16/24))	VN24	(VN16+(VN28-VN16)*(16/24))
17h	VP23	(VP16+(VP28-VP16)*(14/24))	VN23	(VN16+(VN28-VN16)*(14/24))
16h	VP22	(VP16+(VP28-VP16)*(12/24))	VN22	(VN16+(VN28-VN16)*(12/24))
15h	VP21	(VP16+(VP28-VP16)*(10/24))	VN21	(VN16+(VN28-VN16)*(10/24))
14h	VP20	(VP16+(VP28-VP16)*(8/24))	VN20	(VN16+(VN28-VN16)*(8/24))
13h	VP19	(VP16+(VP28-VP16)*(6/24))	VN19	(VN16+(VN28-VN16)*(6/24))
12h	VP18	(VP16+(VP28-VP16)*(4/24))	VN18	(VN16+(VN28-VN16)*(4/24))
11h	VP17	(VP16+(VP28-VP16)*(2/24))	VN17	(VN16+(VN28-VN16)*(2/24))
10h	VP16	(VgP16)	VN16	(VgN16)
0Fh	VP15	(VP9+(VP16-VP9)*(44/48))	VN15	(VN9+(VN16-VN9)*(44/48))
0Eh	VP14	(VP9+(VP16-VP9)*(40/48))	VN14	(VN9+(VN16-VN9)*(40/48))
0Dh	VP13	(VP9+(VP16-VP9)*(36/48))	VN13	(VN9+(VN16-VN9)*(36/48))
0Ch	VP12	(VP9+(VP16-VP9)*(32/48))	VN12	(VN9+(VN16-VN9)*(32/48))
0Bh	VP11	(VP9+(VP16-VP9)*(25/48))	VN11	(VN9+(VN16-VN9)*(25/48))
0Ah	VP10	(VP9+(VP16-VP9)*(18/48))	VN10	(VN9+(VN16-VN9)*(18/48))
09h	VP9	(VgP9)	VN9	(VgN9)
08h	VP8	(VP4+(VP9-VP4)*(36/45))	VN8	(VN4+(VN9-VN4)*(36/45))
07h	VP7	(VP4+(VP9-VP4)*(27/45))	VN7	(VN4+(VN9-VN4)*(27/45))
06h	VP6	(VP4+(VP9-VP4)*(18/45))	VN6	(VN4+(VN9-VN4)*(18/45))
05h	VP5	(VP4+(VP9-VP4)*(9/45))	VN5	(VN4+(VN9-VN4)*(9/45))
04h	VP4	(VgP4)	VN4	(VgN4)
03h	VP3	(VP0+(VP4-VP0)*(48/64))	VN3	(VN0+(VN4-VN0)*(48/64))
02h	VP2	(VP0+(VP4-VP0)*(32/64))	VN2	(VN0+(VN4-VN0)*(32/64))
01h	VP1	(VP0+(VP4-VP0)*(16/64))	VN1	(VN0+(VN4-VN0)*(16/64))
00h	VP0	(VgP0)	VN0	(VgN0)

14. Application

14.1. Application Circuit



14.2. Power Supply Configuration



15. Electrical Characteristics

15.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9327 is used out of the absolute maximum ratings, ILI9327 may be permanently damaged. To use the ILI9327 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9327 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage	IOVCC	V	-0.3 ~ + 4.6	1,2
Power supply voltage	VCI - GND	V	-0.3 ~ + 4.6	1,3
Power supply voltage	DDVDH - GND	V	-0.3 ~ + 6.0	1,4
Power supply voltage	GND -VCL	V	-0.3 ~ + 4.6	1
Power supply voltage	DDVDH - VCL	V	-0.3 ~ + 9.0	1,5
Power supply voltage	VGH - GND	V	-0.3 ~ + 18	1,6
Power supply voltage	GND - VGL	V	-0.3 ~ + 18	1,7
Power supply voltage	VGH - VGL	V	0.3 ~ + 30	
Input voltage	Vt	V	-0.3 ~ IOVCC+ 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	8, 9
Storage temperature	Tstg	°C	-55 ~ + 110	8, 9

Notes:

1. GND must be maintained
2. (High) (VCC = VCC) ≥ GND (Low), (High) IOVCC ≥ GND (Low).
3. Make sure (High) VCI ≥ GND (Low).
4. Make sure (High) DDVDH ≥ GND (Low).
5. Make sure (High) DDVDH ≥ VCL (Low).
6. Make sure (High) VGH ≥ GND (Low).
7. Make sure (High) GND ≥ VGL (Low).
8. For die and wafer products, specified up to 85°C.
9. This temperature specifications apply to the TCP package

15.2. DC Characteristics

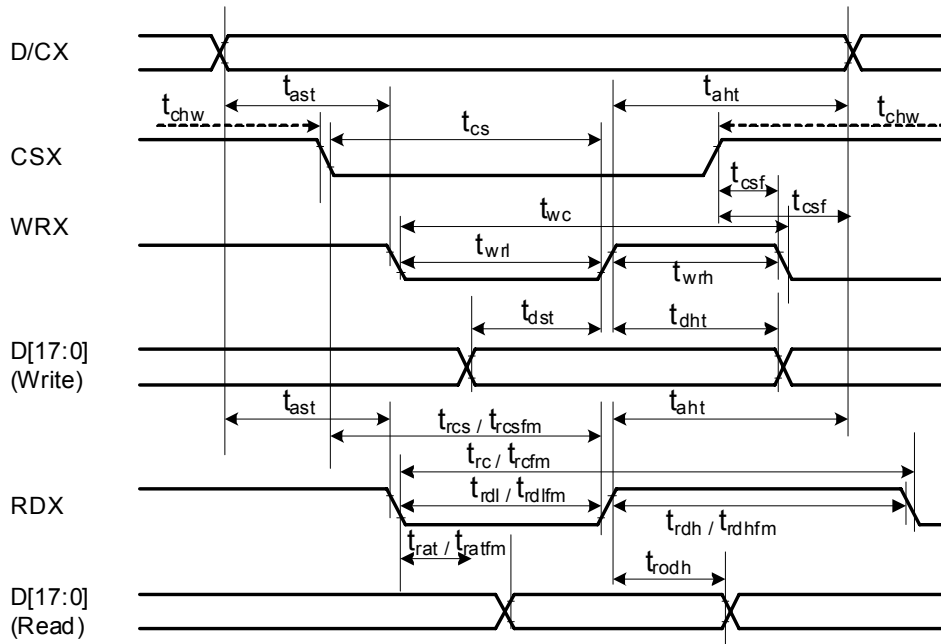
(VCC=VCI=2.50 ~ 3.3V, IOVCC = 1.65 ~ 3.3V, Ta= -40 ~ 85 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog Power Supply Voltage	VCI	Analog Operation Voltage	2.5	2.8	3.6	V
I/O pin Power Supply Voltage	IOVCC	I/O pin Operation Voltage	1.65	2.8	3.6	V
Input high voltage	V _{IH}	IOVCC = 1.65V ~ 3.3V	0.7*IOVCC	-	IOVCC	V
Input low voltage	V _{IL}	IOVCC = 1.65V ~ 3.3V	0.0	-	0.3*IOVCC	V
Output high voltage	V _{OH}	I _{out} = -0.1 mA	0.8*IOVCC	-	IOVCC	V
Output low voltage	V _{OL}	I _{out} = +0.1 mA	0.0	-	0.2*IOVCC	V
I/O leakage current	I _{LI}	V _{in} =0 ~ IOVCC	-0.1		0.1	uA
Current consumption during normal operation (VCC, VCI, IOVCC)	I _{OP}	VCC=VCI=IOVCC=2.8V, Ta=25°C, GRAM data=0000h, Frame rate=60Hz, line inversion	-	TBD	-	mA
Current consumption during standby operation (VCC, VCI, IOVCC)	I _{ST}	VCC=VCI=IOVCC=2.8V, Ta=25°C, CPU interface	-	50	TBD	uA
LCD Drive Power Supply Current (DDVDH-GND)	I _{LCD}	VCC=VCI=IOVCC=2.8V, Ta=25°C, GRAM data=0000h, Frame rate=60Hz, line inversion		7.0	-	mA
LCD Drive voltage	DDVDH		4.5		6	Volt
Output deviation voltage	I _{DEV}				20	mV
Output offset voltage	I _{OFFSET}	Note1			35	mV

Note 1: The Max. value is between with measure point and gamma setting value.

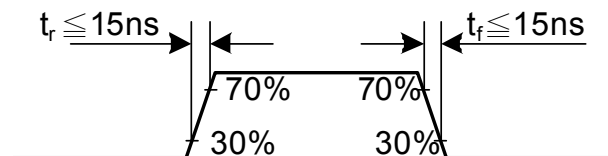
15.3. AC Characteristics

15.3.1. DBI Type B (18/16/9/8 bit) Interface Timing Characteristics

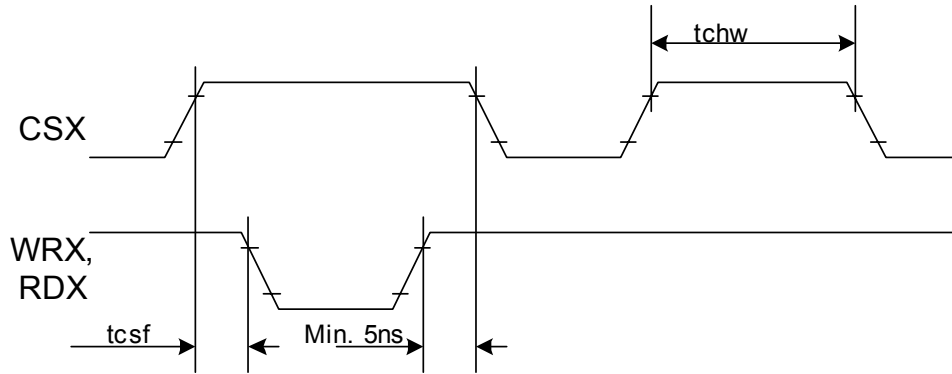


Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" Pulse Width	0	-	ns	
	tcs	Chip Select setup time (Write)	20	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	80	-	ns	
	twrh	Write Control pulse H duration	25	-	ns	
	twrl	Write Control pulse L duration	25	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration (ID)	90	-	ns	
	trdl	Read Control pulse L duration (ID)	45	-	ns	
RDX (FM)	trcfm	Read cycle (FM)	450	-	ns	
	trdhfm	Read Control pulse H duration (FM)	90	-	ns	
	trdlfm	Read Control pulse L duration (FM)	355	-	ns	
DB[17:0], DB[15:0], DB[8:0], DB[7:0]	tdst	Data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Data hold time	10	-	ns	
	trat	Read access time (ID)	-	40	ns	
	tratfm	Read access time (FM)	-	340	ns	
	todh	Output disable time	20	-	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, DGND=0V

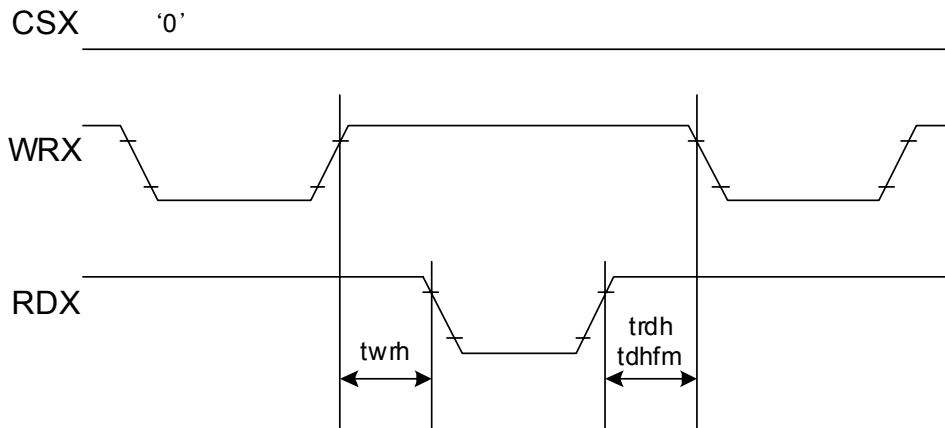


CSX timings:



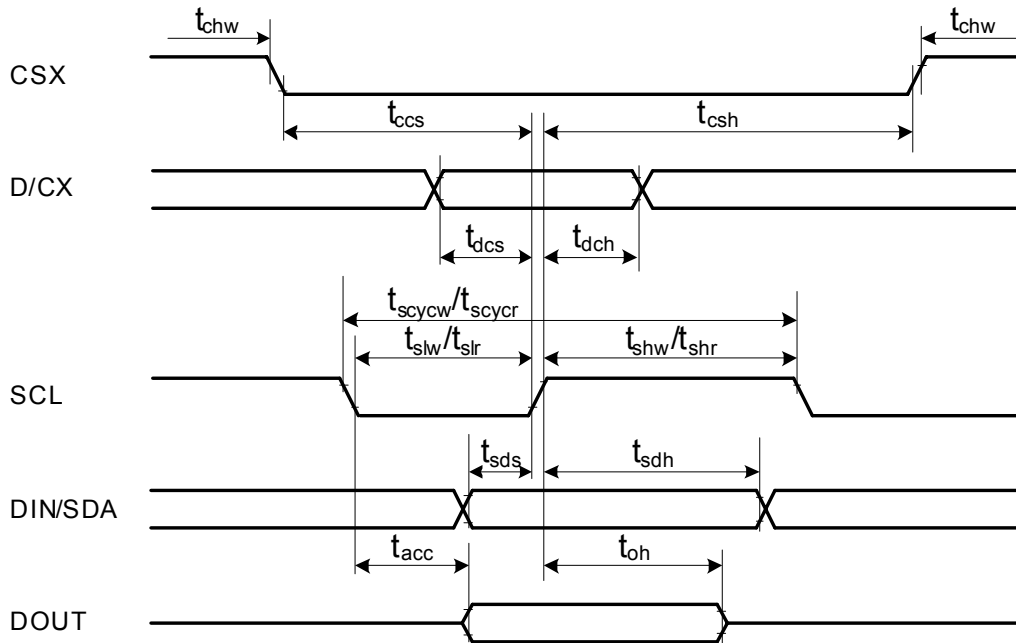
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



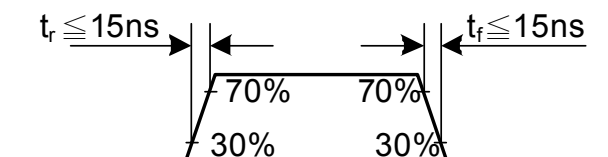
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

15.3.2. DBI Type C (SPI) Interface Timing Characteristics

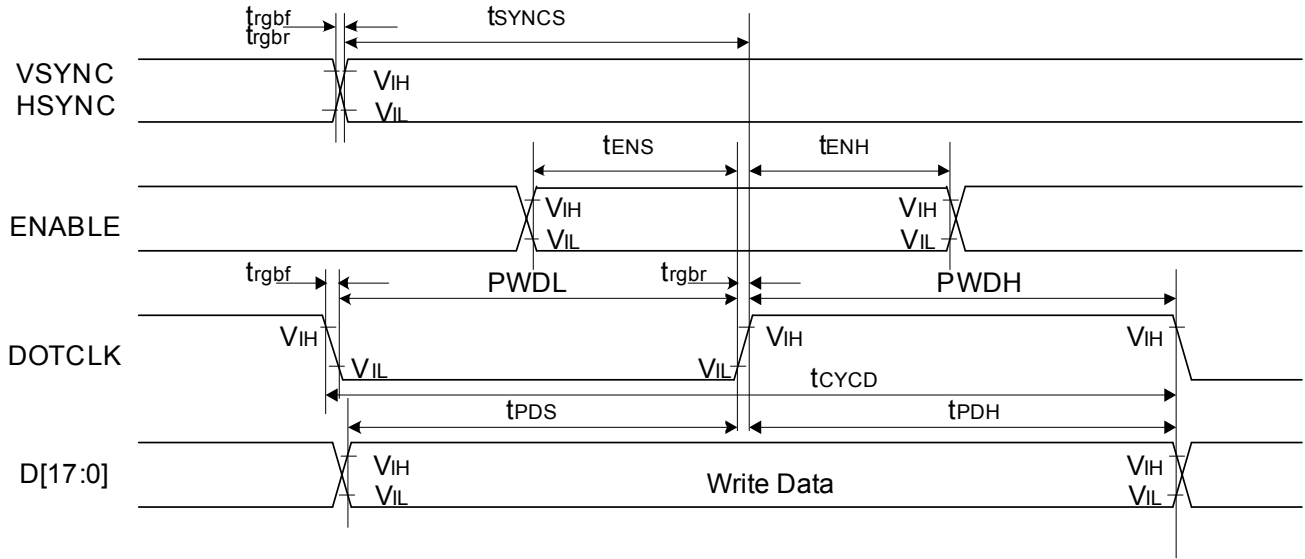


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{ccs}	CSX-SCL time (Write)	15	-	ns	
	t_{csh}	CSX-SCL time (Write)	15	-	ns	
	t_{ccs}	CSX-SCL time (Read)	60	-	ns	
	t_{csh}	CSX-SCL time (Read)	60	-	ns	
	t_{chw}	CSX "H" pulse time	40	-	ns	
SCL	t_{scycw}	Serial clock cycle (Write)	60	-	ns	
	t_{shw}	SCL "H" pulse width (Write)	15	-	ns	
	t_{slw}	SCL "L" pulse width (Write)	15	-	ns	
	t_{scycr}	Serial clock cycle (Read GRAM)	300	-	ns	
	t_{shr}	SCL "H" pulse width (Read GRAM)	110	-	ns	
	t_{slr}	SCL "L" pulse width (Read GRAM)	110	-	ns	
	t_{scycr}	Serial clock cycle (Read ID)	150	-	ns	
	t_{shr}	SCL "H" pulse width (Read GRAM)	54	-	ns	
D/CX	t_{dcs}	D/CX setup time	7	-	ns	
	t_{dch}	D/CX hold time	7	-	ns	
SDA (Input) (Output)	t_{acc}	Access time	10	50	ns	For maximum CL=30pF
	t_{oh}	Output disable time	15	50	ns	For minimum CL=8pF
	t_{sds}	Data setup time	7	-	ns	
	t_{sdh}	Data hold time	7	-	ns	

Note: $T_a = -30$ to 70 °C, $V_{DDI}=1.65V$ to $3.3V$, $V_{DD}=2.5V$ to $3.0V$, $AGND=DGND=0V$

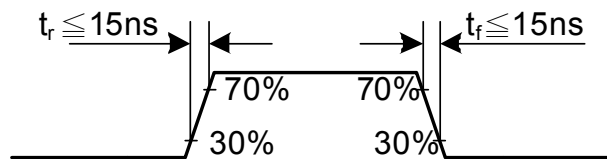


15.3.3. DPI Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{POH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr}, t_{rgb}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{POH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr}, t_{rgb}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: $T_a = -30$ to 70 °C, $V_{DDI}=1.65V$ to $3.3V$, $V_{DD}=2.5V$ to $3.0V$, $AGND=DGND=0V$



16. Revision History

Version No.	Date	Page	Description
0.00	2008/11/24		New Create
0.01	2009/03/03	13~18	Modify pad coordinates
	2009/03/09	12, 18	Modify alignment mark coordinate y=-251→-217
		13	Pad 166 modification: VREG→VREG1OUT
	2009/03/09	120~122	Add DSTB description
		44~45	Add MDDI description and move DSTB description to page 120~122
0.02	2009/03/13	36	Add MDDI max transmit rate 130Mbps
0.03	2009/03/23	149, 181	Modify the gamma register RC8h and gamma adjustment.
		7~9	Modify the pin description for the shared pins for sub-panel control
		186, 187	Add the application circuit and power on/off sequence.
		120	Modify the EPF definition.
0.04	2009/05/06	183	Remove the capacitors of VCOMH and VCOML.
0.05	2009/06/12	34	Modify the DPI (RGB) interface data bus arrangement.
		141	Modify the calculation formula of frame rate.
		163	Add GON/DTE/NW[5:0] description in register EAh.
		131	Update PWM output frequency
0.06	2009/06/15	117	Modify wait time after reset (31ms→ 100 msec)