EK79001

Rev. 1.1

DATA SHEET

1536-Output TFT LCD Source Driver with TCON

fitipower integrated technology Inc.

Table of Contents

Single Chip 1536 Channel Source Driver with Timing Controller for 1024RGB × 600 TFT LCD

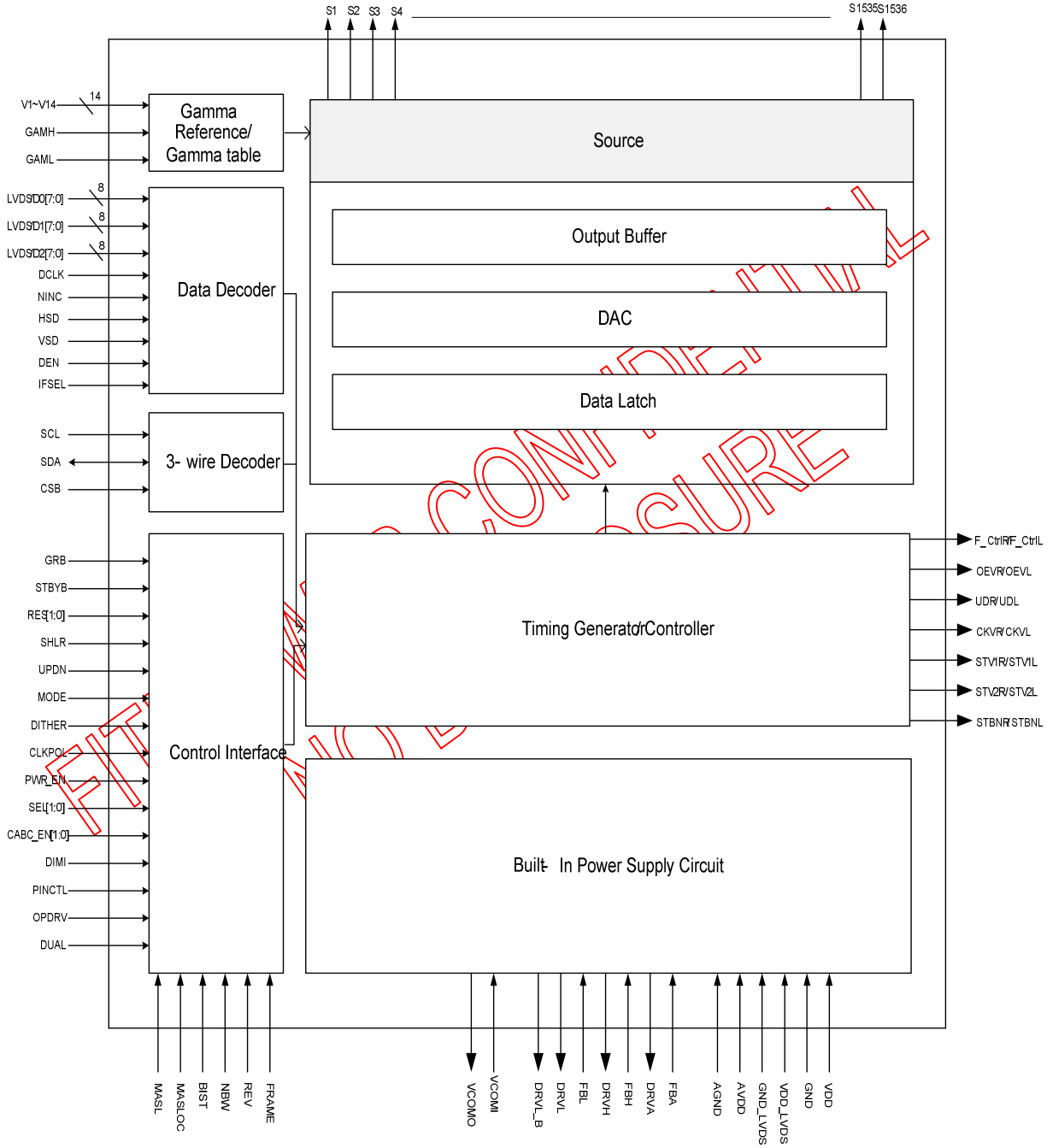
1. GENERAL DESCRIPTION

The EK79001 is a highly integrated solution for small size to middle size a-Si TFT-LCD panels. This chip integrates 1536ch dual gate mode source driver with LVDS and parallel RGB input interface.

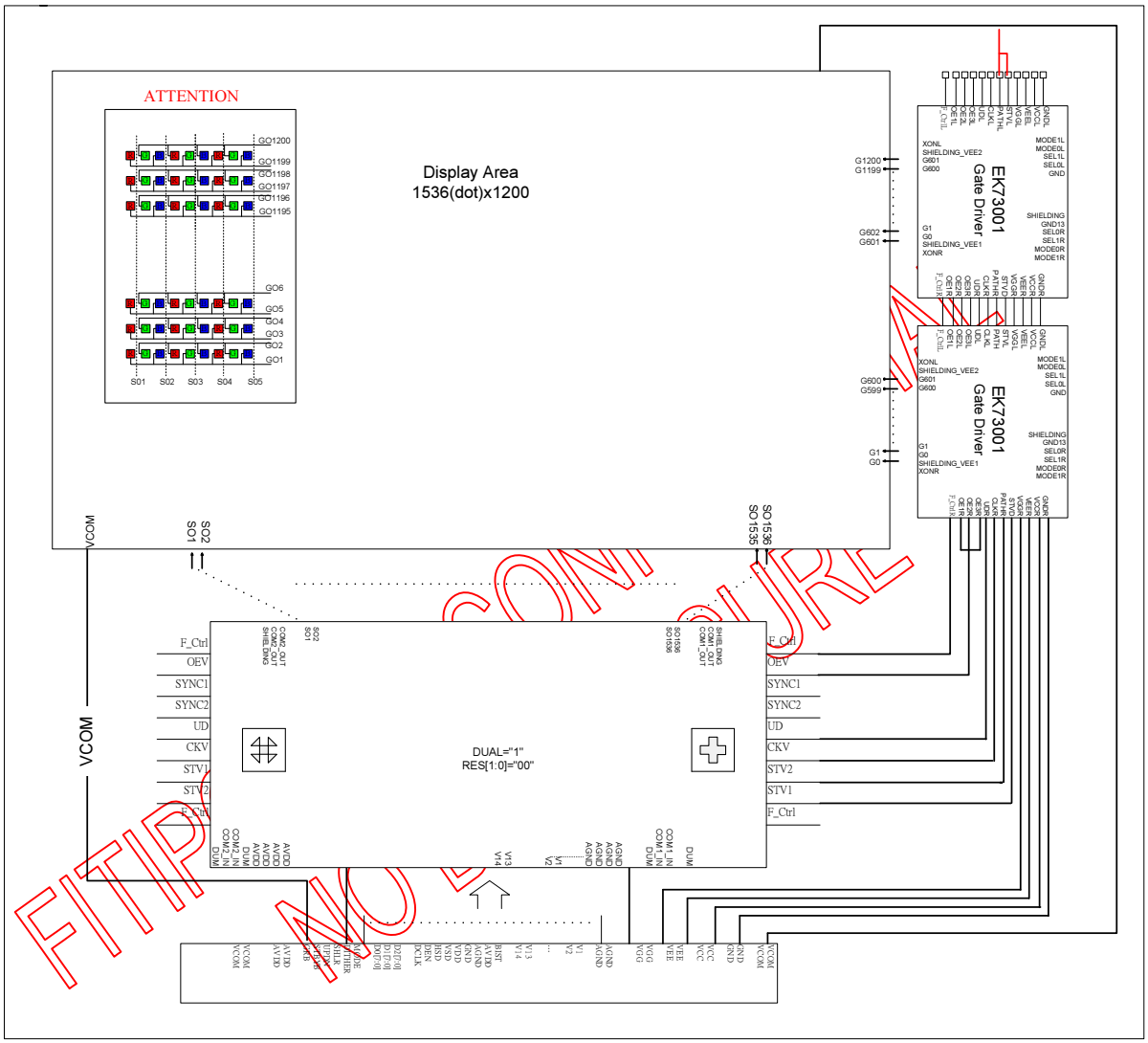
2. FEATURES

- Special design for 1024RGBx600 TFT LCD Panel with LVDS/TTL interface
- Integrate 1536 channel source driver with single or dual gate function
- Support cascade function with bidirectional shift control (CMOS signal)
- Support panel resolution (HxV) : 1024(RGB) x 768 , 1024(RGB) x 600 , 800(RGB) x 600 , 800(RGB) x 480
- 8-bit resolution 256 gray-scale with Dithering (6 bits DAC + 2 bit FRC or HFRC)
- Support Pin Control function for Up/Down, Left/Right ... control
- Power for digital circuit(VDD): 2.3V ~ 3.6V
- Power for analog circuit(AVDD): 8V ~ 13.5V
- Operating frequency : 71 MHz (Max.)
- Embedded Gamma Table for special custom request
- V1~V14 for adjusting Gamma correction
- 1 + 2 dot inversion architecture
- Built-In PWM controller for AVDD, Charge pump for VGH / VGL, and VCOM buffer
- Built-In CABC function
- Built-In AUTO pattern
- Built-In SDRRS function
- Support no clock detection
- COG package
- Chip size = 25000um x 700um
- Output bump pitch = 15um

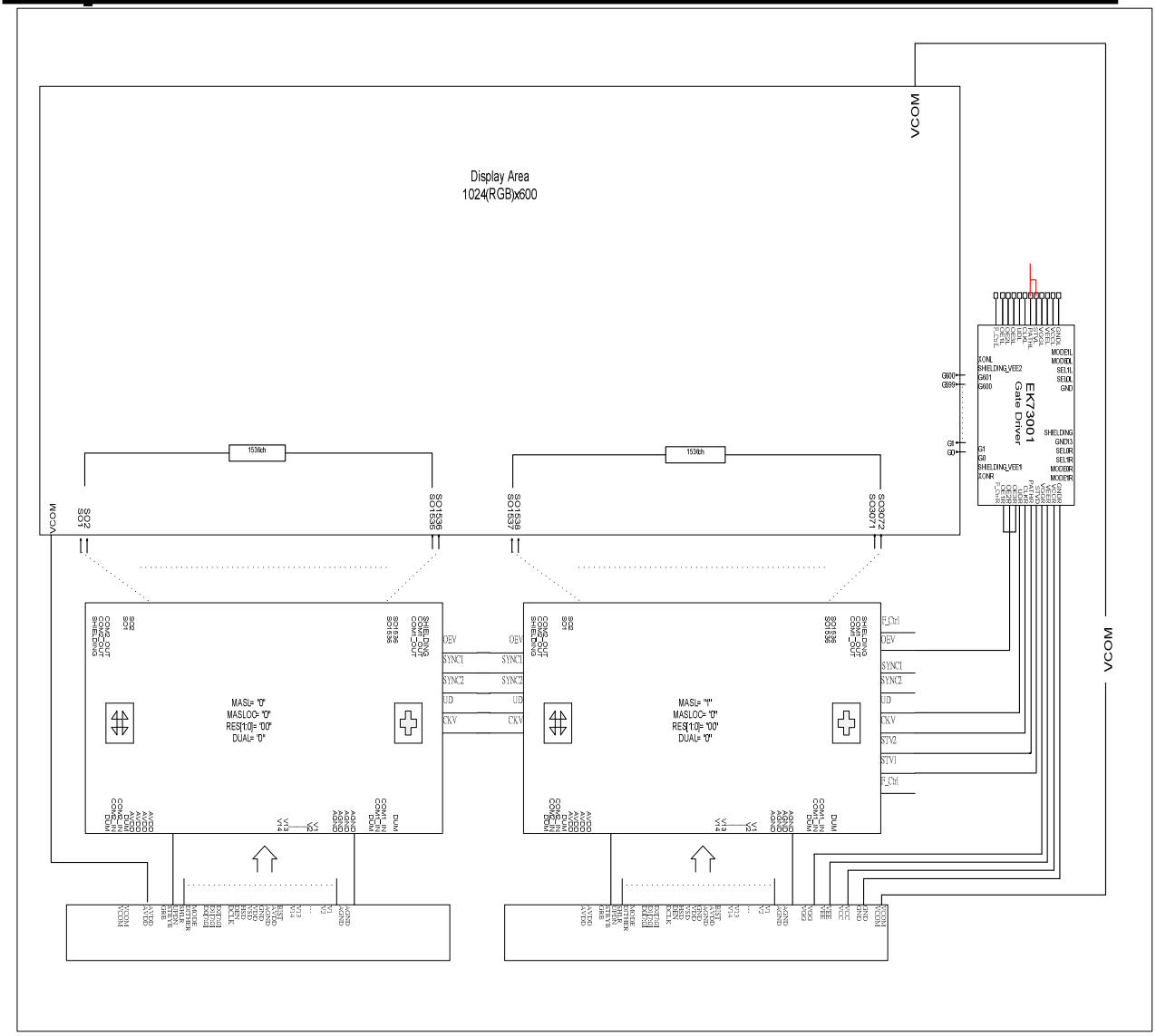
3. BLOCK DIAGRAM



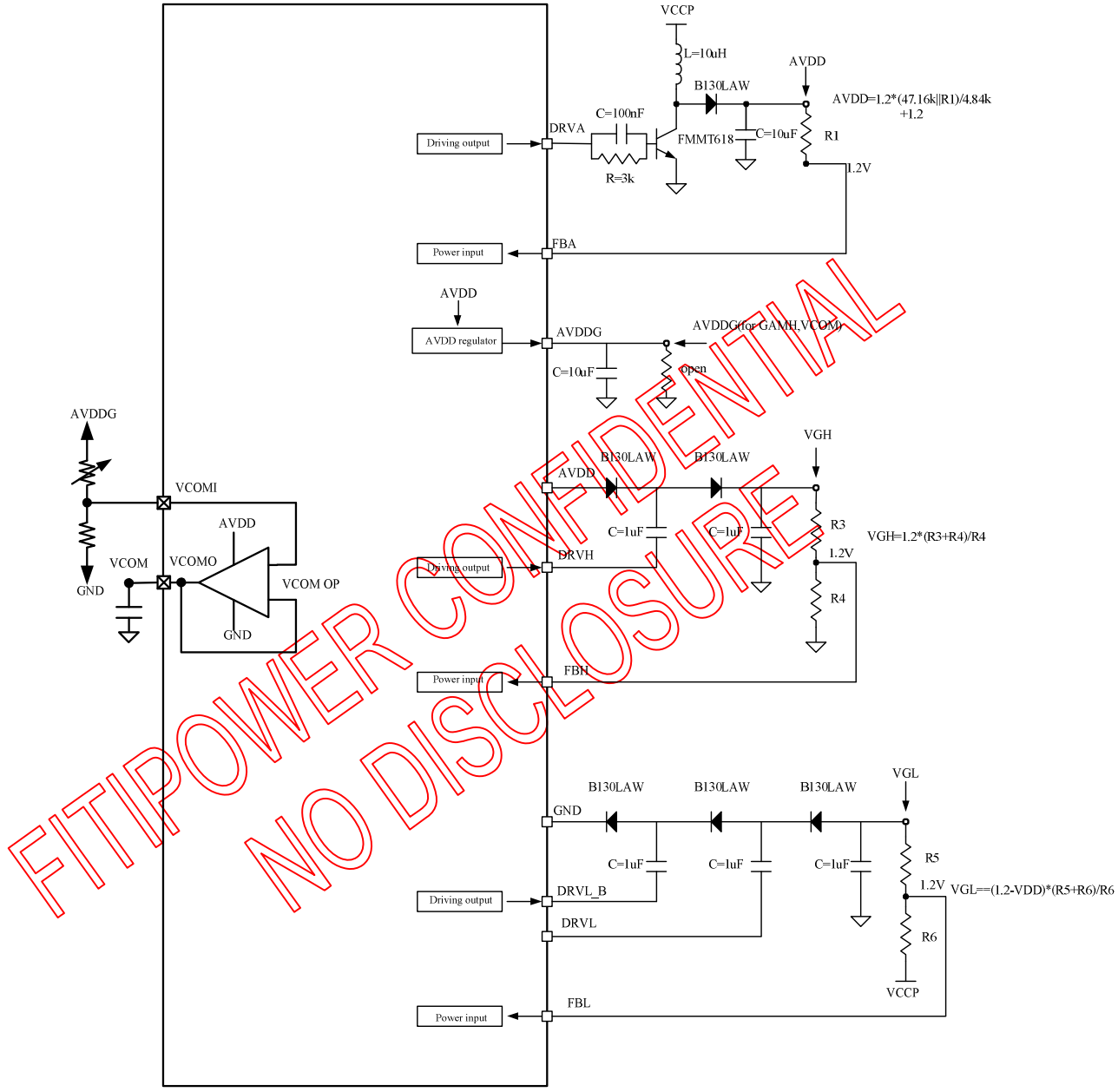
Block Diagram



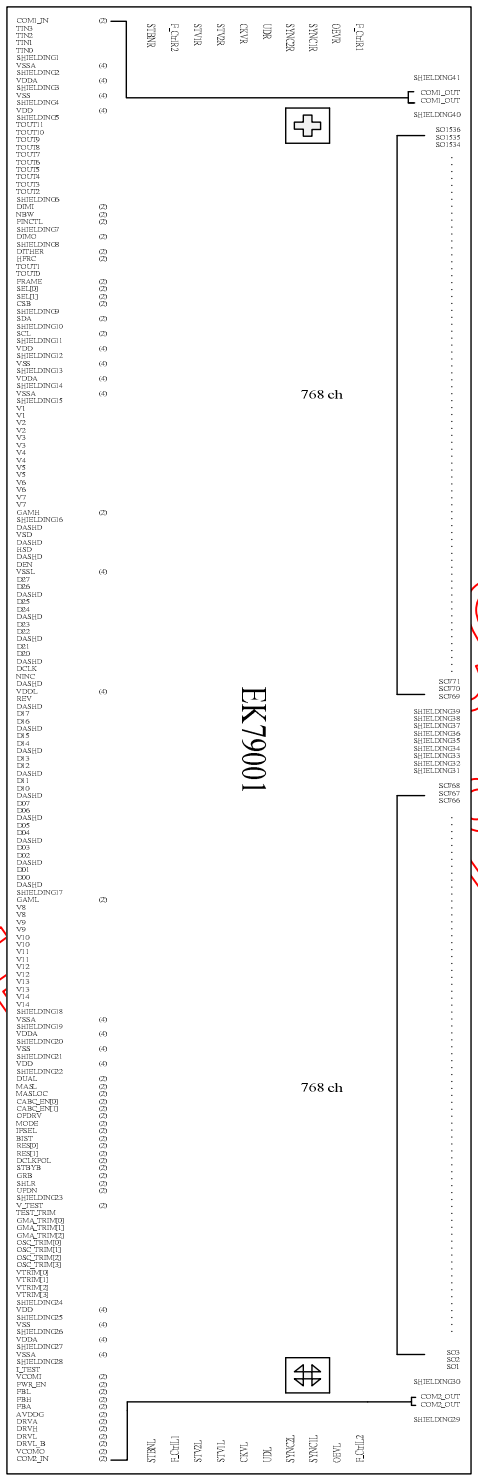
Application Block Diagram-Dual Gate Application



Application Block Diagram-Cascade Application



Application Power Circuit



Pad Sequence(Bump Side)

4. PIN DESCRIPTION

Pin Description

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>D07~D00
D17~D10
D27~D20</td><td>Input</td><td>LVDS or Parallel RGB data Input. Select by “IFSEL” pin.
<table>
<tr><th>Pin name</th><th>TTL input mode
IFSEL=”L”</th><th>LVDS input mode
IFSEL=”H”</th></tr>
<tr><td>D2[0],D2[1]</td><td>B[0],B[1]</td><td>NIND0,PIND0</td></tr>
<tr><td>D2[2],D2[3]</td><td>B[2],B[3]</td><td>NIND1,PIND1</td></tr>
<tr><td>D2[4],D2[5]</td><td>B[4],B[5]</td><td>NIND2,PIND2</td></tr>
<tr><td>D2[6],D2[7]</td><td>B[6],B[7]</td><td>NIND3,PIND3</td></tr>
</table>
LVDS 6 bit data input : PIND[2:0], NIND[2:0].
D[07:00] = R[7:0] data; D[17:10] = G[7:0] data; D[27:20] = B[7:0] data.
For 18bit RGB interface, connect two LSB bits of all the R/G/B data buses to GND.
Note : D07~D00 -> SO1 , SO4 … SO1531 , SO1534
D17~D10 -> SO2 , SO5 … SO1532 , SO1535
D27~D20 -> SO3 , SO6 … SO1533 , SO1536
Please note the relation between RGB data and Color Filter sequence
Note: For LVDS interface, it’s necessary to put on external terminal resistor(on FPC or PCB board) between NIND0/PIND0, NIND1/PIND1, NIND2/PIND2, NIND3/PIND3, NINC/PINC.</td></tr>
<tr><td>DCLK</td><td>Input</td><td>Clock Input pin for LVDS or TTL mode. Select by “IFSEL” pin
<table>
<tr><th>Pin name</th><th>TTL input mode
IFSEL=”L”</th><th>LVDS input mode
IFSEL=”H”</th></tr>
<tr><td>DCLK</td><td>DCLK</td><td>PINC</td></tr>
</table>
Note: For LVDS interface, it’s necessary to put on external terminal resistor(on FPC or PCB board) between NIND0/PIND0, NIND1/PIND1, NIND2/PIND2, NIND3/PIND3, NINC/PINC.</td></tr>
<tr><td>NINC</td><td>Input</td><td>Negative LVDS differential clock input.
Note: For LVDS interface, it’s necessary to put on external terminal resistor(on FPC or PCB board) between NIND0/PIND0, NIND1/PIND1, NIND2/PIND2, NIND3/PIND3, NINC/PINC.</td></tr>
<tr><td>HSD</td><td>Input</td><td>Horizontal Sync input for TTL mode. Negative polarity.
(In LVDS interface connected HSD to FPC for pin setting
HSD=”L”:8 bit
HSD=”H”:6 bit)</td></tr>
<tr><td>VSD</td><td>Input</td><td>Vertical Sync input for TTL mode. Negative polarity.
(In LVDS Interface , connected to FPC and pull low)</td></tr>
<tr><td>DEN</td><td>Input</td><td>Data Input Enable. Active High to enable the data input bus under “DE Mode”. Normally pull low.</td></tr>
<tr><td>MODE</td><td>Input</td><td>DE / SYNC mode select under TTL mode. Normally pull high
H : DE mode.
L : HSD/VSD mode.</td></tr>
<tr><td>IFSEL</td><td>Input</td><td>IFSEL = L : TTL interface
IFSEL = H : LVDS interface</td></tr>
</table>

Pin Name	Pin Type	Description
RES[1:0]	Input	RES[1:0]="01",for 1024(RGB)*768 display resolution(dual or cascade) RES[1:0]="00",for1024(RGB)*600 display resolution(dual or cascade (Default) RES[1:0]="10",for 800(RGB)*600 display resolution(dual or cascade) (601~936 channel disable) RES[1:0]="11", for 800(RGB)*480 display resolution(dual or cascade) (601~936 channel disable)
DITHER	Input	Dithering function enable control. Normally pull low In LVDS 6-bit mode, IC don't care DITHER and HFRC setting. DITHER = "1", Enable internal dithering function DITHER = "0", Disable internal dithering function. If in LVDS 8-bit or TTL mode, IC will bypass D01/D00,D11/D10,D21/D20.
HFRC	Input	H-FRC selection. Normally pull low HFRC = H : H-FRC enable If "DITHER"="L",disable dithering function(HFRC and FRC disable)
DCLKPOL	Input	Input clock edge selection. Normally pull low CLKPOL = "1", Latch data at DCLK rising edge. CLKPOL = "0", Latch data at DCLK falling edge. (Default)
DUAL	Input	Dual Gate function enables control. Normally pull high DUAL = "1", Enable Dual Gate Function. (Default) DUAL = "0", Disable Dual Gate Function Note: Cascade function will be disabled under "dual gate" mode!!
V1~V14	Input	When INTERNAL Gamma Table is used. GAMH tied to AVDDG , GAML tied to GND and V1~V14 pad are un-used. When using external gamma voltage, GAMH and GAML are floating , and V1~V14 are the external gamma correction points. The voltage of these pins must be: AGND<V14<V13<V12<V11<V10<V9<V8;V7<V6<V5<V4<V3<V2<V1< AVDD .
GAMH	Input	When using INTERNAL Gamma Table , tied to AVDDG . Otherwise floating.
GAML	Input	When using INTERNAL Gamma Table , tied to GND . Otherwise floating.
GRB	Input	Global reset pin. Active Low to enter Reset State. Normally pull high. **It's necessary to connecting with an RC delay circuit for stability. (GRB delay VDD larger than 1ms)**
STBYB	Input	Standby mode, Normally pulled high. STBYB = "1",normal operation STBYB = "0", timing controller, source driver will turn off, all output are High-Z
MASL	Input	Master and Slave Mode selection. Normally pull high. MASL = "H", for Master mode. (Default Mode) MASL = "L", for Slave mode. Only the Master chip will issue the Gate and Cascade control signal.
MASLOC	Input	Master location definition pin. Normally pull low. MASLOC = "L", Master locate on right side (Panel top view). (Default Mode) MASLOC = "H", Master locate on left side (Panel top view).

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>SHLR</td><td>Input</td><td>Source Right or Left sequence control. Normally pull high.
SHLR = “L”, shift left: last data = S1←S2←S3.....←S1536 = first data.
SHLR = ‘H’ , shift right: first data = S1→S2→S3.....→S1536 = last data.</td></tr>
<tr><td>UPDN</td><td>Input</td><td>Gate Up or Down scan control. Normally pull low.
UPDN = “L”, STV2 output vertical start pulse and UD pin output logical “0” to Gate driver.
UPDN = “H”, STV1 output vertical start pulse and UD pin output logical “1” to Gate driver.</td></tr>
<tr><td>BIST</td><td>Input</td><td>Normal Operation/BIST pattern select. Normally pull low
BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation</td></tr>
<tr><td>NBW</td><td>Input</td><td>Normally black or normally white setting. Normally pulled low. NBW = H : Normally black
NBW = L : Normally white</td></tr>
<tr><td>REV</td><td>Input</td><td>Controls whether the data of D00~D27 are inverted or not, normally pulled low.
When “REV”=1 these data will be inverted. EX. “00”→“ 3F”, “07”→“ 38”, “15”→“2A”, and so on.</td></tr>
<tr><td>FRAME</td><td>Input</td><td>Frame inverse or not select. Normally pull low.
FRAME = “1”, Uniform
FRAME = “0”, Frame inverse (Default)</td></tr>
<tr><td>SEL[1:0]</td><td>Input</td><td>Gate on sequence select. Normally pull low
<table>
<tr><th>SEL[0]</th><th>SEL[1]</th><th>Pin control function</th></tr>
<tr><td>1</td><td>1</td><td>Z+ƨ</td></tr>
<tr><td>1</td><td>0</td><td>ƨ</td></tr>
<tr><td>0</td><td>1</td><td>ƧZ</td></tr>
<tr><td>0</td><td>0</td><td>Z(default)</td></tr>
</table></td></tr>
<tr><td>OEVR/OEVL</td><td>Output</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>SYNC1R/SYNC1L</td><td>Output</td><td>CABC and BIST sync control</td></tr>
<tr><td>SYNC2R/SYNC2L</td><td>Output</td><td>CABC and BIST sync control</td></tr>
<tr><td>UDR/UDL</td><td>Output</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>CKVR/CKVL</td><td>Output</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>STV1R/STV1L</td><td>Output</td><td>Gate driver control signal</td></tr>
<tr><td>STV2R/STV2L</td><td>Output</td><td>Gate driver control signal</td></tr>
<tr><td>STBNR/STBNL</td><td>Output</td><td>Gate driver control signal</td></tr>
<tr><td>F_CtrlR/F_CtrlL</td><td>Output</td><td>Gate driver control signal (For special Gate on sequence).
NOTE : In Cascade structure, let this pin floating.
In Dual Gate structure , connect this pin to gate driver’s F_Ctrl . And setting gate driver’s SEL[1:0] to “00”.</td></tr>
<tr><td>CABC_EN[1:0]</td><td>Input</td><td>CABC H/W enable pin. Normally pull low.
When CABC_EN=”00”, CABC OFF. (Default mode) When CABC_EN=”01”, User interface Image.
When CABC_EN=”10”, Still Picture.
When CABC_EN=”11”, Moving Image.</td></tr>
<tr><td>DIMI</td><td>Input</td><td>Brightness control signal. Normally pull high.</td></tr>
</table>

Pin Name	Pin Type	Description
DIMO	Output	Backlight dimmer signal for external controller. DIMO = “0”, Turn off external backlight controller DIMO = “1”, Logical control signal to turn on external backlight controller NOTE : If CABC OFF , DIMO = DIMI . Else DIMO is controlled by CABC
PINCTL	Input	Enable pin control function. Normally pull high PINCTL=”0”, Disable pin control function. The following pin will be inactive: MODE,RES[1:0],DITHER,HFRC,DCLKPOL,SHLR,UPDN,BIST,NBW, FRAME,SEL[1:0],CABC_EN[1:0],OPDRV,PWR_EN. PINCTL=”1”, Enable pin control function. NOTE: The related 3-wire control register bit control will be disabled under PINCTL=”1”.
OPDRV	Input	Source OP driving selection. Normally pull low OPDRV = H : 133% OPDRV = L : normal
CSB	Input	Serial communication chip select. Normally pull low
SDA	Input/Output	Serial communication data input. Normally pull low
SCL	Input	Serial communication clock input. Normally pull low
AVDD	PI	Power supply for analog circuits
AGND	PI	Ground pins for analog circuits
VDD	PI	Power supply for digital circuits
GND	PI	Ground pins for digital circuits
VDD_LVDS	PI	LVDS power
GND_LVDS	PI	LVDS ground
PWR_EN	Input	POWER enable. Normally pull low PWR_EN = H , enable PWM , Charge pump and VCOM buffer PWR_EN = L , disable PWM , Charge pump and VCOM buffer
FBA	VI	PWM controller feedback input. (for AVDD)
DRVA	Output	PWM output driver signal for the boost converter (for AVDD)
FBH	VI	Charge Pump controller feedback input. (for VGH)
DRVH	Output	Charge Pump driver signal for the boost converter (for VGH)
FBL	VI	Charge Pump controller feedback input. (for VGL)
DRVL	Output	Charge Pump driver signal for the boost converter (for VGL)
DRVL_B	Output	Inverse of DRVL(for VGL)
VCOMI	Input	VCOM buffer in
VCOMO	Output	VCOM buffer out
AVDDG	Output	AVDD regulator output
SO1~SO1536	Output	Source Driver Output Signals All outputs will be of unknown values under stand-by mode.
COM1_IN COM1_OUT	S	Internal link together between input side and output side
COM2_IN COM2_OUT	S	Internal link together between input side and output side.
TP	T	Float these pins for normal operation
SHIELDING	SH	Those pins are internally connected to the AGND. DO NOT connect to any WOA on the panel. Data Bus Shielding pad
DASHD	SH	Those pins are internally connected to the GND. RECOMMAND to add shielding lines on the FPC to reduce EMI.

Pin Name	Pin Type	Description
DUM	Dummy	Dummy pads. Those pins are floating pads.

Note:
P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,
T: Testing, SH: Shielding, PS: Power Setting, C: Capacitor pin.

EK79001 Pass Line Description:

Pass Line No:	Pad Name	
1	COM1_IN	COM1_OUT
2	COM2_IN	COM2_OUT

4.1. Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

wiring resistance

Pin Name	Wiring Resistance value(Ω)	Pin Name	Wiring resistance value (Ω)
AVDD	<5	RES0	<100
AGND	<5	RES1	<100
VDD	<5	SHLR	<100
GND	<5	UPDN	<100
V1~V14	<5	BIST	<100
DRVx	<5	MODE	<100
FBx	<5	DCLKPOL	<100
VCOMI	<5	DIMO	<100
VCOMO	<5	IFSEL	<100
D00~D07	<5	F_Ctrlx	<500
D10~D17	<5	OEVx	<500
D20~D27	<5	UDx	<500
DCLK	<5	CKVx	<500
NINC	<5	STV1x	<500
VSD	<20	STV2x	<500
HSD	<20	STBNx	<500
DEN	<20	VGH	<10
GRB	<100	VGL	<10
STBYB	<100		
DITHER	<100		

5. 3_WIRE SERIAL PORT INTERFACE

5.1. 3-Wire Command Format

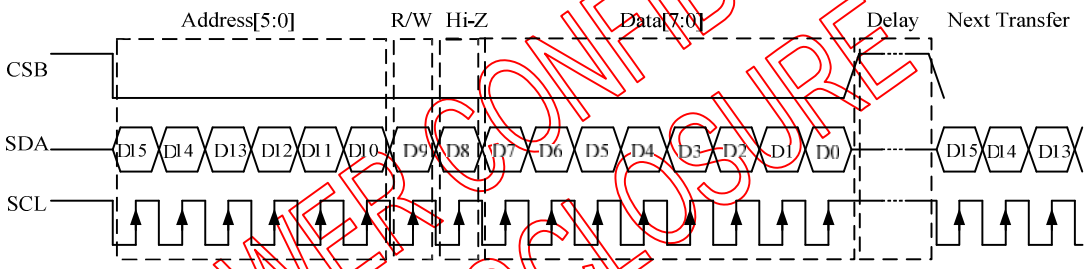
EK79001 use the 3-wire serial port as communication interface for all the function and parameter setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. EK79001 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register. Please refer to the section of “3-Wire Timing.



3-Wire timing chart

3-Wire Command Format

Bit	Description
D15~D10	Register Address [5:0].
D9	W/R control bit. “0” for Write; “1” for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7~D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Write Format

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address[5:0]						0	X	Data(Issue by external controller)							

3-Wire Read Format

MSB															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address[5:0]						1	Hi-Z	Data(Issue by 3-wire engine)							

3-Wire Control Registers:

Following table list all the 3-Wire control registers and bit name definition for EK79001. Refer to the next section for detail register function description please.

Setting of all the 3-Wire registers will take effect at the coming falling edge of VSD except GRB and STB bit.

R0: System Control Register:

Designation	Address	Description
Mode	R0[0]	DE/SYNC mode select. MODE="0", HSD/VSD mode MODE="1", DE mode(default)
DCLKPOL	R0[1]	DCLK polarity control bit. DCLKPOL="0": Data sampling at DCLK falling edge. (Default) DCLKPOL="1": Data sampling at DCLK rising edge.
GRB	R0[2]	Global reset bit. GRB="0", The controller is in reset state. GRB="1", Normal operation. (Default)
STBYB	R0[3]	Standby mode selection bit. STBYB="0", Timing control, driver and DC-DC converter, are off, and all outputs are High-Z. STBYB="1", Normal operation. (Default)
UPDN	R0[4]	G Gate Up or Down scan control. UPDN = "0", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver. (Default) UPDN = "1", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver.
SHLR	R0[5]	Right/Left sequence control of source driver. SHLR="0", Shift left: Last data = S1<S2<S3<…<S960=First data SHLR="1", Shift right: First data = S1<S2<S3<…<S960=Last data(Default)
	R0[6]	Reserved
PWM_EN	R0[7]	POWER enable. PWR_EN = H, enable PWM , Charge pump and VCOM buffer PWR_EN = L, disable PWM , Charge pump and VCOM buffer (Default)

R1: System Control Register:

Designation	Address	Description
		Reserved
RES[1:0]	R1[2:1]	RES[1:0] = "01", for 1024(RGB)*768 display resolution(dual or cascade) RES[1:0] = "00", for 1024(RGB)*600 display resolution(dual or cascade) (default) RES[1:0] = "10", for 800(RGB)*600 display resolution(dual or cascade) (601~936 channel disable) RES[1:0] = "11", for 800(RGB)*480 display resolution(dual or cascade) (601~936 channel disable)
BIST	R1[3]	Normal Operation/BIST pattern select. BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation (Default)
DITHER	R1[4]	Dithering function enable control. DITHER = "1", Enable internal dithering function DITHER = "0", Disable internal dithering function (Default)
HFRC	R1[5]	H-FRC selection. HFRC = H : H-FRC enable HFRC = L : FRC enable (Default) If DITHER="0",disable dithering function(H-FRC and FRC disable)
CABC_EN[1:0]	R1[7:6]	CABC H/W enable pin. Normally pull low. When CABC_EN="00", CABC OFF. (Default mode) When CABC_EN="01", User interface Image. When CABC_EN="10", Still Picture. When CABC_EN="11", Moving Image

R2: System Control Register:

Designation	Address	Description
		Reserved
NBW	R2[6]	Normally black or normally white setting. NBW="H": Normally black. NBW="L": Normally white(Default).
	R2[7]	Reserved

R3: Gate on sequence Controller Register:

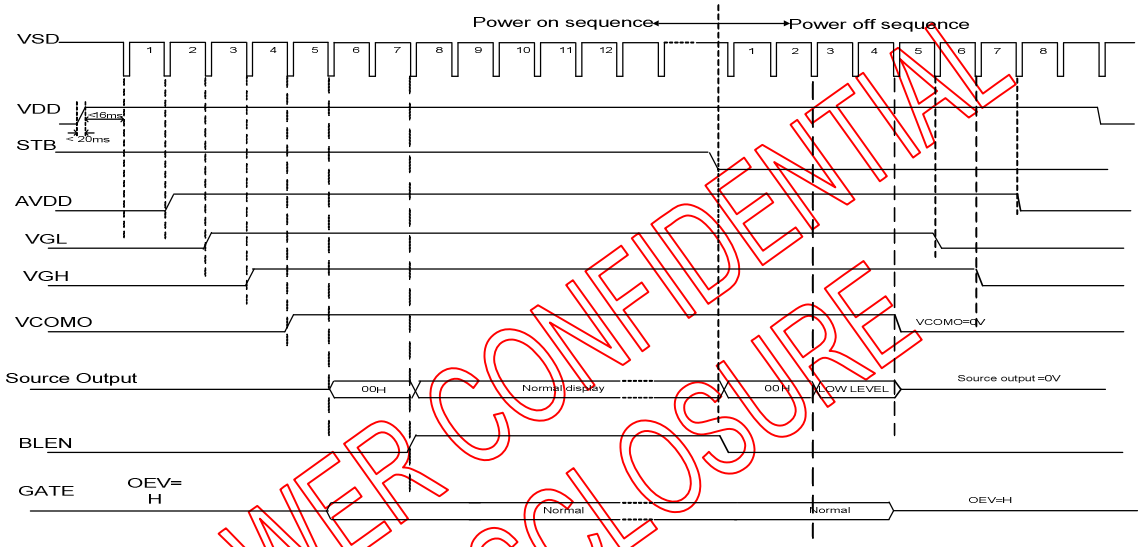
Designation	Address	Description
SEL[1:0]	R3[1:0]	Gate on sequence select. SEL[0] / SEL[1] / Pin control function 1 / 1 / Z+Σ 1 / 0 / Σ 0 / 1 / Σ 0 / 0 / Z(default)
FRAME	R3[2]	Frame inverse or not select. FRAME = "1", Uniform FRAME = "0", Frame inverse(Default)
		Reserved

6. FUNCTION DESCRIPTION

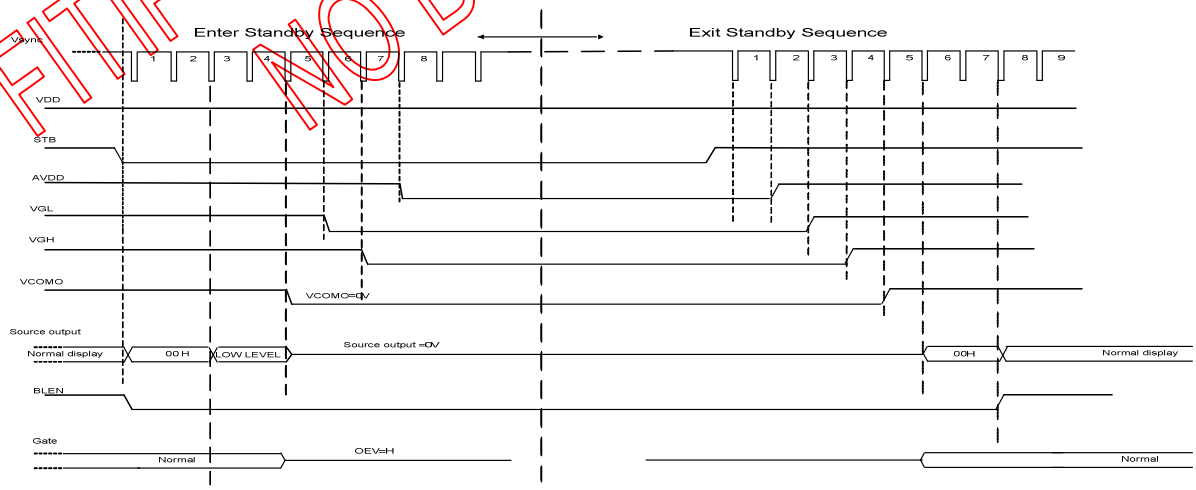
6.1. Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

6.2. Power-On/Off Timing Sequence



Power On/Off timing chart



Enter and Exit Standby Mode timing chart

Note: Low level=3Fh,when NBW=L(Normally white)
Low level=00h,when NBW=H(Normally black)

6.3. Input Data VS Output Channels

6.3.1. DUAL="0"

SHLR="1",right shift

Output	SO1	SO2	SO3	-	SO1534	SO1535	SO1536
Order	First data			→	Last data		
Odd Line	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20
Even Line	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20

SHLR="0",left shift

Output	SO1	SO2	SO3	---	SO1534	SO1535	SO1536
Order	Last data			←	First data		
Odd Line	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20
Even Line	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20

6.3.2. DUAL="1"

SHLR="1",right shift

Output	SO1	SO2	SO3	---	SO1534	SO1535	SO1536
Order	First data			->	Last data		
Odd Line/ Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Odd Line/ Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Even Line/ Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Even Line/ Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20

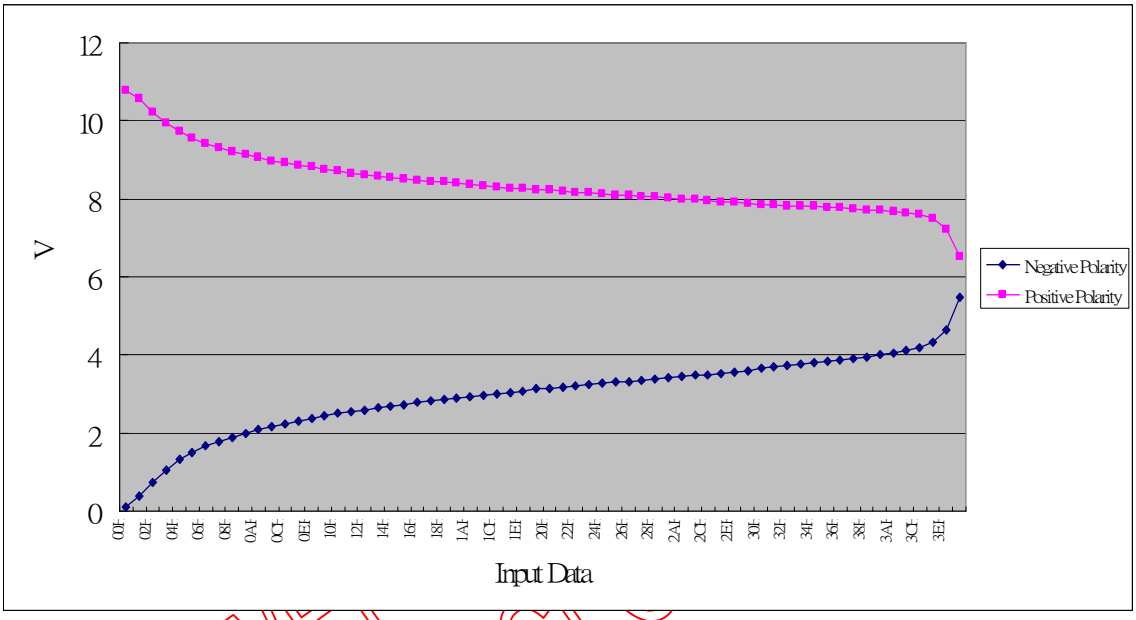
SHLR="0",left shift

Output	SO1	SO2	SO3	---	SO1534	SO1535	SO1536
Order	Last data			<-	First data		
Odd Line/ Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Odd Line/ Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Even Line/ Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Even Line/ Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20

6.4. Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.

Gamma Tables very for each customer.



Remark: AVDD-0.1 > V1 > V2> V3 > V4 > V5 > V6 > V7; V8 > V9 > V10 > V11 > V12 > V13 > V14 > AGND+0.1V

6.5. Input Data and Output Voltage Reference Table

Input Data and Output Voltage Reference Table

@AVDD=11V

V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14	Unit
10.78	10.569	8.708	8.213	7.866	7.243	6.51	5.49	4.63	3.653	3.146	2.493	0.373	0.11	V

Data	Positive
00H	AVDD×0.980
01H	AVDD×0.961
02H	AVDD×0.930
03H	AVDD×0.905
04H	AVDD×0.885
05H	AVDD×0.870
06H	AVDD×0.857
07H	AVDD×0.847
08H	AVDD×0.838
09H	AVDD×0.830
0AH	AVDD×0.823
0BH	AVDD×0.816
0CH	AVDD×0.811
0DH	AVDD×0.806
0EH	AVDD×0.801
0FH	AVDD×0.796
10H	AVDD×0.792
11H	AVDD×0.788
12H	AVDD×0.784
13H	AVDD×0.781
14H	AVDD×0.778
15H	AVDD×0.775
16H	AVDD×0.772
17H	AVDD×0.769
18H	AVDD×0.766
19H	AVDD×0.763
1AH	AVDD×0.761
1BH	AVDD×0.758
1CH	AVDD×0.756
1DH	AVDD×0.753
1EH	AVDD×0.751
1FH	AVDD×0.748

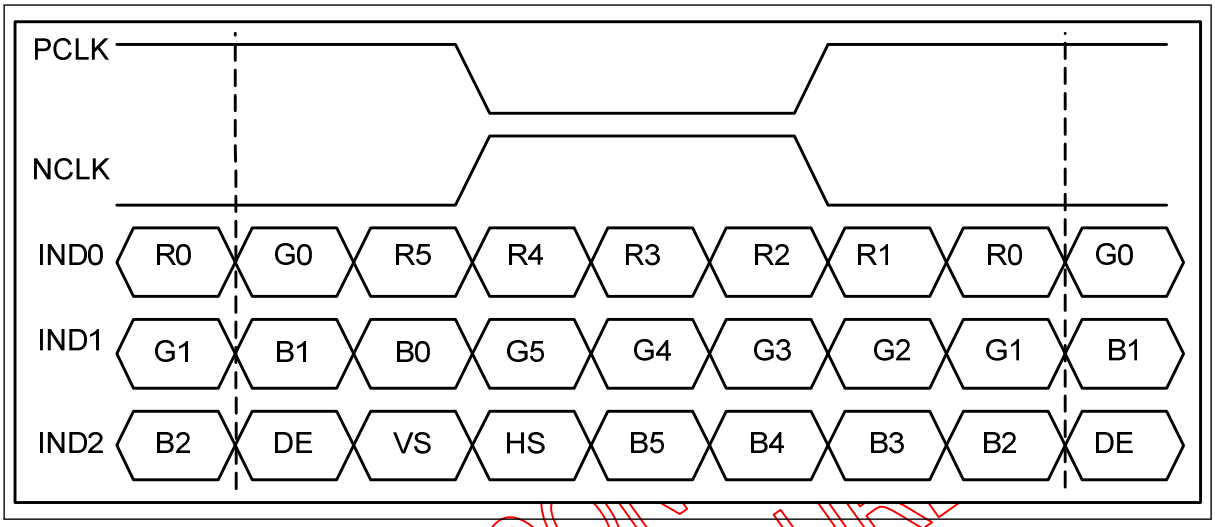
Data	Positive
20H	AVDD×0.747
21H	AVDD×0.745
22H	AVDD×0.743
23H	AVDD×0.741
24H	AVDD×0.739
25H	AVDD×0.737
26H	AVDD×0.735
27H	AVDD×0.732
28H	AVDD×0.731
29H	AVDD×0.729
2AH	AVDD×0.727
2BH	AVDD×0.725
2CH	AVDD×0.723
2DH	AVDD×0.721
2EH	AVDD×0.719
2FH	AVDD×0.717
30H	AVDD×0.715
31H	AVDD×0.713
32H	AVDD×0.711
33H	AVDD×0.710
34H	AVDD×0.709
35H	AVDD×0.707
36H	AVDD×0.706
37H	AVDD×0.704
38H	AVDD×0.702
39H	AVDD×0.700
3AH	AVDD×0.697
3BH	AVDD×0.694
3CH	AVDD×0.690
3DH	AVDD×0.681
3EH	AVDD×0.658
3FH	AVDD×0.592

Data	Negative
00H	AVDD×0.010
01H	AVDD×0.034
02H	AVDD×0.068
03H	AVDD×0.096
04H	AVDD×0.119
05H	AVDD×0.136
06H	AVDD×0.151
07H	AVDD×0.162
08H	AVDD×0.172
09H	AVDD×0.182
0AH	AVDD×0.189
0BH	AVDD×0.197
0CH	AVDD×0.204
0DH	AVDD×0.210
0EH	AVDD×0.215
0FH	AVDD×0.221
10H	AVDD×0.227
11H	AVDD×0.231
12H	AVDD×0.236
13H	AVDD×0.240
14H	AVDD×0.245
15H	AVDD×0.248
16H	AVDD×0.253
17H	AVDD×0.256
18H	AVDD×0.260
19H	AVDD×0.263
1AH	AVDD×0.266
1BH	AVDD×0.270
1CH	AVDD×0.273
1DH	AVDD×0.277
1EH	AVDD×0.280
1FH	AVDD×0.284

Data	Negative
20H	AVDD×0.286
21H	AVDD×0.289
22H	AVDD×0.292
23H	AVDD×0.294
24H	AVDD×0.297
25H	AVDD×0.300
26H	AVDD×0.302
27H	AVDD×0.305
28H	AVDD×0.308
29H	AVDD×0.311
2AH	AVDD×0.314
2BH	AVDD×0.316
2CH	AVDD×0.318
2DH	AVDD×0.321
2EH	AVDD×0.325
2FH	AVDD×0.328
30H	AVDD×0.332
31H	AVDD×0.336
32H	AVDD×0.339
33H	AVDD×0.342
34H	AVDD×0.345
35H	AVDD×0.348
36H	AVDD×0.351
37H	AVDD×0.355
38H	AVDD×0.359
39H	AVDD×0.364
3AH	AVDD×0.369
3BH	AVDD×0.375
3CH	AVDD×0.382
3DH	AVDD×0.394
3EH	AVDD×0.421
3FH	AVDD×0.499

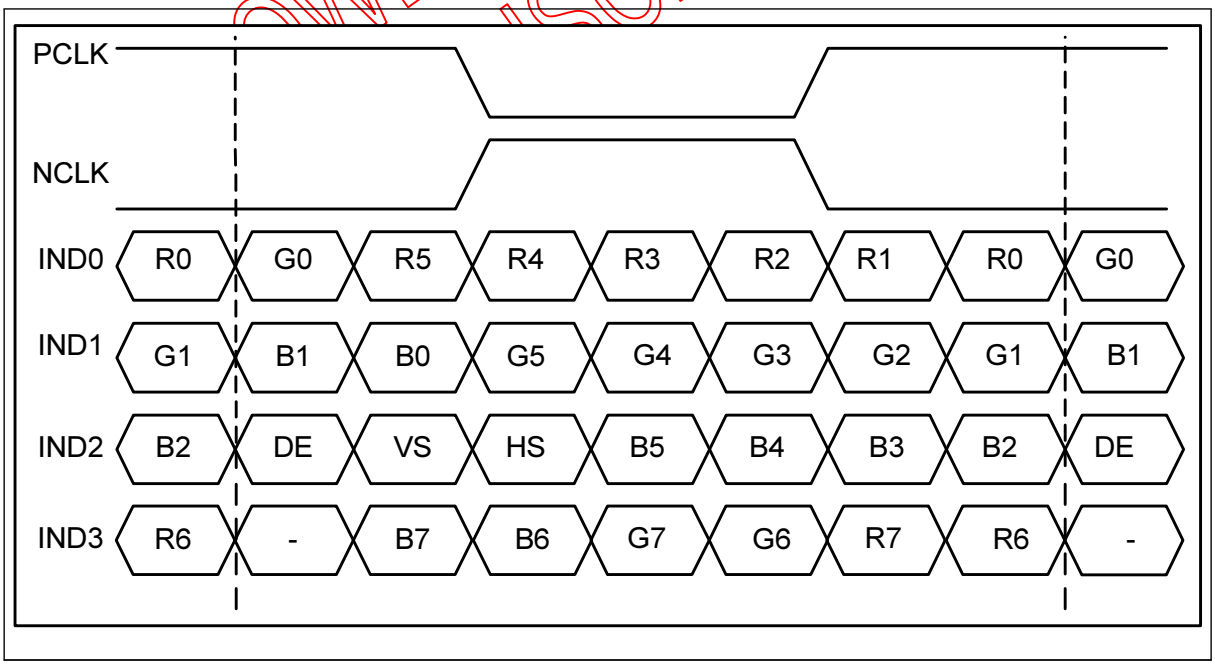
6.6. Data Input Format for LVDS

6.6.1. 6-bit LVDS input(HSD="H")



6-bit LVDS Input Timing chart

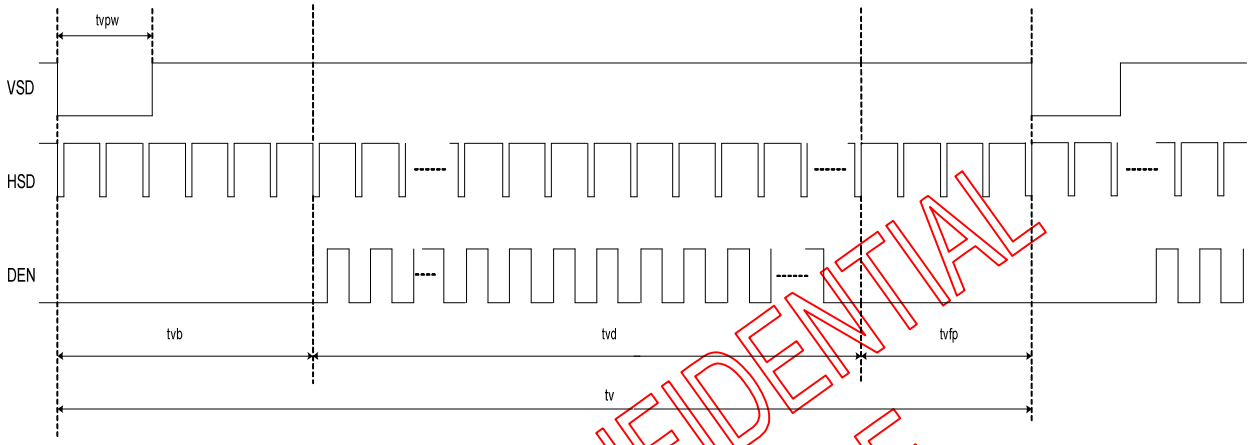
6.6.2. 8-bit LVDS input(HSD="L")



8-bit LVDS Input Timing chart

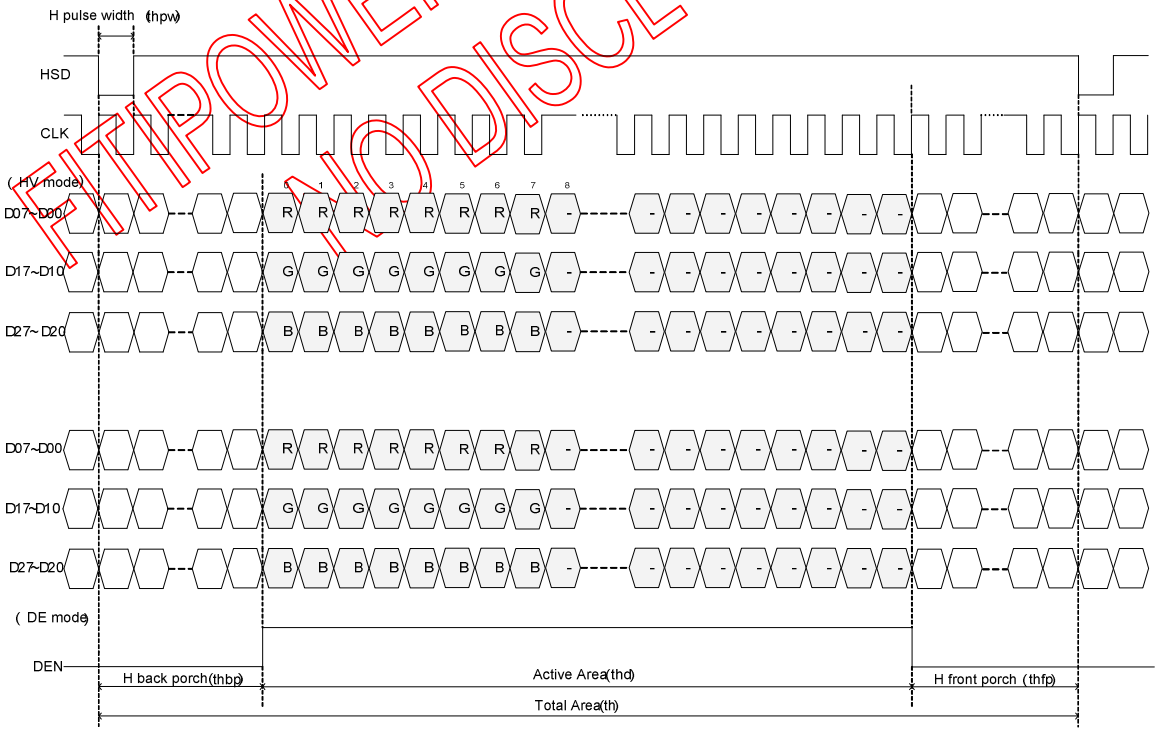
6.7. Data Input Format for TTL

6.7.1. Vertical input timing



Vertical input timing

6.7.2. Horizontal input timing



Horizontal input timing

6.8. Parallel RGB Timing Characteristic

6.8.1. For 1024RGB x 768 panel

DE mode

DE mode					
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	fclk	52	65	71	Mhz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thbp+thfp	90	320	376	DCLK
Vertical display area	tvd		768		H
VSYNC period time	tv	778	806	845	H
VSYNC blanking	tvb+tvfp	10	38	77	H

HV mode(1)

HV mode Horizontal input timing						
Parameter		Symbol	Value			Unit
Horizontal display area		thd	1024			DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min.	Typ.	Max.	
			57	65	70.5	Mhz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		–			
	Max.		140			
HSYNC back porch		thbp	160	160	160	
HSYNC front porch		thfp	16	160	216	

HV mode(2)

Vertical input timing					
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		768		H
VSYNC period time	tv	792	806	840	H
VSYNC pulse width	tvpw	1	–	20	H
VSYNC back porch	tvb	23	23	23	H
VSYNC front porch	tvfp	1	15	49	H

6.8.2. For 1024RGB x 600 panel

DE mode

DE mode					
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	fclk	40.8	51.2	67.2	Mhz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thb+thfp	90	320	376	DCLK
Vertical display area	tvd		600		H
VSYNC period time	tv	610	635	800	H
VSYNC blanking	tvb+tvfp	10	35	200	H

HV mode(1)

HV mode Horizontal input timing						
Parameter		Symbol	Value			Unit
Horizontal display area		thd	1024			DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min.	Typ.	Max.	
			44.9	51.2	63	Mhz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		—			
	Max.		140			
HSYNC back porch		thbp	160	160	160	
HSYNC front porch		thfp	16	160	216	

HV mode(2)

Vertical input timing					
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		H
VSYNC period time	tv	624	635	750	H
VSYNC pulse width	tvpw	1	—	20	H
VSYNC back porch	tvb	23	23	23	H
VSYNC front porch	tvfp	1	12	127	H

6.8.3. For 800RGB x 600 panel

DE mode

DE mode					
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	fclk	32.6	39.6	62.4	Mhz
Horizontal display area	thd		800		DCLK
HSYNC period time	th	890	1000	1300	DCLK
HSYNC blanking	thb+thfp	90	200	500	DCLK
Vertical display area	tvd		600		H
VSYNC period time	tv	610	660	800	H
VSYNC blanking	tvb+tvfp	10	60	200	H

HV mode(1)

HV mode Horizontal input timing						
Parameter		Symbol	Value			Unit
Horizontal display area		thd	800			DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min.	Typ.	Max.	
			34.5	39.6	50.4	Mhz
1 Horizontal Line		th	900	1000	1200	DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		—			
	Max.		40			
HSYNC back porch		thbp	88	88	88	
HSYNC front porch		thfp	12	112	312	

HV mode(2)

Vertical input timing					
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		H
VSYNC period time	tv	640	660	700	H
VSYNC pulse width	tvpw	1	—	20	H
VSYNC back porch	tvb	39	39	39	H
VSYNC front porch	tvfp	1	21	61	H

6.8.4. For 800RGB x 480 panel

DE mode

DE mode					
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	fclk	26.2	29.2	54.6	Mhz
Horizontal display area	thd		800		DCLK
HSYNC period time	th	890	928	1300	DCLK
HSYNC blanking	thb+thfp	90	128	500	DCLK
Vertical display area	tvd		480		H
VSYNC period time	tv	490	525	700	H
VSYNC blanking	tvb+tvfp	10	45	220	H

HV mode(1)

HV mode Horizontal input timing						
Parameter		Symbol	Value			Unit
Horizontal display area		thd	800			DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min.	Typ.	Max.	
			27.7	29.2	39.6	Mhz
1 Horizontal Line		th	900	928	1100	DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		—			
	Max.		40			
HSYNC back porch		thbp	88	88	88	
HSYNC front porch		thfp	12	40	212	

HV mode(2)

Vertical input timing					
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		480		H
VSYNC period time	tv	513	525	600	H
VSYNC pulse width	tvpw	1	—	3	H
VSYNC back porch	tvb	32	32	32	H
VSYNC front porch	tvfp	1	13	88	H

7. ELECTRICAL SPECIFICATION

7.1. Absolute Maximum Ratings

VOLTAGE (TA = 25℃, GND = AGND = GND_LVDS = 0V)

	Min.	Max.	Unit
Digital Supply Voltage, VDD	-0.5	+5.0	V
Analog Supply Voltage, AVDD, V1~V14	-0.5	+15.0	V

TEMPERATURE

	Min.	Max.	Unit
Operating temperature	-20	+85	℃
Storage temperature	-55	+125	℃

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposed to absolute maximum rating conditions for extended periods may affect device reliability.

7.2. Recommended Operating Range

Recommended Operating Range (TA = -20 to 85℃, GND = AGND = GND_LVDS = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	VDD	2.3	3.3	3.6	V
Analog supply voltage	AVDD	8	-	13.5	V
Digital input voltage	VIN	0	-	VDD	V

7.3. DC Electrical Characteristics

DC Characteristics

(TA = -20 to 85℃, VDD = 2.3 to 3.6V, AVDD = 8 to 13.5V, GND = AGND = GND_LVDS = 0V)

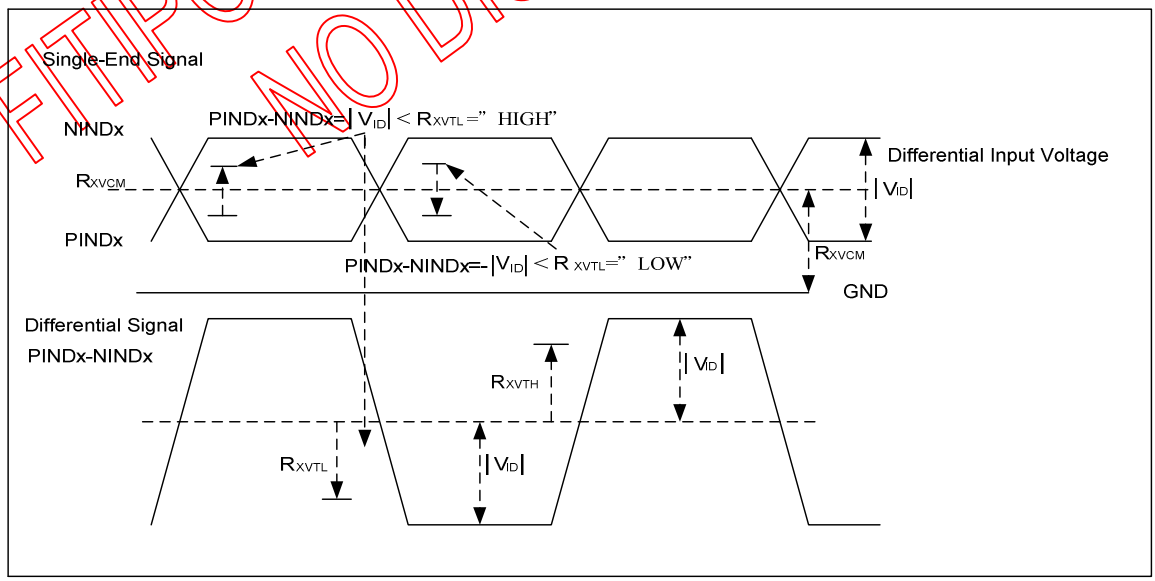
7.3.1. TTL mode

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level input voltage	Vil	For the digital circuit	0	-	0.3×VDD	V
High level input voltage	Vih	For the digital circuit	0.7×VDD	-	VDD	V
Input leakage current	Ii	For the digital circuit	-	-	±1	μA
High level output voltage	Voh	Ioh= -400 μA	VDD-0.4	-	-	V
Low level output voltage	Vol	Iol= +400 μA	-	-	GND+0.4	V
Pull low/high resistor	Ri	For the digital input pin @ VDD=3.3V	200K	250K	300K	ohm
Digital Operation current	Idd	Fclk=65 MHz, FLD=50KHz, VDD=3.3V	-	15	25	mA
Digital Stand-by current	Ist1	Clock and all functions are stopped	-	10	50	μA
Analog Operating Current	Idda	No load, Fclk=65MHz, FLD=50KHz @ AVDD=10V,V1=8V, V14=0.4V	-	10	12	mA
Analog Stand-by current	Ist2	No load, Clock and all functions are Stopped	-	10	50	μA
Input level of V1 ~ V7	Vref1	Gamma correction voltage input	0.4*AVDD	-	AVDD-0.1	V
Input level of V8 ~ V14	Vref2	Gamma correction voltage input	0.1	-	0.6*AVDD	V
Output Voltage deviation	Vod1	Vo = AVSS+0.1V ~ AVSS+0.5V and Vo = AVDD-0.5V ~ AVDD-0.1V	-	±20	±35	mV
Output Voltage deviation	Vod2	Vo = AVSS+0.5V ~ AVDD-0.5V	-	±15	±20	mV
Output Voltage Offset between Chips	Voc	Vo = AVSS+0.5V ~ AVDD-0.5V	-	-	±20	mV
Dynamic Range of Output	Vdr	SO1 ~ SO1536	0.1	-	AVDD-0.1	V
Sinking Current of Outputs	IOLy	SO1 ~ SO1536; Vo=0.1V v.s 1.0V , AVDD=13.5V	80	-	-	uA
Driving Current of Outputs	IOHy	SO1 ~ SO1536; Vo=13.4V v.s 12.5V , AVDD=13.5V	80	-	-	uA
Resistance of Gamma Table	Rg	Rn: Internal gamma resistor	0.7*Rn	1.0*Rn	1.3*Rn	ohm

7.3.2. LVDS mode(Receiver Differential :PIND0~PIND3,NIND0~NIND3,PINC,NINC)

LVDS DC characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential input high threshold voltage	RxVTH			+0.1V	V	RxVCM=1.2V
Differential input low threshold voltage	RxVTL	-0.1			V	
Input voltage range(single-end)	RxVIN	0		2.4	V	
Differential input common mode voltage	RxVCM	$\|V_{ID}\|/2$		2.4 -$\|V_{ID}\|/2$	V	
Differential input voltage	**$\|V_{ID}\|$**	0.2		0.6	V	
Differential input leakage current	RxVTH	-10		+10	V	
LVDS Digital Operating Current	Iddlvsd	-	40(TBD)	50	mA	Fclk=65Mhz, VDD=3.3V
LVDS Digital Standby Current	Istlvds	-	10(TBD)	50	uA	Clock & all functions are stop



LVDS DC Characteristic

7.3.3. Power

Power

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Base drive current for PWM	IDRV	_	_	60	mA	DRVA = 0.7V
DRV output voltage for PWM	VDRV	0	_	VDD	V	
Feedback voltage for PWM	VFB	1.1	1.2	1.3	V	
Duty cycle maximum	Dmax	_	_	85	%	
VCOM buffer input voltage	VCOMI	1	_	AVDD	V	
VCOM buffer output voltage	VCOMO	VCOMI-0.2	VCOMI	VCOMI+0.2	V	
VCOM buffer output current	IVCOM	_	_	10	mA	VCOMO= 5V vs 4.9V

7.4. AC Electrical Characteristics

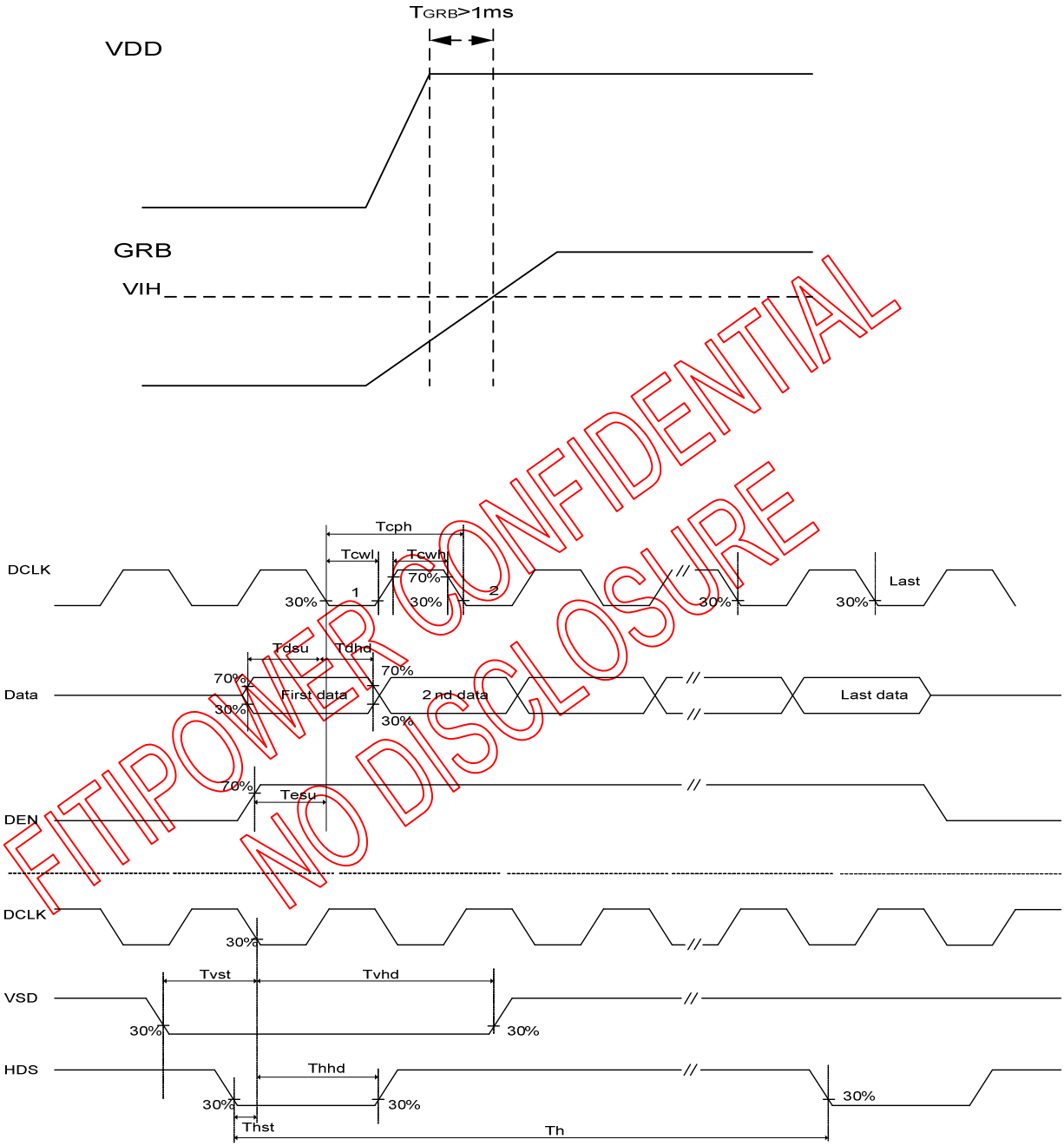
(TA = -20 to 85℃, VDD = 2.3 to 3.6V, AVDD = 8 to 13.5V, GND = AGND = 0V)

TTL mode

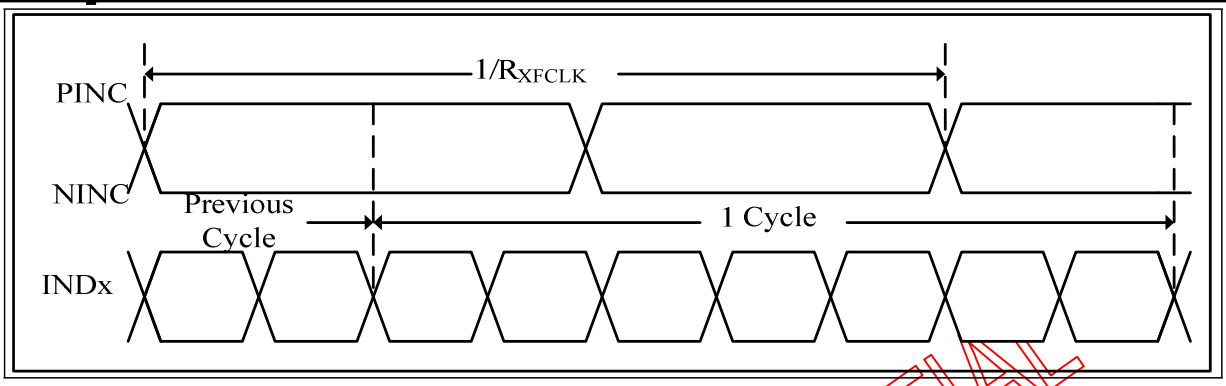
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VDD Power On Slew rate	TPOR	From 0V to 90% VDD	-	-	20	ms
RSTB pulse width	TRST	DCLK = 65MHz	50	-	-	us
DCLK cycle time	Tcph	-	14	-	-	ns
DCLK pulse duty	Tcwh	-	40	50	60	%
VSD setup time	Tvst	-	5	-	-	ns
VSD hold time	Tvhd	-	5	-	-	ns
HSD setup time	Thst	-	5	-	-	ns
HSD hold time	Thhd	-	5	-	-	ns
Data set-up time	Tdsu	D0[7:0], D1[7:0], D2[7:0] to DCLK	5	-	-	ns
Data hold time	Tdhd	D0[7:0], D1[7:0], D2[7:0] to DCLK	5	-	-	ns
DE setup time	Tesu	-	5	-	-	ns
DE hold time	Tehd	-	5	-	-	ns
Output stable time	Tsst	10% to 90% target voltage. CL=90pF, R=10K ohm(Cascade)	-	-	6	us
		Dual gate			3	

LVDS mode

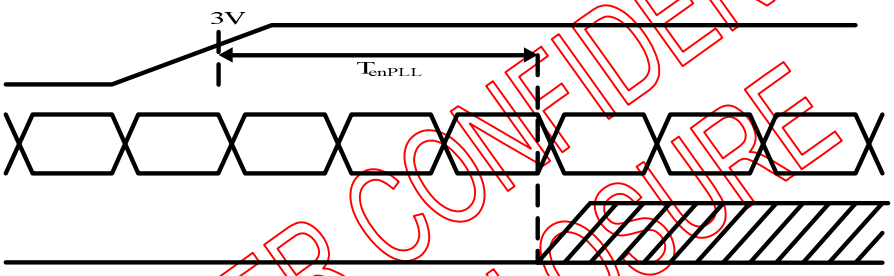
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	R_{xFCLK}		20	-	71	MHz
Input data skew margin	T_{RSKM}	$\|V_{ID}\|$=400mV R_{xVCM}=1.2V R_{xFCLK}=71MHz	500			ps
Clock High Time	T_{LVCH}			4/(7* R_{xFCLK})		ns
						ns
Clock Low Time	T_{LVCL}			3/(7* R_{xFCLK})		ns
PLL wake-up-time	T_{enPLL}				150	us



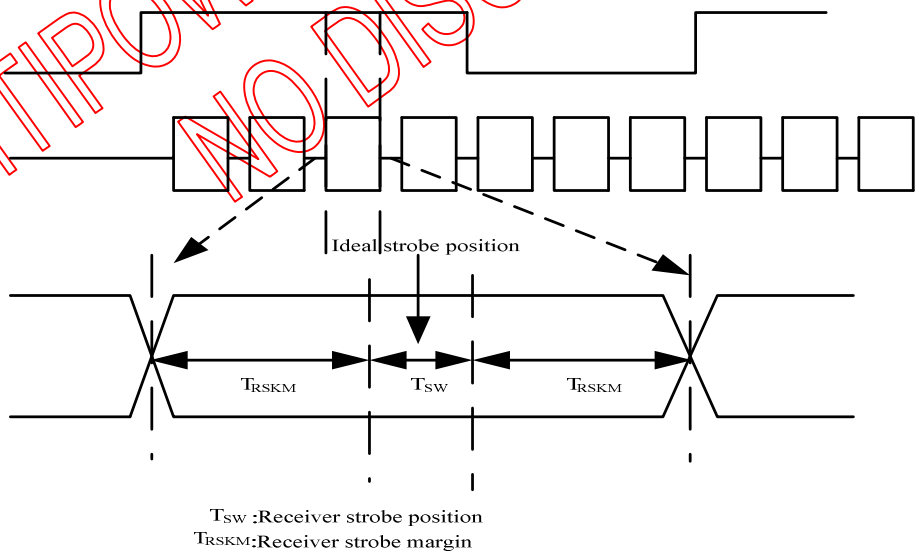
Parallel Input Clock and Data timing



LVDS timing(1)



LVDS timing(2)

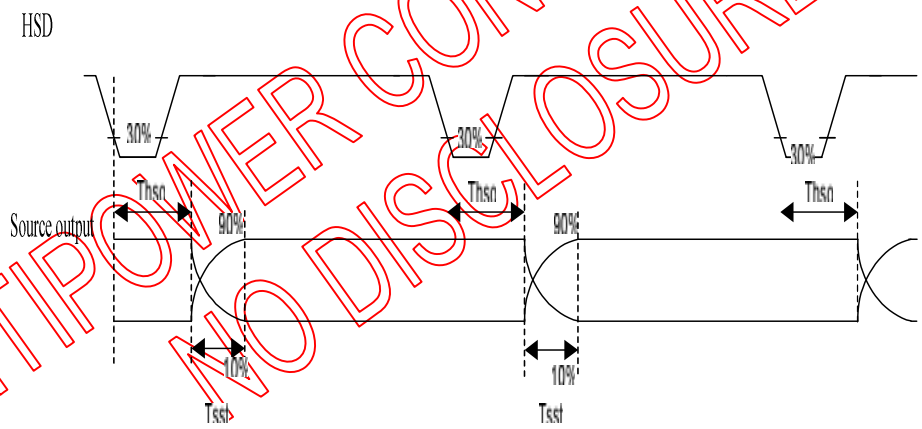


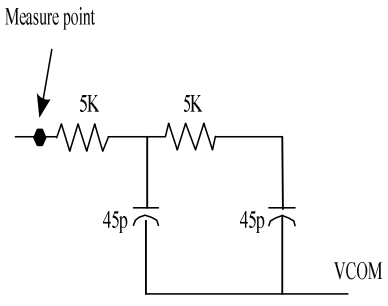
LVDS timing(3)

7.5. Output Timing Table

Output Timing Table

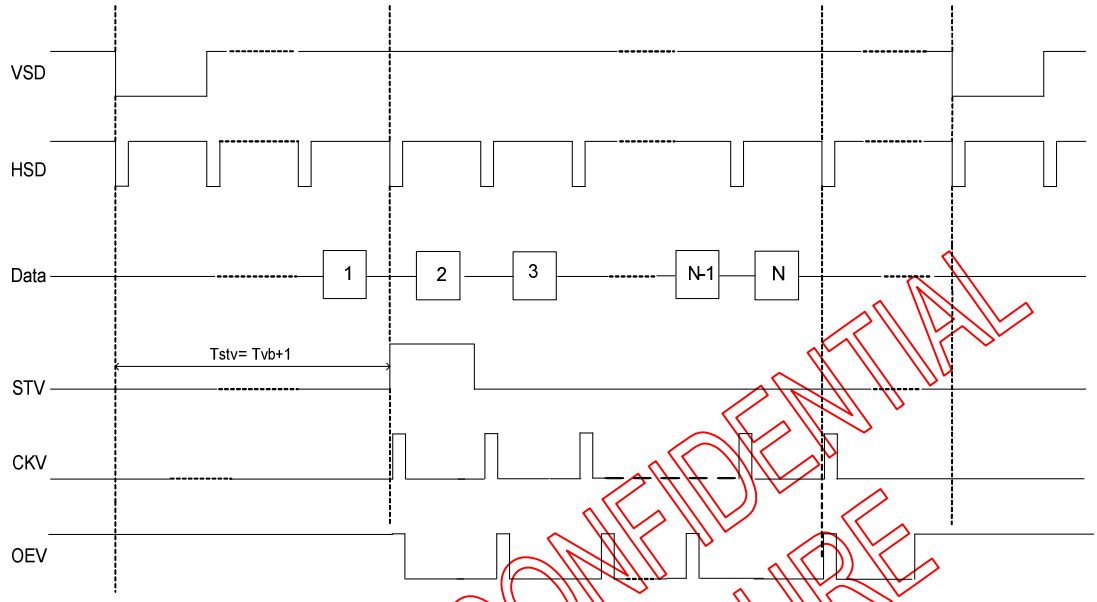
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
DCLK frequency	Fclk	-	65	71	MHz	VDD =2.3~3.6V
DCLK cycle time	Tclk	14.1	15.4		ns	
DCLK pulse duty	Tcwh	40	50	60	%	Tclk
Time from HSD to Source Output	Thso	-	64	-	DCLK	
Time from HSD to LD	Thld	-	64	-	DCLK	
Time from HSD to STV	Thstv	-	2	-	DCLK	
Time from HSD to CKV	Thckv	-	20	-	DCLK	
Time from HSD to OEV	Thoev	-	4	-	DCLK	
LD pulse width	Twld	-	10	-	DCLK	
CKV pulse width	Twckv	-	66	-	DCLK	
OEV pulse width	Twoev	-	74	-	DCLK	





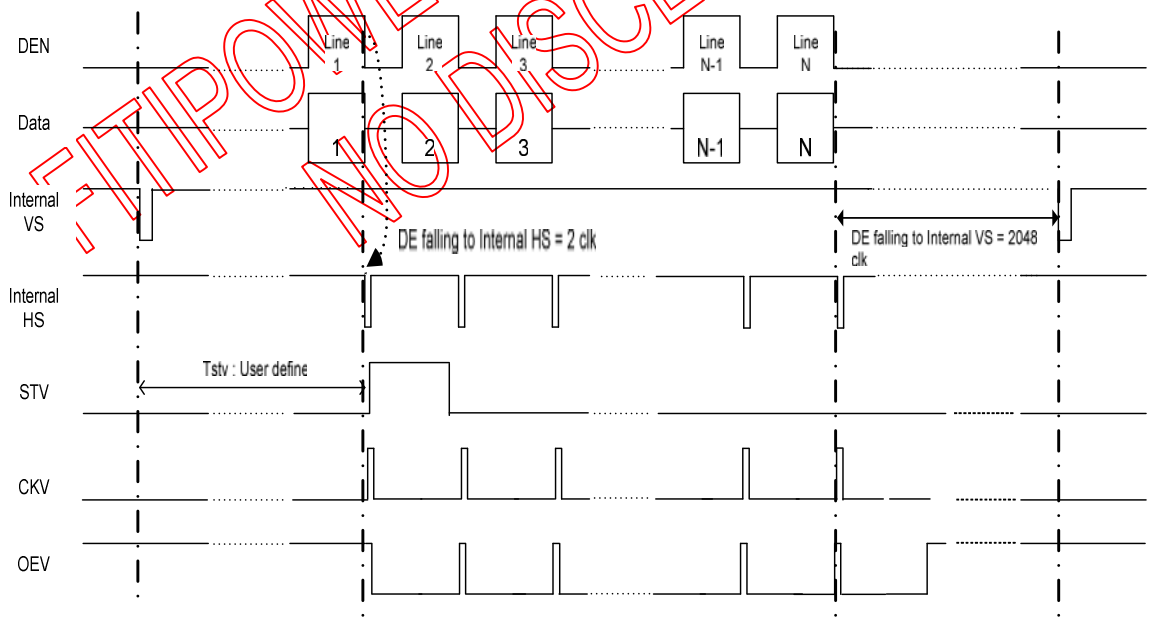
Source Output Timing(Cascade)

7.5.1. Vertical Timing Diagram HV mode(Cascade)



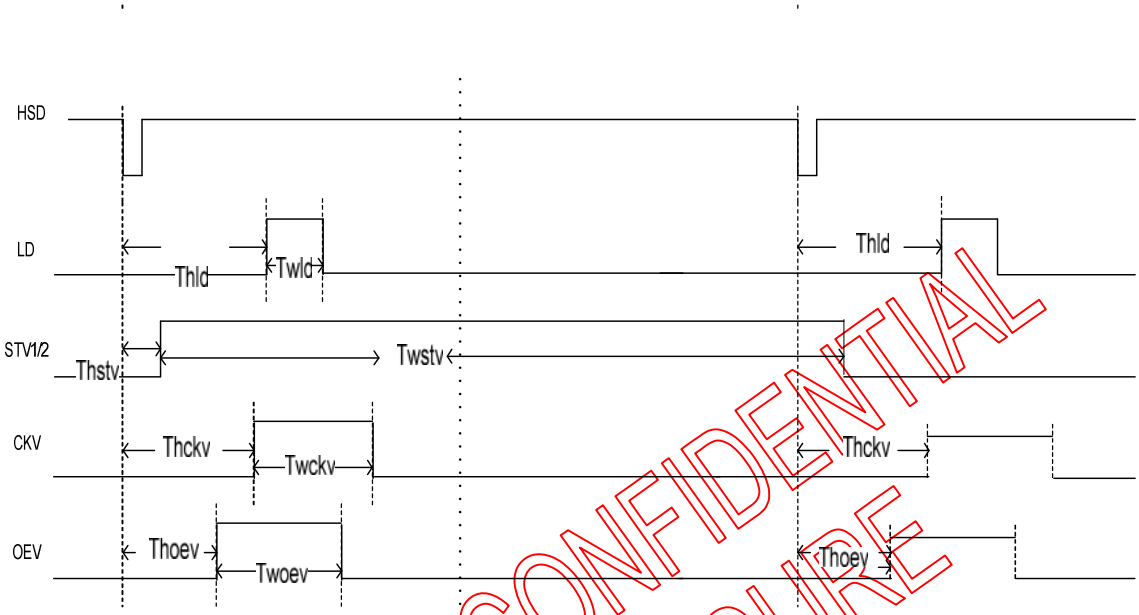
Vertical Timing Diagram HV mode(Cascade)

7.5.2. Vertical Timing Diagram DE mode(Cascade)



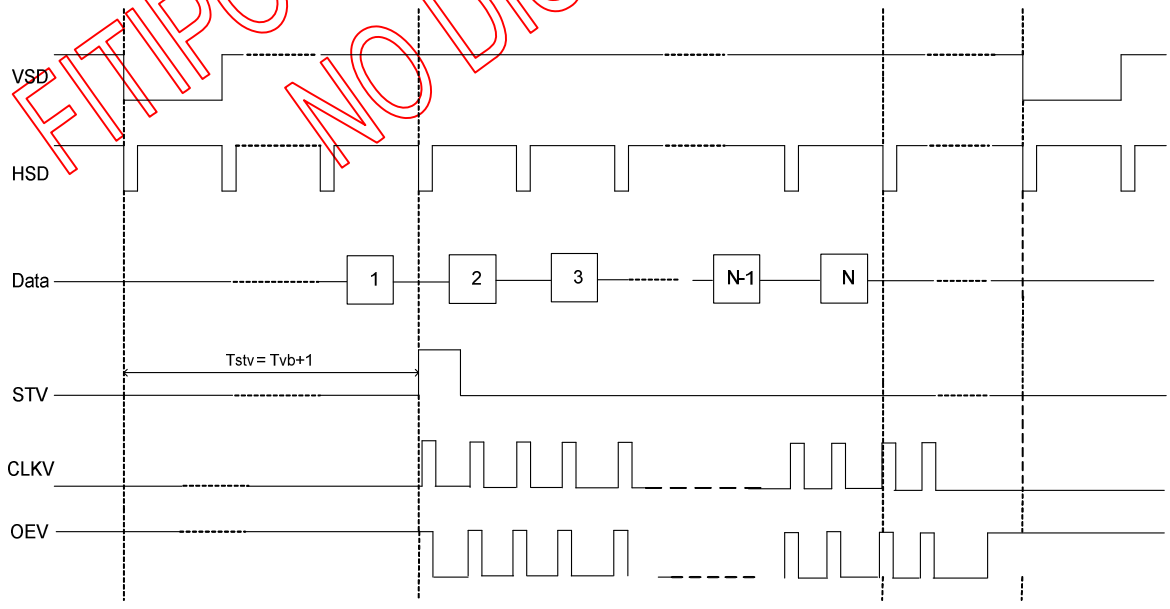
Vertical Timing Diagram DE mode(Cascade)

7.5.3. Gate output timing diagram(Cascade)



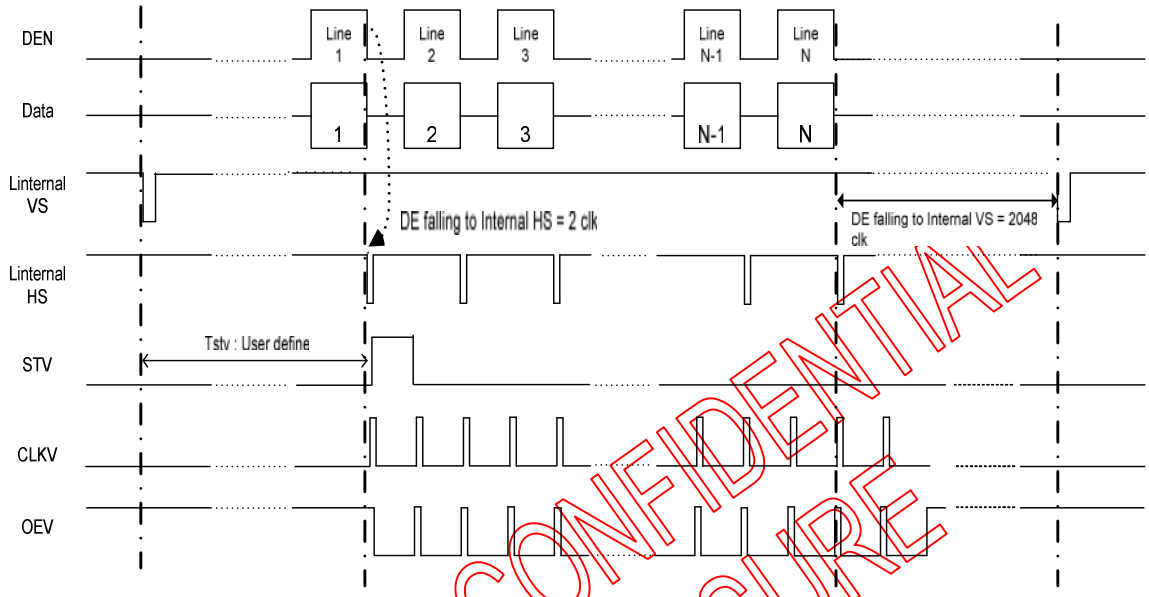
Gate output timing diagram(Cascade)

7.5.4. Vertical Timing Diagram HV mode(Dual Gate)



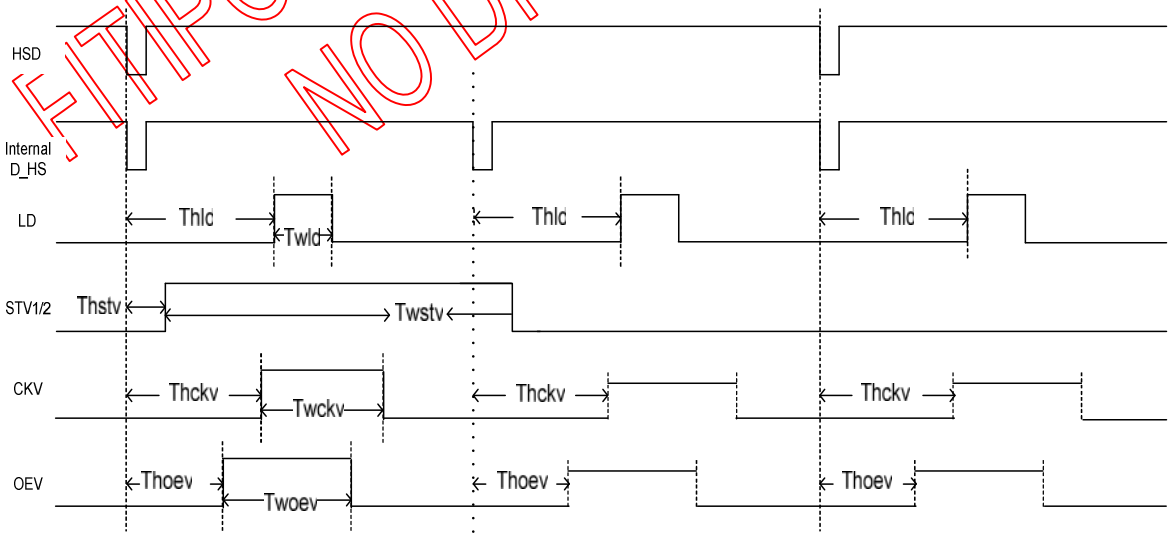
Vertical Timing Diagram HV mode(Dual Gate)

7.5.5. Vertical Timing Diagram DE mode(Dual Gate)



Vertical Timing Diagram DE mode(Dual Gate)

7.5.6. Gate output timing diagram(Dual Gate)

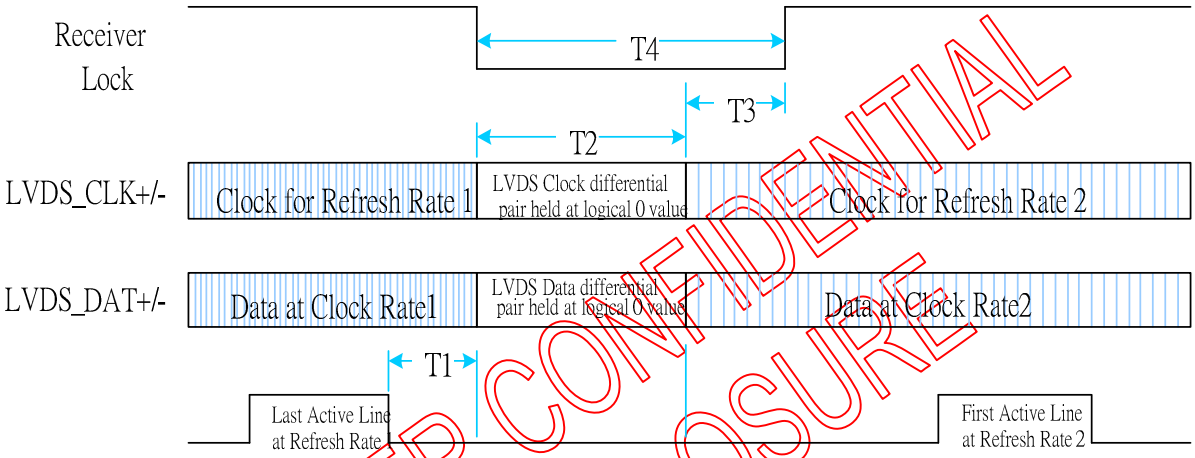


Gate output timing diagram(Dual Gate)

8. SDRRS TIMING DIAGRAM

SDRRS(seamless display refresh rate switching)

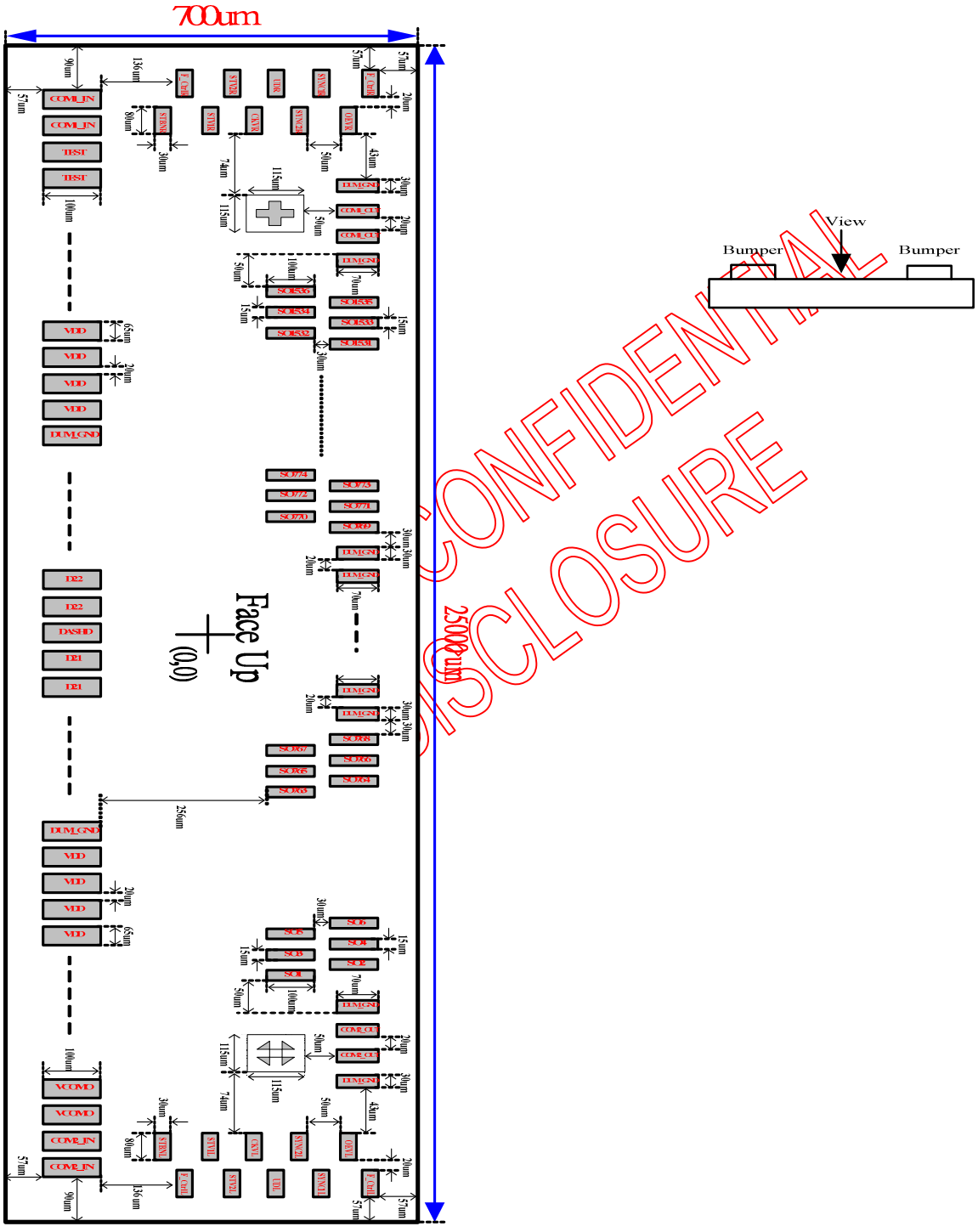
When Showing the still picture.it is accept to refresh rate from 60Hz to low refresh rate (for example 40Hz).The purpose is mainly for power saving. INTEL defined a timing chart switch between different refresh rate.Following this timing chart,the switch between different refresh rates is seamless for end user.



SDRRS timing

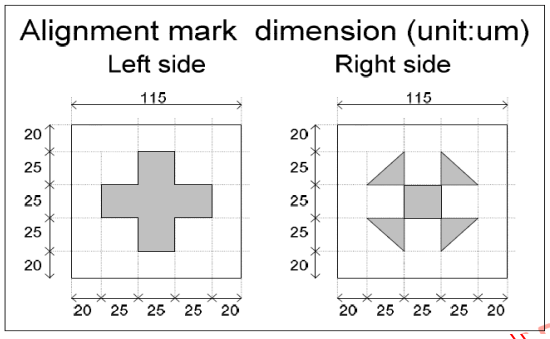
T1-Min delay from start of vertical blank to start of timing change:2 lines(HSYNC periods)
T2-Max delay for clock to transition to new frequency:100us
T3-Max receiver lock delay from stable clock: Display specific
T4-Max period during which panel maintains display(T2+T3): Display specific

9. CHIP OUTLINE DIMENSIONS



Chip Outline Dimensions

9.1. Alignment Mark



Alignment Mark

9.2. Pad Coordinate

Pad	Text Name	CX	CY		42	NBW	-8892.5	-243		84	SHIELDING	-5322.5	-243
1	COM1_IN	-12377.5	-243		43	PINCTL	-8807.5	-243		85	AGND	-5237.5	-243
2	COM1_IN	-12292.5	-243		44	PINCTL	-8722.5	-243		86	AGND	-5152.5	-243
3	TP	-12207.5	-243		45	SHIELDING	-8637.5	-243		87	AGND	-5067.5	-243
4	TP	-12122.5	-243		46	DIMO	-8552.5	-243		88	AGND	-4982.5	-243
5	TP	-12037.5	-243		47	DIMO	-8467.5	-243		89	SHIELDING	-4897.5	-243
6	TP	-11952.5	-243		48	SHIELDING	-8382.5	-243		90	V1	-4812.5	-243
7	SHIELDING	-11867.5	-243		49	DITHER	-8297.5	-243		91	V1	-4727.5	-243
8	AGND	-11782.5	-243		50	DITHER	-8212.5	-243		92	V2	-4642.5	-243
9	AGND	-11697.5	-243		51	HFRC	-8127.5	-243		93	V2	-4557.5	-243
10	AGND	-11612.5	-243		52	HFRC	-8042.5	-243		94	V3	-4472.5	-243
11	AGND	-11527.5	-243		53	TP	-7957.5	-243		95	V3	-4387.5	-243
12	SHIELDING	-11442.5	-243		54	TP	-7872.5	-243		96	V4	-4302.5	-243
13	AVDD	-11357.5	-243		55	FRAME	-7787.5	-243		97	V4	-4217.5	-243
14	AVDD	-11272.5	-243		56	FRAME	-7702.5	-243		98	V5	-4132.5	-243
15	AVDD	-11187.5	-243		57	SEL[0]	-7617.5	-243		99	V5	-4047.5	-243
16	AVDD	-11102.5	-243		58	SEL[0]	-7532.5	-243		100	V6	-3962.5	-243
17	SHIELDING	-11017.5	-243		59	SEL[1]	-7447.5	-243		101	V6	-3877.5	-243
18	GND	-10932.5	-243		60	SEL[1]	-7362.5	-243		102	V7	-3792.5	-243
19	GND	-10847.5	-243		61	CSB	-7277.5	-243		103	V7	-3707.5	-243
20	GND	-10762.5	-243		62	CSB	-7192.5	-243		104	GAMH	-3622.5	-243
21	GND	-10677.5	-243		63	SHIELDING	-7107.5	-243		105	GAMH	-3537.5	-243
22	SHIELDING	-10592.5	-243		64	SDA	-7022.5	-243		106	SHIELDING	-3452.5	-243
23	VDD	-10507.5	-243		65	SDA	-6937.5	-243		107	DASHD	-3367.5	-243
24	VDD	-10422.5	-243		66	SHIELDING	-6852.5	-243		108	VSD	-3282.5	-243
25	VDD	-10337.5	-243		67	SCL	-6767.5	-243		109	DASHD	-3197.5	-243
26	VDD	-10252.5	-243		68	SCL	-6682.5	-243		110	HSD	-3112.5	-243
27	SHIELDING	-10167.5	-243		69	SHIELDING	-6597.5	-243		111	DASHD	-3027.5	-243
28	TP	-10082.5	-243		70	VDD	-6512.5	-243		112	DEN	-2942.5	-243
29	TP	-9997.5	-243		71	VDD	-6427.5	-243		113	GND_LVDS	-2857.5	-243
30	TP	-9912.5	-243		72	VDD	-6342.5	-243		114	GND_LVDS	-2772.5	-243
31	TP	-9827.5	-243		73	VDD	-6257.5	-243		115	GND_LVDS	-2687.5	-243
32	TP	-9742.5	-243		74	SHIELDING	-6172.5	-243		116	GND_LVDS	-2602.5	-243
33	TP	-9657.5	-243		75	GND	-6087.5	-243		117	D27	-2517.5	-243
34	TP	-9572.5	-243		76	GND	-6002.5	-243		118	D26	-2432.5	-243
35	TP	-9487.5	-243		77	GND	-5917.5	-243		119	DASHD	-2347.5	-243
36	TP	-9402.5	-243		78	GND	-5832.5	-243		120	D25	-2262.5	-243
37	TP	-9317.5	-243		79	SHIELDING	-5747.5	-243		121	D24	-2177.5	-243
38	SHIELDING	-9232.5	-243		80	AVDD	-5662.5	-243		122	DASHD	-2092.5	-243
39	DIMI	-9147.5	-243		81	AVDD	-5577.5	-243		123	D23	-2007.5	-243
40	DIMI	-9062.5	-243		82	AVDD	-5492.5	-243		124	D22	-1922.5	-243
41	NBW	-8977.5	-243		83	AVDD	-5407.5	-243		125	DASHD	-1837.5	-243

126	D21	-1752.5	-243
127	D20	-1667.5	-243
128	DASHD	-1582.5	-243
129	DCLK	-1497.5	-243
130	NINC	-1412.5	-243
131	DASHD	-1327.5	-243
132	VDD_LVDS	-1242.5	-243
133	VDD_LVDS	-1157.5	-243
134	VDD_LVDS	-1072.5	-243
135	VDD_LVDS	-987.5	-243
136	REV	-902.5	-243
137	DASHD	-817.5	-243
138	D17	-732.5	-243
139	D16	-647.5	-243
140	DASHD	-562.5	-243
141	D15	-477.5	-243
142	D14	-392.5	-243
143	DASHD	-307.5	-243
144	D13	-222.5	-243
145	D12	-137.5	-243
146	DASHD	-52.5	-243
147	D11	32.5	-243
148	D10	117.5	-243
149	DASHD	202.5	-243
150	D07	287.5	-243
151	D06	372.5	-243
152	DASHD	457.5	-243
153	D05	542.5	-243
154	D04	627.5	-243
155	DASHD	712.5	-243
156	D03	797.5	-243
157	D02	882.5	-243
158	DASHD	967.5	-243
159	D01	1052.5	-243
160	D00	1137.5	-243
161	DASHD	1222.5	-243
162	SHIELDING	1307.5	-243
163	GAML	1392.5	-243
164	GAML	1477.5	-243
165	V8	1562.5	-243
166	V8	1647.5	-243
167	V9	1732.5	-243
168	V9	1817.5	-243
169	V10	1902.5	-243
170	V10	1987.5	-243
171	V11	2072.5	-243
172	V11	2157.5	-243
173	V12	2242.5	-243
174	V12	2327.5	-243
175	V13	2412.5	-243
176	V13	2497.5	-243
177	V14	2582.5	-243
178	V14	2667.5	-243
179	SHIELDING	2752.5	-243
180	AGND	2837.5	-243
181	AGND	2922.5	-243
182	AGND	3007.5	-243
183	AGND	3092.5	-243
184	SHIELDING	3177.5	-243
185	AVDD	3262.5	-243
186	AVDD	3347.5	-243
187	AVDD	3432.5	-243
188	AVDD	3517.5	-243
189	SHIELDING	3602.5	-243
190	GND	3687.5	-243
191	GND	3772.5	-243
192	GND	3857.5	-243
193	GND	3942.5	-243
194	SHIELDING	4027.5	-243
195	VDD	4112.5	-243
196	VDD	4197.5	-243
197	VDD	4282.5	-243
198	VDD	4367.5	-243
199	SHIELDING	4452.5	-243
200	DUAL	4537.5	-243
201	DUAL	4622.5	-243
202	MASL	4707.5	-243
203	MASL	4792.5	-243
204	MASLOC	4877.5	-243
205	MASLOC	4962.5	-243
206	CABC_EN[0]	5047.5	-243
207	CABC_EN[0]	5132.5	-243
208	CABC_EN[1]	5217.5	-243
209	CABC_EN[1]	5302.5	-243
210	OPDRV	5387.5	-243
211	OPDRV	5472.5	-243
212	MODE	5557.5	-243
213	MODE	5642.5	-243
214	IFSEL	5727.5	-243
215	IFSEL	5812.5	-243
216	BIST	5897.5	-243
217	BIST	5982.5	-243
218	RES[0]	6067.5	-243
219	RES[0]	6152.5	-243
220	RES[1]	6237.5	-243
221	RES[1]	6322.5	-243
222	DCLKPOL	6407.5	-243
223	DCLKPOL	6492.5	-243
224	STBYB	6577.5	-243
225	STBYB	6662.5	-243
226	GRB	6747.5	-243
227	GRB	6832.5	-243
228	SHLR	6917.5	-243
229	SHLR	7002.5	-243
230	UPDN	7087.5	-243
231	UPDN	7172.5	-243
232	SHIELDING	7257.5	-243
233	TP	7342.5	-243
234	TP	7427.5	-243
235	TP	7512.5	-243
236	TP	7597.5	-243
237	TP	7682.5	-243
238	TP	7767.5	-243
239	TP	7852.5	-243
240	TP	7937.5	-243
241	TP	8022.5	-243
242	TP	8107.5	-243
243	TP	8192.5	-243
244	TP	8277.5	-243
245	TP	8362.5	-243
246	TP	8447.5	-243
247	SHIELDING	8532.5	-243
248	VDD	8617.5	-243
249	VDD	8702.5	-243
250	VDD	8787.5	-243
251	VDD	8872.5	-243
252	SHIELDING	8957.5	-243
253	GND	9042.5	-243
254	GND	9127.5	-243
255	GND	9212.5	-243
256	GND	9297.5	-243
257	SHIELDING	9382.5	-243
258	AVDD	9467.5	-243
259	AVDD	9552.5	-243
260	AVDD	9637.5	-243
261	AVDD	9722.5	-243
262	SHIELDING	9807.5	-243
263	AGND	9892.5	-243
264	AGND	9977.5	-243
265	AGND	10062.5	-243
266	AGND	10147.5	-243
267	SHIELDING	10232.5	-243
268	TP	10317.5	-243
269	VCOMI	10402.5	-243
270	VCOMI	10487.5	-243
271	PWR_EN	10572.5	-243
272	PWR_EN	10657.5	-243
273	FBL	10742.5	-243
274	FBL	10827.5	-243
275	FBH	10912.5	-243
276	FBH	10997.5	-243
277	FBA	11082.5	-243
278	FBA	11167.5	-243
279	AVDDG	11252.5	-243
280	AVDDG	11337.5	-243
281	DRVA	11422.5	-243
282	DRVA	11507.5	-243
283	DRVH	11592.5	-243
284	DRVH	11677.5	-243
285	DRVL	11762.5	-243
286	DRVL	11847.5	-243
287	DRVL_B	11932.5	-243
288	DRVL_B	12017.5	-243
289	VCOMO	12102.5	-243
290	VCOMO	12187.5	-243
291	COM2_IN	12272.5	-243
292	COM2_IN	12357.5	-243
293	STBNL	12303.0	-82
294	F_CtrlL	12403.0	-42
295	STV2L	12303.0	-2
296	STV1L	12403.0	38
297	CKVL	12303.0	78
298	UDL	12403.0	118
299	SYNC2L	12303.0	158
300	SYNC1L	12403.0	198
301	OEVL	12303.0	238
302	F_CtrlL	12403.0	278
303	SHIELDING	12205.0	258
304	COM2_OUT	12155.0	258
305	COM2_OUT	12105.0	258
306	SHIELDING	12055.0	258
307	SO1	12012.5	113
308	SO2	11997.5	243
309	SO3	11982.5	113
310	SO4	11967.5	243
311	SO5	11952.5	113
312	SO6	11937.5	243
313	SO7	11922.5	113
314	SO8	11907.5	243
315	SO9	11892.5	113
316	SO10	11877.5	243
317	SO11	11862.5	113
318	SO12	11847.5	243
319	SO13	11832.5	113
320	SO14	11817.5	243
321	SO15	11802.5	113
322	SO16	11787.5	243
323	SO17	11772.5	113

324	SO18	11757.5	243
325	SO19	11742.5	113
326	SO20	11727.5	243
327	SO21	11712.5	113
328	SO22	11697.5	243
329	SO23	11682.5	113
330	SO24	11667.5	243
331	SO25	11652.5	113
332	SO26	11637.5	243
333	SO27	11622.5	113
334	SO28	11607.5	243
335	SO29	11592.5	113
336	SO30	11577.5	243
337	SO31	11562.5	113
338	SO32	11547.5	243
339	SO33	11532.5	113
340	SO34	11517.5	243
341	SO35	11502.5	113
342	SO36	11487.5	243
343	SO37	11472.5	113
344	SO38	11457.5	243
345	SO39	11442.5	113
346	SO40	11427.5	243
347	SO41	11412.5	113
348	SO42	11397.5	243
349	SO43	11382.5	113
350	SO44	11367.5	243
351	SO45	11352.5	113
352	SO46	11337.5	243
353	SO47	11322.5	113
354	SO48	11307.5	243
355	SO49	11292.5	113
356	SO50	11277.5	243
357	SO51	11262.5	113
358	SO52	11247.5	243
359	SO53	11232.5	113
360	SO54	11217.5	243
361	SO55	11202.5	113
362	SO56	11187.5	243
363	SO57	11172.5	113
364	SO58	11157.5	243
365	SO59	11142.5	113
366	SO60	11127.5	243
367	SO61	11112.5	113
368	SO62	11097.5	243
369	SO63	11082.5	113
370	SO64	11067.5	243
371	SO65	11052.5	113
372	SO66	11037.5	243
373	SO67	11022.5	113
374	SO68	11007.5	243
375	SO69	10992.5	113
376	SO70	10977.5	243
377	SO71	10962.5	113
378	SO72	10947.5	243
379	SO73	10932.5	113
380	SO74	10917.5	243
381	SO75	10902.5	113
382	SO76	10887.5	243
383	SO77	10872.5	113
384	SO78	10857.5	243
385	SO79	10842.5	113
386	SO80	10827.5	243
387	SO81	10812.5	113
388	SO82	10797.5	243
389	SO83	10782.5	113
390	SO84	10767.5	243
391	SO85	10752.5	113
392	SO86	10737.5	243
393	SO87	10722.5	113
394	SO88	10707.5	243
395	SO89	10692.5	113
396	SO90	10677.5	243
397	SO91	10662.5	113
398	SO92	10647.5	243
399	SO93	10632.5	113
400	SO94	10617.5	243
401	SO95	10602.5	113
402	SO96	10587.5	243
403	SO97	10572.5	113
404	SO98	10557.5	243
405	SO99	10542.5	113
406	SO100	10527.5	243
407	SO101	10512.5	113
408	SO102	10497.5	243
409	SO103	10482.5	113
410	SO104	10467.5	243
411	SO105	10452.5	113
412	SO106	10437.5	243
413	SO107	10422.5	113
414	SO108	10407.5	243
415	SO109	10392.5	113
416	SO110	10377.5	243
417	SO111	10362.5	113
418	SO112	10347.5	243
419	SO113	10332.5	113
420	SO114	10317.5	243
421	SO115	10302.5	113
422	SO116	10287.5	243
423	SO117	10272.5	113
424	SO118	10257.5	243
425	SO119	10242.5	113
426	SO120	10227.5	243
427	SO121	10212.5	113
428	SO122	10197.5	243
429	SO123	10182.5	113
430	SO124	10167.5	243
431	SO125	10152.5	113
432	SO126	10137.5	243
433	SO127	10122.5	113
434	SO128	10107.5	243
435	SO129	10092.5	113
436	SO130	10077.5	243
437	SO131	10062.5	113
438	SO132	10047.5	243
439	SO133	10032.5	113
440	SO134	10017.5	243
441	SO135	10002.5	113
442	SO136	9987.5	243
443	SO137	9972.5	113
444	SO138	9957.5	243
445	SO139	9942.5	113
446	SO140	9927.5	243
447	SO141	9912.5	113
448	SO142	9897.5	243
449	SO143	9882.5	113
450	SO144	9867.5	243
451	SO145	9852.5	113
452	SO146	9837.5	243
453	SO147	9822.5	113
454	SO148	9807.5	243
455	SO149	9792.5	113
456	SO150	9777.5	243
457	SO151	9762.5	113
458	SO152	9747.5	243
459	SO153	9732.5	113
460	SO154	9717.5	243
461	SO155	9702.5	113
462	SO156	9687.5	243
463	SO157	9672.5	113
464	SO158	9657.5	243
465	SO159	9642.5	113
466	SO160	9627.5	243
467	SO161	9612.5	113
468	SO162	9597.5	243
469	SO163	9582.5	113
470	SO164	9567.5	243
471	SO165	9552.5	113
472	SO166	9537.5	243
473	SO167	9522.5	113
474	SO168	9507.5	243
475	SO169	9492.5	113
476	SO170	9477.5	243
477	SO171	9462.5	113
478	SO172	9447.5	243
479	SO173	9432.5	113
480	SO174	9417.5	243
481	SO175	9402.5	113
482	SO176	9387.5	243
483	SO177	9372.5	113
484	SO178	9357.5	243
485	SO179	9342.5	113
486	SO180	9327.5	243
487	SO181	9312.5	113
488	SO182	9297.5	243
489	SO183	9282.5	113
490	SO184	9267.5	243
491	SO185	9252.5	113
492	SO186	9237.5	243
493	SO187	9222.5	113
494	SO188	9207.5	243
495	SO189	9192.5	113
496	SO190	9177.5	243
497	SO191	9162.5	113
498	SO192	9147.5	243
499	SO193	9132.5	113
500	SO194	9117.5	243
501	SO195	9102.5	113
502	SO196	9087.5	243
503	SO197	9072.5	113
504	SO198	9057.5	243
505	SO199	9042.5	113
506	SO200	9027.5	243
507	SO201	9012.5	113
508	SO202	8997.5	243
509	SO203	8982.5	113
510	SO204	8967.5	243
511	SO205	8952.5	113
512	SO206	8937.5	243
513	SO207	8922.5	113
514	SO208	8907.5	243
515	SO209	8892.5	113
516	SO210	8877.5	243
517	SO211	8862.5	113
518	SO212	8847.5	243
519	SO213	8832.5	113
520	SO214	8817.5	243
521	SO215	8802.5	113

522	SO216	8787.5	243
523	SO217	8772.5	113
524	SO218	8757.5	243
525	SO219	8742.5	113
526	SO220	8727.5	243
527	SO221	8712.5	113
528	SO222	8697.5	243
529	SO223	8682.5	113
530	SO224	8667.5	243
531	SO225	8652.5	113
532	SO226	8637.5	243
533	SO227	8622.5	113
534	SO228	8607.5	243
535	SO229	8592.5	113
536	SO230	8577.5	243
537	SO231	8562.5	113
538	SO232	8547.5	243
539	SO233	8532.5	113
540	SO234	8517.5	243
541	SO235	8502.5	113
542	SO236	8487.5	243
543	SO237	8472.5	113
544	SO238	8457.5	243
545	SO239	8442.5	113
546	SO240	8427.5	243
547	SO241	8412.5	113
548	SO242	8397.5	243
549	SO243	8382.5	113
550	SO244	8367.5	243
551	SO245	8352.5	113
552	SO246	8337.5	243
553	SO247	8322.5	113
554	SO248	8307.5	243
555	SO249	8292.5	113
556	SO250	8277.5	243
557	SO251	8262.5	113
558	SO252	8247.5	243
559	SO253	8232.5	113
560	SO254	8217.5	243
561	SO255	8202.5	113
562	SO256	8187.5	243
563	SO257	8172.5	113
564	SO258	8157.5	243
565	SO259	8142.5	113
566	SO260	8127.5	243
567	SO261	8112.5	113
568	SO262	8097.5	243
569	SO263	8082.5	113
570	SO264	8067.5	243
571	SO265	8052.5	113
572	SO266	8037.5	243
573	SO267	8022.5	113
574	SO268	8007.5	243
575	SO269	7992.5	113
576	SO270	7977.5	243
577	SO271	7962.5	113
578	SO272	7947.5	243
579	SO273	7932.5	113
580	SO274	7917.5	243
581	SO275	7902.5	113
582	SO276	7887.5	243
583	SO277	7872.5	113
584	SO278	7857.5	243
585	SO279	7842.5	113
586	SO280	7827.5	243
587	SO281	7812.5	113
588	SO282	7797.5	243
589	SO283	7782.5	113
590	SO284	7767.5	243
591	SO285	7752.5	113
592	SO286	7737.5	243
593	SO287	7722.5	113
594	SO288	7707.5	243
595	SO289	7692.5	113
596	SO290	7677.5	243
597	SO291	7662.5	113
598	SO292	7647.5	243
599	SO293	7632.5	113
600	SO294	7617.5	243
601	SO295	7602.5	113
602	SO296	7587.5	243
603	SO297	7572.5	113
604	SO298	7557.5	243
605	SO299	7542.5	113
606	SO300	7527.5	243
607	SO301	7512.5	113
608	SO302	7497.5	243
609	SO303	7482.5	113
610	SO304	7467.5	243
611	SO305	7452.5	113
612	SO306	7437.5	243
613	SO307	7422.5	113
614	SO308	7407.5	243
615	SO309	7392.5	113
616	SO310	7377.5	243
617	SO311	7362.5	113
618	SO312	7347.5	243
619	SO313	7332.5	113
620	SO314	7317.5	243
621	SO315	7302.5	113
622	SO316	7287.5	243
623	SO317	7272.5	113
624	SO318	7257.5	243
625	SO319	7242.5	113
626	SO320	7227.5	243
627	SO321	7212.5	113
628	SO322	7197.5	243
629	SO323	7182.5	113
630	SO324	7167.5	243
631	SO325	7152.5	113
632	SO326	7137.5	243
633	SO327	7122.5	113
634	SO328	7107.5	243
635	SO329	7092.5	113
636	SO330	7077.5	243
637	SO331	7062.5	113
638	SO332	7047.5	243
639	SO333	7032.5	113
640	SO334	7017.5	243
641	SO335	7002.5	113
642	SO336	6987.5	243
643	SO337	6972.5	113
644	SO338	6957.5	243
645	SO339	6942.5	113
646	SO340	6927.5	243
647	SO341	6912.5	113
648	SO342	6897.5	243
649	SO343	6882.5	113
650	SO344	6867.5	243
651	SO345	6852.5	113
652	SO346	6837.5	243
653	SO347	6822.5	113
654	SO348	6807.5	243
655	SO349	6792.5	113
656	SO350	6777.5	243
657	SO351	6762.5	113
658	SO352	6747.5	243
659	SO353	6732.5	113
660	SO354	6717.5	243
661	SO355	6702.5	113
662	SO356	6687.5	243
663	SO357	6672.5	113
664	SO358	6657.5	243
665	SO359	6642.5	113
666	SO360	6627.5	243
667	SO361	6612.5	113
668	SO362	6597.5	243
669	SO363	6582.5	113
670	SO364	6567.5	243
671	SO365	6552.5	113
672	SO366	6537.5	243
673	SO367	6522.5	113
674	SO368	6507.5	243
675	SO369	6492.5	113
676	SO370	6477.5	243
677	SO371	6462.5	113
678	SO372	6447.5	243
679	SO373	6432.5	113
680	SO374	6417.5	243
681	SO375	6402.5	113
682	SO376	6387.5	243
683	SO377	6372.5	113
684	SO378	6357.5	243
685	SO379	6342.5	113
686	SO380	6327.5	243
687	SO381	6312.5	113
688	SO382	6297.5	243
689	SO383	6282.5	113
690	SO384	6267.5	243
691	SO385	6252.5	113
692	SO386	6237.5	243
693	SO387	6222.5	113
694	SO388	6207.5	243
695	SO389	6192.5	113
696	SO390	6177.5	243
697	SO391	6162.5	113
698	SO392	6147.5	243
699	SO393	6132.5	113
700	SO394	6117.5	243
701	SO395	6102.5	113
702	SO396	6087.5	243
703	SO397	6072.5	113
704	SO398	6057.5	243
705	SO399	6042.5	113
706	SO400	6027.5	243
707	SO401	6012.5	113
708	SO402	5997.5	243
709	SO403	5982.5	113
710	SO404	5967.5	243
711	SO405	5952.5	113
712	SO406	5937.5	243
713	SO407	5922.5	113
714	SO408	5907.5	243
715	SO409	5892.5	113
716	SO410	5877.5	243
717	SO411	5862.5	113
718	SO412	5847.5	243
719	SO413	5832.5	113

720	SO414	5817.5	243
721	SO415	5802.5	113
722	SO416	5787.5	243
723	SO417	5772.5	113
724	SO418	5757.5	243
725	SO419	5742.5	113
726	SO420	5727.5	243
727	SO421	5712.5	113
728	SO422	5697.5	243
729	SO423	5682.5	113
730	SO424	5667.5	243
731	SO425	5652.5	113
732	SO426	5637.5	243
733	SO427	5622.5	113
734	SO428	5607.5	243
735	SO429	5592.5	113
736	SO430	5577.5	243
737	SO431	5562.5	113
738	SO432	5547.5	243
739	SO433	5532.5	113
740	SO434	5517.5	243
741	SO435	5502.5	113
742	SO436	5487.5	243
743	SO437	5472.5	113
744	SO438	5457.5	243
745	SO439	5442.5	113
746	SO440	5427.5	243
747	SO441	5412.5	113
748	SO442	5397.5	243
749	SO443	5382.5	113
750	SO444	5367.5	243
751	SO445	5352.5	113
752	SO446	5337.5	243
753	SO447	5322.5	113
754	SO448	5307.5	243
755	SO449	5292.5	113
756	SO450	5277.5	243
757	SO451	5262.5	113
758	SO452	5247.5	243
759	SO453	5232.5	113
760	SO454	5217.5	243
761	SO455	5202.5	113
762	SO456	5187.5	243
763	SO457	5172.5	113
764	SO458	5157.5	243
765	SO459	5142.5	113
766	SO460	5127.5	243
767	SO461	5112.5	113
768	SO462	5097.5	243
769	SO463	5082.5	113
770	SO464	5067.5	243
771	SO465	5052.5	113
772	SO466	5037.5	243
773	SO467	5022.5	113
774	SO468	5007.5	243
775	SO469	4992.5	113
776	SO470	4977.5	243
777	SO471	4962.5	113
778	SO472	4947.5	243
779	SO473	4932.5	113
780	SO474	4917.5	243
781	SO475	4902.5	113
782	SO476	4887.5	243
783	SO477	4872.5	113
784	SO478	4857.5	243
785	SO479	4842.5	113
786	SO480	4827.5	243
787	SO481	4812.5	113
788	SO482	4797.5	243
789	SO483	4782.5	113
790	SO484	4767.5	243
791	SO485	4752.5	113
792	SO486	4737.5	243
793	SO487	4722.5	113
794	SO488	4707.5	243
795	SO489	4692.5	113
796	SO490	4677.5	243
797	SO491	4662.5	113
798	SO492	4647.5	243
799	SO493	4632.5	113
800	SO494	4617.5	243
801	SO495	4602.5	113
802	SO496	4587.5	243
803	SO497	4572.5	113
804	SO498	4557.5	243
805	SO499	4542.5	113
806	SO500	4527.5	243
807	SO501	4512.5	113
808	SO502	4497.5	243
809	SO503	4482.5	113
810	SO504	4467.5	243
811	SO505	4452.5	113
812	SO506	4437.5	243
813	SO507	4422.5	113
814	SO508	4407.5	243
815	SO509	4392.5	113
816	SO510	4377.5	243
817	SO511	4362.5	113
818	SO512	4347.5	243
819	SO513	4332.5	113
820	SO514	4317.5	243
821	SO515	4302.5	113
822	SO516	4287.5	243
823	SO517	4272.5	113
824	SO518	4257.5	243
825	SO519	4242.5	113
826	SO520	4227.5	243
827	SO521	4212.5	113
828	SO522	4197.5	243
829	SO523	4182.5	113
830	SO524	4167.5	243
831	SO525	4152.5	113
832	SO526	4137.5	243
833	SO527	4122.5	113
834	SO528	4107.5	243
835	SO529	4092.5	113
836	SO530	4077.5	243
837	SO531	4062.5	113
838	SO532	4047.5	243
839	SO533	4032.5	113
840	SO534	4017.5	243
841	SO535	4002.5	113
842	SO536	3987.5	243
843	SO537	3972.5	113
844	SO538	3957.5	243
845	SO539	3942.5	113
846	SO540	3927.5	243
847	SO541	3912.5	113
848	SO542	3897.5	243
849	SO543	3882.5	113
850	SO544	3867.5	243
851	SO545	3852.5	113
852	SO546	3837.5	243
853	SO547	3822.5	113
854	SO548	3807.5	243
855	SO549	3792.5	113
856	SO550	3777.5	243
857	SO551	3762.5	113
858	SO552	3747.5	243
859	SO553	3732.5	113
860	SO554	3717.5	243
861	SO555	3702.5	113
862	SO556	3687.5	243
863	SO557	3672.5	113
864	SO558	3657.5	243
865	SO559	3642.5	113
866	SO560	3627.5	243
867	SO561	3612.5	113
868	SO562	3597.5	243
869	SO563	3582.5	113
870	SO564	3567.5	243
871	SO565	3552.5	113
872	SO566	3537.5	243
873	SO567	3522.5	113
874	SO568	3507.5	243
875	SO569	3492.5	113
876	SO570	3477.5	243
877	SO571	3462.5	113
878	SO572	3447.5	243
879	SO573	3432.5	113
880	SO574	3417.5	243
881	SO575	3402.5	113
882	SO576	3387.5	243
883	SO577	3372.5	113
884	SO578	3357.5	243
885	SO579	3342.5	113
886	SO580	3327.5	243
887	SO581	3312.5	113
888	SO582	3297.5	243
889	SO583	3282.5	113
890	SO584	3267.5	243
891	SO585	3252.5	113
892	SO586	3237.5	243
893	SO587	3222.5	113
894	SO588	3207.5	243
895	SO589	3192.5	113
896	SO590	3177.5	243
897	SO591	3162.5	113
898	SO592	3147.5	243
899	SO593	3132.5	113
900	SO594	3117.5	243
901	SO595	3102.5	113
902	SO596	3087.5	243
903	SO597	3072.5	113
904	SO598	3057.5	243
905	SO599	3042.5	113
906	SO600	3027.5	243
907	SO601	3012.5	113
908	SO602	2997.5	243
909	SO603	2982.5	113
910	SO604	2967.5	243
911	SO605	2952.5	113
912	SO606	2937.5	243
913	SO607	2922.5	113
914	SO608	2907.5	243
915	SO609	2892.5	113
916	SO610	2877.5	243
917	SO611	2862.5	113

918	SO612	2847.5	243
919	SO613	2832.5	113
920	SO614	2817.5	243
921	SO615	2802.5	113
922	SO616	2787.5	243
923	SO617	2772.5	113
924	SO618	2757.5	243
925	SO619	2742.5	113
926	SO620	2727.5	243
927	SO621	2712.5	113
928	SO622	2697.5	243
929	SO623	2682.5	113
930	SO624	2667.5	243
931	SO625	2652.5	113
932	SO626	2637.5	243
933	SO627	2622.5	113
934	SO628	2607.5	243
935	SO629	2592.5	113
936	SO630	2577.5	243
937	SO631	2562.5	113
938	SO632	2547.5	243
939	SO633	2532.5	113
940	SO634	2517.5	243
941	SO635	2502.5	113
942	SO636	2487.5	243
943	SO637	2472.5	113
944	SO638	2457.5	243
945	SO639	2442.5	113
946	SO640	2427.5	243
947	SO641	2412.5	113
948	SO642	2397.5	243
949	SO643	2382.5	113
950	SO644	2367.5	243
951	SO645	2352.5	113
952	SO646	2337.5	243
953	SO647	2322.5	113
954	SO648	2307.5	243
955	SO649	2292.5	113
956	SO650	2277.5	243
957	SO651	2262.5	113
958	SO652	2247.5	243
959	SO653	2232.5	113
960	SO654	2217.5	243
961	SO655	2202.5	113
962	SO656	2187.5	243
963	SO657	2172.5	113
964	SO658	2157.5	243
965	SO659	2142.5	113
966	SO660	2127.5	243
967	SO661	2112.5	113
968	SO662	2097.5	243
969	SO663	2082.5	113
970	SO664	2067.5	243
971	SO665	2052.5	113
972	SO666	2037.5	243
973	SO667	2022.5	113
974	SO668	2007.5	243
975	SO669	1992.5	113
976	SO670	1977.5	243
977	SO671	1962.5	113
978	SO672	1947.5	243
979	SO673	1932.5	113
980	SO674	1917.5	243
981	SO675	1902.5	113
982	SO676	1887.5	243
983	SO677	1872.5	113
984	SO678	1857.5	243
985	SO679	1842.5	113
986	SO680	1827.5	243
987	SO681	1812.5	113
988	SO682	1797.5	243
989	SO683	1782.5	113
990	SO684	1767.5	243
991	SO685	1752.5	113
992	SO686	1737.5	243
993	SO687	1722.5	113
994	SO688	1707.5	243
995	SO689	1692.5	113
996	SO690	1677.5	243
997	SO691	1662.5	113
998	SO692	1647.5	243
999	SO693	1632.5	113
1000	SO694	1617.5	243
1001	SO695	1602.5	113
1002	SO696	1587.5	243
1003	SO697	1572.5	113
1004	SO698	1557.5	243
1005	SO699	1542.5	113
1006	SO700	1527.5	243
1007	SO701	1512.5	113
1008	SO702	1497.5	243
1009	SO703	1482.5	113
1010	SO704	1467.5	243
1011	SO705	1452.5	113
1012	SO706	1437.5	243
1013	SO707	1422.5	113
1014	SO708	1407.5	243
1015	SO709	1392.5	113
1016	SO710	1377.5	243
1017	SO711	1362.5	113
1018	SO712	1347.5	243
1019	SO713	1332.5	113
1020	SO714	1317.5	243
1021	SO715	1302.5	113
1022	SO716	1287.5	243
1023	SO717	1272.5	113
1024	SO718	1257.5	243
1025	SO719	1242.5	113
1026	SO720	1227.5	243
1027	SO721	1212.5	113
1028	SO722	1197.5	243
1029	SO723	1182.5	113
1030	SO724	1167.5	243
1031	SO725	1152.5	113
1032	SO726	1137.5	243
1033	SO727	1122.5	113
1034	SO728	1107.5	243
1035	SO729	1092.5	113
1036	SO730	1077.5	243
1037	SO731	1062.5	113
1038	SO732	1047.5	243
1039	SO733	1032.5	113
1040	SO734	1017.5	243
1041	SO735	1002.5	113
1042	SO736	987.5	243
1043	SO737	972.5	113
1044	SO738	957.5	243
1045	SO739	942.5	113
1046	SO740	927.5	243
1047	SO741	912.5	113
1048	SO742	897.5	243
1049	SO743	882.5	113
1050	SO744	867.5	243
1051	SO745	852.5	113
1052	SO746	837.5	243
1053	SO747	822.5	113
1054	SO748	807.5	243
1055	SO749	792.5	113
1056	SO750	777.5	243
1057	SO751	762.5	113
1058	SO752	747.5	243
1059	SO753	732.5	113
1060	SO754	717.5	243
1061	SO755	702.5	113
1062	SO756	687.5	243
1063	SO757	672.5	113
1064	SO758	657.5	243
1065	SO759	642.5	113
1066	SO760	627.5	243
1067	SO761	612.5	113
1068	SO762	597.5	243
1069	SO763	582.5	113
1070	SO764	567.5	243
1071	SO765	552.5	113
1072	SO766	537.5	243
1073	SO767	522.5	113
1074	SO768	507.5	243
1075	SHIELDING	455.0	258
1076	SHIELDING	405.0	258
1077	SHIELDING	355.0	258
1078	SHIELDING	50.0	258
1079	SHIELDING	0.0	258
1080	SHIELDING	-50.0	258
1081	SHIELDING	-355.0	258
1082	SHIELDING	-405.0	258
1083	SHIELDING	-455.0	258
1084	SO769	-507.5	243
1085	SO770	-522.5	113
1086	SO771	-537.5	243
1087	SO772	-552.5	113
1088	SO773	-567.5	243
1089	SO774	-582.5	113
1090	SO775	-597.5	243
1091	SO776	-612.5	113
1092	SO777	-627.5	243
1093	SO778	-642.5	113
1094	SO779	-657.5	243
1095	SO780	-672.5	113
1096	SO781	-687.5	243
1097	SO782	-702.5	113
1098	SO783	-717.5	243
1099	SO784	-732.5	113
1100	SO785	-747.5	243
1101	SO786	-762.5	113
1102	SO787	-777.5	243
1103	SO788	-792.5	113
1104	SO789	-807.5	243
1105	SO790	-822.5	113
1106	SO791	-837.5	243
1107	SO792	-852.5	113
1108	SO793	-867.5	243
1109	SO794	-882.5	113
1110	SO795	-897.5	243
1111	SO796	-912.5	113
1112	SO797	-927.5	243
1113	SO798	-942.5	113
1114	SO799	-957.5	243
1115	SO800	-972.5	113

1116	SO801	-987.5	243
1117	SO802	-1002.5	113
1118	SO803	-1017.5	243
1119	SO804	-1032.5	113
1120	SO805	-1047.5	243
1121	SO806	-1062.5	113
1122	SO807	-1077.5	243
1123	SO808	-1092.5	113
1124	SO809	-1107.5	243
1125	SO810	-1122.5	113
1126	SO811	-1137.5	243
1127	SO812	-1152.5	113
1128	SO813	-1167.5	243
1129	SO814	-1182.5	113
1130	SO815	-1197.5	243
1131	SO816	-1212.5	113
1132	SO817	-1227.5	243
1133	SO818	-1242.5	113
1134	SO819	-1257.5	243
1135	SO820	-1272.5	113
1136	SO821	-1287.5	243
1137	SO822	-1302.5	113
1138	SO823	-1317.5	243
1139	SO824	-1332.5	113
1140	SO825	-1347.5	243
1141	SO826	-1362.5	113
1142	SO827	-1377.5	243
1143	SO828	-1392.5	113
1144	SO829	-1407.5	243
1145	SO830	-1422.5	113
1146	SO831	-1437.5	243
1147	SO832	-1452.5	113
1148	SO833	-1467.5	243
1149	SO834	-1482.5	113
1150	SO835	-1497.5	243
1151	SO836	-1512.5	113
1152	SO837	-1527.5	243
1153	SO838	-1542.5	113
1154	SO839	-1557.5	243
1155	SO840	-1572.5	113
1156	SO841	-1587.5	243
1157	SO842	-1602.5	113
1158	SO843	-1617.5	243
1159	SO844	-1632.5	113
1160	SO845	-1647.5	243
1161	SO846	-1662.5	113
1162	SO847	-1677.5	243
1163	SO848	-1692.5	113
1164	SO849	-1707.5	243
1165	SO850	-1722.5	113
1166	SO851	-1737.5	243
1167	SO852	-1752.5	113
1168	SO853	-1767.5	243
1169	SO854	-1782.5	113
1170	SO855	-1797.5	243
1171	SO856	-1812.5	113
1172	SO857	-1827.5	243
1173	SO858	-1842.5	113
1174	SO859	-1857.5	243
1175	SO860	-1872.5	113
1176	SO861	-1887.5	243
1177	SO862	-1902.5	113
1178	SO863	-1917.5	243
1179	SO864	-1932.5	113
1180	SO865	-1947.5	243
1181	SO866	-1962.5	113
1182	SO867	-1977.5	243
1183	SO868	-1992.5	113
1184	SO869	-2007.5	243
1185	SO870	-2022.5	113
1186	SO871	-2037.5	243
1187	SO872	-2052.5	113
1188	SO873	-2067.5	243
1189	SO874	-2082.5	113
1190	SO875	-2097.5	243
1191	SO876	-2112.5	113
1192	SO877	-2127.5	243
1193	SO878	-2142.5	113
1194	SO879	-2157.5	243
1195	SO880	-2172.5	113
1196	SO881	-2187.5	243
1197	SO882	-2202.5	113
1198	SO883	-2217.5	243
1199	SO884	-2232.5	113
1200	SO885	-2247.5	243
1201	SO886	-2262.5	113
1202	SO887	-2277.5	243
1203	SO888	-2292.5	113
1204	SO889	-2307.5	243
1205	SO890	-2322.5	113
1206	SO891	-2337.5	243
1207	SO892	-2352.5	113
1208	SO893	-2367.5	243
1209	SO894	-2382.5	113
1210	SO895	-2397.5	243
1211	SO896	-2412.5	113
1212	SO897	-2427.5	243
1213	SO898	-2442.5	113
1214	SO899	-2457.5	243
1215	SO900	-2472.5	113
1216	SO901	-2487.5	243
1217	SO902	-2502.5	113
1218	SO903	-2517.5	243
1219	SO904	-2532.5	113
1220	SO905	-2547.5	243
1221	SO906	-2562.5	113
1222	SO907	-2577.5	243
1223	SO908	-2592.5	113
1224	SO909	-2607.5	243
1225	SO910	-2622.5	113
1226	SO911	-2637.5	243
1227	SO912	-2652.5	113
1228	SO913	-2667.5	243
1229	SO914	-2682.5	113
1230	SO915	-2697.5	243
1231	SO916	-2712.5	113
1232	SO917	-2727.5	243
1233	SO918	-2742.5	113
1234	SO919	-2757.5	243
1235	SO920	-2772.5	113
1236	SO921	-2787.5	243
1237	SO922	-2802.5	113
1238	SO923	-2817.5	243
1239	SO924	-2832.5	113
1240	SO925	-2847.5	243
1241	SO926	-2862.5	113
1242	SO927	-2877.5	243
1243	SO928	-2892.5	113
1244	SO929	-2907.5	243
1245	SO930	-2922.5	113
1246	SO931	-2937.5	243
1247	SO932	-2952.5	113
1248	SO933	-2967.5	243
1249	SO934	-2982.5	113
1250	SO935	-2997.5	243
1251	SO936	-3012.5	113
1252	SO937	-3027.5	243
1253	SO938	-3042.5	113
1254	SO939	-3057.5	243
1255	SO940	-3072.5	113
1256	SO941	-3087.5	243
1257	SO942	-3102.5	113
1258	SO943	-3117.5	243
1259	SO944	-3132.5	113
1260	SO945	-3147.5	243
1261	SO946	-3162.5	113
1262	SO947	-3177.5	243
1263	SO948	-3192.5	113
1264	SO949	-3207.5	243
1265	SO950	-3222.5	113
1266	SO951	-3237.5	243
1267	SO952	-3252.5	113
1268	SO953	-3267.5	243
1269	SO954	-3282.5	113
1270	SO955	-3297.5	243
1271	SO956	-3312.5	113
1272	SO957	-3327.5	243
1273	SO958	-3342.5	113
1274	SO959	-3357.5	243
1275	SO960	-3372.5	113
1276	SO961	-3387.5	243
1277	SO962	-3402.5	113
1278	SO963	-3417.5	243
1279	SO964	-3432.5	113
1280	SO965	-3447.5	243
1281	SO966	-3462.5	113
1282	SO967	-3477.5	243
1283	SO968	-3492.5	113
1284	SO969	-3507.5	243
1285	SO970	-3522.5	113
1286	SO971	-3537.5	243
1287	SO972	-3552.5	113
1288	SO973	-3567.5	243
1289	SO974	-3582.5	113
1290	SO975	-3597.5	243
1291	SO976	-3612.5	113
1292	SO977	-3627.5	243
1293	SO978	-3642.5	113
1294	SO979	-3657.5	243
1295	SO980	-3672.5	113
1296	SO981	-3687.5	243
1297	SO982	-3702.5	113
1298	SO983	-3717.5	243
1299	SO984	-3732.5	113
1300	SO985	-3747.5	243
1301	SO986	-3762.5	113
1302	SO987	-3777.5	243
1303	SO988	-3792.5	113
1304	SO989	-3807.5	243
1305	SO990	-3822.5	113
1306	SO991	-3837.5	243
1307	SO992	-3852.5	113
1308	SO993	-3867.5	243
1309	SO994	-3882.5	113
1310	SO995	-3897.5	243
1311	SO996	-3912.5	113
1312	SO997	-3927.5	243
1313	SO998	-3942.5	113

1314	SO999	-3957.5	243
1315	SO1000	-3972.5	113
1316	SO1001	-3987.5	243
1317	SO1002	-4002.5	113
1318	SO1003	-4017.5	243
1319	SO1004	-4032.5	113
1320	SO1005	-4047.5	243
1321	SO1006	-4062.5	113
1322	SO1007	-4077.5	243
1323	SO1008	-4092.5	113
1324	SO1009	-4107.5	243
1325	SO1010	-4122.5	113
1326	SO1011	-4137.5	243
1327	SO1012	-4152.5	113
1328	SO1013	-4167.5	243
1329	SO1014	-4182.5	113
1330	SO1015	-4197.5	243
1331	SO1016	-4212.5	113
1332	SO1017	-4227.5	243
1333	SO1018	-4242.5	113
1334	SO1019	-4257.5	243
1335	SO1020	-4272.5	113
1336	SO1021	-4287.5	243
1337	SO1022	-4302.5	113
1338	SO1023	-4317.5	243
1339	SO1024	-4332.5	113
1340	SO1025	-4347.5	243
1341	SO1026	-4362.5	113
1342	SO1027	-4377.5	243
1343	SO1028	-4392.5	113
1344	SO1029	-4407.5	243
1345	SO1030	-4422.5	113
1346	SO1031	-4437.5	243
1347	SO1032	-4452.5	113
1348	SO1033	-4467.5	243
1349	SO1034	-4482.5	113
1350	SO1035	-4497.5	243
1351	SO1036	-4512.5	113
1352	SO1037	-4527.5	243
1353	SO1038	-4542.5	113
1354	SO1039	-4557.5	243
1355	SO1040	-4572.5	113
1356	SO1041	-4587.5	243
1357	SO1042	-4602.5	113
1358	SO1043	-4617.5	243
1359	SO1044	-4632.5	113
1360	SO1045	-4647.5	243
1361	SO1046	-4662.5	113
1362	SO1047	-4677.5	243
1363	SO1048	-4692.5	113
1364	SO1049	-4707.5	243
1365	SO1050	-4722.5	113
1366	SO1051	-4737.5	243
1367	SO1052	-4752.5	113
1368	SO1053	-4767.5	243
1369	SO1054	-4782.5	113
1370	SO1055	-4797.5	243
1371	SO1056	-4812.5	113
1372	SO1057	-4827.5	243
1373	SO1058	-4842.5	113
1374	SO1059	-4857.5	243
1375	SO1060	-4872.5	113
1376	SO1061	-4887.5	243
1377	SO1062	-4902.5	113
1378	SO1063	-4917.5	243
1379	SO1064	-4932.5	113
1380	SO1065	-4947.5	243
1381	SO1066	-4962.5	113
1382	SO1067	-4977.5	243
1383	SO1068	-4992.5	113
1384	SO1069	-5007.5	243
1385	SO1070	-5022.5	113
1386	SO1071	-5037.5	243
1387	SO1072	-5052.5	113
1388	SO1073	-5067.5	243
1389	SO1074	-5082.5	113
1390	SO1075	-5097.5	243
1391	SO1076	-5112.5	113
1392	SO1077	-5127.5	243
1393	SO1078	-5142.5	113
1394	SO1079	-5157.5	243
1395	SO1080	-5172.5	113
1396	SO1081	-5187.5	243
1397	SO1082	-5202.5	113
1398	SO1083	-5217.5	243
1399	SO1084	-5232.5	113
1400	SO1085	-5247.5	243
1401	SO1086	-5262.5	113
1402	SO1087	-5277.5	243
1403	SO1088	-5292.5	113
1404	SO1089	-5307.5	243
1405	SO1090	-5322.5	113
1406	SO1091	-5337.5	243
1407	SO1092	-5352.5	113
1408	SO1093	-5367.5	243
1409	SO1094	-5382.5	113
1410	SO1095	-5397.5	243
1411	SO1096	-5412.5	113
1412	SO1097	-5427.5	243
1413	SO1098	-5442.5	113
1414	SO1099	-5457.5	243
1415	SO1100	-5472.5	113
1416	SO1101	-5487.5	243
1417	SO1102	-5502.5	113
1418	SO1103	-5517.5	243
1419	SO1104	-5532.5	113
1420	SO1105	-5547.5	243
1421	SO1106	-5562.5	113
1422	SO1107	-5577.5	243
1423	SO1108	-5592.5	113
1424	SO1109	-5607.5	243
1425	SO1110	-5622.5	113
1426	SO1111	-5637.5	243
1427	SO1112	-5652.5	113
1428	SO1113	-5667.5	243
1429	SO1114	-5682.5	113
1430	SO1115	-5697.5	243
1431	SO1116	-5712.5	113
1432	SO1117	-5727.5	243
1433	SO1118	-5742.5	113
1434	SO1119	-5757.5	243
1435	SO1120	-5772.5	113
1436	SO1121	-5787.5	243
1437	SO1122	-5802.5	113
1438	SO1123	-5817.5	243
1439	SO1124	-5832.5	113
1440	SO1125	-5847.5	243
1441	SO1126	-5862.5	113
1442	SO1127	-5877.5	243
1443	SO1128	-5892.5	113
1444	SO1129	-5907.5	243
1445	SO1130	-5922.5	113
1446	SO1131	-5937.5	243
1447	SO1132	-5952.5	113
1448	SO1133	-5967.5	243
1449	SO1134	-5982.5	113
1450	SO1135	-5997.5	243
1451	SO1136	-6012.5	113
1452	SO1137	-6027.5	243
1453	SO1138	-6042.5	113
1454	SO1139	-6057.5	243
1455	SO1140	-6072.5	113
1456	SO1141	-6087.5	243
1457	SO1142	-6102.5	113
1458	SO1143	-6117.5	243
1459	SO1144	-6132.5	113
1460	SO1145	-6147.5	243
1461	SO1146	-6162.5	113
1462	SO1147	-6177.5	243
1463	SO1148	-6192.5	113
1464	SO1149	-6207.5	243
1465	SO1150	-6222.5	113
1466	SO1151	-6237.5	243
1467	SO1152	-6252.5	113
1468	SO1153	-6267.5	243
1469	SO1154	-6282.5	113
1470	SO1155	-6297.5	243
1471	SO1156	-6312.5	113
1472	SO1157	-6327.5	243
1473	SO1158	-6342.5	113
1474	SO1159	-6357.5	243
1475	SO1160	-6372.5	113
1476	SO1161	-6387.5	243
1477	SO1162	-6402.5	113
1478	SO1163	-6417.5	243
1479	SO1164	-6432.5	113
1480	SO1165	-6447.5	243
1481	SO1166	-6462.5	113
1482	SO1167	-6477.5	243
1483	SO1168	-6492.5	113
1484	SO1169	-6507.5	243
1485	SO1170	-6522.5	113
1486	SO1171	-6537.5	243
1487	SO1172	-6552.5	113
1488	SO1173	-6567.5	243
1489	SO1174	-6582.5	113
1490	SO1175	-6597.5	243
1491	SO1176	-6612.5	113
1492	SO1177	-6627.5	243
1493	SO1178	-6642.5	113
1494	SO1179	-6657.5	243
1495	SO1180	-6672.5	113
1496	SO1181	-6687.5	243
1497	SO1182	-6702.5	113
1498	SO1183	-6717.5	243
1499	SO1184	-6732.5	113
1500	SO1185	-6747.5	243
1501	SO1186	-6762.5	113
1502	SO1187	-6777.5	243
1503	SO1188	-6792.5	113
1504	SO1189	-6807.5	243
1505	SO1190	-6822.5	113
1506	SO1191	-6837.5	243
1507	SO1192	-6852.5	113
1508	SO1193	-6867.5	243
1509	SO1194	-6882.5	113
1510	SO1195	-6897.5	243
1511	SO1196	-6912.5	113

1512	SO1197	-6927.5	243
1513	SO1198	-6942.5	113
1514	SO1199	-6957.5	243
1515	SO1200	-6972.5	113
1516	SO1201	-6987.5	243
1517	SO1202	-7002.5	113
1518	SO1203	-7017.5	243
1519	SO1204	-7032.5	113
1520	SO1205	-7047.5	243
1521	SO1206	-7062.5	113
1522	SO1207	-7077.5	243
1523	SO1208	-7092.5	113
1524	SO1209	-7107.5	243
1525	SO1210	-7122.5	113
1526	SO1211	-7137.5	243
1527	SO1212	-7152.5	113
1528	SO1213	-7167.5	243
1529	SO1214	-7182.5	113
1530	SO1215	-7197.5	243
1531	SO1216	-7212.5	113
1532	SO1217	-7227.5	243
1533	SO1218	-7242.5	113
1534	SO1219	-7257.5	243
1535	SO1220	-7272.5	113
1536	SO1221	-7287.5	243
1537	SO1222	-7302.5	113
1538	SO1223	-7317.5	243
1539	SO1224	-7332.5	113
1540	SO1225	-7347.5	243
1541	SO1226	-7362.5	113
1542	SO1227	-7377.5	243
1543	SO1228	-7392.5	113
1544	SO1229	-7407.5	243
1545	SO1230	-7422.5	113
1546	SO1231	-7437.5	243
1547	SO1232	-7452.5	113
1548	SO1233	-7467.5	243
1549	SO1234	-7482.5	113
1550	SO1235	-7497.5	243
1551	SO1236	-7512.5	113
1552	SO1237	-7527.5	243
1553	SO1238	-7542.5	113
1554	SO1239	-7557.5	243
1555	SO1240	-7572.5	113
1556	SO1241	-7587.5	243
1557	SO1242	-7602.5	113
1558	SO1243	-7617.5	243
1559	SO1244	-7632.5	113
1560	SO1245	-7647.5	243
1561	SO1246	-7662.5	113
1562	SO1247	-7677.5	243
1563	SO1248	-7692.5	113
1564	SO1249	-7707.5	243
1565	SO1250	-7722.5	113
1566	SO1251	-7737.5	243
1567	SO1252	-7752.5	113
1568	SO1253	-7767.5	243
1569	SO1254	-7782.5	113
1570	SO1255	-7797.5	243
1571	SO1256	-7812.5	113
1572	SO1257	-7827.5	243
1573	SO1258	-7842.5	113
1574	SO1259	-7857.5	243
1575	SO1260	-7872.5	113
1576	SO1261	-7887.5	243
1577	SO1262	-7902.5	113
1578	SO1263	-7917.5	243
1579	SO1264	-7932.5	113
1580	SO1265	-7947.5	243
1581	SO1266	-7962.5	113
1582	SO1267	-7977.5	243
1583	SO1268	-7992.5	113
1584	SO1269	-8007.5	243
1585	SO1270	-8022.5	113
1586	SO1271	-8037.5	243
1587	SO1272	-8052.5	113
1588	SO1273	-8067.5	243
1589	SO1274	-8082.5	113
1590	SO1275	-8097.5	243
1591	SO1276	-8112.5	113
1592	SO1277	-8127.5	243
1593	SO1278	-8142.5	113
1594	SO1279	-8157.5	243
1595	SO1280	-8172.5	113
1596	SO1281	-8187.5	243
1597	SO1282	-8202.5	113
1598	SO1283	-8217.5	243
1599	SO1284	-8232.5	113
1600	SO1285	-8247.5	243
1601	SO1286	-8262.5	113
1602	SO1287	-8277.5	243
1603	SO1288	-8292.5	113
1604	SO1289	-8307.5	243
1605	SO1290	-8322.5	113
1606	SO1291	-8337.5	243
1607	SO1292	-8352.5	113
1608	SO1293	-8367.5	243
1609	SO1294	-8382.5	113
1610	SO1295	-8397.5	243
1611	SO1296	-8412.5	113
1612	SO1297	-8427.5	243
1613	SO1298	-8442.5	113
1614	SO1299	-8457.5	243
1615	SO1300	-8472.5	113
1616	SO1301	-8487.5	243
1617	SO1302	-8502.5	113
1618	SO1303	-8517.5	243
1619	SO1304	-8532.5	113
1620	SO1305	-8547.5	243
1621	SO1306	-8562.5	113
1622	SO1307	-8577.5	243
1623	SO1308	-8592.5	113
1624	SO1309	-8607.5	243
1625	SO1310	-8622.5	113
1626	SO1311	-8637.5	243
1627	SO1312	-8652.5	113
1628	SO1313	-8667.5	243
1629	SO1314	-8682.5	113
1630	SO1315	-8697.5	243
1631	SO1316	-8712.5	113
1632	SO1317	-8727.5	243
1633	SO1318	-8742.5	113
1634	SO1319	-8757.5	243
1635	SO1320	-8772.5	113
1636	SO1321	-8787.5	243
1637	SO1322	-8802.5	113
1638	SO1323	-8817.5	243
1639	SO1324	-8832.5	113
1640	SO1325	-8847.5	243
1641	SO1326	-8862.5	113
1642	SO1327	-8877.5	243
1643	SO1328	-8892.5	113
1644	SO1329	-8907.5	243
1645	SO1330	-8922.5	113
1646	SO1331	-8937.5	243
1647	SO1332	-8952.5	113
1648	SO1333	-8967.5	243
1649	SO1334	-8982.5	113
1650	SO1335	-8997.5	243
1651	SO1336	-9012.5	113
1652	SO1337	-9027.5	243
1653	SO1338	-9042.5	113
1654	SO1339	-9057.5	243
1655	SO1340	-9072.5	113
1656	SO1341	-9087.5	243
1657	SO1342	-9102.5	113
1658	SO1343	-9117.5	243
1659	SO1344	-9132.5	113
1660	SO1345	-9147.5	243
1661	SO1346	-9162.5	113
1662	SO1347	-9177.5	243
1663	SO1348	-9192.5	113
1664	SO1349	-9207.5	243
1665	SO1350	-9222.5	113
1666	SO1351	-9237.5	243
1667	SO1352	-9252.5	113
1668	SO1353	-9267.5	243
1669	SO1354	-9282.5	113
1670	SO1355	-9297.5	243
1671	SO1356	-9312.5	113
1672	SO1357	-9327.5	243
1673	SO1358	-9342.5	113
1674	SO1359	-9357.5	243
1675	SO1360	-9372.5	113
1676	SO1361	-9387.5	243
1677	SO1362	-9402.5	113
1678	SO1363	-9417.5	243
1679	SO1364	-9432.5	113
1680	SO1365	-9447.5	243
1681	SO1366	-9462.5	113
1682	SO1367	-9477.5	243
1683	SO1368	-9492.5	113
1684	SO1369	-9507.5	243
1685	SO1370	-9522.5	113
1686	SO1371	-9537.5	243
1687	SO1372	-9552.5	113
1688	SO1373	-9567.5	243
1689	SO1374	-9582.5	113
1690	SO1375	-9597.5	243
1691	SO1376	-9612.5	113
1692	SO1377	-9627.5	243
1693	SO1378	-9642.5	113
1694	SO1379	-9657.5	243
1695	SO1380	-9672.5	113
1696	SO1381	-9687.5	243
1697	SO1382	-9702.5	113
1698	SO1383	-9717.5	243
1699	SO1384	-9732.5	113
1700	SO1385	-9747.5	243
1701	SO1386	-9762.5	113
1702	SO1387	-9777.5	243
1703	SO1388	-9792.5	113
1704	SO1389	-9807.5	243
1705	SO1390	-9822.5	113
1706	SO1391	-9837.5	243
1707	SO1392	-9852.5	113
1708	SO1393	-9867.5	243
1709	SO1394	-9882.5	113

1710	SO1395	-9897.5	243		1765	SO1450	-10722.5	113		1820	SO1505	-11547.5	243
1711	SO1396	-9912.5	113		1766	SO1451	-10737.5	243		1821	SO1506	-11562.5	113
1712	SO1397	-9927.5	243		1767	SO1452	-10752.5	113		1822	SO1507	-11577.5	243
1713	SO1398	-9942.5	113		1768	SO1453	-10767.5	243		1823	SO1508	-11592.5	113
1714	SO1399	-9957.5	243		1769	SO1454	-10782.5	113		1824	SO1509	-11607.5	243
1715	SO1400	-9972.5	113		1770	SO1455	-10797.5	243		1825	SO1510	-11622.5	113
1716	SO1401	-9987.5	243		1771	SO1456	-10812.5	113		1826	SO1511	-11637.5	243
1717	SO1402	-10002.5	113		1772	SO1457	-10827.5	243		1827	SO1512	-11652.5	113
1718	SO1403	-10017.5	243		1773	SO1458	-10842.5	113		1828	SO1513	-11667.5	243
1719	SO1404	-10032.5	113		1774	SO1459	-10857.5	243		1829	SO1514	-11682.5	113
1720	SO1405	-10047.5	243		1775	SO1460	-10872.5	113		1830	SO1515	-11697.5	243
1721	SO1406	-10062.5	113		1776	SO1461	-10887.5	243		1831	SO1516	-11712.5	113
1722	SO1407	-10077.5	243		1777	SO1462	-10902.5	113		1832	SO1517	-11727.5	243
1723	SO1408	-10092.5	113		1778	SO1463	-10917.5	243		1833	SO1518	-11742.5	113
1724	SO1409	-10107.5	243		1779	SO1464	-10932.5	113		1834	SO1519	-11757.5	243
1725	SO1410	-10122.5	113		1780	SO1465	-10947.5	243		1835	SO1520	-11772.5	113
1726	SO1411	-10137.5	243		1781	SO1466	-10962.5	113		1836	SO1521	-11787.5	243
1727	SO1412	-10152.5	113		1782	SO1467	-10977.5	243		1837	SO1522	-11802.5	113
1728	SO1413	-10167.5	243		1783	SO1468	-10992.5	113		1838	SO1523	-11817.5	243
1729	SO1414	-10182.5	113		1784	SO1469	-11007.5	243		1839	SO1524	-11832.5	113
1730	SO1415	-10197.5	243		1785	SO1470	-11022.5	113		1840	SO1525	-11847.5	243
1731	SO1416	-10212.5	113		1786	SO1471	-11037.5	243		1841	SO1526	-11862.5	113
1732	SO1417	-10227.5	243		1787	SO1472	-11052.5	113		1842	SO1527	-11877.5	243
1733	SO1418	-10242.5	113		1788	SO1473	-11067.5	243		1843	SO1528	-11892.5	113
1734	SO1419	-10257.5	243		1789	SO1474	-11082.5	113		1844	SO1529	-11907.5	243
1735	SO1420	-10272.5	113		1790	SO1475	-11097.5	243		1845	SO1530	-11922.5	113
1736	SO1421	-10287.5	243		1791	SO1476	-11112.5	113		1846	SO1531	-11937.5	243
1737	SO1422	-10302.5	113		1792	SO1477	-11127.5	243		1847	SO1532	-11952.5	113
1738	SO1423	-10317.5	243		1793	SO1478	-11142.5	113		1848	SO1533	-11967.5	243
1739	SO1424	-10332.5	113		1794	SO1479	-11157.5	243		1849	SO1534	-11982.5	113
1740	SO1425	-10347.5	243		1795	SO1480	-11172.5	113		1850	SO1535	-11997.5	243
1741	SO1426	-10362.5	113		1796	SO1481	-11187.5	243		1851	SO1536	-12012.5	113
1742	SO1427	-10377.5	243		1797	SO1482	-11202.5	113		1852	SHIELDING	-12055.0	258
1743	SO1428	-10392.5	113		1798	SO1483	-11217.5	243		1853	COM1_OUT	-12105.0	258
1744	SO1429	-10407.5	243		1799	SO1484	-11232.5	113		1854	COM1_OUT	-12155.0	258
1745	SO1430	-10422.5	113		1800	SO1485	-11247.5	243		1855	SHIELDING	-12205.0	258
1746	SO1431	-10437.5	243		1801	SO1486	-11262.5	113		1856	F_CtrlR	-12403.0	278
1747	SO1432	-10452.5	113		1802	SO1487	-11277.5	243		1857	OEVR	-12303.0	238
1748	SO1433	-10467.5	243		1803	SO1488	-11292.5	113		1858	SYNC1R	-12403.0	198
1749	SO1434	-10482.5	113		1804	SO1489	-11307.5	243		1859	SYNC2R	-12303.0	158
1750	SO1435	-10497.5	243		1805	SO1490	-11322.5	113		1860	UDR	-12403.0	118
1751	SO1436	-10512.5	113		1806	SO1491	-11337.5	243		1861	CKVR	-12303.0	78
1752	SO1437	-10527.5	243		1807	SO1492	-11352.5	113		1862	STV2R	-12403.0	38
1753	SO1438	-10542.5	113		1808	SO1493	-11367.5	243		1863	STV1R	-12303.0	-2
1754	SO1439	-10557.5	243		1809	SO1494	-11382.5	113		1864	F_CtrlR	-12403.0	-42
1755	SO1440	-10572.5	113		1810	SO1495	-11397.5	243		1865	STBNR	-12303.0	-82
1756	SO1441	-10587.5	243		1811	SO1496	-11412.5	113			ALIGNMENT_M	-12131.5	115.5
1757	SO1442	-10602.5	113		1812	SO1497	-11427.5	243			ARK_L		
1758	SO1443	-10617.5	243		1813	SO1498	-11442.5	113			ALIGNMENT_M	12131.5	115.5
1759	SO1444	-10632.5	113		1814	SO1499	-11457.5	243			ARK_R		
1760	SO1445	-10647.5	243		1815	SO1500	-11472.5	113					
1761	SO1446	-10662.5	113		1816	SO1501	-11487.5	243					
1762	SO1447	-10677.5	243		1817	SO1502	-11502.5	113					
1763	SO1448	-10692.5	113		1818	SO1503	-11517.5	243					
1764	SO1449	-10707.5	243		1819	SO1504	-11532.5	113					

10. DEFINITIONS

10.1. Data Sheet Status

Preliminary Data Sheet	This data sheet contains preliminary data; supplementary data may be published later.
Data Sheet	This data sheet contains final product specifications.

Contents in the document are subject to change without notice.

10.2. Life Support Application

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. fitipower customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify fitipower for any damages resulting from such improper use or sale.

11. REVISION HISTORY

Reversion	Content	Date
0.1	New Issue.	2010/04/12
0.2	1.Modify SEL[0:1] pin define(p11) 2.Update Gamma table(p18,p19,p20)	2010/06/01
0.3	1.Modify application power circuit(p7) 2.Modify PINCTRL Pin Description(p12) 3.Add R2/R3 register(p16) 4.Modify gamma table(p19,20,21)	2010/08/30
0.4	Modify Dual gate diagram(p5)	2011/03/24
0.5	1.Modify TTL input timing(p23~p27) 2. Modify GRB pin definition and GRB delay time spec(p10,33)	2011/05/27
1.0	Modify external terminal resistor for LVDS IF(p9)	2012/08/23
1.1	1. Modify wiring resistance (p13) 2. Modify chip outline dimensions (p40)	2013/08/28