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DATA SHEET

SEN6A40
68-ROW driver for dot-matrix STN LCD

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1 GENERAL

1.1 Description

The SEN6A40 is a 68-ROW (COMMON) driver for dot-matrix STN LCD. It is desinged to be paired with the SEN6A39 80-COLUMN (SEGMENT) driver.

1.2 Features

- 68-output ROW (COMMON) driver for dot-matrix STN LCD.
- Display duty : up to 1/240.
- Capability of being cascaded in application to expand common number.
- Support 1-bit, bidirectional data shift.
- Output data shift on the falling edge or rising edge of LP input.
- Data shift directioin can be:
  - O1 → O68,
  - O68 →O1, or
  - O1→ O34 and O68 → O35.
- External LCD bias voltage.
- Operating voltage range (control logic): 2.7 ~ 5.5 volts.
- Operating voltage range (LCD-bias high voltage, V_{DD}-V5): 8~ 30 volts.
- Operating temperature range: -20 to +75 °C.
- Storage temperature range: -40 to +125 °C.

1.3 Ordering information

Table 1 Ordering information

TYPE NUMBER	DESCRIPTION
SEN6A40-LQFPG	LQFP100 Green package.
SEN6A40-QFPG	QFP100 Green package.
SEN6A40-LQFP	LQFP100 package.
SEN6A40-QFP	QFP100 package.

2 FUNCTIONAL BLOCK DIAGRAM AND DESCRIPTION

2.1 Funtional block diagram

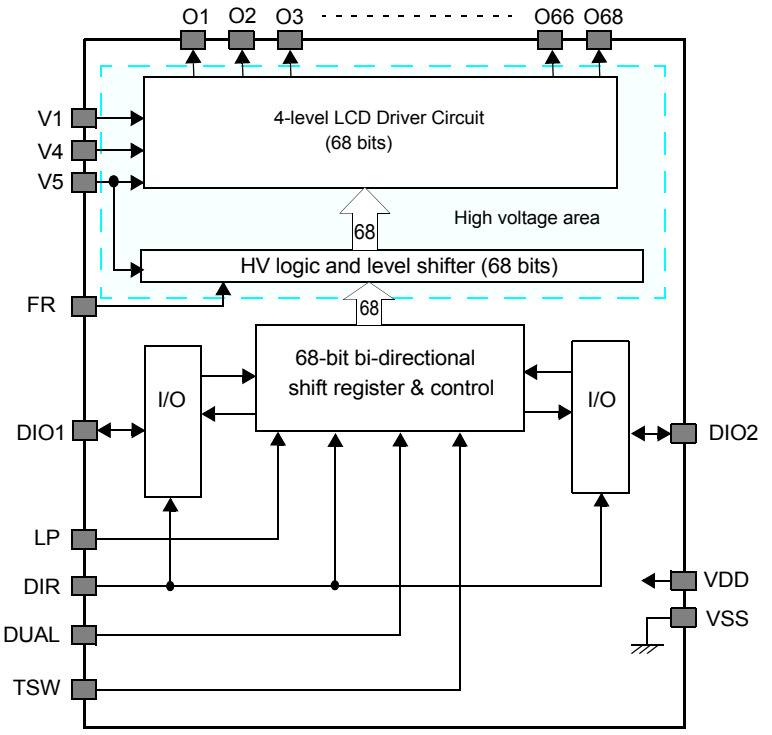


Fig.1 Functional Block Diagram

3 PINNING INFORMATION

3.1 Pinning diagram

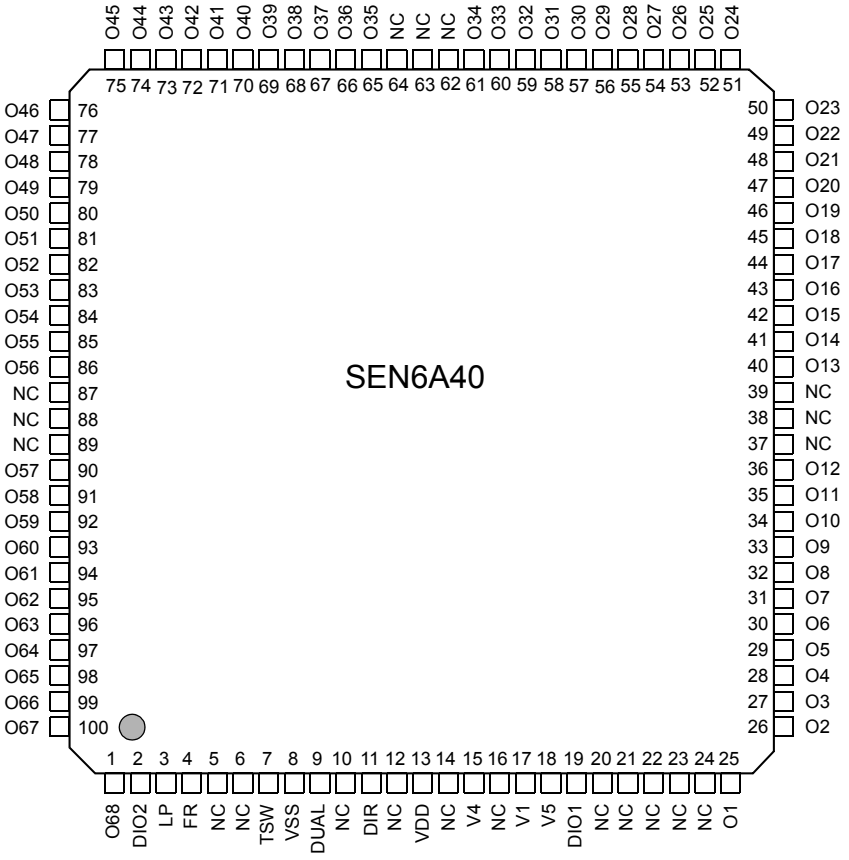


Fig.2 Pin diagram of QFP100/LQFP100 package

3.2 Signal description

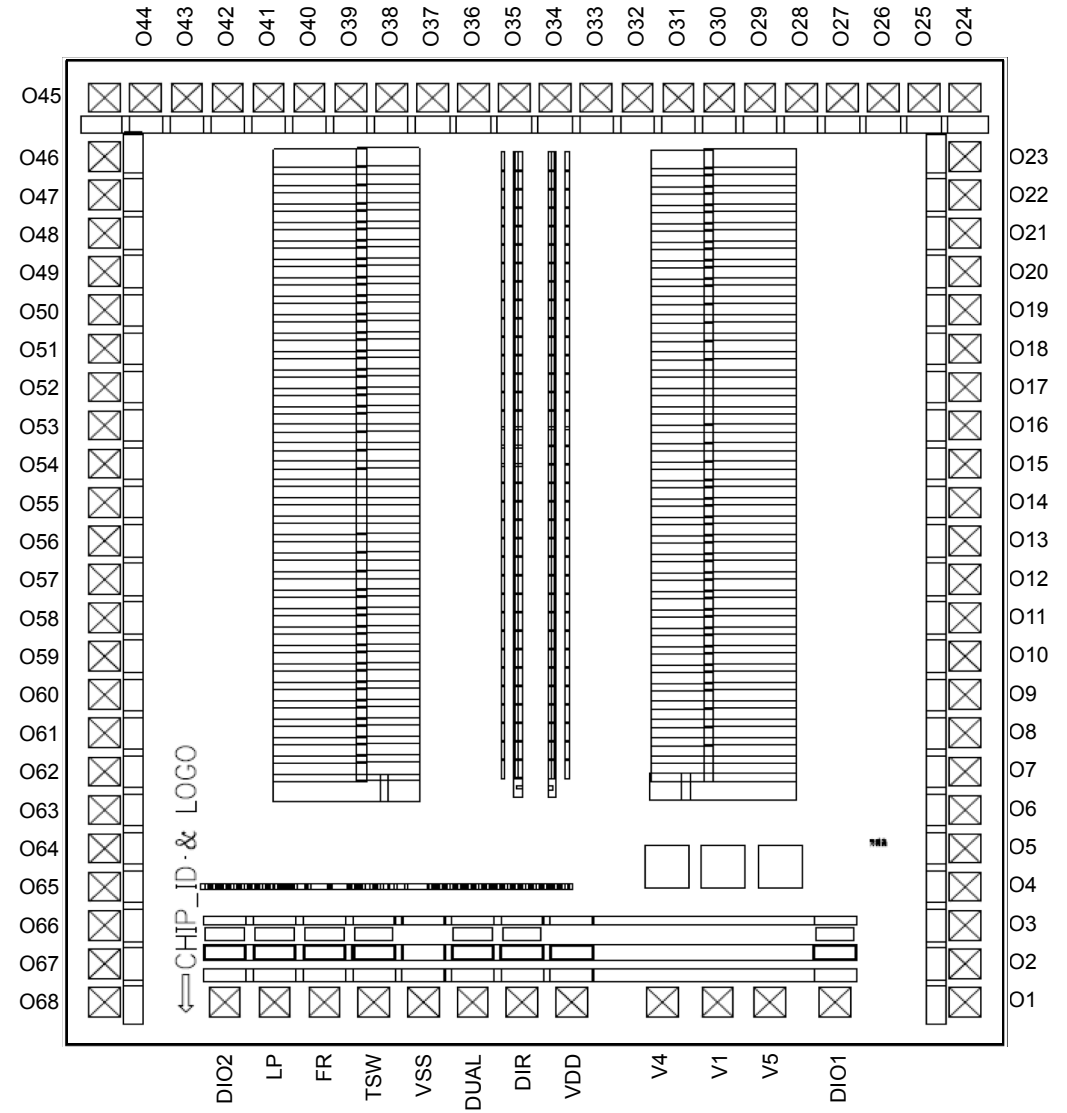
Table 2 Pin signal description.

To avoid a latch-up effect at power-on: $V_{SS} - 0.5\ V <$ voltage at any pin at any time $< V_{DD} + 0.5\ V$.

Pin number	SYMBOL	I/O	DESCRIPTION
1, 25~36, 40~61, 65~86, 90~100	O68, O1~O12, O13~O34, O35~O56, O57~O67	Output	COMMON driver output. Please refer to Fig. 2 for pin assignment and Table 4 for output voltage level.
2, 19	DIO2, DIO1	I/O	Input/output for COMMON scan data. COMMON scan data is sent out by the controller SAP1024B from its CDATA output. The COMMON scan data is for horizontal scan line synchronization.
3	LP	I	Horizontal line pule, used as shift clock of the internal 68-bit shift register.
4	FR	I	Frame signal. This signal is used to generate alternating LCD bias voltage.
5, 6, 10, 12, 14, 16, 20~24, 37~39, 62~64, 87~89	NC		No Connection. These pins should be left open in application.
7	TSW	I	Terminal switch. When this pin is connected to VDD, O1~O68 are output on the falling edge of LP. When this pin is connected to VSS, O1~O68 are output on the rising edge of LP.
8	VSS		Ground.
9	DUAL	I	Select dual input mode or single input mode. Please refer to Table 5.
11	DIR		Select the shift direction of the scan data. Please refer to Table 5.
13	VDD		Power supply for control logic.
15, 17, 18	V4, V1, V5	Input	LCD bias voltage.

4 PAD DIAGRAM AND COORDINATES

4.1 Pad diagram



Note:

1. For chip_on_board (COB) bonding, chip carrier should be connected to VDD or left open. Chip carrier is the metal pad to which die is attached.
2. The chip size is : (X-axis, Y-axis)= 2432 μm x 2717μm.
3. The Chip ID is: 3007.

Fig.3 Pad locations.

4.2 Pad description

Table 3 Pad signal names and coordinates
The unit for coordinates is μm.

PAD NO.	PAD NAME	COORDINATES		PAD NO.	PAD NAME	COORDINATES		PAD NO.	PAD NAME	COORDINATES	
		X	Y			X	Y			X	Y
1	O68	98.50	117.20	35	O34	1253.5	2587.80	69	DIO1	1970.1	117.3
2	O67	98.50	222.20	36	O33	1358.5	2587.80	70	V5	1802.6	117.3
3	O66	98.50	327.20	37	O32	1463.5	2587.80	71	V1	1669.0	117.3
4	O65	98.50	432.20	38	O31	1568.5	2587.80	72	V4	1527.5	117.3
5	O64	98.50	537.20	39	O30	1673.5	2587.80	73	VDD	1295.3	117.3
6	O63	98.50	642.20	40	O29	1778.5	2587.80	74	DIR	1168.2	117.3
7	O62	98.50	747.20	41	O28	1883.5	2587.80	75	DUAL	1041.1	117.3
8	O61	98.50	852.20	42	O27	1988.5	2587.80	76	VSS	915.6	117.3
9	O60	98.50	957.20	43	O26	2093.5	2587.80	77	TSW	788.4	117.3
10	O59	98.50	1062.20	44	O25	2198.5	2587.80	78	FR	661.3	117.3
11	O58	98.50	1167.20	45	O24	2303.5	2587.80	79	LP	533.8	117.3
12	O57	98.50	1272.20	46	O23	2303.5	2427.2	80	DIO2	406.7	117.3
13	O56	98.50	1377.20	47	O22	2303.5	2322.2				
14	O55	98.50	1482.20	48	O21	2303.5	2217.2				
15	O54	98.50	1587.20	49	O20	2303.5	2112.2				
16	O53	98.50	1692.20	50	O19	2303.5	2007.2				
17	O52	98.50	1797.20	51	O18	2303.5	1902.2				
18	O51	98.50	1902.20	52	O17	2303.5	1797.2				
19	O50	98.50	2007.20	53	O16	2303.5	1692.2				
20	O49	98.50	2112.20	54	O15	2303.5	1587.2				
21	O48	98.50	2217.20	55	O14	2303.5	1482.2				
22	O47	98.50	2322.20	56	O13	2303.5	1377.2				
23	O46	98.50	2427.20	57	O12	2303.5	1272.2				
24	O45	98.50	2587.80	58	O11	2303.5	1167.2				
25	O44	203.5	2587.80	59	O10	2303.5	1062.2				
26	O43	308.5	2587.80	60	O9	2303.5	957.2				
27	O42	413.5	2587.80	61	O8	2303.5	852.2				
28	O41	518.5	2587.80	62	O7	2303.5	747.2				
29	O40	623.5	2587.80	63	O6	2303.5	642.2				
30	O39	728.5	2587.80	64	O5	2303.5	537.2				
31	O38	833.5	2587.80	65	O4	2303.5	432.2				
32	O37	938.5	2587.80	66	O3	2303.5	327.2				
33	O36	1043.5	2587.80	67	O2	2303.5	222.2				
34	O35	1148.5	2587.80	68	O1	2303.5	117.2				

5 FUNCTIONAL DESCRIPTION

5.1 Row output drive (O1~O68)

The output voltage level of outputs O1~O68 is determined by input data (row scan data) and FR (frame signal), as given in Table 4.

Table 4 output voltage level of O1~O68

FR	Data	SEN6A40 O1~O68 outpust	SEN6A39 O1~O80 outputs
L	L	V1	V2
L	H	V5	VDD
H	L	V4	V3
H	H	VDD	V5

5.2 Single/Dual Mode selection

The mode selection and scan data shift direction is given in the following table.

Table 5 Mode selection

Mode	**DIR pin**	**DUAL pin**	**Data shift direction**	**DIO1**	**DIO2**
Single mode, left-to-right shift	VDD	VSS	O1 → O68	IN	OUT
Dual mode		VDD	O1 → O34, O68 → O35	IN	IN
Single mode, right-to-left shift	VSS	don't care (VDD or VSS)	O68 → O1	OUT	IN

5.3 Cascading connection

5.3.1 SINGLE MODE, LEFT-TO-RIGHT SHIFT

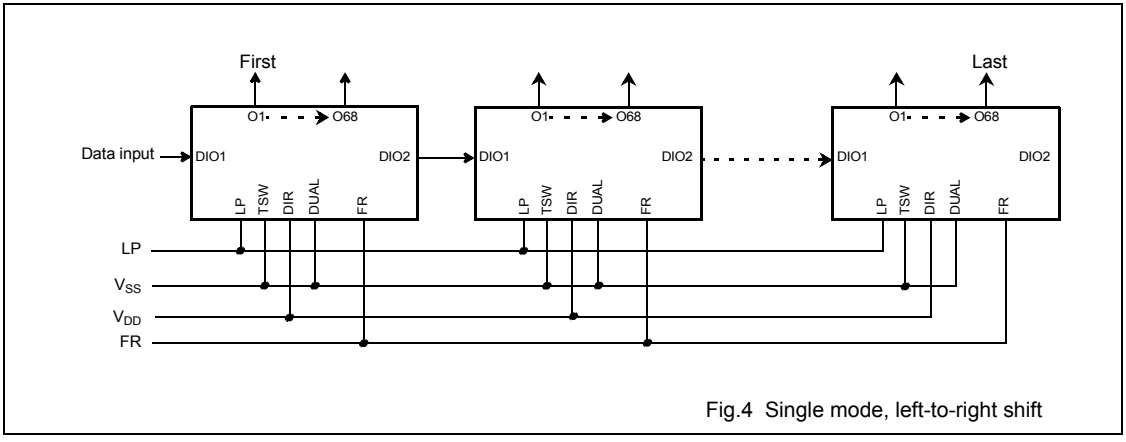


Fig.4 Single mode, left-to-right shift

5.3.2 SINGLE MODE, RIGHT-TO-LEFT SHIFT

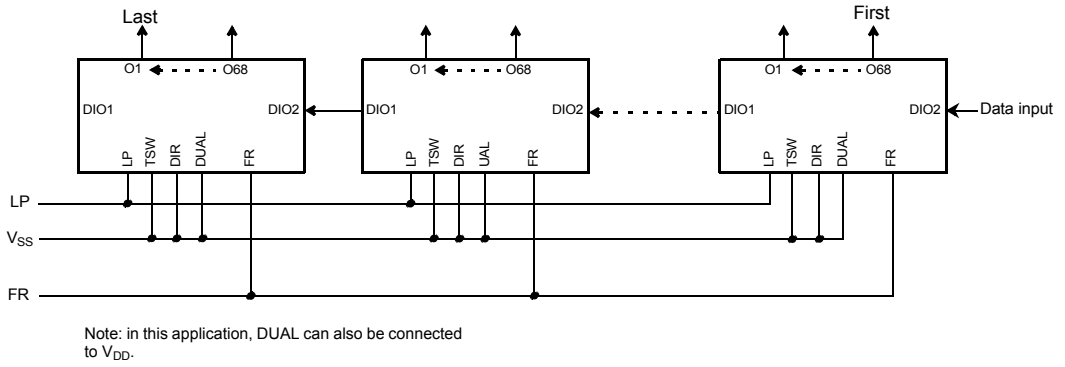


Fig.5 Single mode, right-to-left Shift

5.3.3 DUAL MODE

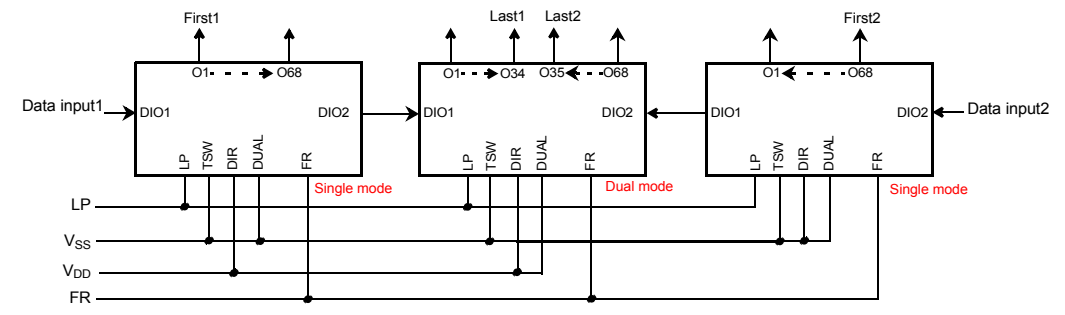


Fig.6 Dual Mode

6 ABSOLUTE MAXIMUM RATING

Table 6 Absolute maximum rating

VDD = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = 25±2°C.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
VDD	Voltage on the VDD input.	−0.3	+7.0	V
VDD-V5	LCD bias voltage (note 1).	0	30	V
Vi(max)	Maximum input voltage to input pins (note 2).	-0.3	VDD + 0.3	
T_{amb}	Operating ambient temperature range.	-20	+ 75	°C
T_{stg}	Storage temperature range.	−40	+125	°C

Note:

1. The following conditions must always be met: VDD ≥ V1 > V4 > V5, VSS=0 V.
2. For the input pins: FR, LP, DIR, DUAL, TSW, DIO1, and DIO2.

7 DC CHARACTERISTICS

Table 7 DC Characteristics

VDD = 5V ±10%; V_{SS} = 0 V; all voltages with respect to VSS unless otherwise specified; T_{amb} = 25±2 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD	Supply voltage for control logic	Please refer to Fig. 10 for DC power-up sequence.	2.7	5.0	5.5	V
VDD-V5	LCD bias voltage	Note 1.	12		30	
V_{IL}	Input LOW voltage of input pins	DIO1, DIO2, LP, TSW, FR, DUAL, DIR	0		0.2 VDD	V
V_{IH}	Input HIGH voltage of input pins	DIO1, DIO2, LP, TSW, FR, DUAL, DIR	0.8 VDD		VDD	V
V_{OL}	Output LOW voltage level of the DIO1 and DIO2 pins	I_{OL}=400μA	0.0		0.4	V
V_{OH}	Output HIGH voltage level of the DIO1 and DIO2 pins	I_{OH}=-400μA	VDD – 0.4		VDD	V
I_{STBY}	Standby current	Note 2.			2	μA
I_{SS}	Operating current	Note 3.			80	μA
I_{EE}	Operating current	Note 4.			80	μA
R_{ON1}	Driver ON resistance at V_{LCD}= 30 V	Note 5.			1.0	KΩ
R_{ON2}	Driver ON resistance at V_{LCD}= 20 V	Note 6.			1.0	KΩ

Notes:

1. The following coditions: $V_{DD} \geq V1 > V4 > V5$ must always be met.
2. V_{DD}-V5=30 V, LP=LOW, Output unloaded; measured at the V_{SS} pin.
3. Condition for the measurement: $V_{LCD}=V_{DD}$-V5=30 V, V_{DD}=5.5 V, LP=14 KHz, No load. This is the current flowing from V_{DD} to V_{SS}, measured at the V_{SS} pin.
4. Condition for the measurement: $V_{LCD}=V_{DD}$-V5=30 V, V_{DD}=5.5 V, LP=14 KHz, No load. This is the current flowing from V_{DD} to V5, measured at the V5 pin.
5. Condition for the measurment: V_{DD}-V5=30 V, $|V_{DE}-V_O|$=0.5 V, where V_{DE}= one of V1, V4, or V5. $V1=V_{DD}$ - (1/9) x (V_{DD}-V5), $V4=V_{DD}$ - (8/9) x (V_{DD}-V5). For the driver circuits (O1~O68), please refer to Section 12, Pin Circuits.
6. Condition for the measurment: V_{DD}-V5=20 V, $|V_{DE}-V_O|$=0.5 V, where V_{DE}= one of V1, V4, or V5. $V1=V_{DD}$ - (1/9) x (V_{DD}-V5), $V4=V_{DD}$ - (8/9) x (V_{DD}-V5). For the driver circuits (O1~O68), please refer to Section 12, Pin Circuits.

8 AC CHARACTERISTICS

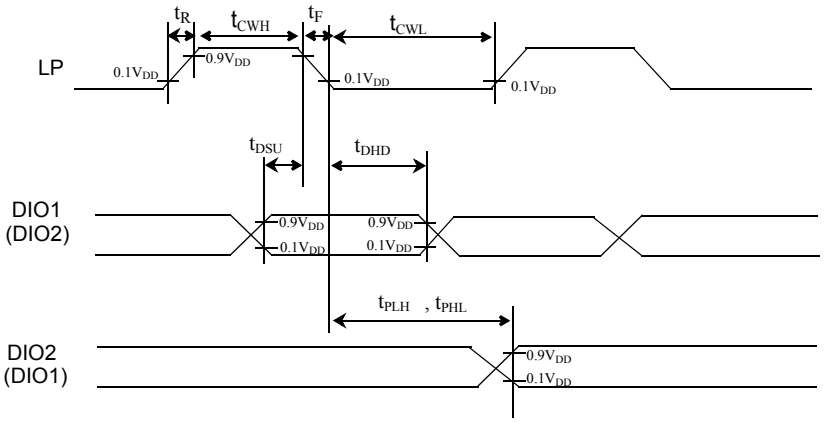


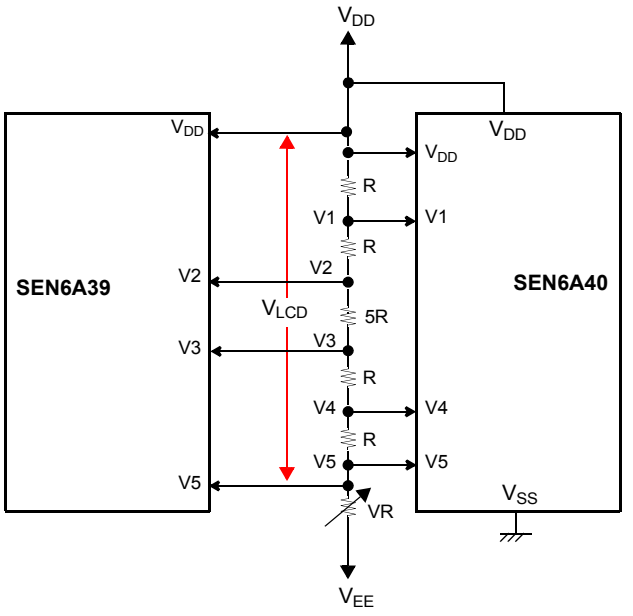
Fig.7 AC characteristics

Table 8 AC Characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = 25 ±2 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{CWH}	High period of the LP clock		30		ns
T_{CWH}	Low period of the LP clock		1000		ns
t_R	LP rise time			50	ns
t_F	LP fall time			50	ns
t_{DSU}	Input data setup time	For both DIO1 and DIO2	30		ns
t_{DHD}	Input data hold time.	For both DIO1 and DIO2	50		ns
t_{PLH} ,t_{PHL}	Output delay time	LP→DIO1, LP→DIO2, Load=10 pF.		250	ns

9 LCD BIAS VOLTAGE



$V_{LCD}=V_{DD}-V5$

$V1 = V_{DD} - (1/9)\ V_{LCD}$

$V2 = V_{DD} - (2/9)\ V_{LCD}$

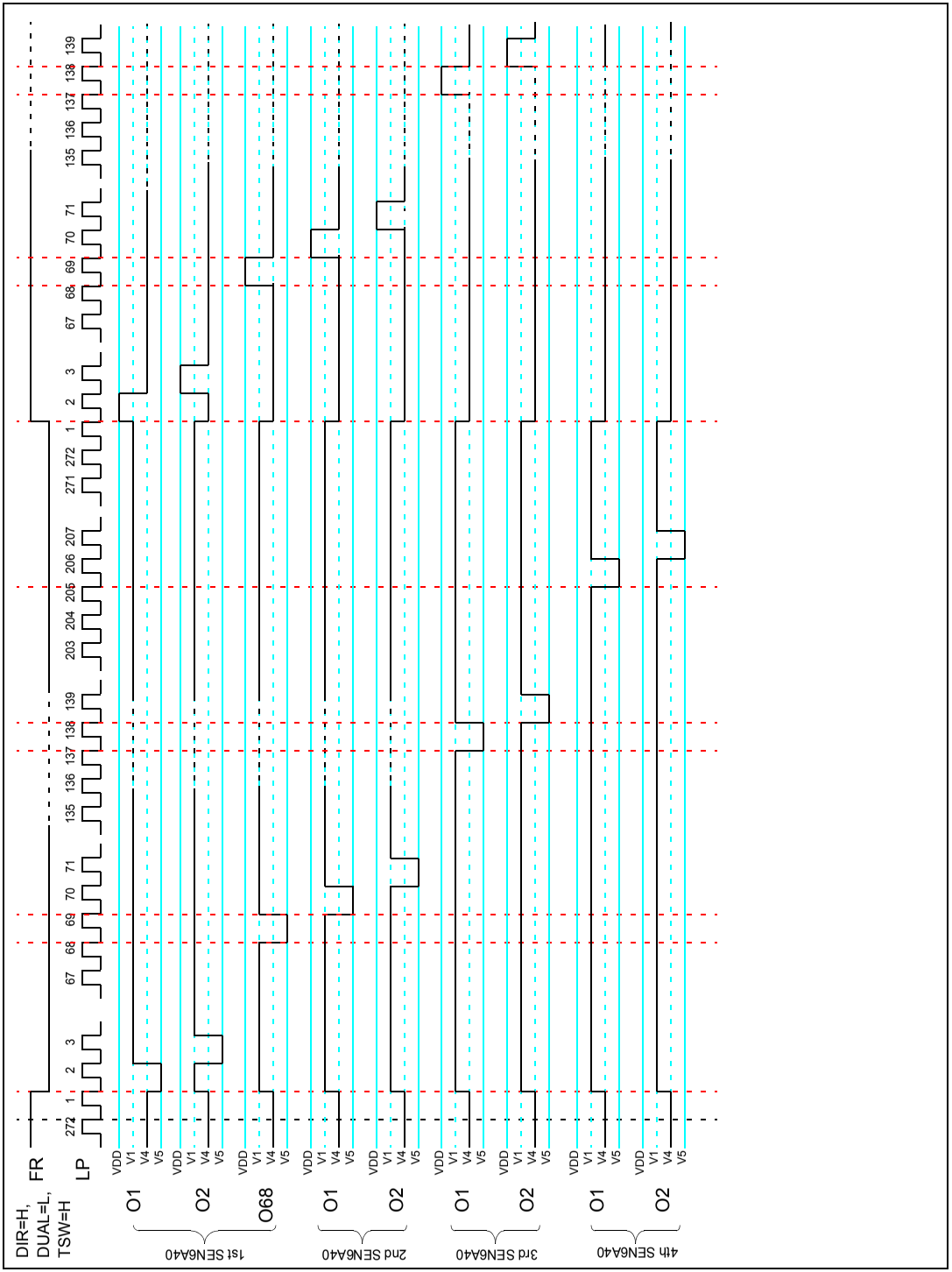
$V3 = V_{DD} - (7/9)\ V_{LCD}$

$V4 = V_{DD} - (8/9)\ V_{LCD}$

$V5 = V_{DD} - (9/9)\ V_{LCD}$

Fig.8 LCD bias voltage

10 TIMING DIAGRAM



11 APPLICATION EXAMPLES

11.1 EXAMPLE 1 (64X160)

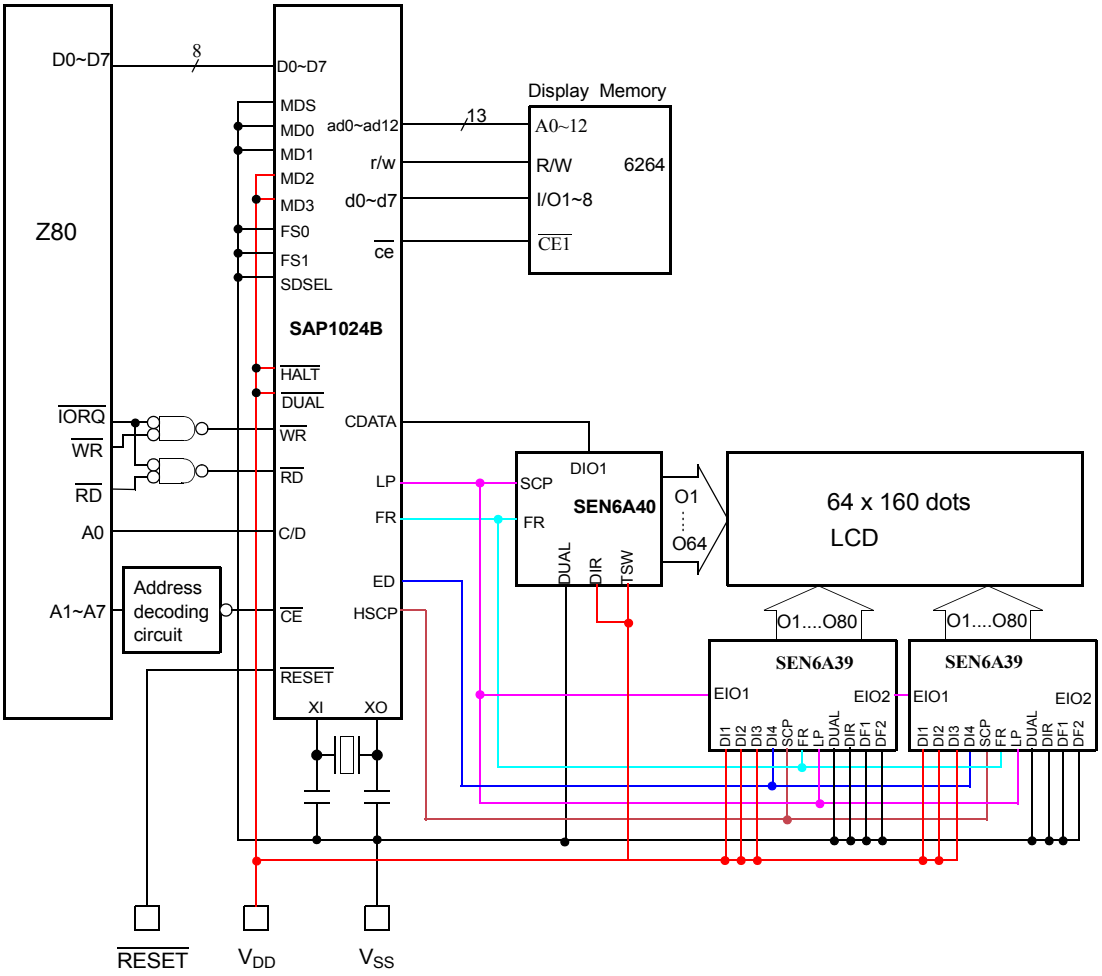
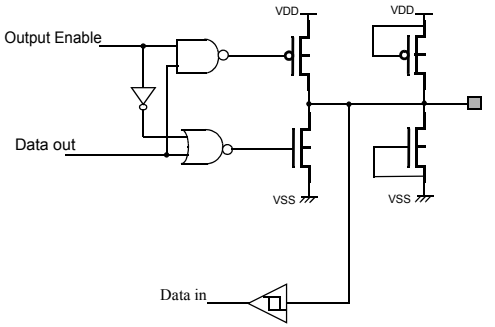
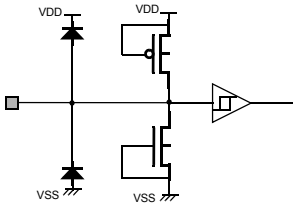
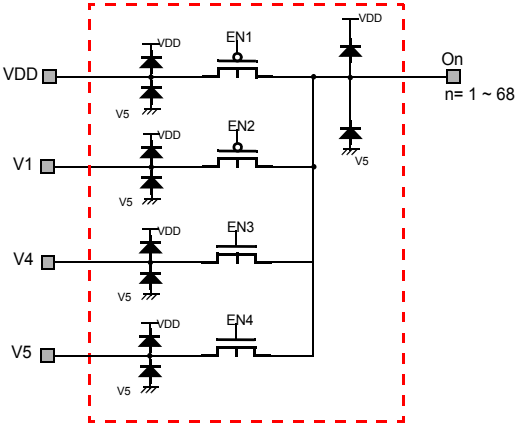


Fig.9 64 X 160 dots application

12 PIN CIRCUITS

Table 9 MOS-level schematics of all input, output, and I/O pins.

SYMBOL	Input/ output	CIRCUIT	NOTES
DIO1, DIO2	I/O		
FR, LP, DIR, DUAL, TSW	Inputs		
O1~O68, VDD, V1, V4, V5	Driver outputs, High voltage inputs		

13 APPLICATION NOTES

1. It is recommended that the following power-up sequence be followed to ensure reliable operation of your display system. As the ICs are fabricated in CMOS and there is intrinsic latch-up problem associated with any CMOS devices, proper power-up sequence can reduce the danger of triggering latch-up. When powering up the system, control logic power must be powered on first. When powering down the system, control logic must be shut off later than or at the same time with the LCD bias (V5).

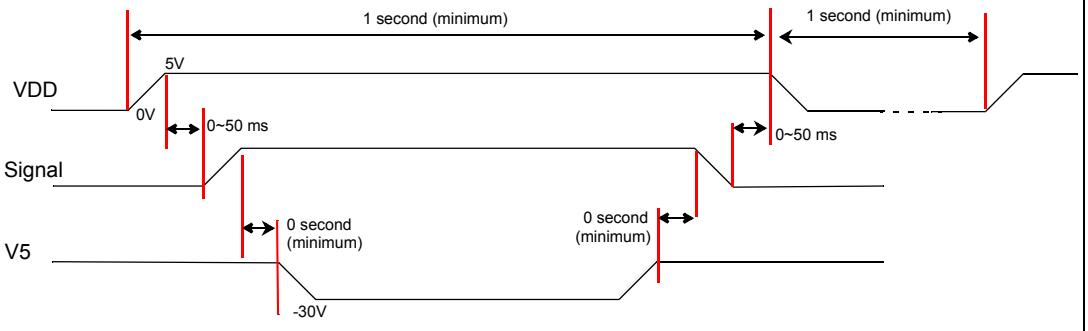
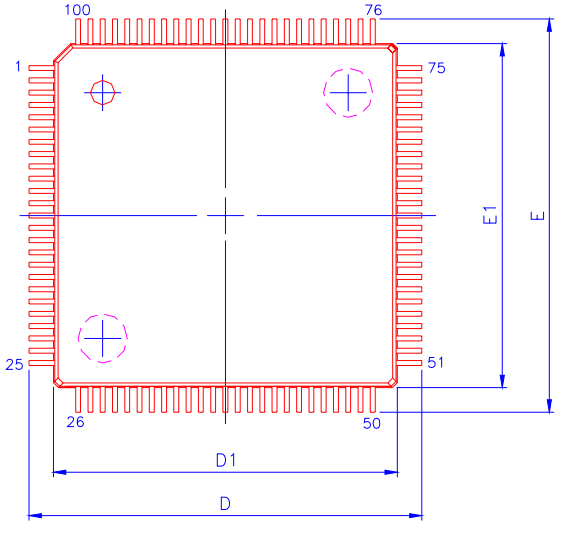
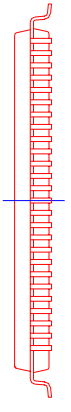


Fig.10 Recommended power up/down sequence

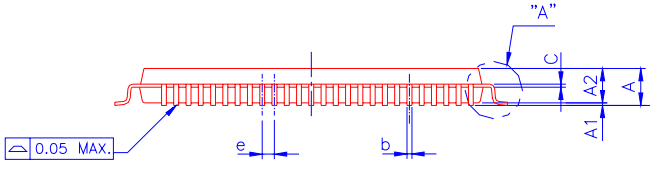
14 PACKAGE OUTLINE INFORMATION

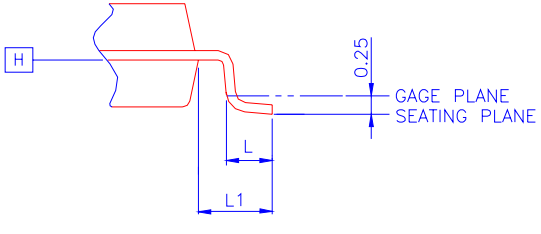




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		





DETAIL A

NOTES:

1. JEDEC OUTLINE:MS-026 BED
2. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

SEN6A40
LQFP100 Package Outline Drawing

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. For more in-depth account of soldering ICs, please refer to dedicated reference materials.

15.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, please contact Avant for drypack information.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

15.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Avant customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Avant for any damages resulting from such improper use or sale.