ePAPER DISPLAY MODULE DATASHEET

Datasheet Release 2023-01-20
For
CFAP122250A2-0213

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1. General Information

Datasheet Revision History
Datasheet Release Date: 2023-01-20 Datasheet for the CFAP122250A2-0213 ePaper display module.

Product Change Notifications
You can check for or subscribe to Part Change Notices for this display module on our website.

Variations
Slight variations between lots are normal (e.g., contrast, color, or intensity).

Volatility
This display module has volatile memory.

Disclaimer
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2. Description Overview

This ePaper display is a TFT active matrix electrophoretic display with interface and a reference system design. The 2.13" active area contains 122×250 pixels and has 1-bit white/black full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

3. Features

- High contrast
- High reflectance
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Bi-Stable Display
- Commercial temperature range
- Landscape or portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On-chip display RAM
- Waveform stored in On-chip OTP or can be written by MCU
- Serial peripheral interface (SPI)
- On-chip oscillator
- On-chip booster and regulator control for generating V_{COM}, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor
- Build-in temperature sensor
- Supports partial updates

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.13	inch	
Display Resolution	122 × 250	pixel	dpi: 112
Active Area	48.55 (H) x 23.70 (W)	mm	
Pixel Pitch	0.194 × 0.194	mm	
Pixel Configuration	Square		
Outline Dimension	59.2 (H) x 29.2 (W) × 1.0 (D)	mm	
Weight (Typical)	3.2±0.5	g	

5. Input/Output Terminals

5.1. Pin Out List

Pin #	Type	Single	Description
1	-	NC	No Connection and Do Not Connect with Other NC Pins
2	O	GDR	N-Channel MOSFET Gate Drive Control
3	O	RESE	Current Sense Input for the Control Loop
4	-	NC	No Connection and Do Not Connect with Other NC Pins
5	C	VSH2	Positive source driving voltage (red)
6	O	TSCL	I2C interface for digital temperature sensor clock pin
7	I/O	TSDA	I2C interface for digital temperature sensor data pin
8	I	BS1	Bus Selection Pin. 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.
9	O	BUSY	Busy State Output Pin. When Busy is low, the operation of chip should not be interrupted and no commands should be issued to the module. The driver IC will put Busy pin low when the driver IC is working.
10	I	RES #	Reset, active low
11	I	D/C #	Data /Command Control Pin. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.
12	I	CS #	Chip Select Input Pin. Chip is selected when line is low
13	I	SCL	Serial Clock Pin (SPI)
14	I/O	SDA	Serial Data Pin (SPI)
15	I	VDDIO	Power for Interface Logic Pins. Connect to VCI.
16	I	VCI	Power Supply Pin for the Chip
17	P	VSS	Ground
18	C	VDD	Core Logic Power Pin. Can be internally regulated from VCI. Connect a capacitor between VDD and VSS.
19	C	VPP	Power Supply for OTP Programming. Leave open when not in use
20	C	VSH1	Positive Source Driving Voltage
21	C	VGH	Power Supply Pin for VGH and VSH
22	C	VSL	Negative Source Driving Voltage
23	C	VGL	Power Supply Pin for VCOM, VGL, and VSL
24	C	VCOM	VCOM Driving Voltage

5.2. MCU Interface Selection

The CFAP122250A2-0213 can support 3-wire/4-wire serial peripheral interface. The BS1 pin is used to control the interface, see the following configurations.

MCU Interface Selection

BS1	MPU Interface
L	4-Lines Serial Peripheral Interface (SPI)
H	3-Lines Serial Peripheral Interface (SPI) – 9 bits SPI

5.3. MCU Serial Peripheral Interface (4-Wire SPI)

The 4-Wire SPI consists of serial clock SCLK, serial data SDA, D/C# and CS#. The control pins status in 4-Wire SPI in writing command/data is shown in Table 6-2 and the Write Procedure 4-Wire SPI.

Table 6-2: Control Pins Status of 4-Wire SPI

Function	SCLK Pin	SDA Pin	D/C# Pin	CS# Pin
Write Command	Rising Edge	Command Bits	L	L
Write Data	Rising Edge	Data Bits	H	L

Notes:
(1) L is connected to V_{SS} and H is connected to V_{DDIO}
(2) SDA is shifted into an 8-bit shift register on every rising edge of SCLK in the order of MSB first. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

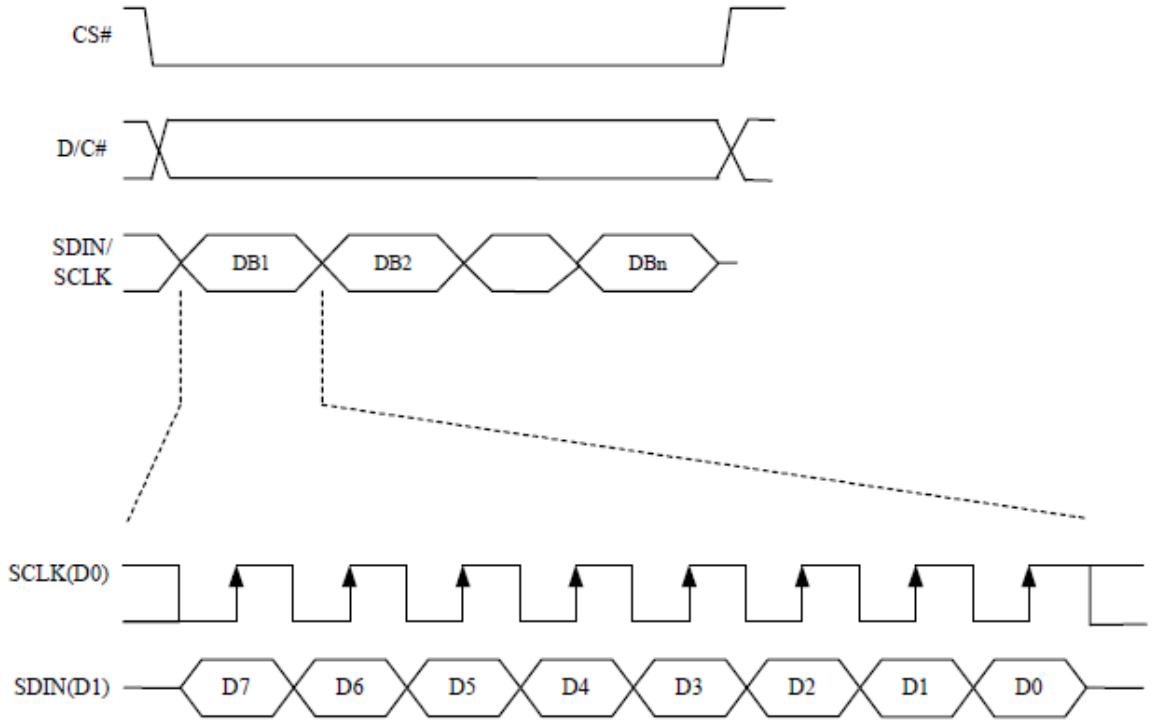


Figure 6-2: Write Procedure in 4-Wire SPI

5.4. MCU Serial Peripheral Interface (3-Wire SPI)

The 3-wire SPI consists of serial clock SCLK, serial data SDIN and CS#. The operation is similar to 4-wire SPI except the D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the write operation, 9-bits are shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which indicates whether the following byte is command or data. When D/C# bit is 0, the following byte is a command. When D/C# bit is 1, the following byte is data.

Table 6-3 Shows the Write Procedure in 3-Wire SPI

Function	SCLK Pin	SDIN Pin	D/C# Bit	CS# Pin
Write Command	Rising edge	Command Bit	L	L
Write Data	Rising edge	Data Bit	H	L

Note: "L" is connected to V_{SS}. "H" is connected to V_{DDIO}.

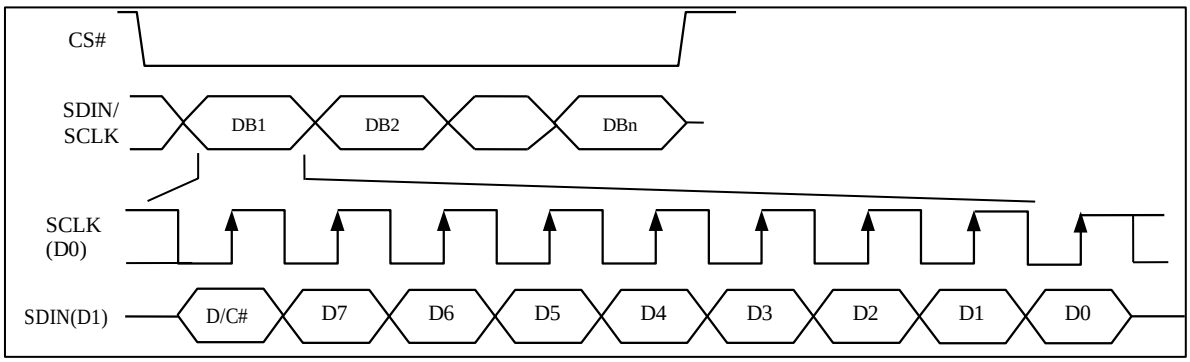


Figure 6-3: Control Pins Status of 3-Wire SPI

6. Temperature Register Mapping

If the temperature value MSByte bit D11 = 0, then

The temperature is positive and value (DegC) = + (Temperature value) / 16

If the temperature value MSByte bit D11 = 1, then

The temperature is negative and value (DegC) = ~ (2's complement of temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

7. Command Table

For more information on the commands, see the SSD1680 controller datasheet.

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	**01**	0	0	0	0	0	0	0	1	Driver Output Control	Set the number of gate. Set A[8:0] = 0127h Mux gate lines setting Set B[8:0] = 00h Gate scanning sequence and direction
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	1	-	0	0	0	0	0	0	0	A8		
0	1	-	0	0	0	0	0	B2	B1	B0		
0	0	**03**	0	0	0	0	0	0	1	1	Gate Driving Voltage Control	Set Gate driving voltage. A[4:0] = 17h [POR], VGH at 20V VGH setting from 10 to 20V
0	1	-	0	0	0	A4	A3	A2	A1	A0		
0	0	**04**	0	0	0	0	0	1	0	0	Source Driving Voltage Control	Set Source output voltage. A[7:0] = 41h [POR], VSH/VSL at 15V B[7:0] = ACh[POR], VSH2 at 5.4V C[7:0] = 32h[POR], VSL at -15V
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	1	-	B7	B6	B5	B4	B3	B2	B1	B0		
0	1	-	C7	C6	C5	C4	C3	C2	C1	C0		
0	0	**08**	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting The command requires CLKEN=1. Refer to Register 0x22 for details. BUSY will be high during operation.
0	0	**09**	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write register for Initial Code Setting Selection A[7:0]~D[7:0]: Reserved
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	1		D7	D6	D5	D4	D3	D2	D1	D0		
0	0	**0A**	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting
0	0	**0C**	0	0	0	0	1	1	0	0	Booster Soft Start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR] Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]: Bit[6:4] Driving Strength Selection 000 1(Weakest) 001 2

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
				A6	A5	A4	A3	A2	A1	A0		010 3 011 4 100 5 101 6 110 7 111 8(Strongest)
				B6	B5	B4	B3	B2	B1	B0		
				C6	C5	C4	C3	C2	C1	C0		
				0	D5	D4	D3	D2	D1	D0		Bit[3:0] Min Off Time setting of GDR 0000-0011 NA 0100 - 2.6 0101 - 3.2 0110 - 3.9 0111 - 4.6 1000 - 5.4 1001 - 6.3 1010 - 7.3 1011 - 8.4 1100 - 9.8 1101 - 11.5 1110 - 13.8 1111 - 16.5 D[5:4] duration setting of phase 3 D[3:2] duration setting of phase 2 D[1:0] duration setting of phase 1 00 - 10ms 01 - 20ms 10 - 30 ms 11 - 40 ms
0	0	**10**	0	0	0	1	0	0	0	0	Deep Sleep Mode	Deep Sleep Mode Control A[1:0] 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2 After this command initiated, the chip will enter Deep Sleep Mode, BUSY will be kept high. To exit Deep Sleep Mode, send HWRESET to driver
01			0	0	0	0	0	0	0	A_0		
			0	0	0	0	0	A_2	A_1	A_0		
0	1		1	A6	A5	A4	A3	A2	A1	A0		
0	1		1	B6	B5	B4	B3	B2	B1	B0		
0	1		1	C6	C5	C4	C3	C2	C1	C0		
0	1		0	0	D5	D4	D3	D2	D1	D0		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	**11**	0	0	0	1	0	0	0	1	Data Entry Mode Setting	Define data entry sequence. A[2:0] = 011 [POR] A[1:0] = ID[1:0] Address automatic increment / decrement setting.The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 - Y decrement, X decrement, 01 - Y decrement, X increment, 10 - Y increment, X decrement, 11 - Y increment, X increment[POR] A[2] = AM Set the direction in which the address counter is updated automatically after data is written to the RAM. When AM = 0, the address counter is updated in the X direction. [POR] When AM = 1, the address counter is updated in the Y direction.
0	1	-	0	0	0	0	0	A2	A1	A0		
0	0	**12**	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode. **Note**: RAM is unaffected by this command.
0	0	**18**	0	0	0	1	1	0	0	0	Temperature Sensor Selection	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	0	**1A**	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to Temperature Register)	Write to Temperature Register. A[7:0] MSByte 01111111[POR] B[7:0] LSByte 11110000[POR]
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	1	-	B7	B6	B5	B4	0	0	0	0		
0	0	**20**	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence. The Display Update Sequence Option is located at R22h. Do not interrupt this operation to avoid corruption of panel images.

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="3">Display Update Control 1</td><td rowspan="3">RAM content option for display Update.
A[7:0] = 00h [POR]
B[7:0] = 00h [POR]

A[3:0] BW RAM option:
0000 Normal
0100 Bypass RAM content as 0
1000 Inverse RAM content
B[7] Source Output Mode:
0: Available source from S0 – S175
1: Available Source from S8 – S167</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td>Display Update Sequence Option:
<table><tr><th>Operating Sequence</th><th>Hex</th></tr><tr><td>Enable Clock</td><td>80</td></tr><tr><td>Disable clock</td><td>01</td></tr><tr><td>Enable clock, enable analog</td><td>C0</td></tr><tr><td>Disable analog, disable clock</td><td>03</td></tr><tr><td>Enable clock, load LUT with Display Mode 1, disable clock</td><td>91</td></tr><tr><td>Enable clock signal, load LUT with Display Mode 2, disable clock</td><td>99</td></tr><tr><td>Enable clock, load temperature value, load LUT with Display Mode 1, disable clock</td><td>81</td></tr><tr><td>Enable clock, load temperature value, load LUT with Display Mode 2, display clock</td><td>89</td></tr><tr><td>Enable clock, enable analog, display with Display Mode 2, disable analog, disable OSC</td><td>C7</td></tr><tr><td>Enable clock, enable analog display with Display Mode 2, disable analog, disable OSC</td><td>CF</td></tr><tr><td>Enable clock, enable analog, load temp value, Display with Display Mode 1, disable analog, disable OSC</td><td>F7</td></tr><tr><td>Enable Clock Signal, Enable Analog, Load temperature value, DISPLAY with Display Mode 2, Disable Analog, Disable OSC</td><td>FF [POR]</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	**24**	0	0	1	0	0	1	0	0	Write RAM	After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly. For white pixel, RAM(BW)=1. 0 for black.
0	0	**26**	0	0	1	0	0	1	1	0	Write RAM 2	After this command, data entries will be written into the RAM 2 until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) holds the red data of the screen. For non-Red pixel[Black or White]: Content of Write RAM hold the background of the partial refresh.
0	0	**2C**	0	0	1	0	1	0	1	1	Write VCOM Register	Write VCOM Register from MCU Interface A[7:0] = 00h [POR]
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	0	**2D**	0	0	1	0	1	1	0	1	OTP Register Read	Read Register for Display Option: A[7:0] VCOM OTP Selection (command 0x37, Byte A) B[7:0] VCOM Register (Command 0x2C) C[7:0]~G[7:0] Display Mode (Command 0x37, 5 bytes B-F) H[7:0]~K[7:0] Waveform Version (Command 0x37, 4 bytes G-J)
1	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
1	1		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
1	1	-	K7	K6	K5	K4	K3	K2	K1	K0		
0	0	**2F**	0	0	1	0	1	1	1	1	Status Bit Read	Read IC Status Bit [POR 0x01] A[5] HV Ready Detection flag 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status not valid after RESET, must be initiated by commands 0x14 and 0x15 respectively.
1	1	-	0	0	A5	A4	0	0	A1	A0		
0	0	**30**	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of waveform setting Write the contents into the RAM before sending this command. CLKEN =1 required. Refer to Register 0x22. BUSY will be high.
0	0	**32**	0	0	1	1	0	0	1	0	Write LUT	Write LUT register from MCU interface

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td rowspan="3">Register</td><td rowspan="3">[153 bytes] which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR[n] and XON[nXY]
Refer to SSD1680 datasheet for more detail.</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>0</td><td>0</td><td>39</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td rowspan="2">OTP Program Mode</td><td rowspan="2">OTP Program Mode
A[1:0] = 00 Normal Mode [POR]
A[1:0] = 11 Internal generated OTP programming voltage</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Border Waveform Control</td><td rowspan="2">Select border waveform for VBD
A[7:0]=C0h [POR]
A[7:6] Select VBD option
<table>
<tr><th>A[7:6]</th><th>VBD level</th></tr>
<tr><td>00</td><td>GS transition defined in A[2:0]</td></tr>
<tr><td>01</td><td>Fix Level defined in A[5:4]</td></tr>
<tr><td>10</td><td>VCOM</td></tr>
<tr><td>11[POR]</td><td>HiZ</td></tr>
</table>
Fix Level Setting for VBD
<table>
<tr><th>A[5:4]</th><th>VBD level</th></tr>
<tr><td>00</td><td>VSS</td></tr>
<tr><td>01</td><td>VSH1</td></tr>
<tr><td>10</td><td>VSL</td></tr>
<tr><td>11[POR]</td><td>VSH2</td></tr>
</table>
A[2] GS Transition Control
<table>
<tr><th>A[2]</th><th>GS Transition Control</th></tr>
<tr><td>0</td><td>Follow LUT (Output VCOM@ RED)</td></tr>
<tr><td>1</td><td>Follow LUT</td></tr>
</table>
A [1:0] GS transition setting for VBD
<table>
<tr><th>A[1:0]</th><th>VBD Transition</th></tr>
<tr><td>00</td><td>LUT0</td></tr>
<tr><td>01</td><td>LUT1</td></tr>
<tr><td>10</td><td>LUT2</td></tr>
<tr><td>11</td><td>LUT3</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>0</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>44</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="3">Set RAM X - Address Start / End Position</td><td rowspan="3">Specify the start/end positions of the window address in the X direction by an address unit

A[4:0]: X-Start, POR = 00h
B[4:0]: X-End, POR = 14h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="5">Set Ram Y-Address Start / End Position</td><td rowspan="5">Specify the start/end positions of the window address in the Y direction by an address unit

A[8:0]: Y-Start, POR = 0127h

B[8:0]: Y-End, POR = 0000h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B8</td></tr>
</table>

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	**4E**	0	1	0	0	1	1	1	0	Set RAM X - Address Counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0] : POR is 00h
0	1	-	0	0	0	A4	A3	A2	A1	A0		
0	0	**4F**	0	1	0	0	1	1	1	1	Set RAM Y - Address Counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0] : POR is 0127h
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	1	-	0	0	0	0	0	0	0	A8		

8. Absolute Maximum Rating

Symbol	Parameter	Rating	Unit
V_{CI}	Logic Supply Voltage	-0.5 to +4.0	V
V_{IN}	Logic Input Voltage	-0.5 to V_{CI}+0.5	V
V_{OUT}	Logic Output Voltage	-0.5 to V_{CI}+0.5	V
T_{OPR}	Operation Temperature Range	0 to 50	°C
T_{STG}	Storage Temperature Range	-25 to 70	°C
	Optimal Storage Temperature	23±3	°C
RH	Optimal Storage Humidity	55±10	%
IMPORTANT: It is recommended that you use a UV protective film when operating the module in direct sunlight.			

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the DC Characteristics tables or Pin Out List section.

IMPORTANT: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

- For proper operation, it is recommended that V_{CI} be constrained to the range $V_{SS} < V_{CI}$.
- Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}).
- Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected. This device is light sensitive.
- Unused outputs must be left open.

9. DC Characteristics

The following specifications apply for V_{SS}=0V, V_{CI}=3.0V, T_{OPR}=25ɗ.

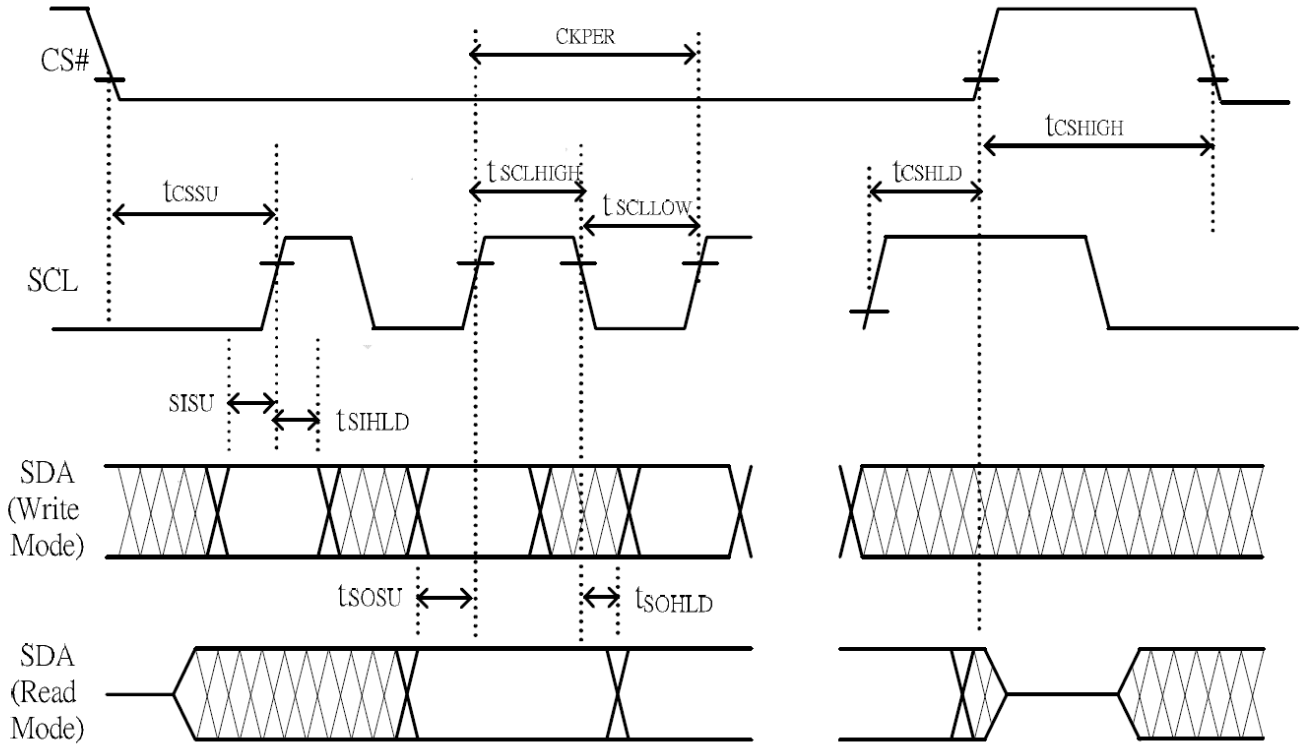
Symbol	Parameter	Test Condition	Applicable Pin	Min	Typ	Max	Unit
V_{CI}	Logic Supply Voltage		VCI	2.2	3.3	3.7	V
V_{DD}	Core Logic Voltage		VDD	1.7	1.8	1.9	V
V_{IH}	High-Level Input Voltage		-	$0.8V_{DDIO}$			V
V_{IL}	Low-Level Input Voltage					$0.2V_{DDIO}$	V
V_{OH}	High-Level Output Voltage	I_{OH} = -100uA	-	$0.9V_{DDIO}$			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 100uA				$0.1V_{DDIO}$	V
I_{update}	Module Operating Current	VCI = 3.0V	-	-	3	-	mA
I_{sleep}	Deep Sleep Current	DC/DC off No clock No input load RAM data not retained	-	-	1	5	µA

9.1. Power Consumption

Parameter	Symbol	Conditions	Typical	Max	Unit
Panel Power Consumption During Update	-	-	9	-	mW
Power Consumption in Standby Mode	-	-	-	0.003	mW

10. Serial Peripheral Interface Timing

The following specifications apply for V_{SS}=0V, V_{CI}=2.4V, T_{OPR}=25°C



Write Mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency	-	-	20	MHz
t_{CSSU}	CS# set up time (time CS# must be low before the first rising edge)	60	-	-	ns
t_{CSHLD}	CS# Hold time (time CS# has to remain low after the last falling edge)	65	-	-	ns
t_{CSHIGH}	Time CS# has to remain high between transfers	100	-	-	ns
$t_{SCLHIGH}$	Time SCL must remain high	25	-	-	ns
t_{SCLLOW}	Time SCL must remain low	25	-	-	ns
t_{SISU}	Time Data In must be stable before rising edge	10	-	-	ns
t_{SIHLD}	Time Data In must be stable after rising edge	40	-	-	ns

Read Mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency	-	-	2.5	MHz
t_{CSSU}	CS# set up time (time CS# must be low before the first rising edge)	100	-	-	ns
t_{CSHLD}	CS# Hold time (time CS# has to remain low after the last falling edge)	50	-	-	ns
t_{CSHIGH}	Time CS# has to remain high between transfers	250	-	-	ns
$t_{SCLHIGH}$	Time SCL must remain high	180	-	-	ns
t_{SCLLOW}	Time SCL must remain low	180	-	-	ns
t_{SOSU}	Time Data Out must be stable before rising edge	-	50	-	ns
t_{SOHLD}	Time Data Out must be stable after rising edge	-	0	-	ns

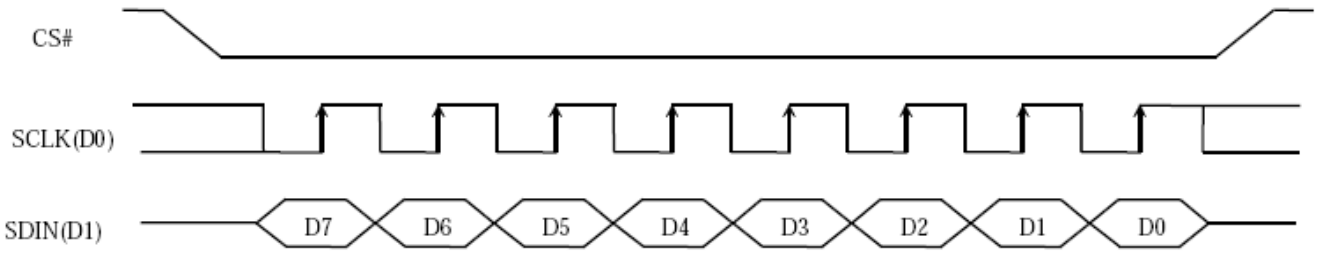
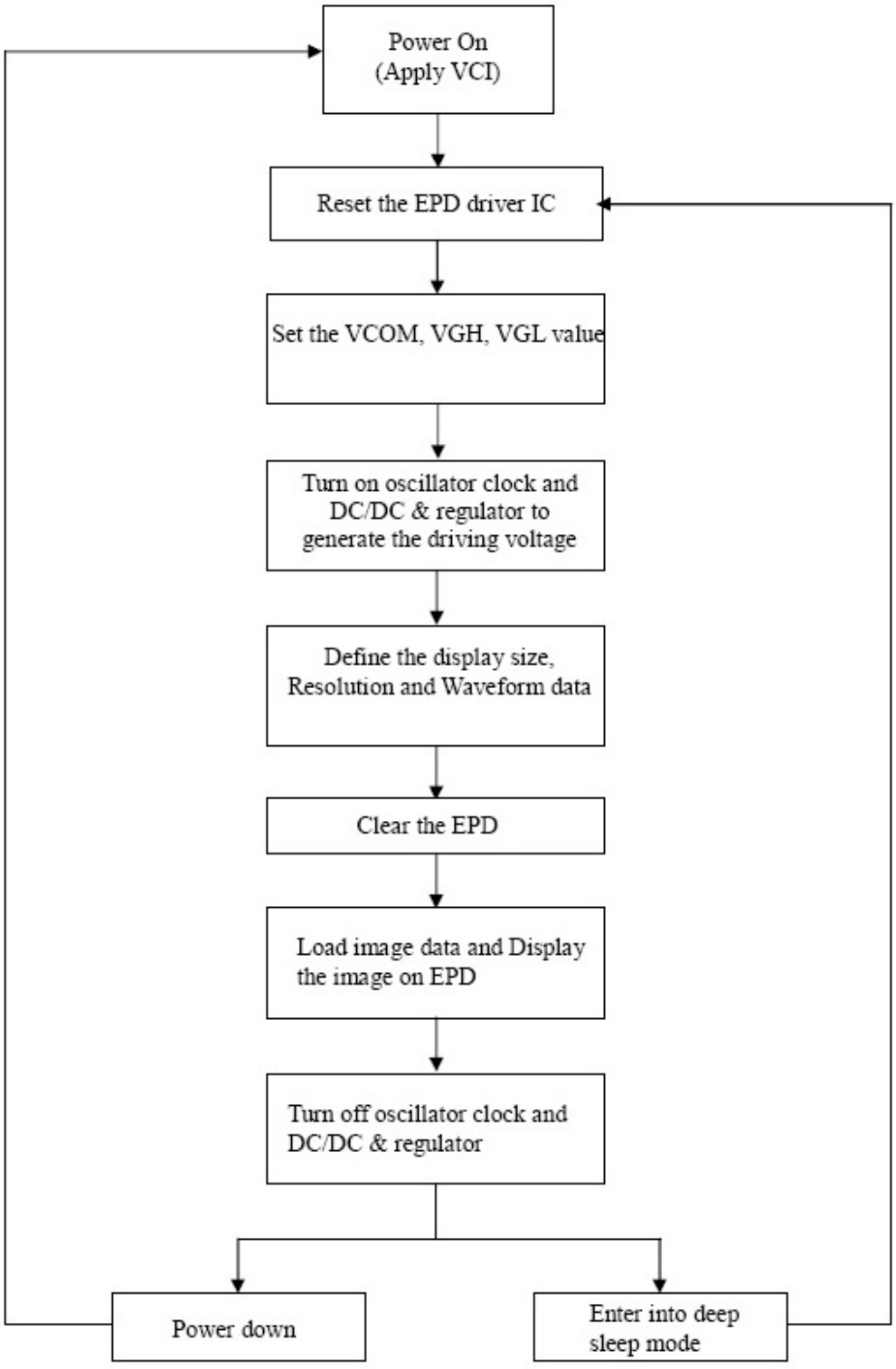


Figure 11-1: Serial Peripheral Interface Characteristics

11. Typical Operating Sequence



12. Optical Characteristics

12.1. Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

Symbol	Parameter	Conditions	Min	Typical	Max	Unit	Note
R	Reflectance	White	30	35	-	%	Note 1
CR	Contrast Ratio	Indoor	8:1		-	-	-
T_{UPDATE}	Update Time	25℃	-	3	-	sec	-
Panel Life	-	~23°C	-	5 years	-	-	Note 2

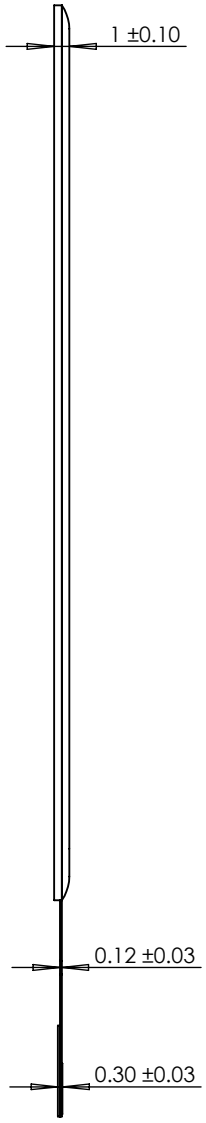
Note (1): Luminance Meter: Eye-One Pro Spectrophotometer
Note (2): Panel life is not guaranteed when working in temperatures below 0 degrees or above 40 degrees. Store panel with display white and face up.

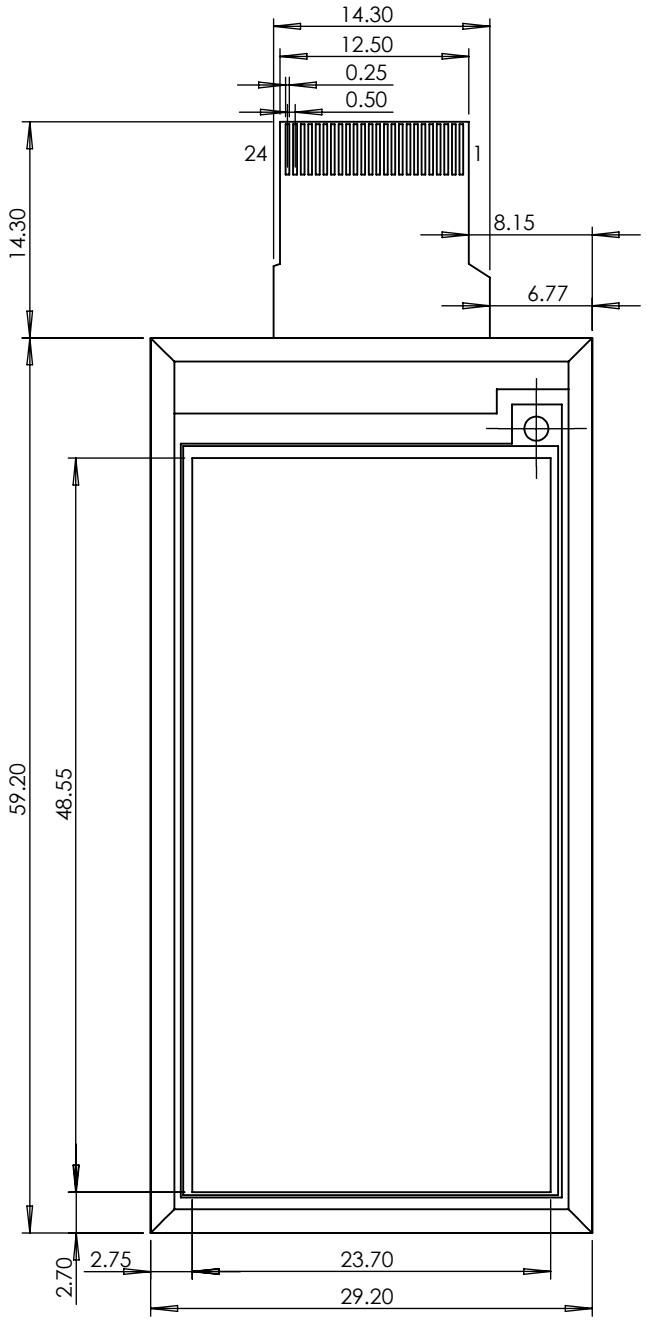
12.2. Definition of Contrast Ratio

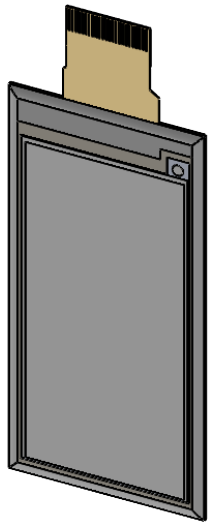
The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) ():

R1: White Reflectance Rd: Dark Reflectance

CR = R1/Rd







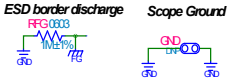
Pin	Function
1	NC
2	GDR
3	RESE
4	NC
5	VSH2
6	TSCL
7	TSDA
8	BS1
9	BUSY
10	RES#
11	D/C#
12	CS#
13	SCL
14	SDA
15	VDDIO
16	VCI
17	VSS
18	VDD
19	VPP
20	VSH1
21	VGH
22	VSL
23	VGL
24	VCOM

Units: millimeters
Tolerance: ±0.2

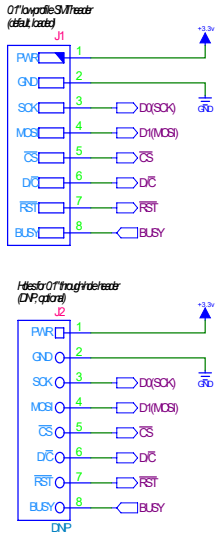
Crystalfontz

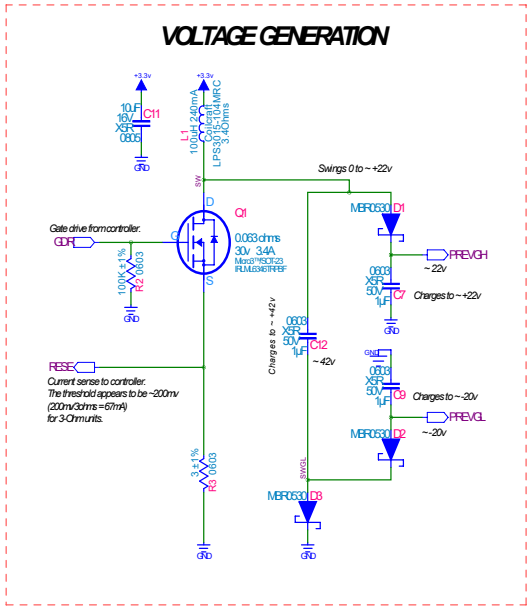
Part Number:	Date:	Filename:	Revision:
CFAP122250A2-0213	2023-01-20	CFAP122250A2-0213 mm.pdf	v1.1
	Web: www.crystalfontz.com/product/cfap122250A20213		Sheet: 1 of 1

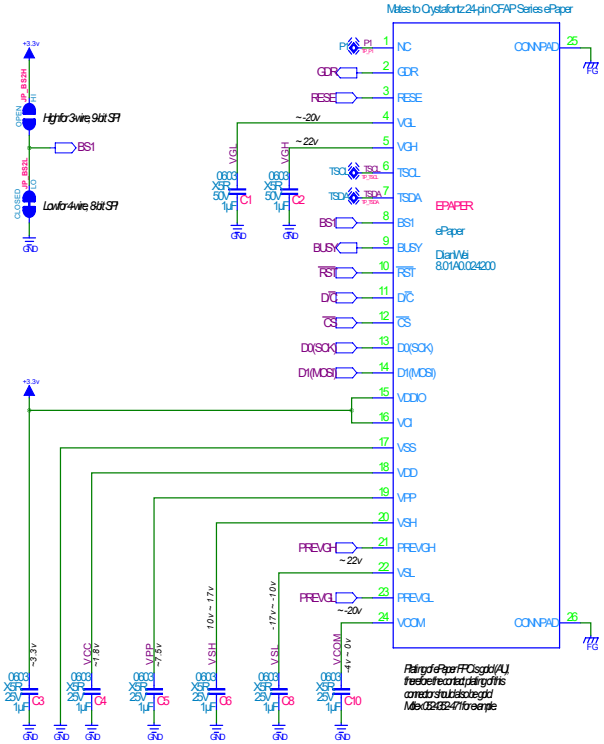
14. ePaper Breakout Board Schematic



REV	ENGINEER	DATE	REMARKS
0v0	BAC	2018-04-04	Initial Creation
0v1	BAC	2018-05-17	Ind val, C12 val, JP_0P47 open, CNFPC
-	-	-	-
-	-	-	-
-	-	-	-







CFA-10084: ePaper Adapter Board 24-pin (3-ohm)

Page 1 / 1: Schematic

PRODUCT NAME	PRODUCT REVISION	PCB NUMBER	PCB REVISION
CFA-10084	0v1	PCB-10084	0v1