ePAPER DISPLAY MODULE DATASHEET

Datasheet Release 2020-09-24
for
CFAP200200A3-0154

Rev A0

Crystalfontz America, Inc.
12412 East Saltese Avenue
Spokane Valley, WA 99216-0357
Phone: 888-206-9720
Fax: 509-892-1203
Email: support@crystalfontz.com
URL: www.crystalfontz.com

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1. General Information

Datasheet Revision History
Datasheet Release Date: 2020-09-24 Datasheet for the CFAP200200A3-0154 ePaper display module.

Product Change Notifications
You can check for or subscribe to Part Change Notices for this display module on our website.

Variations
Slight variations between lots are normal (e.g., contrast, color, or intensity).

Volatility
This display module has volatile memory.

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2. Description Overview

A square black-and-white 200x200 pixel ePaper display module, perfect for small, low power, long term display. Once an image is shown on the display, it remains visible while entirely disconnected from power. The display is an active matrix electrophoretic display (AMEPD).

Ultra-thin with a depth of 1.05mm and weight of only 2.1 grams, ePaper has a clear advantage over other display technologies for small handheld battery-operated devices or devices powered by solar.

Built-in voltage generation requires only a few external components. An integrated circuit contains a gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border.

3. Features

- 200x200 Pixels, 183 ppi
- High Contrast
- High Reflectance, Pure Reflective Mode
- Ultra-Wide Viewing Angle
- Ultra-Low Power Consumption, Bi-Stable Display, Low Current Deep Sleep Mode
- Commercial Temperature Range
- Antiglare Hard-Coated Front-Surface
- On-Chip Display RAM
- Low Voltage Detect for Supply Voltage
- Internal Temperature Sensor
- 10-byte OTP Space for Module Identification
- Waveform Stored in On-Chip OTP
- Serial Peripheral Interface Available
- On-Chip Oscillator, Booster and Regulator Control for Generating VCOM, Gate and Source Driving Voltage
- I^2C Signal Master Interface to Read External Temperature Sensor
- Full screen update time: 2 seconds
- Partial refresh time: 0.26 seconds
- Recommended time between updates: 180 seconds
- SSD1681 Controller chip

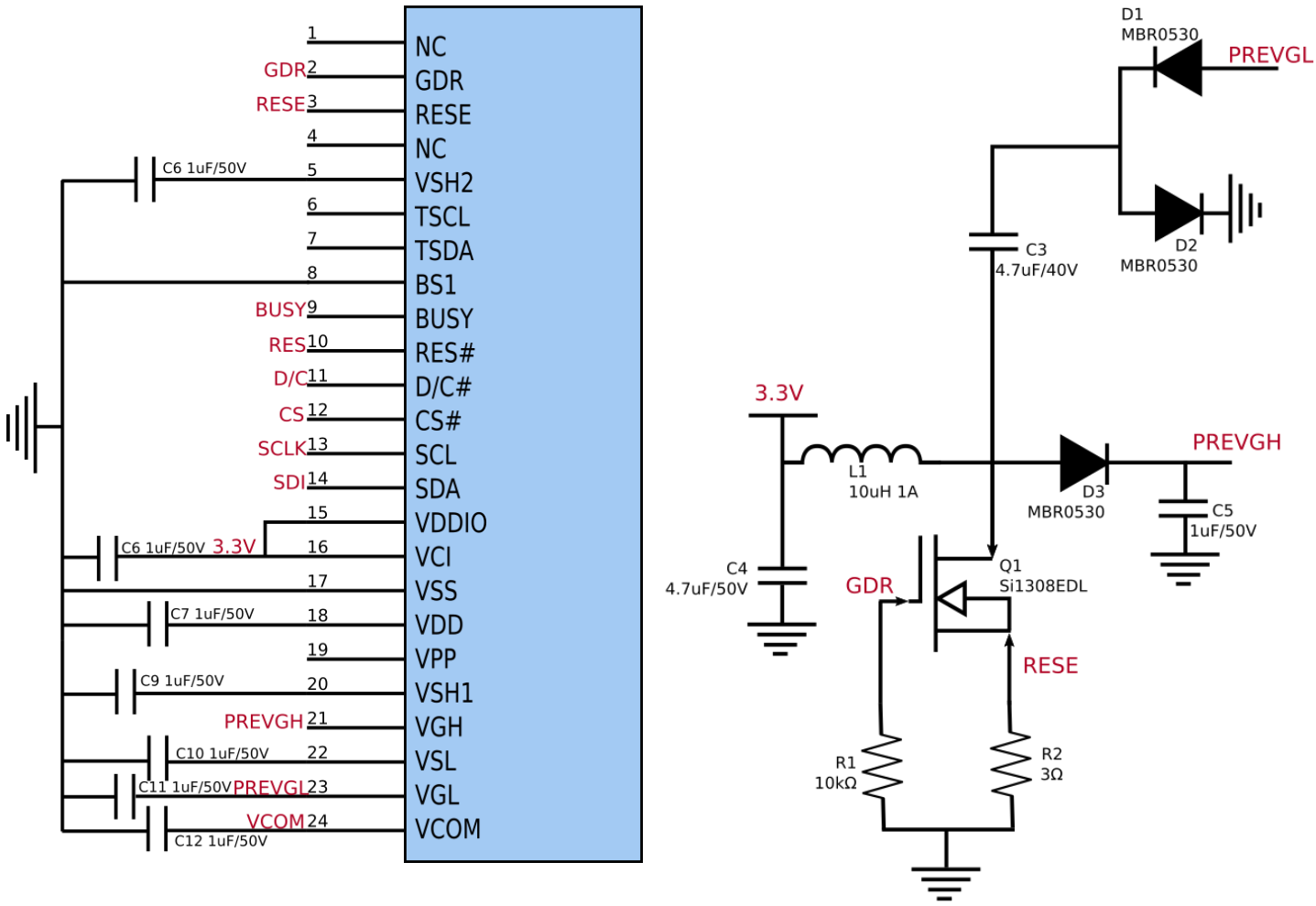
4. Mechanical Specifications

Parameter	Specifications (mm)	Specification (in)
Screen Size	39.1	1.54
Active Area	27.00 (H) × 27.00 (W)	1.06 x 1.06
Pixel Pitch	0.135 × 0.135	0.005 x 0.005
Outline Dimension	37.32 (H) × 31.80 (W) × 1.05 (D)	1.47 x 1.25 x 0.041
Weight (typical)	2.1 grams	0.074 ounces
Display Resolution	200 (H) × 200 (W)	

5. Pin Functions

Pin #	Type	Single	Description
1	-	NC	No Connection and Do Not Connect with Other NC Pins
2	O	GDR	N-Channel MOSFET Gate Drive Control
3	O	RESE	Current Sense Input for the Control Loop
4	C	NC	No Connection and Do Not Connect with Other NC Pins
5	C	VSH2	Positive Source Driving Voltage
6	O	TSCL	I^2C Interface to Digital Temperature Sensor Clock Pin
7	I/O	TSDA	I^2C Interface to Digital Temperature Sensor Data Pin
8	I	BS1	Bus Selection Pin – Low 4-Wire SPI, High 3-Wire SPI
9	O	BUSY	Busy State Output Pin – high when chip is busy
10	I	RES#	Reset Pin – active low
11	I	D/C#	Data /Command Control Pin – Data high, command low
12	I	CS#	Chip Select Input Pin - active low
13	I/O	SCL	Serial Clock Pin (SPI)
14	I/O	SDA	Serial Data Pin (SPI)
15	I	VDDIO	Power for Interface Logic Pins
16	I	VCI	Power Supply Pin for the Chip
17	-	VSS	Ground
18	C	VDD	Core Logic Power Pin
19	C	VPP	Power Supply for OTP Programming
20	C	VSH1	Positive Source Driving Voltage
21	C	VGH	Positive Gate Driving Voltage
22	C	VSL	Negative Source Driving Voltage
23	C	VGL	Negative Gate Driving Voltage
24	C	VCOM	VCOM Driving Voltage

6. Reference Circuit



7. MCU Interface

7.1. MCU Serial Peripheral Interface (4-Wire SPI)

The 4-wire SPI consists of SCL (serial clock), SDA (serial data), D/C# and CS#.

Function	CS# Pin	D/C# Pin	SCL Pin	SDA Pin
Write Command	L	L	↑	Command bit
Write Data	L	H	↑	Data bit

Note: ↑indicates rising edge of signal

SDA is shifted into an 8-bit shift register in the order of D7, D6, … D0 on the rising edge of the clock signal. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

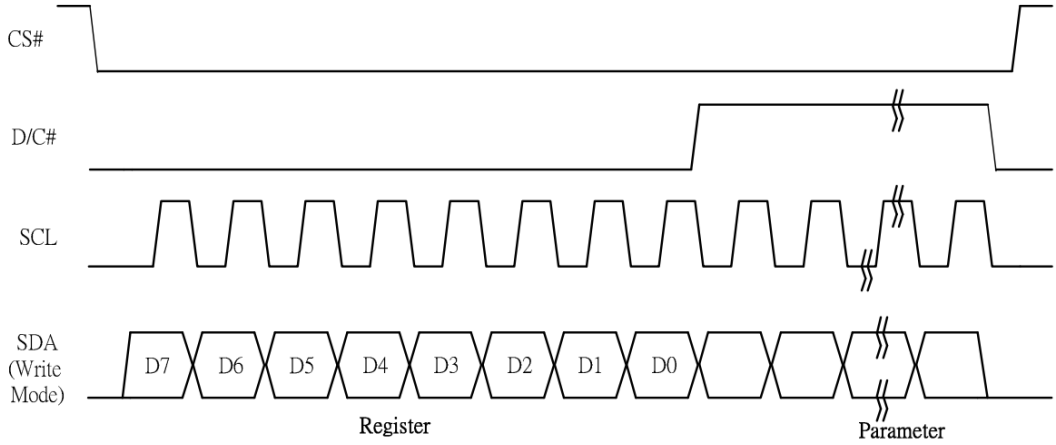


Figure: Write Procedure in 4-Wire SPI Mode

7.2. MCU Serial Peripheral Interface (3-Wire SPI)

The 3-wire serial interface consists of SCL (serial clock), SDA (serial data) and CS#.

3-wire SPI operation is similar to 4-wire, except instead of using the D/C# pin, a 9th bit is included to indicate Data or Command. The 9-bits are shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS# Pin	D/C# Pin	SCLK Pin
Write Command	L	Tie LOW	↑
Write Data	L	Tie LOW	↑

Note: ↑stands for rising edge of signal

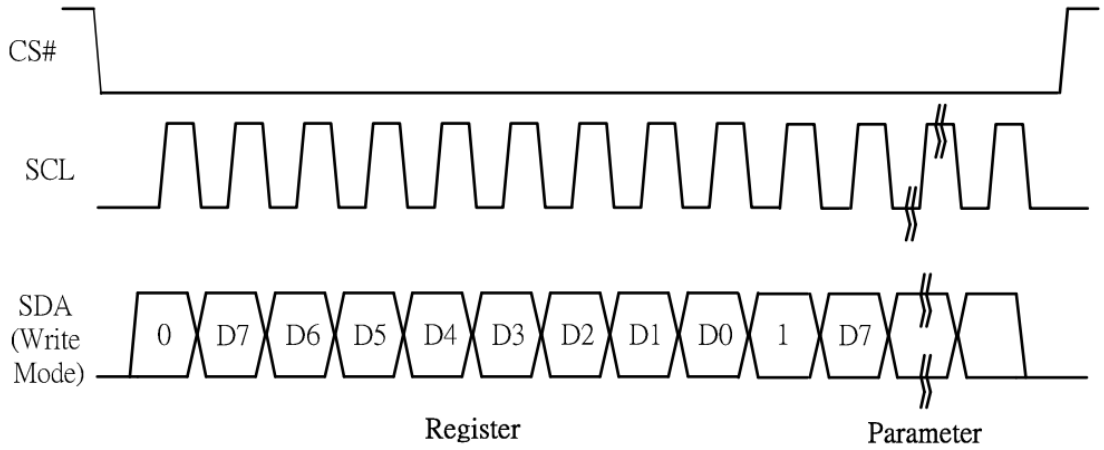


Figure: Write Procedure in 3-Wire SPI Mode

7.3. External Temperature Sensor Operation

To sense the ambient temperature, use any kind of external temperature sensor to get the temperature value then converted to hex format. Then use the SPI interface to send command 0x1A and the HEX temperature value to the module.

To convert the temperature value to hex:

- When the Temperature value MSByte bit D11 = 0, the temperature is positive and value (DegC) = + (Temperature value)/16
- When the Temperature value MSByte bit D11 = 1, the temperature is negative and value (DegC) = ~ (2's complement of Temperature value)/16

12-bit Binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

8. Command Table

<table>
<tr><th>R/W #</th><th>D/C #</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output Control</td><td rowspan="4">Gate setting
Set A[8:0] = 0C7h [POR], 200 MUX
MUX gate lines setting as (A[8:0] + 1)
Set B[2:0] = 000 [POR]
Gate scanning sequence and direction
B[2]: GD - selects the 1st output Gate
GD = 0 [POR]
G0 is the 1st gate output channel, gate output sequence is G0, G1, G2, G3,…
GD = 1
G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2,…
B[1]: SM - Changes scanning order of gate driver
SM = 0 [POR] : G0, G1, G2, G3…G199
SM = 1 : G0, G2, G4…G198, G1, G3…G199
B[0]: TB - Changes scanning direction
TB = 0 [POR] : Scan from G0 to G199
TB = 1 : Scan from G199 to G0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Gate Driving Voltage Control</td><td rowspan="2">Set Gate driving voltage
A[4:0] = 00h [POR]
VGH setting for 20V = 00h [POR] and 17h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="4">Source Driving Voltage Control</td><td rowspan="4">Set Source driving voltage
A[7:0] = 41h [POR], VSH1 at 15V
B[7:0] = A8h [POR], VSH2 at 5V
C[7:0] = 32h [POR], VSL at -15V

VSH1≥VSH2</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td><td>C0</td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Deep Sleep Mode</td><td rowspan="2"><table><tr><th>A[1:0]</th><th>Description</th></tr><tr><td>00</td><td>Normal Mode [POR]</td></tr><tr><td>01</td><td>Enter Deep Sleep Mode</td></tr></table>To exit Deep Sleep, send HWRESET to driver.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>11</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Data Entry</td><td>Define data entry sequence</td></tr>
</table>

<table>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td><td>Mode Setting</td><td>A[2:0] = 011 [POR]
A[1:0] = ID[1:0]
Address automatic increment / decrement setting.
The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address.

00 –Y decrement, X decrement,
01 –Y decrement, X increment,
10 –Y increment, X decrement,
11 –Y increment, X increment [POR]

A[2] = AM
Set the direction in which the address counter is updated automatically after data are written to the RAM.

AM= 0, the address counter is updated in the X direction. [POR]

AM = 1, the address counter is updated in the Y direction.</td></tr>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>SWRESET</td><td>Resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode
Note: RAM are unaffected by this command.</td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Activate Display Update Sequence
The Display Update Sequence Option is located at R22h.
Do not interrupt this operation to avoid corruption of panel images.</td></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="3">Display Update Control 1</td><td rowspan="3">RAM Content Option for Display Update
A[7:0] = 00h [POR]
B[7] = 00h [POR]

<table><tr><th>A[3:0]</th><th></th></tr><tr><td>000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Display Update Control 2</td><td>Display Update Sequence Option: Enable the stage for Master Activation
A[7:0] = FFh [POR]

<table><tr><th>Operating Sequence</th><th>Parameter (in Hex)</th></tr><tr><td>Enable Clock Signal</td><td>80</td></tr><tr><td>Disable Clock signal</td><td>01</td></tr><tr><td>Enable Clock Signal
→Enable Analog</td><td>C0</td></tr><tr><td>Disable Analog
→Disable clock signal</td><td>03</td></tr><tr><td>Enable Clock signal
→Load LUT with DISPLAY mode 1
→Disable clock signal</td><td>91</td></tr></table></td></tr>
</table>

0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Enable Clock signal →Load LUT with DISPLAY mode 2 →Disable clock signal: 99 Enable Clock signal →Load temperature value →Load LUT with DISPLAY mode 1 →Disable clock signal: B1 Enable Clock signal →Load temperature value →Load LUT with DISPLAY mode 2 →Disable clock signal: B9 Enable Clock signal →Enable Analog →Load LUT with DISPLAY mode 1 →Disable analog →Disable OSC: C7 Enable clock signal →Enable Analog → DISPLAY mode 2 →Disable Analog →Disable OSC: CF Enable Clock signal →Enable Analog →Load temperature value →Load LUT with DISPLAY mode 1 →Disable analog →Disable OSC: F7 Enable Clock signal →Enable Analog →Load temperature value →Load LUT with DISPLAY mode 2 →Disable analog →Disable OSC: FF
0	0	24	0	0	1	0	0	1	0	0	Write RAM	After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly. For White pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register. The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[3:0] = 9h, duration = 10s. VCOM sense duration = (A[3:0]+1) sec
0	1		0	1	0	0	A_3	A_2	A_1	A_0		

<table>
<tr><td>0</td><td>0</td><td>2A</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Program VCOM OTP</td><td>Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail.</td></tr>
<tr><td>0</td><td>0</td><td>2B</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="3">Write Register for VCOM Control</td><td rowspan="3">Reduces glitch when ACVCOM toggles. Two data bytes D04h and D63h should be set for this command.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>2C</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Write VCOM Register</td><td rowspan="2">Write VCOM register from MCU interface.
A[7:0] = 00h [POR]
<table><tr><td>A[7:0]</td><td>VCOM</td><td>A[7:0]</td><td>VC</td></tr><tr><td>08h</td><td>-0.2</td><td>44h</td><td>-1.7</td></tr><tr><td>0Ch</td><td>-0.3</td><td>18h</td><td>-1.8</td></tr><tr><td>10h</td><td>-0.4</td><td>4Ch</td><td>-1.9</td></tr><tr><td>14h</td><td>-0.5</td><td>50h</td><td>-2</td></tr><tr><td>18h</td><td>-0.6</td><td>54h</td><td>-2.1</td></tr><tr><td>1Ch</td><td>-0.7</td><td>58h</td><td>-2.2</td></tr><tr><td>20h</td><td>-0.8</td><td>5Ch</td><td>-2.3</td></tr><tr><td>24h</td><td>-0.9</td><td>60h</td><td>-2.4</td></tr><tr><td>28h</td><td>-1</td><td>64h</td><td>-2.5</td></tr><tr><td>2Ch</td><td>-1.1</td><td>68h</td><td>-2.6</td></tr><tr><td>30h</td><td>-1.2</td><td>6Ch</td><td>-2.7</td></tr><tr><td>34h</td><td>-1.3</td><td>70h</td><td>-2.8</td></tr><tr><td>38h</td><td>-1.4</td><td>74h</td><td>-2.9</td></tr><tr><td>3Ch</td><td>-1.5</td><td>78h</td><td>-3</td></tr><tr><td>40h</td><td>-1.6</td><td>Other</td><td>NA</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>2D</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td rowspan="12">OTP Register Read for Display Option</td><td rowspan="12">Read Register for Display Option:
A[7:0]: VCOM OTP Selection (Command 0x37, Byte A)
B[7:0]: VCOM Register (Command 0x2C)
C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes]
H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>C_7</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>D_7</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>E_7</td><td>E_6</td><td>E_5</td><td>E_4</td><td>E_3</td><td>E_2</td><td>E_1</td><td>E_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>F_7</td><td>F_6</td><td>F_5</td><td>F_4</td><td>F_3</td><td>F_2</td><td>F_1</td><td>F_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>G_7</td><td>G_6</td><td>G_5</td><td>G_4</td><td>G_3</td><td>G_2</td><td>G_1</td><td>G_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>H_7</td><td>H_6</td><td>H_5</td><td>H_4</td><td>H_3</td><td>H_2</td><td>H_1</td><td>H_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>I_7</td><td>I_6</td><td>I_5</td><td>I_4</td><td>I_3</td><td>I_2</td><td>I_1</td><td>I_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>J_7</td><td>J_6</td><td>J_5</td><td>J_4</td><td>J_3</td><td>J_2</td><td>J_1</td><td>J_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>K_7</td><td>K_6</td><td>K_5</td><td>K_4</td><td>K_3</td><td>K_2</td><td>K_1</td><td>K_0</td></tr>
<tr><td>0</td><td>0</td><td>2E</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td rowspan="10">User ID Read</td><td rowspan="10">Read 10 Byte User ID stored in OTP:
A[7:0]]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>C_7</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>D_7</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>E_7</td><td>E_6</td><td>E_5</td><td>E_4</td><td>E_3</td><td>E_2</td><td>E_1</td><td>E_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>F_7</td><td>F_6</td><td>F_5</td><td>F_4</td><td>F_3</td><td>F_2</td><td>F_1</td><td>F_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>G_7</td><td>G_6</td><td>G_5</td><td>G_4</td><td>G_3</td><td>G_2</td><td>G_1</td><td>G_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>H_7</td><td>H_6</td><td>H_5</td><td>H_4</td><td>H_3</td><td>H_2</td><td>H_1</td><td>H_0</td></tr>
</table>

1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail.
0	0	32	0	0	1	1	0	0	1	0	Write LUT Register	Write LUT register from MCU interface [153 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], and FR[n]
0 0 0 … 0 0	1 1 1 … 1 1	LUT [30 bytes]										
0	0	36	0	0	1	1	0	1	1	0	Program OTP	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored in OTP
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	39	0	0	1	1	1	0	0	1	OTP Program Mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: follow the reference code sequences EXACTLY
0	1		0	0	0	0	0	0	A_1	A_0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0] = 00h B[4:0] = 18h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set RAM Y - address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0] = 0C7h B[8:0] = 0000h
0	1		A_7	A_6	A_5	A_4	0	0	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		

0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0] = 00h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0] = 0C7h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		

9. Maximum Ratings

9.1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.5 to +4.0	V
Operating Temp. range	T_{OPR}	0 to +50	°C
Storage Temp. range	T_{STG}	-25 to +60	°C
Humidity Range	RH	40~70	%
IMPORTANT: A UV protective film is recommended when operating the module in direct sunlight.			

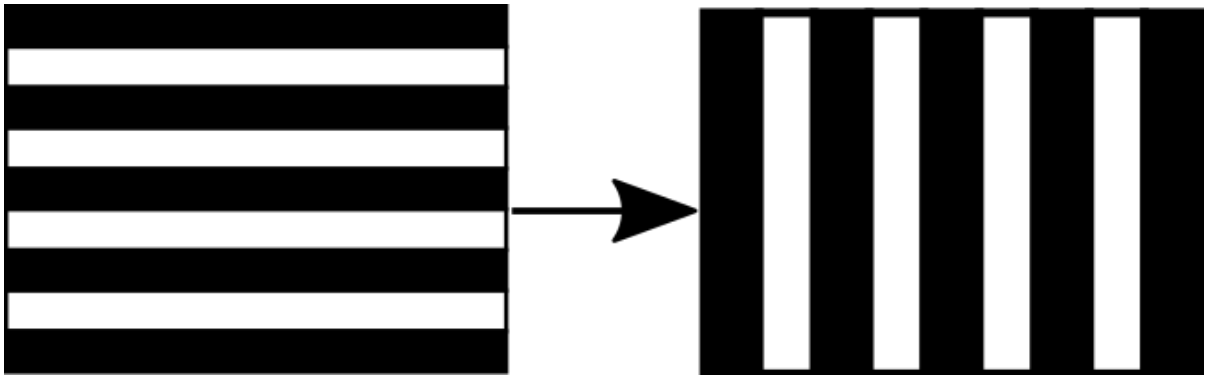
9.2. DC Characteristics

The following specifications apply for: V_{SS} = 0V, V_{CI} = 3.3V, T_{OPR} = 25°C

Parameter	Symbol	Conditions	Module Pin	Min	Typ	Max	Unit
Logic Supply Voltage	V_{CI}	-	V_{CI}	2.2	3.3	3.7	V
High Level Input Voltage	V_{IH}	-	SCL, SDA, CS#, D/C#, RES#, BS1	0.8V_{DDIO}	-	V_{CI}	V
Low Level Input Voltage	V_{IL}	-		-	-	0.2V_{DDIO}	V
High Level Output Voltage	V_{OH}	IOH= -100uA	BUSY	0.9V_{DDIO}	-	-	V
Low Level Output Voltage	V_{OL}	IOL= 100uA		-	-	0.1V_{DDIO}	V
Module Operating Current	I_{UPDATE}	-	-	-	1.5	-	mA
Deep Sleep Mode	I_{SLEEP}	V_{CI}=3.3V	-	-	-	2	µA

The typical power consumption is measured with the following pattern transition: from horizontal pattern to vertical pattern, shown below.

Note: The standby power is the consumed power when the panel controller is in standby mode. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Crystalfontz. V_{COM} is recommended to be set in the range of assigned value ±0.1V.



10. Serial Peripheral Interface Timing

The following specifications apply for: V_{SS} = 0V, V_{CI} = 2.2V to 3.7V, T_{OPR} = 25°C, write mode. Timing given is from 20% to 80% of V_{DDIO}-V_{SS}

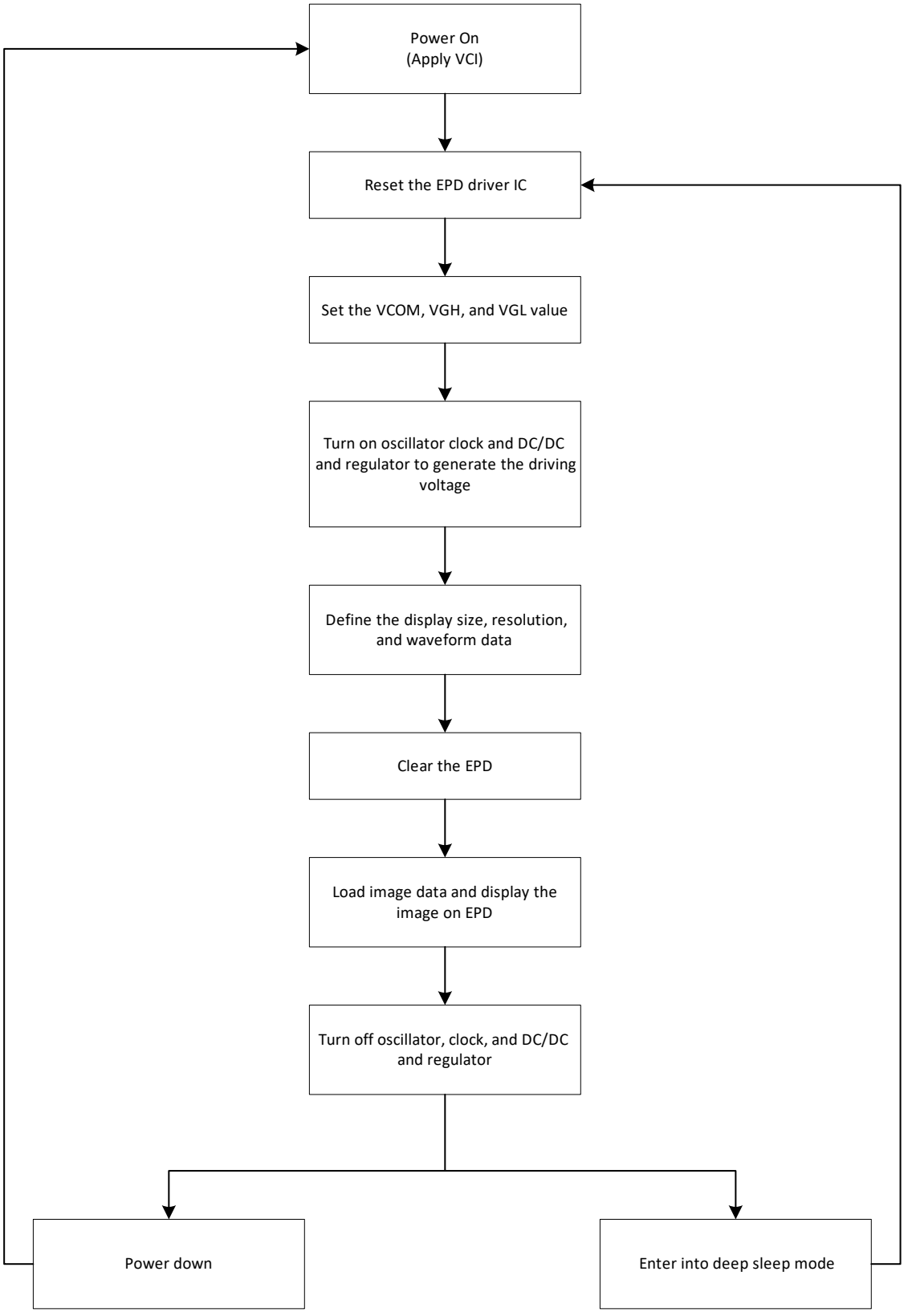
Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	Clock Cycle Frequency	-	-	20	MHz
t_{CSSU}	Chip Select Setup Time	20	-	-	ns
t_{CSHLD}	Chip Select Hold Time	20	-	-	ns
t_{CSHIGH}	Chip Select HIGH	120	-	-	ns
t_{SCLLOW}	Clock Low Time	25	-	-	ns
$t_{SCLHIGH}$	Clock High Time	25	-	-	ns
t_{SDASU}	SDA Setup Time	10	-	-	ns
t_{SDAHLD}	SDA Hold Time	40	-	-	ns

11. Power Consumption

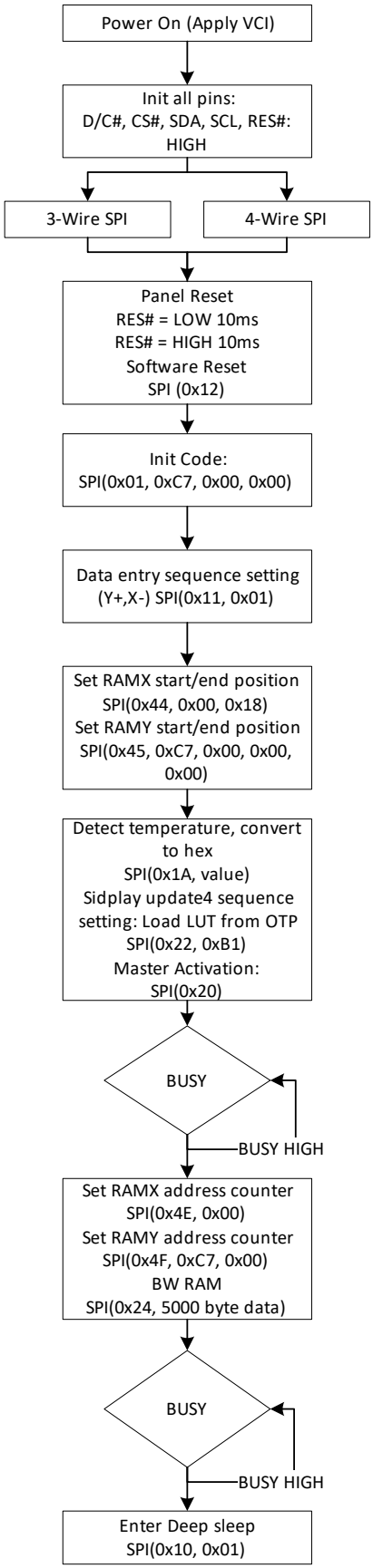
Parameter	Symbol	Condition	Typ	Max	Unit
Panel power consumption during Update	-	25°C	8	-	mA
Deep Sleep Mode	-	25°C	2	-	µA

12. Typical Operating Sequence

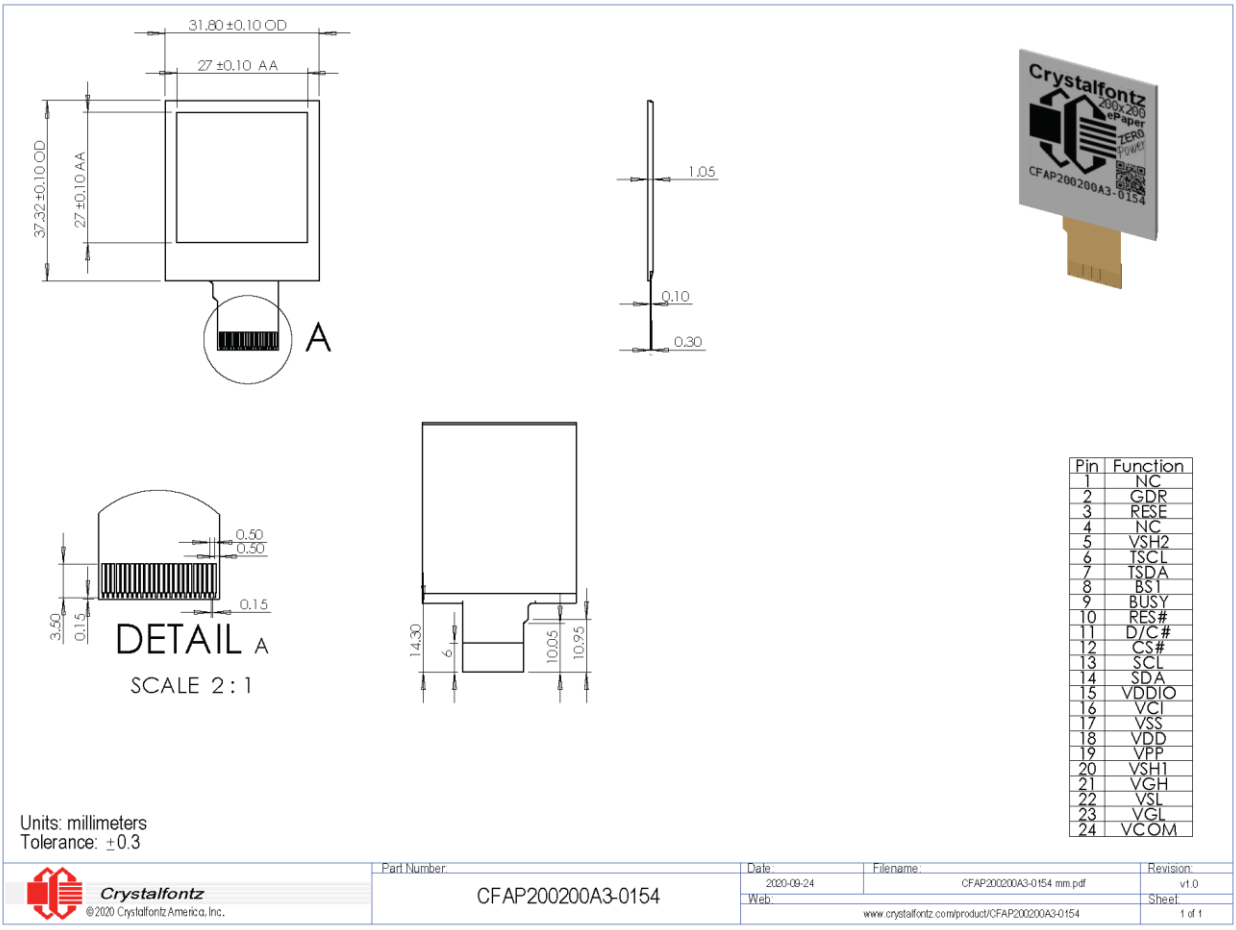
12.1. Normal Operation Flow



12.2. Refernce Program Code



13. Optical Characteristics



13.1. Specifications

Measurements are made with the illumination under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

Symbol	Parameter	Conditions	Min	Type	Max	Unit	Note
R	Reflectance	White	30	35	-	%	13-1
Gn	2Gray Level	-	-	DS＋(WS-DS) x n (m-1)	-	L*	13-2
CR	Contrast Ratio	Indoor	-	10	-	-	-
Panel Life	-	0°C~50°C	-	5 years	-	-	13-3

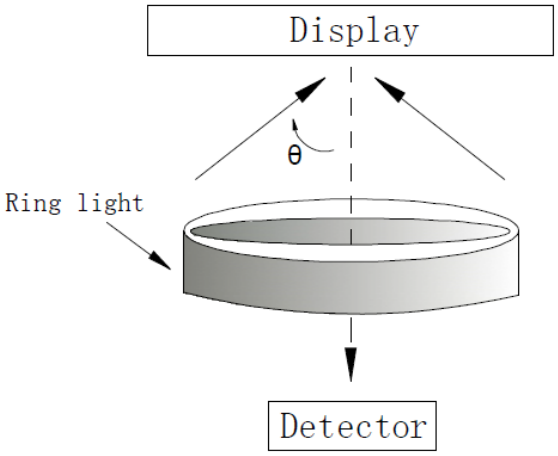
Note (13-1): Luminance meter: Eye – One Pro Spectrophotometer
Note (13-2): WS: White State, DS: Dark State, m: 2
Note (13-3): Panel life is not guaranteed when used outside of conditions described herein, or outside of the 45-70%RH. Display must be updated at least once per day.

13.2. Definition of Contrast Ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) ():

R1: White Reflectance Rd: Dark Reflectance

CR = R1/Rd

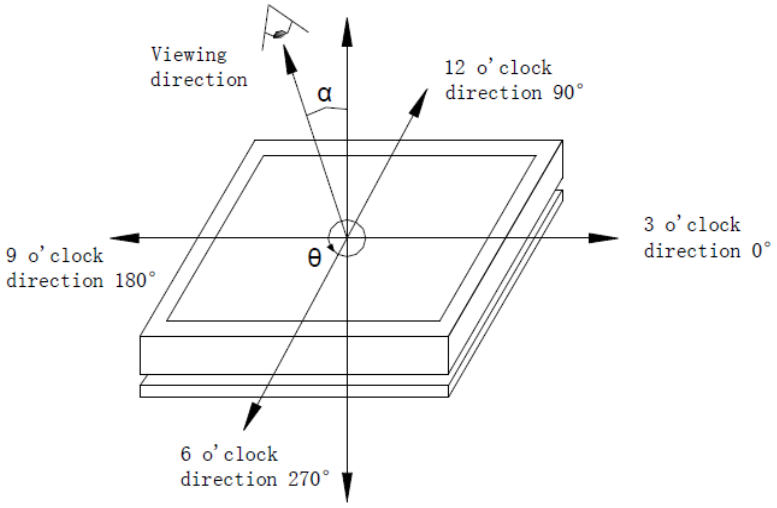


13.3. Reflection Ratio

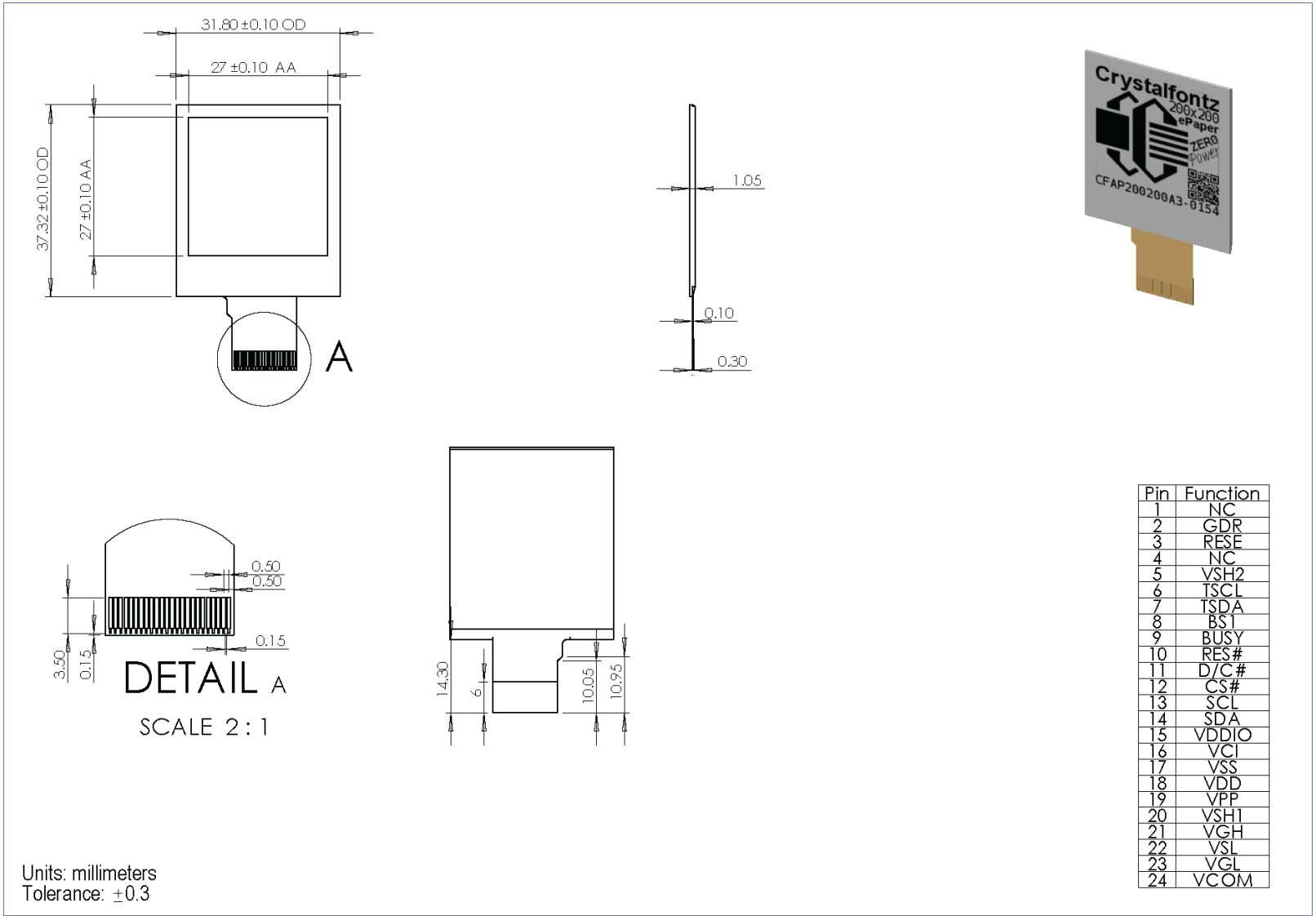
The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{CENTER} / $L_{WHITE\ BOARD}$)

L_{CENTER} is the luminance measured at center in a white area (R=G =B=1). $L_{WHITE\ BOARD}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



14. Mechanical Drawing



15. ePaper Breakout Board Schematic