Crystalfontz America, Incorporated

GRAPHIC TFT MODULE DATA SHEET

photo is CFAF320480C4-035T-TS with touch screen

Data Sheet Release 2013-05-06 for the CFAF320480C4-035T Family:
CFAF320480C4-035T (no touch screen)
CFAF320480C4-035T-TS (with touch screen)

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Data Sheet Revision History

Data Sheet Release: 2013-05-06
Improved information in OPTICAL SPECIFICATIONS (Pg. 18) and LED Backlight Characteristics (Pg. 20).
Modules have not changed.

Data Sheet Release: 2013-05-03
First Data Sheet for the new CFAF320480C4-035T Family of modules.

Hardware Revisions

For information about CFAF320480C4-035T Family hardware revisions, see the Part Change Notifications (PCNs) under “News” in our website’s navigation bar.

About Variations

We work continuously to improve our products. Because display technologies are quickly evolving, these products may have component or process changes. Slight variations (for example, contrast, color, or intensity) between lots are normal. If you need the highest consistency, whenever possible, order and arrange delivery for your production runs at one time so your displays will be from the same lot.

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CONTENTS

LIST OF FIGURES

MAIN FEATURES

- Full-color (262K) 320xRGBx480 display consists of a TFT panel, integrated controller, an FPC (Flexible Printed Circuit) tail, and a white LED backlight.
  - *CFAF320480C4-035T:* no touch screen.
  - *CFAF320480C4-035T-TS*: with an integrated 4-wire analog touch screen.
- Module dimensions
  - Active Area
    - Diagonal is 88.90 millimeters
      Inches = 3.5-inches
    - Active area width and height is 48.96 (W) x 73.44 (H) millimeters.
      Inches = 1.93" (W) x 2.89" (H).
  - Overall module width and height:
    - FPC *unfolded* is 55.50 (W) x 127.55 (H) mm (Shape and length of FPC may vary slightly.)
      Inches = 2.19" (W) x 5.02" (H)
    - FPC *folded* is 55.50 (W) x (H) 85.96 mm
      Inches = 2.19" (W) x 3.38" (H).
  - Overall module depth:
    - *CFAF320480C4-035T:* maximum is 2.85 (D) mm.
      Inches = 0.11" (D).
    - *CFAF320480C4-035T-TS*: maximum is 4.05 (D) mm.
      Inches = 0.16" (D).
- Integrated Himax HX8357-B or compatible controller. See APPENDIX C: HIMAX HX8357-B CONTROLLER DATA SHEET (Pg. 34).
- Requires only a single source 3.0v for both power supply and logic.
- Interface modes:
  - 8-bit, 9-bit, 16-bit or 18-bit parallel interface to host.
  - 16-bit or 18-bit "DOTCLK" RGB interface.
  - 3- or 4-wire SPI to host.
- The 50-pin FPC mates with standard 0.5mm ZIF sockets such as HFJ150CT-ND and HFK150CT-ND from Digi-Key.
- Transmissive display with edge-lit LED backlight (6 white LEDs). The white LED backlight has anode (A,+) and cathode (K -) pins brought out on the FPC.
- 6:00 o'clock viewing angle (polarizer viewing direction).
- Wide temperature operation is from -20°C to +70°C.
- This TFT display is included in a kit with a powerful ARM9-based Linux CFA10036 SOM (System On Module), a small OLED for status messages and debugging, the CFA10037 development board with a large prototype area (on 0.1" centers), and the CFA10055 carrier board for the TFT. For more information, see ACCESSORIES ANS KITS (Pg. 6).
- RoHs compliant. When available, Certificate of Compliance for ISO, RoHS, and REACH will be under the web page's Doc/Files tab.

EXPLANATION OF PART NUMBER CODES IN THIS DATA SHEET

CFA	F	320	480	C	-	035	T	-	x
❶	❷	❸	❹	❺		❻	❼		❽

❶	**Brand**	Crystalfontz America, Inc.
❷	**Display Type**	F – TFT
❸	**Number of Pixels (Width)**	320 pixels
❹	**Number of Pixels (Height)**	480 pixels
❺	**Model Identifier**	C
❻	**Diagonal Dimension**	035 – 3.5-inch diagonal
❼	**Backlight Type & Color**	T – white LED backlight
❽	**Configuration Codes (*x*)**	(blank) – no touch screen TS – with touch screen

ACCESSORIES ANS KITS

Accessories and kits with the CFAF320480C4-035T Family are described below.

ACCESSORIES

CFA10036 SOM (System On Module)

The CFA10036 is a small, highly functional ARM9-based Linux SOM (System On Module) shipped with a full Linux operating system. Because a full Linux mainline kernel is already ported to the CFA10036, you can devote your resources to applications in the languages of your choice. It is low cost, easy to use, and has lots of GPIO.

CFAL12832D-B OLED

The CFAL12832D-B 128x32 OLED graphics module displays light (near-white) characters on a dark (near-black) background. Less than 0.5-inch high (11.5 mm), the CFAL12832D-B mounts onto the CFA10036 with a ZIF connector. (See KIT365B3758 photo.) The OLED is useful for status messages and debugging.

CFA10037 Development Board

To easily prototype a CFA10036 SOM based design, we offer the CFA10037 development board.The CFA10037 gives access to all the port pins of the CFA10036, including all the port pins of its Freescale i.MX28 processor (i.MX283 or i.MX287). The CFA10037 has a generous prototype area with well-decoupled power distribution in a prototype-friendly 0.1" center format.

Carrier Boards for CFAF320480C4-035T and CFAF320480C4-035T-TS

A carrier board with the TFT display can be mounted to the CFA10037 development board, along with the CFA10036 SOM and the optional CFAL12832D-B OLED.

Carrier Board	TFT mounted on top of Carrier Board	
CFA100554	CFAF320480C4-035T	
CFA100558	CFAF320480C4-035T-TS *(Shown in photo.)*	

USB633 TTL-To-USB Converter

The USB633 is a small PCB that can mount on the CFA10036 SOM's DUART for debugging and early board bring up. Dedicated Rx/Tx debug UART port with 0.1" centers. You can connect a USB633 TTL-to-USB converter to the dedicated DUART.

CFA10040PWR

The CFA10040PWR is a110 VAC +5v wall power supply that can be used to power the CFA10037 development board. Cord length is ~63 inches.

WR-USB-Y03 Cable

The WR-USB-Y03 is about 6-feet long. Connect the cable's smaller 2 mm female USB connector to the CFA10037's USB connector. Connect the cable's larger USB-A female connector to your host's USB-A connector.

WR-JMPY-40 and WR-JMPY-41

Package of 20 female-to -female jumper wires, useful to connect to the optional CFA10037 prototype area headers. Assorted colors.

- WR-JMPY-40: Seven inches long *(shown in photo above).*
- WR-JMPY-41*:* Four inches long.

KITS

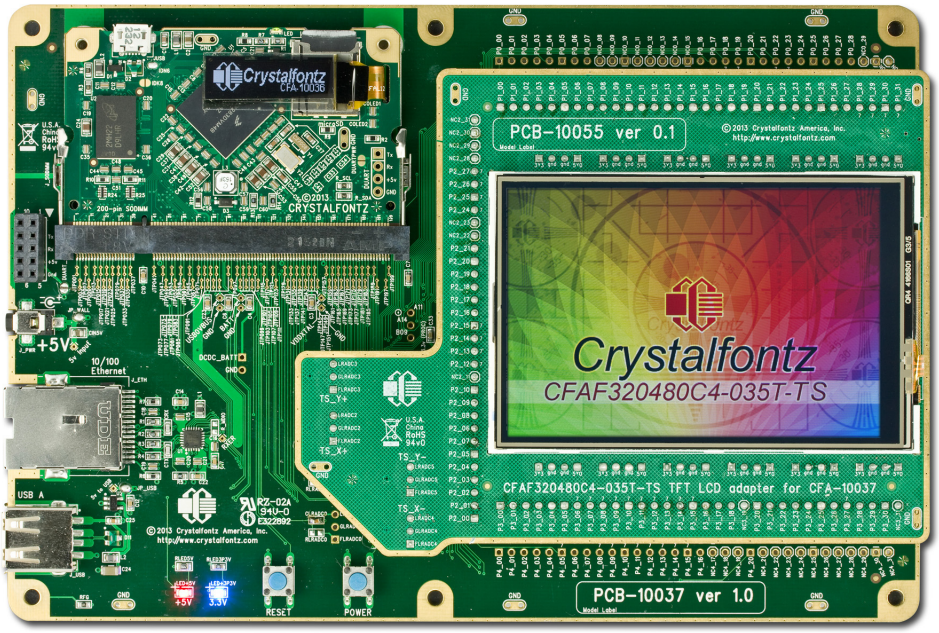

Figure 1. KIT365B3758

Kit	with SOM & Development Board	with TFT	with Carrier Board
KIT365B3754	CFA10036 SOM with Freescale i.MX283 processor mounted on the CFA10037 development board	CFAF320480C4-035T	CFA100554
KIT365B3758		CFAF320480C4-035T-TS *(Photo shows touch screen.)*	CFA100558

MECHANICAL SPECIFICATIONS

PHYSICAL CHARACTERISTICS

ITEM	SPECIFICATION
Number of Pixels	320 x RGB x 480 pixels
Pixel Pitch	0.051 (W) x 0.051 (H) mm
Active Area	
Active Area Diagonal	Millimeters: 88.90 mm Inches: 3.50"
Active Area Width and Height	Millimeters: 48.96 (W) x 73.44 (H) mm Inches: 1.93" (W) x 2.89" (H)
Module Outline Dimensions	
Overall module width and height with FPC unfolded*	Millimeters: 55.50 (W) x 127.55 (H) mm Inches: 2.19" (W) x 5.02" (H)
Overall module width and height with FPC folded	Millimeters: 55.50 (W) x 85.96 (H) mm Inches: 2.19" (W) x 3.38" (H)
**For reference only. Shape and length of FPC may vary slightly.*	
Module Depth Maximum	*CFAF320480C4-035T* Millimeters: 2.85 (D) mm Inches: 0.11" (D) *CFAF320480C4-035T-TS* Millimeters: 4.05 (D) mm Inches: 0.16" (D)
FPC Bend Radius	>R.95 mm
Weight	*CFAF320480C4-035T* 19 grams *CFAF320480C4-035T-TS* 28 grams

MODULE OUTLINE DRAWINGS

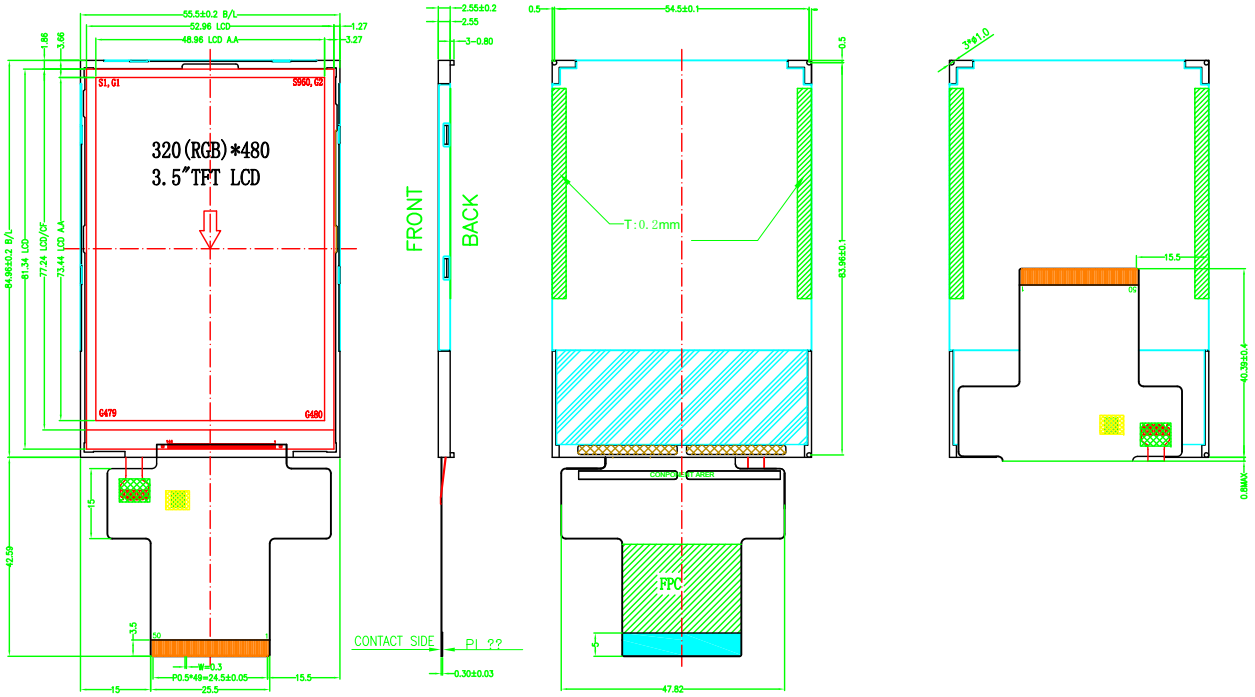

Figure 2. CFAF320480C4-035T Module Outline Drawing

Note:

1. Tolerance is ±0.3 mm unless specified.
2. FPC = Flexible Printed Circuit. Length is for reference only.
3. Diagonal = 3.5 inches.

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Part No.(s):	Scale:	Drawing Number:
CFA320480C4-035T	Not to scale	
	Units: Millimeters	Date: 2013-04-29

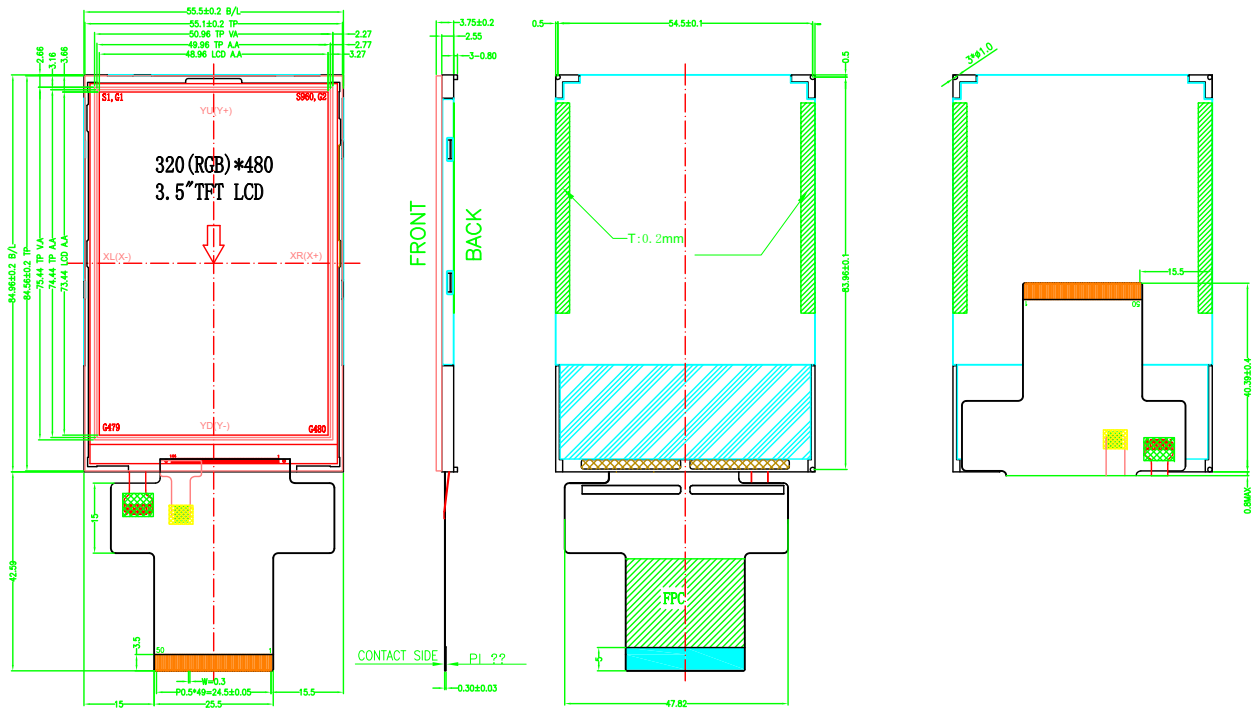


Figure 3. CFAF320480C4-035T-TS Module Outline Drawing

Note:

1. Tolerance is ±0.3 mm unless specified.
2. FPC = Flexible Printed Circuit. Length is for reference only.
3. Diagonal = 3.5 inches.

Crystalfontz America, Inc. www.crystalfontz.com/products/	Part No.(s): CFA320480C4-035T-TS	Scale: Not to scale	Drawing Number:
		Units: Millimeters	Date: 2013-04-29

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature (Ta) = 25°C			
Absolute Maximum Ratings	**Symbol**	**Minimum**	**Maximum**
Digital Logic Supply and Input/Output Supply	$V_{LOGIC\ I/O}$	-0.3v	+4.6v
Analog Supply	V_{ANALOG}		
Operating Temperature*	T_{OP}	-20°C	+70°C
Storage Temperature*	T_{ST}	-30°C	+80°C
Humidity	RH	0%	90%
Input voltage	V_{IN}	-0.3v	$V_{LOGIC\ I/O}$+0.3v

Caution
These are stress ratings only. Functional operation of the module at these or any other conditions beyond those listed under Recommended DC Characteristics (3.0v Operation) (Pg. 13) is not implied.

Extended exposure to the absolute maximum ratings listed above may affect device reliability. Stresses beyond those listed above can cause permanent damage.

RECOMMENDED DC CHARACTERISTICS (3.0V OPERATION)

RECOMMENDED DC CHARACTERISTICS	SYMBOL	MINIMUM	TYPICAL	MAXIMUM
Digital Logic Supply and Input/Output Supply	$V_{LOGIC\ I/O}$	+1.7v	+1.8v / +3.3v	+3.3v
Analog Supply	V_{ANALOG}	+2.5v	+3.3v	
Current consumption for Normal Operation	V_{OP}	—	10 mA	15 mA
Input High Voltage	V_{IH}	+0.7v * $V_{LOGIC\ I/O}$ for $V_{LOGIC\ I/O}$ = +1.8v V_{IH} = +0.7v * +1.8v = +1.26v for $V_{LOGIC\ I/O}$ = +3.3v V_{IH} = +0.7v * +3.3v = +2.31v	—	$V_{LOGIC\ I/O}$
Input Low Voltage	V_{IL}	0v (GND)	—	+0.3v * $V_{LOGIC\ I/O}$ for $V_{LOGIC\ I/O}$ = +1.8v V_{IL} = +0.3v * +1.8v = 0.54v for $V_{LOGIC\ I/O}$ = +3.3v V_{IL} = +0.3v * +3.3v = +0.99v
Output High Voltage @0.1mA	V_{OH}	+0.8v * $V_{LOGIC\ I/O}$ for $V_{LOGIC\ I/O}$ = +1.8v V_{OH}= +0.8v * +1.8v = +1.44v for $V_{LOGIC\ I/O}$ = +3.3v V_{OH}= +0.8v * +3.3v = +2.64v	—	$V_{LOGIC\ I/O}$
Output Low Voltage @0.1mA	V_{OL}	0v (GND)	—	+0.2v * $V_{LOGIC\ I/O}$ for $V_{LOGIC\ I/O}$ = +1.8v V_{OL} = +0.2v * +1.8v = 0.36v for $V_{LOGIC\ I/O}$ = +3.3v V_{OL} = +0.2v * +3.3v = +0.66v

This is a summary of the module's major operating parameters. For detailed information see APPENDIX C: HIMAX HX8357-B CONTROLLER DATA SHEET (Pg. 34).

DETAILS OF INTERFACE PIN FUNCTION

<table>
<tr><th>PIN</th><th>SIGNAL</th><th>LEVEL</th><th>DIRECTION</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>GND</td><td>0v</td><td></td><td>Ground. Must be connected to an external ground.</td></tr>
<tr><td>2-3</td><td>$V_{LOGIC\ I/O}$</td><td>1.65v to 3.3v</td><td>I</td><td>Digital Logic Supply and Input/Output Supply</td></tr>
<tr><td>4-5</td><td>V_{ANALOG}</td><td>+2.5v to +3.3v</td><td>I</td><td>Analog supply,</td></tr>
<tr><td>6
7
8</td><td>IM0
IM1
IM2</td><td></td><td>I</td><td>
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface Mode</th><th>DB Pins In Use</th></tr>
<tr><td colspan="5">Parallel (also known as DOTCLK or DPI) Interface</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>18-bit RGB / DPI</td><td>DB17-BD0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>9-bit RGB / DPI</td><td>DB8-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>16-bit RGB / DPI</td><td>DB15-DB0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8-bit RGB / DPI</td><td>DB7-DB0</td></tr>
<tr><td colspan="5">3 or 4-wire SPI</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-wire, 9-bit SPI</td><td>SDI, SCL, CS</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4-wire, 8-bit SPI</td><td>SDI, SCL,CS, RS</td></tr>
<tr><td colspan="5">Note: If pin is not used, tie to GND or make no connection.</td></tr>
</table>
DPI is Display Pixel Interface.
</td></tr>
<tr><td>9</td><td>$\overline{RST}$</td><td>L</td><td>I</td><td>Reset signal.
Low: Display controller is reset. The $\overline{RST}$ pin should be pulsed low shortly after power is applied.
High: The $\overline{RST}$ pin should be brought high ($V_{LOGIC\ I/O}$) for normal operation.</td></tr>
<tr><td>10</td><td>V_{SYNC}</td><td></td><td rowspan="2">I</td><td rowspan="2">Vertical and Horizontal frame synchronizing signal used for RGB / DPI mode.
The pin should be pulled high ($V_{LOGIC\ I/O}$) when not in use.</td></tr>
<tr><td>11</td><td>H_{SYNC}</td><td></td></tr>
<tr><td>12</td><td>P_{CLK}</td><td>H/L</td><td>I</td><td>Pixel Clock Signal for RGB / DPI mode.
The pin should be pulled low when not in use.</td></tr>
<tr><td>13</td><td>DE</td><td>H/L</td><td>I/O</td><td>Data Enable signal for RGB / DPI mode.
The pin should be pulled low when not in use.</td></tr>
</table>

PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION (Continued)
14-31	DB17-DB0	H/L	I/O	*In MIPI databus interface mode, DB7-DB0 are used like:* 18-bit bidirectional data bus. 8-bit bus: use DB7-DB0 9-bit bus: use DB8-DB0 6-bit bus: use DB15-DB0 8-bit bus: use DB17-DB0 *In MIPI DPI interface mode, DB17-DB0 are treated as 18-bit bus* *RGB data bus* 6-bit bus: use DB5-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0 If not used: please connect to V_{SSD}. **MIPI** is **M**obile **I**ndustry **P**rocessor **I**nterface. See MIPI Alliance.
32	GND	0v		Ground. Must be connected to an external ground.
33	MISO		O	SPI data signal: **M**aster **I**n **S**lave **O**ut. If unused, leave disconnected / floating.
34	MOSI		I	SPI data signal: **M**aster **O**ut **S**lave **I**n. The data is received on the rising edge of the SCK signal. If unused, tie to V_{SSD}.
35	$\overline{RD}$		I	DBI Type-B: Serves as a read signal and read data at the low level. If unused, tie to $V_{LOGIC\ I/O}$.
36	$\overline{WR}$_SCK		I	*DBI Type-B:* Serves as a write signal and write data at the low level. *DBI Type-C:* Serves as SCK (Serial Clock). If unused, tie to $V_{LOGIC\ I/O}$.
37	D/$\overline{C}$	H/L	I	Data/Command control. Determines whether data bits are data or command. *1 – High*: Addresses the data register. *0 – Low:* Addresses the command register. If unused, tie to $V_{LOGIC\ I/O}$.
38	$\overline{CS}$	H/L	I	Chip select input. *Low:* Controller chip is selected. Communications with host is possible. *High:* Controller chip is not selected. Host interface signals are ignored by the controller.
39-42	See description column			*CFAF320480C4-035T* (no touch screen): No Connection. *CFAF320480C4-035T-TS* (with touch screen): XR(X+): right YD(Y-): down XL(X-): left YU(Y+): up

PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION (Continued)
43	A1 (LED +)			Common supply pin for LEDs. “A” (anode) or “+” of LED backlight.
44-49	LEDK1-LEDK6 (LED -)			Individual supply pins for LED. “K” (cathode or kathode for German and original Greek spelling) or “-” of LED backlight.
50	GND			Ground.
For backlight connections, please refer to LED Backlight Characteristics (Pg. 20).				

ADDITIONAL INFORMATION ON INTERFACE TYPES

- I want to display video. Which interface is faster, SPI or parallel?

  The SPI interface is a clocked interface. Each command or data bit is clocked. With the 18-bit parallel interface, you are able to pass 18 bits of command or data at a time. Using the same controller at the same clock speed, the parallel interface will always be faster.

- What if I need RS-232 serial interface?

  Three-wire or four-wire SPI interface is not RS-232 but does not require the control lines that the 8-, 9-, of 16-bit interfaces do.

ABOUT THE 4-WIRE ANALOG RESISTIVE TOUCH SCREEN

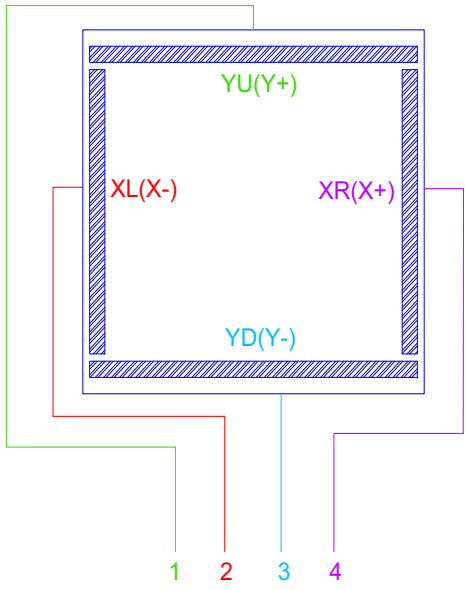


Figure 4. Touch Screen Connections

The touch screen must be driven in one direction, then read in the other direction.

- ❑ Typically, the kind of microcontroller that supports the RGB / DPI interface (ARM9, etc) will also have ADC pins that can be used directly to read the touch screen.
- ❑ TI (Texas Instruments) makes I^2C / SPI and low level touch screen controllers. Typical: www.ti.com/product/tsc2046e.
- ❑ Some microcontrollers have analog inputs that may work directly. TSHARC (www.tsharc.com) makes a high-level controller from a preprogrammed PIC microcontroller.

Basic Concept

Put a gradient across one set of electrodes. Set both electrodes as digital outputs, driving one high and the other one low. Look at either of the *other* set of electrodes (both set as inputs, at least one analog). The analog input will pick up the voltage of the gradient at the contact point. To read the other channel, rotate the whole process 90 degrees.

You may need to address other factors, including references, calibration, drift, non-contact, detecting "taps", and "double-taps".

More Information

- ❑ A comparison of three types of touch screens: www.howstuffworks.com/question716.htm.
- ❑ An introductory explanation of how four-wire resistive touch screens work: www.elotouch.com/Technologies/AT4/howitworks.asp.
- ❑ Information on the structure of a resistive touch screen: www.dmccoltd.com/english/tecnical/logs/tec20041126_a.asp.
- ❑ Another source on resistive touch screen construction: http://www.ti.com/lit/an/slyt209a/slyt209a.pdf.

ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and is susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other static sensitive devices such as expansion cards, motherboards, or integrated circuits. Ground your body, work surfaces, and equipment.

OPTICAL SPECIFICATIONS

Ambient Temperature (Ta) = 25°C, Maximum 75% Relative Humidity					
ITEM	SYMBOL	ADDITIONAL TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM
Color Depth				262K	
Contrast Ratio (CR)[1]		θ = φ - 0°		500	
TFT Response Time[2]	Tr			5 ms	
	Tf			15 ms	
Red Chromaticity	Rx		0.611	0.641	0.671
	Ry		0.290	0.320	0.350
Green Chromaticity	Gx		0.270	0.300	0.330
	Gy		0.536	0.566	0.596
Blue Chromaticity	Bx		0.104	0.134	0.164
	By		0.098	0.128	0.158
White Chromaticity	Wx		0.267	0.297	0.327
	Wy		0.301	0.331	0.361
Viewing Angle, Horizontal	θ_{X+}	Center CR≥10		70 degrees	
	θ_{X-}			70 degrees	
Viewing Angle, Vertical	θ_{Y+}			60 degrees	
	θ_{Y-}			60 degrees	
Viewing Direction				6:00	

[1] *Contrast Ratio = (brightness with pixels light)/(brightness with pixels dark).*

[2] *Response Time: The amount of time it takes a pixel to change from active to inactive or back again.Tr = T rise, Tf = T fall.*

Definition of Response Time (Tr, Tf)

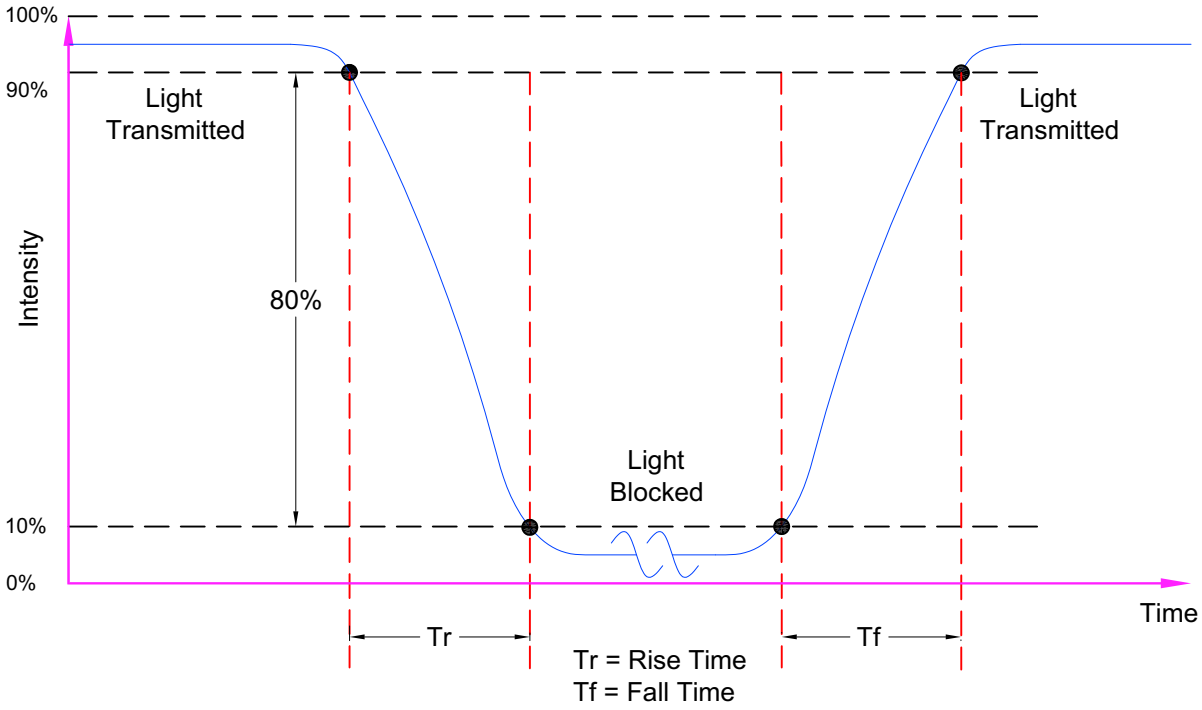


Figure 5. Definition of Response Time (Tr, Tf)

Definition of Vertical and Horizontal Viewing Angles (CR≥2)

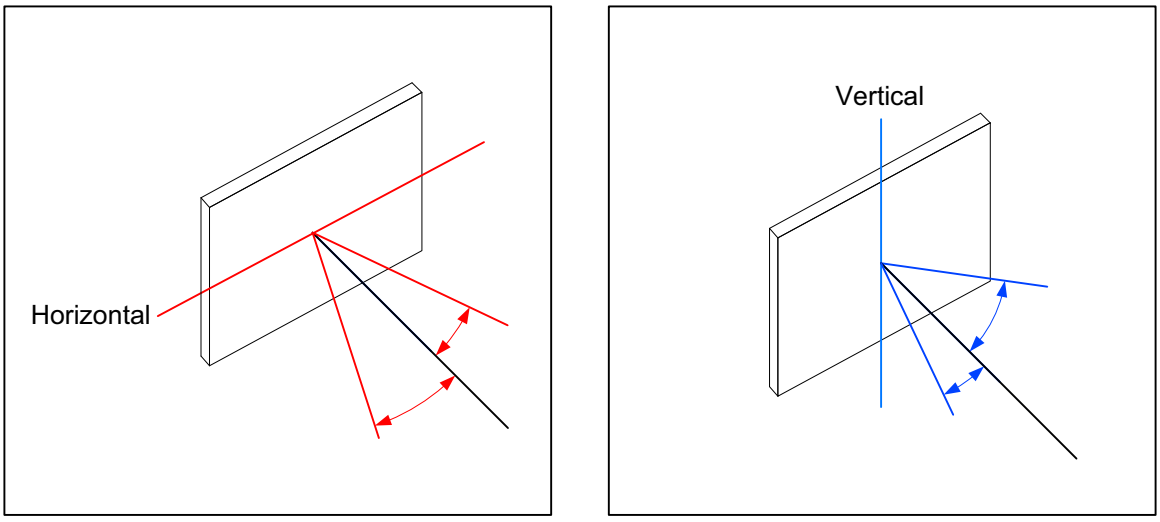


Figure 6. Definition of Horizontal and Vertical Viewing Angles (CR>2)

Definition of 6 O'Clock and 12:00 O'Clock Viewing Angles

This module has a 12:00 o'clock viewing angle.

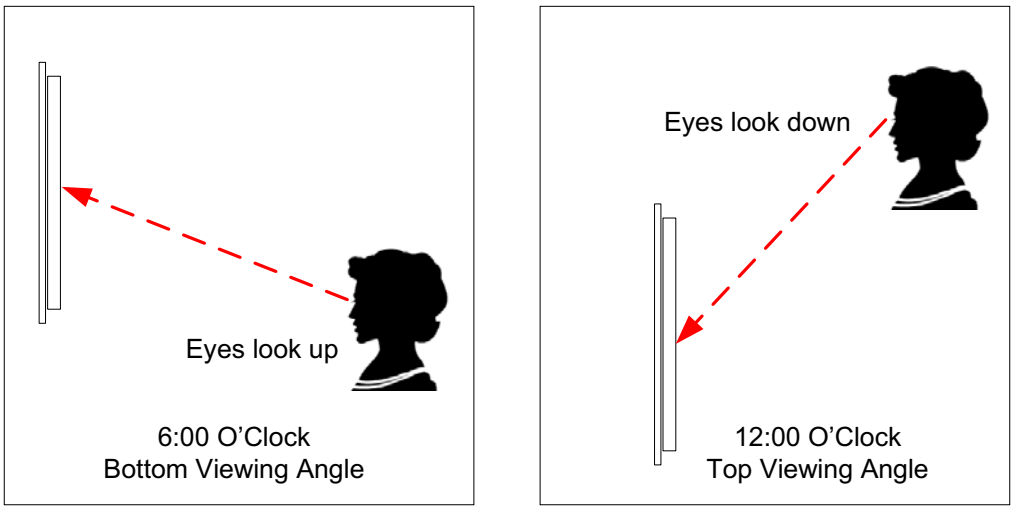


Figure 7. Definition of 6:00 O'Clock and 12:00 O'clock Viewing Angles

LED BACKLIGHT CHARACTERISTICS

The CFAF320480C4-035T Family uses an LED backlight. LED backlights are easy to use, but they are also easily damaged by abuse.

CAUTION

Do not connect +5v directly to the backlight terminals. This will ruin the backlight.

NOTE

We recommend that the LED backlight be dimmed or turned off during periods of inactivity to conserve its lifetime.

LEDs are "current" devices. The important aspect of driving an LED is the current flowing through it, not the voltage across it. Ideally, a current source would be used to drive the LEDs. In practice, a simple current limiting resistor in line from a voltage source will work well in most applications and is much less complex than a current source.

You need to know what the forward voltage of the LEDs is so you can calculate the current limiting resistor (R_{LIMIT}). The forward voltage will vary slightly from display to display.

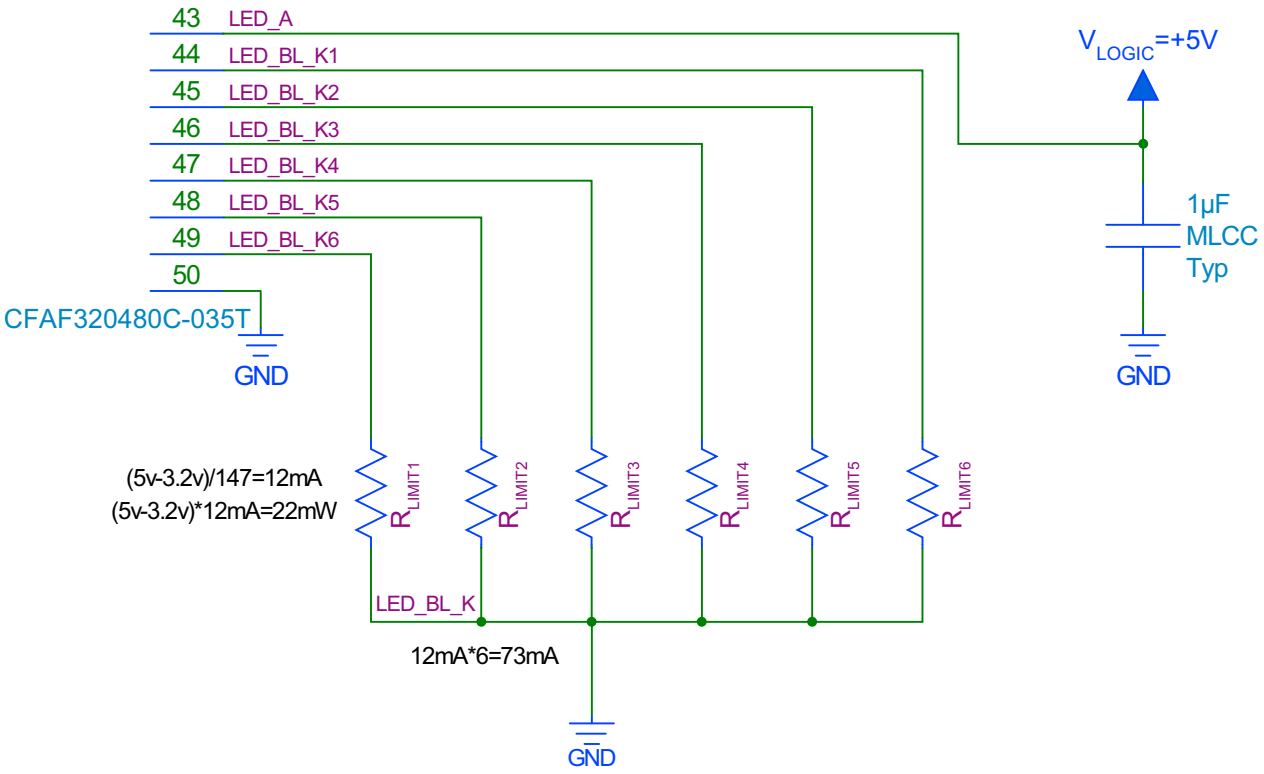


Figure 8. Typical LED Backlight Connections for “Always On”

The general equation to calculate R_{LIMIT} is:

$$R_{LIMIT} = \frac{V_{LOGIC} \text{ (Supply Voltage)} - V_{LED} \text{ (Typical LED Forward Voltage)}}{I_{LED} \text{ (Typical LED Forward Current, Single LED)}}$$

The specific R_{LIMIT} calculation for the CFAF320480C4-035T Family at V_{LOGIC} = +5.0v is:

$$R_{LIMIT} = \frac{5.0v - 3.2v}{0.015A} = 120\ \Omega \text{ (minimum — use next larger standard size)}$$

How to Calculate the Power Rating of the Resistor

The general equation to calculate the power rating of the resistor is:

P = IE

where

P= Power. Measured in Watts (W).

I= Current. Measured in amperes (A). "I" is from the outdated term “Intensity”.

E= Voltage. Measured in volts (v). “E” is from the outdated term “Electromotive force”.

The specific power rating calculation for CFAF320480C4-035T Family is:

P = 0.015A x (5.0v - 3.2v) = 0.0027W = 2.7mW

Please select a resistor that can safely dissipate 2.7 mW while keeping its temperature at an acceptably low value for your application.

PWM Dimming

The backlight may be dimmed by PWM (Pulse Width Modulation). The typical range for the PWM frequency is from 100 to 300 Hz.

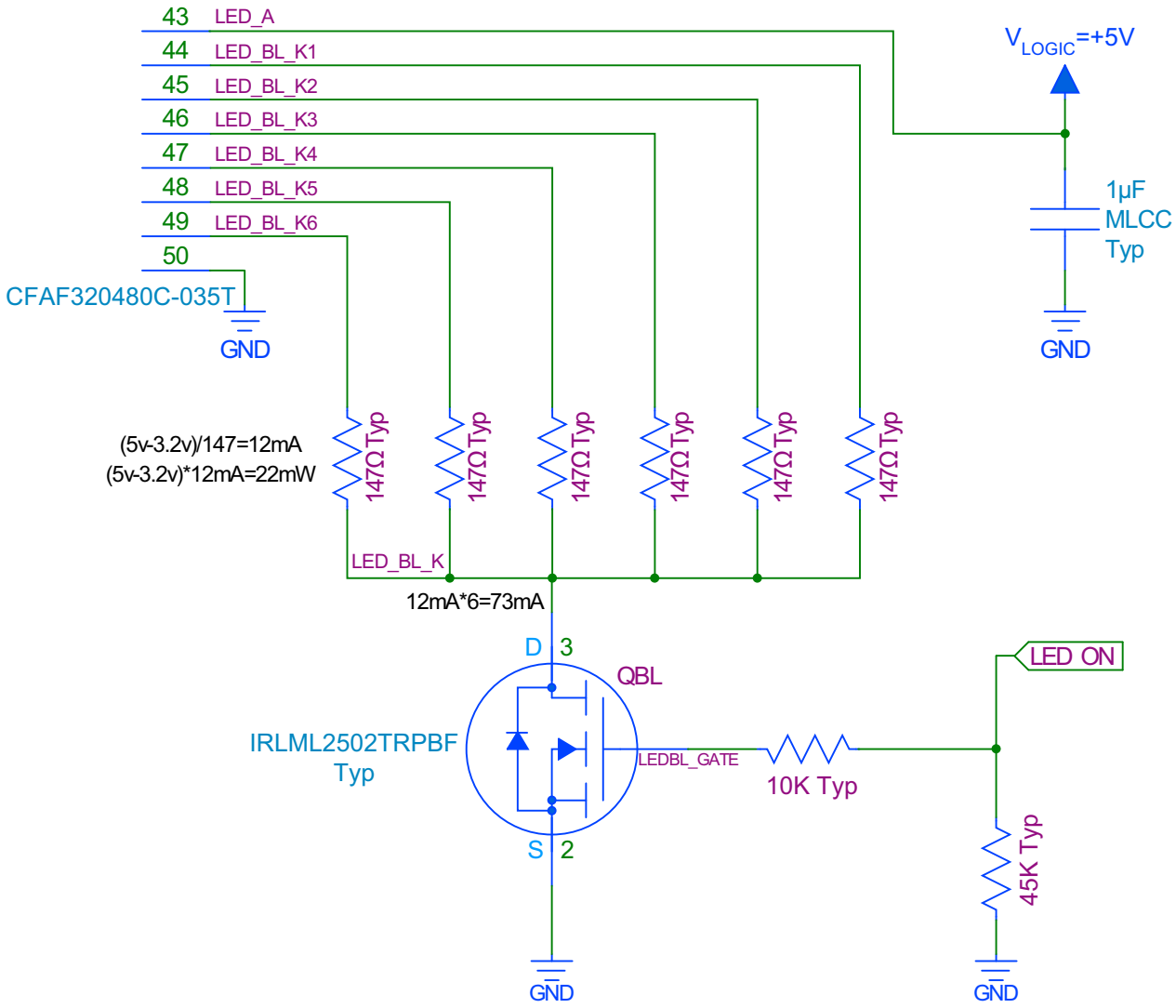


Figure 9. Typical LED Backlight Connections for PWM Dimming

LED Backlight Characteristics *Edge-lit with six LEDs in parallel.* *Ambient temperature: TA = 25°C*			
PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**
Forward Current (I_{LED})	—	90 mA* 15mA per LED 15mA x 6 = 90 mA	90 mA* 15mA per LED 15mA x 6 = 90 mA
**Caution: Driving the backlight above 90 mA will shorten its lifetime.*			
Forward Voltage (V_{LED})	—	+3.2v	—
Luminous Intensity* (IV) when I_{LED} = 90 mA			
CFAF320480C4-035T Includes TFT panel.	—	110 cd/m^2	—
CFAF320480C4-035T-TS Includes TFT panel and touch screen.	—	85 cd/m^2	—
Uniformity (minimum/maximum x 100%)	80%	—	—

SOURCES FOR DRIVER LIBRARIES

When purchased as part of our kits KIT365B3754 (for *CFAF320480C4-035T*) and KIT365B3758 (for *CFAF320480C4-035T-TS*), these displays are supported for Linux through GitHub.

MODULE RELIABILITY AND LONGEVITY

MODULE RELIABILITY

PART NUMBER	SPECIFICATION
CFAF320480C4-035T and *CFAF320480C4-035T-TS*	Brightness will be >50% of a new module's initial brightness for at least 50,000 hours of operation when supply to each LED is below 90 mA.

Under operating and storage temperature specification limitations, humidity noncondensing) RH up to 65%, and no exposure to direct sunlight. Value listed above is approximate and represent typical lifetime.

The white LEDs dim over time, especially if driven with high currents. The dimming may not be noticeable when a single display is installed. However, if a new display is installed next to a display that has been on continuously for a very long time, you will see the difference. To preserve the lifetime of white LEDs, we recommend that white LED backlights are dimmed or turned off when not needed. Also, please do not use more current than you need to achieve your brightness requirements.

MODULE LONGEVITY (EOL/REPLACEMENT POLICY)

Crystalfontz is committed to making all of our modules available for as long as possible. For each module we introduce, we intend to offer it indefinitely. We do not preplan a module's obsolescence. The majority of modules we have introduced are still available.

We recognize that discontinuing a module may cause problems for some customers. However, rapidly changing technologies, component availability, or low customer order levels may force us to discontinue ("End of Life" EOL) a module. For example, we must occasionally discontinue a module when a supplier discontinues a component or a manufacturing process becomes obsolete. When we discontinue a module, we will do our best to find an acceptable replacement module with the same fit, form, and function.

In most situations, you will not notice a difference when comparing a "fit, form, and function" replacement module to the discontinued module. However, sometimes a change in component or process for the replacement module results in a slight variation, perhaps an improvement, over the previous design.

Although the replacement module is still within the stated Data Sheet specifications and tolerances of the discontinued module, changes may require modification to your circuit and/or firmware. Possible changes include:

- *Controller.* A new controller may require minor changes in your code.
- *Component tolerances.* Module components have manufacturing tolerances. In extreme cases, the tolerance stack can change the visual or operating characteristics.

Please understand that we avoid changing a module whenever possible; we only discontinue a module if we have no other option. We will post Part Change Notices on the product's web page as soon as possible. If interested, you can subscribe to future part change notifications.

CARE AND HANDLING PRECAUTIONS

For optimum operation of the module and to prolong its life, please follow the precautions below.

Excessive voltage will shorten the life of the module. You must drive the display within the specified voltage limit. See Absolute Maximum Ratings (Pg. 12).

ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and is susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other static sensitive devices such as expansion cards, motherboards, or integrated circuits. Ground your body, work surfaces, and equipment.

DESIGN AND MOUNTING

- *CFAF320480C4-035T*: The exposed surface of the “glass” is actually a polarizer laminated on top of the glass.To protect the soft plastic polarizer from damage, the module ships with a protective film over the polarizer. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- *CFAF320480C4-035T-TS*: To protect the touch screen from damage, the module ships with a protective film over the touch screen. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- *CFAF320480C4-035T*: The polarizer is made out of soft plastic and is easily scratched or damaged. When handling the module, avoid touching the polarizer. Finger oils are difficult to remove.
- *CFAF320480C4-035T*: To protect the soft plastic polarizer from damage, place a transparent plate (for example, acrylic, polycarbonate, or glass) in front of the module, leaving a small gap between the plate and the display surface. We use GE HP-92 Lexan, which is readily available and works well.
- Do not disassemble or modify the module.
- Do not reverse polarity to the power supply connections. Reversing polarity will immediately ruin the module.
- Use care to keep the exposed terminals clean. Contamination, including fingerprints may make soldering difficult, and the reliability of the soldered connection poor.
- Sharp bends can damage the FPC. Do not crease FPC. Do not bend FPC tightly against the edge of the TFT panel.
- Do not repeatedly bend the FPC beyond its elastic region.

Hand Soldering

For prototype work, hand soldering may be acceptable. Preset soldering iron to <260°C. Do not apply heat for more than 3 to 4 seconds. The FPC is quite fragile; use extreme care when soldering by hand. Great care must be taken since the conductors of the tail are completely exposed in the area where they are soldered. Solder only to the exposed terminals of the FPC connector. The use of Kapton® tape to help locate and secure the FPC may be useful.

AVOID SHOCK, IMPACT, TORQUE, OR TENSION

- Do not expose the module to strong mechanical shock, impact, torque, or tension.
- Do not drop, toss, bend, or twist the module.
- Do not place weight or pressure on the module

IF LCD PANEL BREAKS

All electronics may contain harmful substances. Avoid contamination by using care to avoid damage during handling. If any residues, gases, powders, liquids, or broken fragments come in contact with your skin, eyes, mouth, or lungs, immediately contact your local poison control or emergency medical center.

HOW TO CLEAN

1. Turn display off.
2. Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter. If you no longer have the protective film, use standard transparent office tape (for example, Scotch® brand “Crystal Clear Tape”).
3. If the polarizer is dusty, you may carefully blow it off with clean, dry, oil-free compressed air.
4. If you must clean with a liquid, never use glass cleaners, as they may contain ammonia or alcohol that will damage the touch screen or polarizer over time. Never apply liquids directly on the touch screen or polarizer. Long contact with moisture may permanently spot or stain the polarizer. Use filtered water to slightly moisten a clean lint-free microfiber cloth designed for cleaning optics. (For example, use a cloth sold for cleaning plastic eyeglasses.)
5. The plastic is easily scratched or damaged. Use a light touch as you clean the touch screen or polarizer. Wipe gently.
6. Use a dry microfiber cloth to remove any trace of moisture before turning on the TFT.
7. Gently wash the microfiber cloths in warm, soapy water and air dry before reuse.

OPERATION

- We do not recommend connecting this module to a PC's parallel port as an "end product.” This module is not "user friendly" and connecting it to a PC's parallel port is often difficult, frustrating, and can result in a "dead" display due to mishandling. For more information, see our forum thread at http://www.crystalfontz.com/forum/showthread.php?s=&threadid=3257.
- Your circuit should be designed to protect the module from ESD and power supply transients.
- Observe the operating temperature limitations: a minimum of 0°C to a maximum of +50°C noncondensing with minimal fluctuation. Operation outside of these limits may shorten life and/or harm display. Changes in temperature can result in changes in contrast.
  - At lower temperatures of this range, response time is delayed.
  - At higher temperatures of this range, display becomes dark. (You may need to adjust the contrast.)
- Operate away from dust, moisture, and direct sunlight.

STORAGE AND RECYCLING

- Store in an ESD-approved container away from dust, moisture, and direct sunlight, fluorescent lamps, or any ultraviolet ray.
- Observe the storage temperature limitations: from -30°C minimum to +80°C maximum with minimal fluctuations. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Maximum storage life is 10 years within storage temperature limitations and normal humidity.
- Do not allow weight to be placed on the modules while they are in storage.
- Please recycle your outdated Crystalfontz modules at an approved facility.

APPENDIX A: QUALITY ASSURANCE STANDARDS

INSPECTION CONDITIONS

- Environment
  - Temperature: 25±5°C
  - Humidity: 30~85% RH (noncondensing)
- For visual inspection of active display area
  - Source lighting: two 20-Watt or one 40-Watt fluorescent light
  - Display adjusted for best contrast
  - Viewing distance: 30±5 cm (about 12 inches)
  - Viewing angle: inspect at 45° angle of vertical line right and left, top and bottom

COLOR DEFINITIONS

We try to describe the appearance of our modules as accurately as possible. For the photos, we adjust for optimal appearance. Actual display appearance may vary due to (1) different operating conditions, (2) small variations of component tolerances, (3) inaccuracies of our camera, (4) color interpretation of the photos on your monitor, and/or (5) personal differences in the perception of color.

ACCEPTANCE SAMPLING

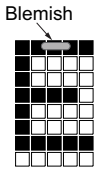
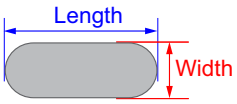
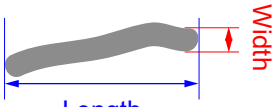
DEFECT TYPE	AQL*
Major	≤.65%
Minor	<1.0%
* Acceptable Quality Level: maximum allowable error rate or variation from standard	

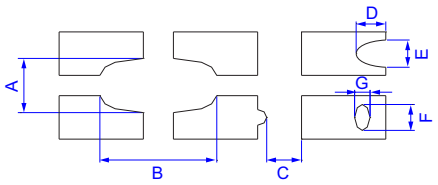
DEFECTS CLASSIFICATION

Defects are defined as:

- Major Defect: results in failure or substantially reduces usability of unit for its intended purpose.
- Minor Defect: deviates from standards but is not likely to reduce usability for its intended purpose.

ACCEPTANCE STANDARDS

#	DEFECT TYPE	ACCEPTANCE STANDARDS CRITERIA			MAJOR / MINOR
1	Electrical defects	1. No display, display malfunctions, or shorted segments. 2. Current consumption exceeds specifications.			Major
2	Viewing area defect	Viewing area does not meet specifications).			Major
3	Contrast adjustment defect	Contrast adjustment fails or malfunctions.			Major
4	Blemishes or foreign matter on display segments		*Defect Size (mm)*	*Acceptable Qty*	Minor
			≤0.3	3	
			≤2 defects within 10 mm of each other		
5	Other blemishes or foreign matter outside of display segments	Defect size = (A + B)/2 	*Defect Size (mm)*	*Acceptable Qty*	Minor
			≤0.15	Ignore	
			0.15 to 0.20	3	
			0.20 to 0.25	2	
			0.25 to 0.30	1	
6	Dark lines or scratches in display area 	*Defect Width (mm)*	*Defect Length (mm)*	*Acceptable Qty*	Minor
		≤0.03	≤3.0	3	
		0.03 to 0.05	≤2.0	2	
		0.05 to 0.08	≤2.0	1	
		0.08 to 0.10	≤3.0	0	
		≥0.10	>3.0	0	
7	Bubbles between polarizer film and glass		*Defect Size (mm)*	*Acceptable Qty*	Minor
			≤0.20	Ignore	
			0.20 to 0.40	3	
			0.40 to 0.60	2	
			≥0.60	0	

<table>
<tr><th>#</th><th>DEFECT TYPE</th><th>ACCEPTANCE STANDARDS CRITERIA (Continued)</th><th>MAJOR / MINOR</th></tr>
<tr><td>8</td><td>Display pattern defect</td><td> 

<table>
<tr><th>Dot Size (mm)</th><th>Acceptable Qty</th></tr>
<tr><td>((A+B)/2)≤0.2</td><td rowspan="4">≤3 total defects

≤2 pinholes per digit</td></tr>
<tr><td>C>0</td></tr>
<tr><td>((D+E)/2)≤0.25</td></tr>
<tr><td>((F+G)/2)≤0.25</td></tr>
</table></td><td>Minor</td></tr>
<tr><td>9</td><td>Backlight defects</td><td>1. Light fails or flickers.*
2. Color and luminance do not correspond to specifications.*
3. Exceeds standards for display’s blemishes or foreign matter (see test 5, Pg. 28), and dark lines or scratches (see test 6, Pg. 28).
*Minor if display functions correctly. Major if the display fails.</td><td>Minor</td></tr>
<tr><td>10</td><td>COB defects</td><td>1. Pinholes >0.2 mm.
2. Seal surface has pinholes through to the IC.
3. More than 3 locations of sealant beyond 2 mm of the sealed areas.</td><td>Minor</td></tr>
<tr><td>11</td><td>PCB defects</td><td>1. Oxidation or contamination on connectors.*
2. Wrong parts, missing parts, or parts not in specification.*
3. Jumpers set incorrectly.
4. Solder (if any) on bezel, LED pad, zebra pad, or screw hole pad is not smooth.
*Minor if display functions correctly. Major if the display fails.</td><td>Minor</td></tr>
<tr><td>12</td><td>Soldering defects</td><td>1. Unmelted solder paste.
2. Cold solder joints, missing solder connections, or oxidation.*
3. Solder bridges causing short circuits.*
4. Solder balls.
*Minor if display functions correctly. Major if the display fails.</td><td>Minor</td></tr>
</table>

APPENDIX B: TFT MODULE TERMS AND SYMBOLS

Crystalfontz Term / Symbol	Equivalent	Equivalent	Equivalent	Description
A (LED +)				Supply pin for LED. “A” (anode) or “+” of LED backlight. If more than one, may be labeled as A_1, A_2, ...
cd/m^2	lumen	nits		Candela per square meter. A unit of measurement used to measure Luminous Intensity. cd/m^2 = 1 lumen.
$\overline{CS}$	CS#	CSX		Chip select input. *Low:* Controller chip is selected. Communications with host are possible. *High:* Controller chip is not selected. Host interface signals are ignored by the controller.
COF				Chip On Flex. Controller is on the FPC. Similar in appearance to “TAB”. The flex circuit on COF is typically much thinner than the flex of a “flex tail”.
COG				Chip On Glass. Controller is on the glass panel.
DB0 ~ DB*n*	D0 ~ D*n*			Parallel databus.
D/$\overline{C}$	RS or DCX	A0	CD or D/C#	Data/Command control. Determines whether data bits are data or command. *1 – High:* Addresses the data register. *0 – Low:* Addresses the command register.
DE				Data Enable signal for RGB / DPI mode.
DPI	DOTCLK	parallel		Displays Pixel Interface
ESD				Electro-Static Discharge. Sudden and brief electrical current that flows between two objects. ESD between a human and a TFT module can cause permanent damage.
FPC				Flexible Printed Circuit. Also called “flex tail”. Typically much thicker than the “flex” film of COF (Chip On Flex).
GND	V_{SS}			Ground. Must be connected to an external ground.
H_{SYNC}				Horizontal frame synchronizing signal used for RGB mode.
I_{DD}				Typical power supply current for TFT. Total electrical current (I) in the Drains of a CMOS circuit

Crystalfontz Term / Symbol (Continued)	Equivalent	Equivalent	Equivalent	Description
I_{LED}				Current used by LED backlight.
I_{OP}	V_{CCI}			Current for normal OPeration, typically measured in milliamperes (mA). 1 mA = 0.001A (Ampere)
I_{ST}				Current for STandby mode, typically measured in microampere (µA). 1 µA = 0.000001A (Ampere)
I/O	IO			Input/Output
K (LED -)				Supply pin for LED. “K” (cathode or kathode for German and original Greek spelling) or “-” of LED backlight. If more than one, may be labeled as K_1, K_2, ...
MIPI				Mobile Industry Processor Interface. See MIPI Alliance.
MISO	D_{OUT}			SPI data signal: Master In Slave Out.
MOSI	DINI_SDA			SPI data signal: Master Out Slave In.
mm				Millimeter or millimetre. Unit of length equal to one thousandth of a meter. 1 millimeter = 0.0394 inches.
mW				Milliwatt is equal to one thousandth of a Watt. Watts = Volts x Amps.
NC	nc			No Connection.
P_{CLK}				Pixel clock signal for RGB / DPI mode.
PWM				Pulse Width Modulation is a way to simulate intermediate levels by switching a level between full on and full off. PWM is typically used to control the brightness of LED backlights, relying on the natural averaging by the human eye.
$\overline{RD}_{8080}$	$\overline{RD}$ (E)	E ($\overline{RD}$)	E or RDX	Host interface input. *8080 Host:* Active low. Signal on the databus is latched at the rising edge of $\overline{RD}$.
RGB				Typically used to indicate that Red, Green, and Blue are combined to produce a broad array of colors.
RH	Rh			Relative Humidity

Crystalfontz Term / Symbol (Continued)	Equivalent	Equivalent	Equivalent	Description
RoHS				Restriction of Hazardous Substances Directive, an environmental standard.
$\overline{RST}$	$\overline{RES}$	RST#	RES#	Reset signal. *Low:* Display controller is reset. The $\overline{RST}$ pin should be pulsed low shortly after power is applied. *High:* The $\overline{RST}$ pin should be brought high for normal operation.
SCK	SCL			Serial Clock
Ta	TA			“Ambient temperature” is the temperature of the air that surrounds a component.
Tf				Unit of measurement for TFT response time. f = falling edge. See Definition of Response Time (Tr, Tf) (Pg. 19).
TFT				Thin-Film Transistor fabricated directly on the display substrate.
T_{OP}				OPerating Temperature.
Tr				Unit of measurement for TFT response time. r = rising edge. See Definition of Response Time (Tr, Tf) (Pg. 19).
T_{ST}	T_{STG}			STorage Temperature.
V_{ANALOG}	V_{CI}			Analog supply,
V_{IH}	V_{ICH}			High level input voltage.
V_{IL}	V_{LCH}			Low level input voltage.
V_{IN}	V_T			Input voltage
V_{LED}				Forward voltage for LED backlight.
V_{LOGIC}	V_{CC}	V_{DD}		Power supply input. Must be connected to an external source.
$V_{LOGIC\ I/O}$	V_{CCIO}	IO_{VCC}		Digital Logic Supply and Input/Output Supply
V_{OH}	V_{OHC}			High level output voltage.
V_{OL}	V_{OLC}			Low level output voltage.
V_{SSD}				Digital ground.

Crystalfontz Term / Symbol (Continued)	Equivalent	Equivalent	Equivalent	Description
V_{SYNC}				Vertical frame synchronizing signal used for RGB mode.
$\overline{WR}_{8080}$	R/$\overline{W}$ ($\overline{WR}$)	$\overline{WR}$ (R/$\overline{W}$)	R/W#	Host interface input. *8080 Host:* Active low. Signal on the databus is latched at the rising edge of $\overline{WR}$ signal.
$\overline{WR}$_SCK				*DBI Type-B:* Serves as a write signal and write data at the low level. *DBI Type-C:* it serves as SCK (Serial Clock). If unused, tie to $V_{LOGIC\ I/O}$.

APPENDIX C: HIMAX HX8357-B CONTROLLER DATA SHEET

The complete *Himax HX8357-B Data Sheet* (188 pages) publication date January 2010 follows.

Appendix

DATA SHEET

(DOC No. HX8357-B-DS)

HX8357-B

320RGB x 480 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

Preliminary version 01 January, 2010

Himax Technologies, Inc.
http://www.himax.com.tw

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January, 2010

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1. General Description

This document describes Himax's HX8357-B is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 320RGBx480 dots.

The HX8357-B can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8357-B also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8357-B is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pages.

2. Features

2.1 Display

- Resolution:
  - 320(H) x RGB(H) x 480(V)
- Display Color modes
  - Normal Display Mode On
    - 65,536(R(5),G(6),B(5)) colors
    - 262,144(R(6),G(6),B(6)) colors
  - Idle Mode On
    - 8 (R(1),G(1),B(1)) colors.

2.2 Display Module

- On module VCOM control (-2.0 to 5.5V Common electrode output voltage range)
- On module DC/DC converter
  - DDVDH = 4.6 to 6.0V (Source output voltage range)
  - VGH = +9.0 to +16.5V (Positive Gate output voltage range)
  - VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- Frame Memory area 320 (H) x 480 (V) x 18 bit

2.3 Display/Control Interface

- Display Interface types supported
  - MIPI-DBI Type-B 8-/9-/16-/18-bit MPU parallel interface.
  - MIPI-DBI Type-C OPTION1/3 Serial data transfer interface.
  - MIPI-DPI 16-/18-data lines parallel video (RGB) interface.
- Color modes
  - 16 bit/pixel: R(5), G(6), B(5)
  - 18 bit/pixel: R(6), G(6), B(6)

2.4 Display Module

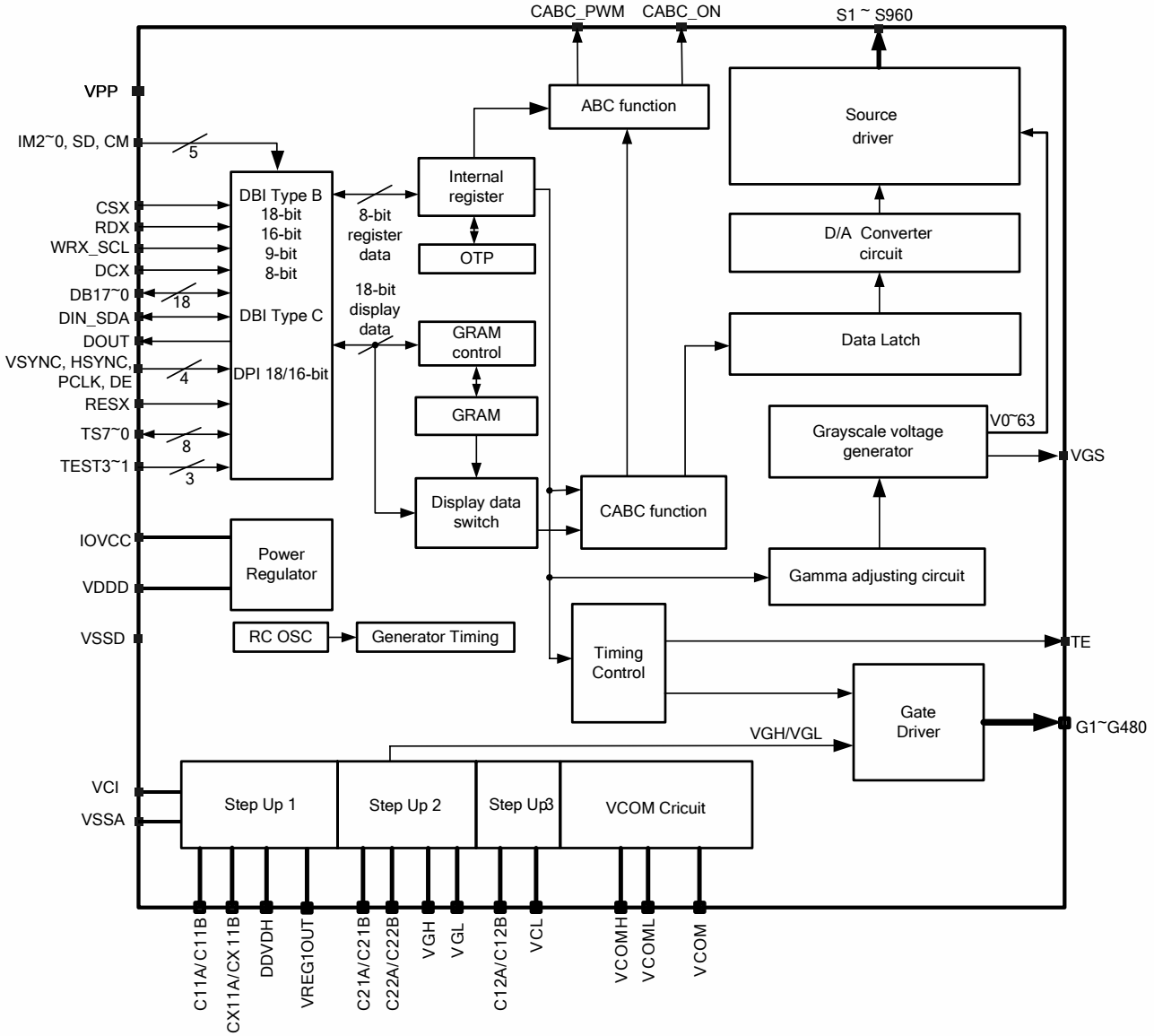
- Logic power supply (IOVCC): 1.65V ~ 3.3V
- Analog power supply (VCI): 2.5V ~ 3.3V
- OTP programming voltage (VPP): 7.5V ± 0.2

2.5 Miscellaneous

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
- Temperature range: -40 ~ +85 °C
- Proprietary multi phase driving for lower power consumption
- Support Line inversion or Frame inversion
- Support Vertical scrolling
- Support Partial display mode
- Support normal black/normal white LCD
- Support wide view angle display
- Support Deep standby mode
- On-chip OTP (One-time-programming) and MTP(Five-time-programming for some register) non-volatile memory
- Support Content Adaptive Brightness Control(CABC) function

3. Device Overview

3.1 Block Diagram



3.2 Pin Description

<table>
<tr><th colspan="6">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th colspan="2">Description</th></tr>
<tr><td>IM2, IM1, IM0</td><td>I</td><td>3</td><td>VSSD/ IOVCC</td><td colspan="2">Select the MPU interface mode as listed below.
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface mode</th><th>DB pins</th><th>Color mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Type-B 18-bit</td><td>DB17-DB0: Data</td><td>262K</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Type-B 9-bit</td><td>DB17-DB9: Unused,
DB8-DB0: Data</td><td>262K</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Type-B 16-bit</td><td>DB17-DB16: Unused,
DB15-DB0: Data</td><td>65K / 262K</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Type-B 8-bit</td><td>DB17-DB8: Unused,
DB7-DB0: Data.</td><td>65K / 262K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Inhibited</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DBI Type-C Option 1
(9 bits)</td><td>DB17-DB0: Data,
DIN_SDA, DOUT</td><td>8 / 262K</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Inhibited</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DBI Type-C Option 3
(8 bits)</td><td>DB17-DB0: Data.
DIN_SDA, DOUT</td><td>8 / 262K</td></tr>
</table>
Pixel format (RGB565/RGB666) is selected by Command (0x3Ah)</td></tr>
<tr><td>CSX</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.
If not use, please connect to IOVCC.</td></tr>
<tr><td>RESX</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td colspan="2">Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
If not use, please connect to IOVCC.</td></tr>
<tr><td>WRX_SCL</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">DBI Type-B: Serves as a write signal and write data at the low level.
DBI Type-C: it servers as SCL (Serial Clock).
If not use, please connect to IOVCC.</td></tr>
<tr><td>RDX</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">DBI Type-B: Serves as a read signal and read data at the low level.
If not use, please connect to IOVCC.</td></tr>
<tr><td>DCX</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Data / Command Selection pin
If not use, please connect to IOVCC.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Frame synchronizing signal for DPI I/F mode.
If not use, please connect to IOVCC.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Frame synchronizing signal for DPI I/F mode.
If not use, please connect to IOVCC.</td></tr>
<tr><td>PCLK</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Pixel clock signal for DPI I/F mode.
If not use, please connect to VSSD.</td></tr>
<tr><td>DE</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">A DATA ENABLE signal for DPI I/F mode.
If not use, please connect to VSSD.</td></tr>
<tr><td>SD</td><td>I</td><td>1</td><td>MCU</td><td colspan="2">Control pin of Normal display or shut down display in DPI(RM=1) interface mode.
<table>
<tr><th>SD</th><th>Display mode</th></tr>
<tr><td>0</td><td>Normal display</td></tr>
<tr><td>1</td><td>Shut down display</td></tr>
</table></td></tr>
<tr><td>CM</td><td>I</td><td>1</td><td>MCU</td><td colspan="2">Color mode direction H/W select pin in DPI interface mode.
<table>
<tr><th>CM</th><th>Color mode</th></tr>
<tr><td>0</td><td>Normal display color</td></tr>
<tr><td>1</td><td>8-Color mode</td></tr>
</table></td></tr>
</table>

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S960	O	960	LCD	Output voltages applied to the liquid crystal.
G1~G480	O	480	LCD	Gate driver output pins. These pins output VGH, VGL
VCOM	O	16	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
TE	O	1	MPU	Tearing effect output. **If not used, please open this pin.**
CABC_ON	O	1	LED driver IC	If use CABC function (setting by BL), the pin can connect to external LED driver IC. The output voltage rage = VSSD~ IOVCC. **If not used, please open this pin.**
CABC_PWM	O	1	LED driver IC	Backlight On/Off control pin. If use CABC function, the pin can connect to external LED driver IC. The output voltage rage = VSSD~ IOVCC. **If not used, please open this pin.**
DOUT	O	1	MPU	Serial data output pin in serial bus system interface. **If not used, please open this pin.**

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
DB17~0	I/O	18	MPU	When Operates in MIPI DBI interface mode, it is used liked an 18-bit bi-directional data bus. 8-bit bus: use DB7-DB0 9-bit bus: use DB8-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0 When Operation in MIPI DPI interface mode, it is an 18-bit bus RGB data bus. 6-bit bus: use DB5-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0 **If not used, please connect to VSSD.**
DIN_SDA	I/O	1	MPU	Serial data input pin or input/output pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal. **If not used, please connect to VSSD.**

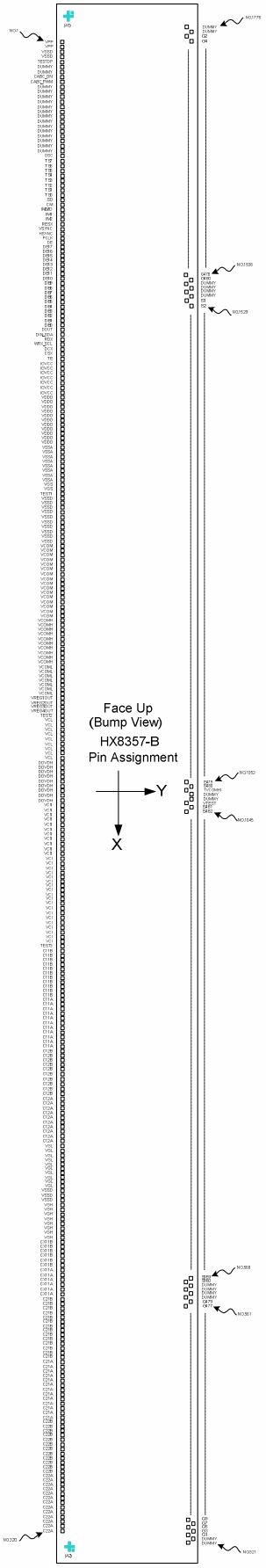
Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	7	Power Supply	IO Pad and Digital power supply, 1.65V~3.3V
VCI	P	19	Power Supply	Analog power supply, 2.5V~3.3V
VPP	P	2	Power Supply	Power supply pin used in OTP program mode and operates at 7.5V ± 0.2. If not in OTP program mode, please let it open.
VSSD	P	15	Ground	Digital ground
VSSA	P	8	Ground	Analog ground
VDDD	O	11	Stabilizing Capacitor	Output from internal logic voltage. Connect to a stabilizing capacitor
VREG1OUT VREG2OUT VREG3OUT VREG4OUT	P	4	Stabilizing Capacitor	Internal generated stable power for source driver unit.
VCI1	O	11	Open	Internal reference voltage output pin, please open this pin.
VCOMH	P	10	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	P	7	Stabilizing capacitor	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
VCL	P	9	Stabilizing capacitor	A negative voltage for VCOML circuit, VCL=-VCI
DDVDH	P	9	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and DDVDH. (See “configuration of the power supply”).
VGH	P	8	Stabilizing capacitor	An output from the step-up circuit2.or 4 ~ 6 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSA and VGH. (See “configuration of the power supply”).
VGL	P	10	Stabilizing capacitor	An output from the step-up circuit2.or -3 ~ -5 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSA and VGL. Place a schottkey barrier diode between VSSD and VGL. Place a schottkey barrier diode (see “configuration of the power supply”).
VGS	I	2	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.
C11A,C11B CX11A,CX11B	P	34	Step-up Capacitor	Connect to the step-up capacitors according to the step-up 1 factor. Leave this pin open if the internal step-up circuit is not used.
C12A, C12B	P	20	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.
C21A,C21B C22A,C22B	P	52	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.

Test Pin and Others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST3-1	I	3	GND	Test pin input (Internal pull low)
OSC	I	1	Open	A test pin. Disconnect it.
TESTDP	I	1	Open	A test pin. Disconnect it.
VTEST	O	1	Open	A test pin. Disconnect it.
TVCOMHI	O	1	Open	A test pin. Disconnect it.
TS7~0	O	8	Open	A test pin. Disconnect it.
DUMMY	-	31	Open	Dummy pin. Disconnect it.

3.3 Pin Assignment

- Chip Size : 23250 x 847 um (Include seal ring and scribe line)
- Chip thickness : 250 um ± 25 um
- Pad Location : PAD Center
- Coordinate Origin : Chip Center
- Au Bump Size :
  1. 80 um x 50 um
     Input:
     No. 1 to 320
  2. 120 um x 15 um
     Staggered LCD output side
     No. 321 to 1776
- The chip size includes the core size, seal ring size and scribe line size.
- Au bump pitch : Refer to Pad Coordinate.
- Au bump height : 15 um ± 3 um.
- Numbers in the figure corresponds to pad coordinate numbers.



3.4 Pad Coordinates

No.	Name	X	Y	Bump size
1	VPP	-11165	-309	50 * 80
2	VPP	-11095	-309	50 * 80
3	VSSD	-11025	-309	50 * 80
4	VSSD	-10955	-309	50 * 80
5	TESTDP	-10885	-309	50 * 80
6	DUMMY1	-10815	-309	50 * 80
7	DUMMY2	-10745	-309	50 * 80
8	CABC_ON	-10675	-309	50 * 80
9	CABC_PWM	-10605	-309	50 * 80
10	DUMMY3	-10535	-309	50 * 80
11	DUMMY4	-10465	-309	50 * 80
12	DUMMY5	-10395	-309	50 * 80
13	DUMMY6	-10325	-309	50 * 80
14	DUMMY7	-10255	-309	50 * 80
15	DUMMY8	-10185	-309	50 * 80
16	DUMMY9	-10115	-309	50 * 80
17	DUMMY10	-10045	-309	50 * 80
18	DUMMY11	-9975	-309	50 * 80
19	DUMMY12	-9905	-309	50 * 80
20	DUMMY13	-9835	-309	50 * 80
21	DUMMY14	-9765	-309	50 * 80
22	DUMMY15	-9695	-309	50 * 80
23	DUMMY16	-9625	-309	50 * 80
24	OSC	-9555	-309	50 * 80
25	TS7	-9485	-309	50 * 80
26	TS6	-9415	-309	50 * 80
27	TS5	-9345	-309	50 * 80
28	TS4	-9275	-309	50 * 80
29	TS3	-9205	-309	50 * 80
30	TS2	-9135	-309	50 * 80
31	TS1	-9065	-309	50 * 80
32	TS0	-8995	-309	50 * 80
33	SD	-8925	-309	50 * 80
34	CM	-8855	-309	50 * 80
35	IM0	-8785	-309	50 * 80
36	IM1	-8715	-309	50 * 80
37	IM2	-8645	-309	50 * 80
38	RESX	-8575	-309	50 * 80
39	VSYNC	-8505	-309	50 * 80
40	HSYNC	-8435	-309	50 * 80
41	PCLK	-8365	-309	50 * 80
42	DE	-8295	-309	50 * 80
43	DB17	-8225	-309	50 * 80
44	DB16	-8155	-309	50 * 80
45	DB15	-8085	-309	50 * 80
46	DB14	-8015	-309	50 * 80
47	DB13	-7945	-309	50 * 80
48	DB12	-7875	-309	50 * 80
49	DB11	-7805	-309	50 * 80
50	DB10	-7735	-309	50 * 80
51	DB9	-7665	-309	50 * 80
52	DB8	-7595	-309	50 * 80
53	DB7	-7525	-309	50 * 80
54	DB6	-7455	-309	50 * 80
55	DB5	-7385	-309	50 * 80
56	DB4	-7315	-309	50 * 80
57	DB3	-7245	-309	50 * 80
58	DB2	-7175	-309	50 * 80
59	DB1	-7105	-309	50 * 80
60	DB0	-7035	-309	50 * 80

No.	Name	X	Y	Bump size
61	DOUT	-6965	-309	50 * 80
62	DIN_SDA	-6895	-309	50 * 80
63	RDX	-6825	-309	50 * 80
64	WRX_SCL	-6755	-309	50 * 80
65	DCX	-6685	-309	50 * 80
66	CSX	-6615	-309	50 * 80
67	TE	-6545	-309	50 * 80
68	IOVCC	-6475	-309	50 * 80
69	IOVCC	-6405	-309	50 * 80
70	IOVCC	-6335	-309	50 * 80
71	IOVCC	-6265	-309	50 * 80
72	IOVCC	-6195	-309	50 * 80
73	IOVCC	-6125	-309	50 * 80
74	IOVCC	-6055	-309	50 * 80
75	VDDD	-5985	-309	50 * 80
76	VDDD	-5915	-309	50 * 80
77	VDDD	-5845	-309	50 * 80
78	VDDD	-5775	-309	50 * 80
79	VDDD	-5705	-309	50 * 80
80	VDDD	-5635	-309	50 * 80
81	VDDD	-5565	-309	50 * 80
82	VDDD	-5495	-309	50 * 80
83	VDDD	-5425	-309	50 * 80
84	VDDD	-5355	-309	50 * 80
85	VDDD	-5285	-309	50 * 80
86	VSSA	-5215	-309	50 * 80
87	VSSA	-5145	-309	50 * 80
88	VSSA	-5075	-309	50 * 80
89	VSSA	-5005	-309	50 * 80
90	VSSA	-4935	-309	50 * 80
91	VSSA	-4865	-309	50 * 80
92	VSSA	-4795	-309	50 * 80
93	VSSA	-4725	-309	50 * 80
94	VGS	-4655	-309	50 * 80
95	VGS	-4585	-309	50 * 80
96	TEST1	-4515	-309	50 * 80
97	VSSD	-4445	-309	50 * 80
98	VSSD	-4375	-309	50 * 80
99	VSSD	-4305	-309	50 * 80
100	VSSD	-4235	-309	50 * 80
101	VSSD	-4165	-309	50 * 80
102	VSSD	-4095	-309	50 * 80
103	VSSD	-4025	-309	50 * 80
104	VSSD	-3955	-309	50 * 80
105	VSSD	-3885	-309	50 * 80
106	VSSD	-3815	-309	50 * 80
107	VCOM	-3745	-309	50 * 80
108	VCOM	-3675	-309	50 * 80
109	VCOM	-3605	-309	50 * 80
110	VCOM	-3535	-309	50 * 80
111	VCOM	-3465	-309	50 * 80
112	VCOM	-3395	-309	50 * 80
113	VCOM	-3325	-309	50 * 80
114	VCOM	-3255	-309	50 * 80
115	VCOM	-3185	-309	50 * 80
116	VCOM	-3115	-309	50 * 80
117	VCOM	-3045	-309	50 * 80
118	VCOM	-2975	-309	50 * 80
119	VCOM	-2905	-309	50 * 80
120	VCOM	-2835	-309	50 * 80

No.	Name	X	Y	Bump size
121	VCOM	-2765	-309	50 * 80
122	VCOM	-2695	-309	50 * 80
123	VCOMH	-2625	-309	50 * 80
124	VCOMH	-2555	-309	50 * 80
125	VCOMH	-2485	-309	50 * 80
126	VCOMH	-2415	-309	50 * 80
127	VCOMH	-2345	-309	50 * 80
128	VCOMH	-2275	-309	50 * 80
129	VCOMH	-2205	-309	50 * 80
130	VCOMH	-2135	-309	50 * 80
131	VCOMH	-2065	-309	50 * 80
132	VCOMH	-1995	-309	50 * 80
133	VCOML	-1925	-309	50 * 80
134	VCOML	-1855	-309	50 * 80
135	VCOML	-1785	-309	50 * 80
136	VCOML	-1715	-309	50 * 80
137	VCOML	-1645	-309	50 * 80
138	VCOML	-1575	-309	50 * 80
139	VCOML	-1505	-309	50 * 80
140	VREG1OUT	-1435	-309	50 * 80
141	VREG2OUT	-1365	-309	50 * 80
142	VREG3OUT	-1295	-309	50 * 80
143	VREG4OUT	-1225	-309	50 * 80
144	TEST2	-1155	-309	50 * 80
145	VCL	-1085	-309	50 * 80
146	VCL	-1015	-309	50 * 80
147	VCL	-945	-309	50 * 80
148	VCL	-875	-309	50 * 80
149	VCL	-805	-309	50 * 80
150	VCL	-735	-309	50 * 80
151	VCL	-665	-309	50 * 80
152	VCL	-595	-309	50 * 80
153	VCL	-525	-309	50 * 80
154	DDVDH	-455	-309	50 * 80
155	DDVDH	-385	-309	50 * 80
156	DDVDH	-315	-309	50 * 80
157	DDVDH	-245	-309	50 * 80
158	DDVDH	-175	-309	50 * 80
159	DDVDH	-105	-309	50 * 80
160	DDVDH	-35	-309	50 * 80
161	DDVDH	35	-309	50 * 80
162	DDVDH	105	-309	50 * 80
163	VCI1	175	-309	50 * 80
164	VCI1	245	-309	50 * 80
165	VCI1	315	-309	50 * 80
166	VCI1	385	-309	50 * 80
167	VCI1	455	-309	50 * 80
168	VCI1	525	-309	50 * 80
169	VCI1	595	-309	50 * 80
170	VCI1	665	-309	50 * 80
171	VCI1	735	-309	50 * 80
172	VCI1	805	-309	50 * 80
173	VCI1	875	-309	50 * 80
174	VCI	945	-309	50 * 80
175	VCI	1015	-309	50 * 80
176	VCI	1085	-309	50 * 80
177	VCI	1155	-309	50 * 80
178	VCI	1225	-309	50 * 80
179	VCI	1295	-309	50 * 80
180	VCI	1365	-309	50 * 80

No.	Name	X	Y	Bump size
181	VCI	1435	-309	50 * 80
182	VCI	1505	-309	50 * 80
183	VCI	1575	-309	50 * 80
184	VCI	1645	-309	50 * 80
185	VCI	1715	-309	50 * 80
186	VCI	1785	-309	50 * 80
187	VCI	1855	-309	50 * 80
188	VCI	1925	-309	50 * 80
189	VCI	1995	-309	50 * 80
190	VCI	2065	-309	50 * 80
191	VCI	2135	-309	50 * 80
192	VCI	2205	-309	50 * 80
193	TEST3	2275	-309	50 * 80
194	C11B	2345	-309	50 * 80
195	C11B	2415	-309	50 * 80
196	C11B	2485	-309	50 * 80
197	C11B	2555	-309	50 * 80
198	C11B	2625	-309	50 * 80
199	C11B	2695	-309	50 * 80
200	C11B	2765	-309	50 * 80
201	C11B	2835	-309	50 * 80
202	C11B	2905	-309	50 * 80
203	C11B	2975	-309	50 * 80
204	C11B	3045	-309	50 * 80
205	C11A	3115	-309	50 * 80
206	C11A	3185	-309	50 * 80
207	C11A	3255	-309	50 * 80
208	C11A	3325	-309	50 * 80
209	C11A	3395	-309	50 * 80
210	C11A	3465	-309	50 * 80
211	C11A	3535	-309	50 * 80
212	C11A	3605	-309	50 * 80
213	C11A	3675	-309	50 * 80
214	C11A	3745	-309	50 * 80
215	C11A	3815	-309	50 * 80
216	CX11B	3885	-309	50 * 80
217	CX11B	3955	-309	50 * 80
218	CX11B	4025	-309	50 * 80
219	CX11B	4095	-309	50 * 80
220	CX11B	4165	-309	50 * 80
221	CX11B	4235	-309	50 * 80
222	CX11B	4305	-309	50 * 80
223	CX11B	4375	-309	50 * 80
224	CX11B	4445	-309	50 * 80
225	CX11B	4515	-309	50 * 80
226	CX11A	4585	-309	50 * 80
227	CX11A	4655	-309	50 * 80
228	CX11A	4725	-309	50 * 80
229	CX11A	4795	-309	50 * 80
230	CX11A	4865	-309	50 * 80
231	CX11A	4935	-309	50 * 80
232	CX11A	5005	-309	50 * 80
233	CX11A	5075	-309	50 * 80
234	CX11A	5145	-309	50 * 80
235	CX11A	5215	-309	50 * 80
236	VGL	5285	-309	50 * 80
237	VGL	5355	-309	50 * 80
238	VGL	5425	-309	50 * 80
239	VGL	5495	-309	50 * 80
240	VGL	5565	-309	50 * 80

No.	Name	X	Y	Bump size
241	VGL	5635	-309	50 * 80
242	VGL	5705	-309	50 * 80
243	VGL	5775	-309	50 * 80
244	VGL	5845	-309	50 * 80
245	VGL	5915	-309	50 * 80
246	VSSD	5985	-309	50 * 80
247	VSSD	6055	-309	50 * 80
248	VSSD	6125	-309	50 * 80
249	VGH	6195	-309	50 * 80
250	VGH	6265	-309	50 * 80
251	VGH	6335	-309	50 * 80
252	VGH	6405	-309	50 * 80
253	VGH	6475	-309	50 * 80
254	VGH	6545	-309	50 * 80
255	VGH	6615	-309	50 * 80
256	VGH	6685	-309	50 * 80
257	C12B	6755	-309	50 * 80
258	C12B	6825	-309	50 * 80
259	C12B	6895	-309	50 * 80
260	C12B	6965	-309	50 * 80
261	C12B	7035	-309	50 * 80
262	C12B	7105	-309	50 * 80
263	C12A	7175	-309	50 * 80
264	C12A	7245	-309	50 * 80
265	C12A	7315	-309	50 * 80
266	C12A	7385	-309	50 * 80
267	C12A	7455	-309	50 * 80
268	C12A	7525	-309	50 * 80
269	C21B	7595	-309	50 * 80
270	C21B	7665	-309	50 * 80
271	C21B	7735	-309	50 * 80
272	C21B	7805	-309	50 * 80
273	C21B	7875	-309	50 * 80
274	C21B	7945	-309	50 * 80
275	C21B	8015	-309	50 * 80
276	C21B	8085	-309	50 * 80
277	C21B	8155	-309	50 * 80
278	C21B	8225	-309	50 * 80
279	C21B	8295	-309	50 * 80
280	C21B	8365	-309	50 * 80
281	C21B	8435	-309	50 * 80
282	C21B	8505	-309	50 * 80
283	C21A	8575	-309	50 * 80
284	C21A	8645	-309	50 * 80
285	C21A	8715	-309	50 * 80
286	C21A	8785	-309	50 * 80
287	C21A	8855	-309	50 * 80
288	C21A	8925	-309	50 * 80
289	C21A	8995	-309	50 * 80
290	C21A	9065	-309	50 * 80
291	C21A	9135	-309	50 * 80
292	C21A	9205	-309	50 * 80
293	C21A	9275	-309	50 * 80
294	C21A	9345	-309	50 * 80
295	C21A	9415	-309	50 * 80
296	C22B	9485	-309	50 * 80
297	C22B	9555	-309	50 * 80
298	C22B	9625	-309	50 * 80
299	C22B	9695	-309	50 * 80
300	C22B	9765	-309	50 * 80

No.	Name	X	Y	Bump size
301	C22B	9835	-309	50 * 80
302	C22B	9905	-309	50 * 80
303	C22B	9975	-309	50 * 80
304	C22B	10045	-309	50 * 80
305	C22B	10115	-309	50 * 80
306	C22B	10185	-309	50 * 80
307	C22B	10255	-309	50 * 80
308	C22A	10325	-309	50 * 80
309	C22A	10395	-309	50 * 80
310	C22A	10465	-309	50 * 80
311	C22A	10535	-309	50 * 80
312	C22A	10605	-309	50 * 80
313	C22A	10675	-309	50 * 80
314	C22A	10745	-309	50 * 80
315	C22A	10815	-309	50 * 80
316	C22A	10885	-309	50 * 80
317	C22A	10955	-309	50 * 80
318	C22A	11025	-309	50 * 80
319	C22A	11095	-309	50 * 80
320	C22A	11165	-309	50 * 80
321	DUMMY17	11205	124	15 * 120
322	DUMMY18	11190	269	15 * 120
323	G1	11175	124	15 * 120
324	G3	11160	269	15 * 120
325	G5	11145	124	15 * 120
326	G7	11130	269	15 * 120
327	G9	11115	124	15 * 120
328	G11	11100	269	15 * 120
329	G13	11085	124	15 * 120
330	G15	11070	269	15 * 120
331	G17	11055	124	15 * 120
332	G19	11040	269	15 * 120
333	G21	11025	124	15 * 120
334	G23	11010	269	15 * 120
335	G25	10995	124	15 * 120
336	G27	10980	269	15 * 120
337	G29	10965	124	15 * 120
338	G31	10950	269	15 * 120
339	G33	10935	124	15 * 120
340	G35	10920	269	15 * 120
341	G37	10905	124	15 * 120
342	G39	10890	269	15 * 120
343	G41	10875	124	15 * 120
344	G43	10860	269	15 * 120
345	G45	10845	124	15 * 120
346	G47	10830	269	15 * 120
347	G49	10815	124	15 * 120
348	G51	10800	269	15 * 120
349	G53	10785	124	15 * 120
350	G55	10770	269	15 * 120
351	G57	10755	124	15 * 120
352	G59	10740	269	15 * 120
353	G61	10725	124	15 * 120
354	G63	10710	269	15 * 120
355	G65	10695	124	15 * 120
356	G67	10680	269	15 * 120
357	G69	10665	124	15 * 120
358	G71	10650	269	15 * 120
359	G73	10635	124	15 * 120
360	G75	10620	269	15 * 120

No.	Name	X	Y	Bump size
361	G77	10605	124	15 * 120
362	G79	10590	269	15 * 120
363	G81	10575	124	15 * 120
364	G83	10560	269	15 * 120
365	G85	10545	124	15 * 120
366	G87	10530	269	15 * 120
367	G89	10515	124	15 * 120
368	G91	10500	269	15 * 120
369	G93	10485	124	15 * 120
370	G95	10470	269	15 * 120
371	G97	10455	124	15 * 120
372	G99	10440	269	15 * 120
373	G101	10425	124	15 * 120
374	G103	10410	269	15 * 120
375	G105	10395	124	15 * 120
376	G107	10380	269	15 * 120
377	G109	10365	124	15 * 120
378	G111	10350	269	15 * 120
379	G113	10335	124	15 * 120
380	G115	10320	269	15 * 120
381	G117	10305	124	15 * 120
382	G119	10290	269	15 * 120
383	G121	10275	124	15 * 120
384	G123	10260	269	15 * 120
385	G125	10245	124	15 * 120
386	G127	10230	269	15 * 120
387	G129	10215	124	15 * 120
388	G131	10200	269	15 * 120
389	G133	10185	124	15 * 120
390	G135	10170	269	15 * 120
391	G137	10155	124	15 * 120
392	G139	10140	269	15 * 120
393	G141	10125	124	15 * 120
394	G143	10110	269	15 * 120
395	G145	10095	124	15 * 120
396	G147	10080	269	15 * 120
397	G149	10065	124	15 * 120
398	G151	10050	269	15 * 120
399	G153	10035	124	15 * 120
400	G155	10020	269	15 * 120
401	G157	10005	124	15 * 120
402	G159	9990	269	15 * 120
403	G161	9975	124	15 * 120
404	G163	9960	269	15 * 120
405	G165	9945	124	15 * 120
406	G167	9930	269	15 * 120
407	G169	9915	124	15 * 120
408	G171	9900	269	15 * 120
409	G173	9885	124	15 * 120
410	G175	9870	269	15 * 120
411	G177	9855	124	15 * 120
412	G179	9840	269	15 * 120
413	G181	9825	124	15 * 120
414	G183	9810	269	15 * 120
415	G185	9795	124	15 * 120
416	G187	9780	269	15 * 120
417	G189	9765	124	15 * 120
418	G191	9750	269	15 * 120
419	G193	9735	124	15 * 120
420	G195	9720	269	15 * 120

No.	Name	X	Y	Bump size
421	G197	9705	124	15 * 120
422	G199	9690	269	15 * 120
423	G201	9675	124	15 * 120
424	G203	9660	269	15 * 120
425	G205	9645	124	15 * 120
426	G207	9630	269	15 * 120
427	G209	9615	124	15 * 120
428	G211	9600	269	15 * 120
429	G213	9585	124	15 * 120
430	G215	9570	269	15 * 120
431	G217	9555	124	15 * 120
432	G219	9540	269	15 * 120
433	G221	9525	124	15 * 120
434	G223	9510	269	15 * 120
435	G225	9495	124	15 * 120
436	G227	9480	269	15 * 120
437	G229	9465	124	15 * 120
438	G231	9450	269	15 * 120
439	G233	9435	124	15 * 120
440	G235	9420	269	15 * 120
441	G237	9405	124	15 * 120
442	G239	9390	269	15 * 120
443	G241	9375	124	15 * 120
444	G243	9360	269	15 * 120
445	G245	9345	124	15 * 120
446	G247	9330	269	15 * 120
447	G249	9315	124	15 * 120
448	G251	9300	269	15 * 120
449	G253	9285	124	15 * 120
450	G255	9270	269	15 * 120
451	G257	9255	124	15 * 120
452	G259	9240	269	15 * 120
453	G261	9225	124	15 * 120
454	G263	9210	269	15 * 120
455	G265	9195	124	15 * 120
456	G267	9180	269	15 * 120
457	G269	9165	124	15 * 120
458	G271	9150	269	15 * 120
459	G273	9135	124	15 * 120
460	G275	9120	269	15 * 120
461	G277	9105	124	15 * 120
462	G279	9090	269	15 * 120
463	G281	9075	124	15 * 120
464	G283	9060	269	15 * 120
465	G285	9045	124	15 * 120
466	G287	9030	269	15 * 120
467	G289	9015	124	15 * 120
468	G291	9000	269	15 * 120
469	G293	8985	124	15 * 120
470	G295	8970	269	15 * 120
471	G297	8955	124	15 * 120
472	G299	8940	269	15 * 120
473	G301	8925	124	15 * 120
474	G303	8910	269	15 * 120
475	G305	8895	124	15 * 120
476	G307	8880	269	15 * 120
477	G309	8865	124	15 * 120
478	G311	8850	269	15 * 120
479	G313	8835	124	15 * 120
480	G315	8820	269	15 * 120

No.	Name	X	Y	Bump size
481	G317	8805	124	15 * 120
482	G319	8790	269	15 * 120
483	G321	8775	124	15 * 120
484	G323	8760	269	15 * 120
485	G325	8745	124	15 * 120
486	G327	8730	269	15 * 120
487	G329	8715	124	15 * 120
488	G331	8700	269	15 * 120
489	G333	8685	124	15 * 120
490	G335	8670	269	15 * 120
491	G337	8655	124	15 * 120
492	G339	8640	269	15 * 120
493	G341	8625	124	15 * 120
494	G343	8610	269	15 * 120
495	G345	8595	124	15 * 120
496	G347	8580	269	15 * 120
497	G349	8565	124	15 * 120
498	G351	8550	269	15 * 120
499	G353	8535	124	15 * 120
500	G355	8520	269	15 * 120
501	G357	8505	124	15 * 120
502	G359	8490	269	15 * 120
503	G361	8475	124	15 * 120
504	G363	8460	269	15 * 120
505	G365	8445	124	15 * 120
506	G367	8430	269	15 * 120
507	G369	8415	124	15 * 120
508	G371	8400	269	15 * 120
509	G373	8385	124	15 * 120
510	G375	8370	269	15 * 120
511	G377	8355	124	15 * 120
512	G379	8340	269	15 * 120
513	G381	8325	124	15 * 120
514	G383	8310	269	15 * 120
515	G385	8295	124	15 * 120
516	G387	8280	269	15 * 120
517	G389	8265	124	15 * 120
518	G391	8250	269	15 * 120
519	G393	8235	124	15 * 120
520	G395	8220	269	15 * 120
521	G397	8205	124	15 * 120
522	G399	8190	269	15 * 120
523	G401	8175	124	15 * 120
524	G403	8160	269	15 * 120
525	G405	8145	124	15 * 120
526	G407	8130	269	15 * 120
527	G409	8115	124	15 * 120
528	G411	8100	269	15 * 120
529	G413	8085	124	15 * 120
530	G415	8070	269	15 * 120
531	G417	8055	124	15 * 120
532	G419	8040	269	15 * 120
533	G421	8025	124	15 * 120
534	G423	8010	269	15 * 120
535	G425	7995	124	15 * 120
536	G427	7980	269	15 * 120
537	G429	7965	124	15 * 120
538	G431	7950	269	15 * 120
539	G433	7935	124	15 * 120
540	G435	7920	269	15 * 120

No.	Name	X	Y	Bump size
541	G437	7905	124	15 * 120
542	G439	7890	269	15 * 120
543	G441	7875	124	15 * 120
544	G443	7860	269	15 * 120
545	G445	7845	124	15 * 120
546	G447	7830	269	15 * 120
547	G449	7815	124	15 * 120
548	G451	7800	269	15 * 120
549	G453	7785	124	15 * 120
550	G455	7770	269	15 * 120
551	G457	7755	124	15 * 120
552	G459	7740	269	15 * 120
553	G461	7725	124	15 * 120
554	G463	7710	269	15 * 120
555	G465	7695	124	15 * 120
556	G467	7680	269	15 * 120
557	G469	7665	124	15 * 120
558	G471	7650	269	15 * 120
559	G473	7635	124	15 * 120
560	G475	7620	269	15 * 120
561	G477	7605	124	15 * 120
562	G479	7590	269	15 * 120
563	DUMMY19	7575	124	15 * 120
564	DUMMY20	7560	269	15 * 120
565	DUMMY21	7395	124	15 * 120
566	DUMMY22	7380	269	15 * 120
567	S960	7365	124	15 * 120
568	S959	7350	269	15 * 120
569	S958	7335	124	15 * 120
570	S957	7320	269	15 * 120
571	S956	7305	124	15 * 120
572	S955	7290	269	15 * 120
573	S954	7275	124	15 * 120
574	S953	7260	269	15 * 120
575	S952	7245	124	15 * 120
576	S951	7230	269	15 * 120
577	S950	7215	124	15 * 120
578	S949	7200	269	15 * 120
579	S948	7185	124	15 * 120
580	S947	7170	269	15 * 120
581	S946	7155	124	15 * 120
582	S945	7140	269	15 * 120
583	S944	7125	124	15 * 120
584	S943	7110	269	15 * 120
585	S942	7095	124	15 * 120
586	S941	7080	269	15 * 120
587	S940	7065	124	15 * 120
588	S939	7050	269	15 * 120
589	S938	7035	124	15 * 120
590	S937	7020	269	15 * 120
591	S936	7005	124	15 * 120
592	S935	6990	269	15 * 120
593	S934	6975	124	15 * 120
594	S933	6960	269	15 * 120
595	S932	6945	124	15 * 120
596	S931	6930	269	15 * 120
597	S930	6915	124	15 * 120
598	S929	6900	269	15 * 120
599	S928	6885	124	15 * 120
600	S927	6870	269	15 * 120

No.	Name	X	Y	Bump size
601	S926	6855	124	15 * 120
602	S925	6840	269	15 * 120
603	S924	6825	124	15 * 120
604	S923	6810	269	15 * 120
605	S922	6795	124	15 * 120
606	S921	6780	269	15 * 120
607	S920	6765	124	15 * 120
608	S919	6750	269	15 * 120
609	S918	6735	124	15 * 120
610	S917	6720	269	15 * 120
611	S916	6705	124	15 * 120
612	S915	6690	269	15 * 120
613	S914	6675	124	15 * 120
614	S913	6660	269	15 * 120
615	S912	6645	124	15 * 120
616	S911	6630	269	15 * 120
617	S910	6615	124	15 * 120
618	S909	6600	269	15 * 120
619	S908	6585	124	15 * 120
620	S907	6570	269	15 * 120
621	S906	6555	124	15 * 120
622	S905	6540	269	15 * 120
623	S904	6525	124	15 * 120
624	S903	6510	269	15 * 120
625	S902	6495	124	15 * 120
626	S901	6480	269	15 * 120
627	S900	6465	124	15 * 120
628	S899	6450	269	15 * 120
629	S898	6435	124	15 * 120
630	S897	6420	269	15 * 120
631	S896	6405	124	15 * 120
632	S895	6390	269	15 * 120
633	S894	6375	124	15 * 120
634	S893	6360	269	15 * 120
635	S892	6345	124	15 * 120
636	S891	6330	269	15 * 120
637	S890	6315	124	15 * 120
638	S889	6300	269	15 * 120
639	S888	6285	124	15 * 120
640	S887	6270	269	15 * 120
641	S886	6255	124	15 * 120
642	S885	6240	269	15 * 120
643	S884	6225	124	15 * 120
644	S883	6210	269	15 * 120
645	S882	6195	124	15 * 120
646	S881	6180	269	15 * 120
647	S880	6165	124	15 * 120
648	S879	6150	269	15 * 120
649	S878	6135	124	15 * 120
650	S877	6120	269	15 * 120
651	S876	6105	124	15 * 120
652	S875	6090	269	15 * 120
653	S874	6075	124	15 * 120
654	S873	6060	269	15 * 120
655	S872	6045	124	15 * 120
656	S871	6030	269	15 * 120
657	S870	6015	124	15 * 120
658	S869	6000	269	15 * 120
659	S868	5985	124	15 * 120
660	S867	5970	269	15 * 120

No.	Name	X	Y	Bump size
661	S866	5955	124	15 * 120
662	S865	5940	269	15 * 120
663	S864	5925	124	15 * 120
664	S863	5910	269	15 * 120
665	S862	5895	124	15 * 120
666	S861	5880	269	15 * 120
667	S860	5865	124	15 * 120
668	S859	5850	269	15 * 120
669	S858	5835	124	15 * 120
670	S857	5820	269	15 * 120
671	S856	5805	124	15 * 120
672	S855	5790	269	15 * 120
673	S854	5775	124	15 * 120
674	S853	5760	269	15 * 120
675	S852	5745	124	15 * 120
676	S851	5730	269	15 * 120
677	S850	5715	124	15 * 120
678	S849	5700	269	15 * 120
679	S848	5685	124	15 * 120
680	S847	5670	269	15 * 120
681	S846	5655	124	15 * 120
682	S845	5640	269	15 * 120
683	S844	5625	124	15 * 120
684	S843	5610	269	15 * 120
685	S842	5595	124	15 * 120
686	S841	5580	269	15 * 120
687	S840	5565	124	15 * 120
688	S839	5550	269	15 * 120
689	S838	5535	124	15 * 120
690	S837	5520	269	15 * 120
691	S836	5505	124	15 * 120
692	S835	5490	269	15 * 120
693	S834	5475	124	15 * 120
694	S833	5460	269	15 * 120
695	S832	5445	124	15 * 120
696	S831	5430	269	15 * 120
697	S830	5415	124	15 * 120
698	S829	5400	269	15 * 120
699	S828	5385	124	15 * 120
700	S827	5370	269	15 * 120
701	S826	5355	124	15 * 120
702	S825	5340	269	15 * 120
703	S824	5325	124	15 * 120
704	S823	5310	269	15 * 120
705	S822	5295	124	15 * 120
706	S821	5280	269	15 * 120
707	S820	5265	124	15 * 120
708	S819	5250	269	15 * 120
709	S818	5235	124	15 * 120
710	S817	5220	269	15 * 120
711	S816	5205	124	15 * 120
712	S815	5190	269	15 * 120
713	S814	5175	124	15 * 120
714	S813	5160	269	15 * 120
715	S812	5145	124	15 * 120
716	S811	5130	269	15 * 120
717	S810	5115	124	15 * 120
718	S809	5100	269	15 * 120
719	S808	5085	124	15 * 120
720	S807	5070	269	15 * 120

No.	Name	X	Y	Bump size
721	S806	5055	124	15 * 120
722	S805	5040	269	15 * 120
723	S804	5025	124	15 * 120
724	S803	5010	269	15 * 120
725	S802	4995	124	15 * 120
726	S801	4980	269	15 * 120
727	S800	4965	124	15 * 120
728	S799	4950	269	15 * 120
729	S798	4935	124	15 * 120
730	S797	4920	269	15 * 120
731	S796	4905	124	15 * 120
732	S795	4890	269	15 * 120
733	S794	4875	124	15 * 120
734	S793	4860	269	15 * 120
735	S792	4845	124	15 * 120
736	S791	4830	269	15 * 120
737	S790	4815	124	15 * 120
738	S789	4800	269	15 * 120
739	S788	4785	124	15 * 120
740	S787	4770	269	15 * 120
741	S786	4755	124	15 * 120
742	S785	4740	269	15 * 120
743	S784	4725	124	15 * 120
744	S783	4710	269	15 * 120
745	S782	4695	124	15 * 120
746	S781	4680	269	15 * 120
747	S780	4665	124	15 * 120
748	S779	4650	269	15 * 120
749	S778	4635	124	15 * 120
750	S777	4620	269	15 * 120
751	S776	4605	124	15 * 120
752	S775	4590	269	15 * 120
753	S774	4575	124	15 * 120
754	S773	4560	269	15 * 120
755	S772	4545	124	15 * 120
756	S771	4530	269	15 * 120
757	S770	4515	124	15 * 120
758	S769	4500	269	15 * 120
759	S768	4485	124	15 * 120
760	S767	4470	269	15 * 120
761	S766	4455	124	15 * 120
762	S765	4440	269	15 * 120
763	S764	4425	124	15 * 120
764	S763	4410	269	15 * 120
765	S762	4395	124	15 * 120
766	S761	4380	269	15 * 120
767	S760	4365	124	15 * 120
768	S759	4350	269	15 * 120
769	S758	4335	124	15 * 120
770	S757	4320	269	15 * 120
771	S756	4305	124	15 * 120
772	S755	4290	269	15 * 120
773	S754	4275	124	15 * 120
774	S753	4260	269	15 * 120
775	S752	4245	124	15 * 120
776	S751	4230	269	15 * 120
777	S750	4215	124	15 * 120
778	S749	4200	269	15 * 120
779	S748	4185	124	15 * 120
780	S747	4170	269	15 * 120

No.	Name	X	Y	Bump size
781	S746	4155	124	15 * 120
782	S745	4140	269	15 * 120
783	S744	4125	124	15 * 120
784	S743	4110	269	15 * 120
785	S742	4095	124	15 * 120
786	S741	4080	269	15 * 120
787	S740	4065	124	15 * 120
788	S739	4050	269	15 * 120
789	S738	4035	124	15 * 120
790	S737	4020	269	15 * 120
791	S736	4005	124	15 * 120
792	S735	3990	269	15 * 120
793	S734	3975	124	15 * 120
794	S733	3960	269	15 * 120
795	S732	3945	124	15 * 120
796	S731	3930	269	15 * 120
797	S730	3915	124	15 * 120
798	S729	3900	269	15 * 120
799	S728	3885	124	15 * 120
800	S727	3870	269	15 * 120
801	S726	3855	124	15 * 120
802	S725	3840	269	15 * 120
803	S724	3825	124	15 * 120
804	S723	3810	269	15 * 120
805	S722	3795	124	15 * 120
806	S721	3780	269	15 * 120
807	S720	3765	124	15 * 120
808	S719	3750	269	15 * 120
809	S718	3735	124	15 * 120
810	S717	3720	269	15 * 120
811	S716	3705	124	15 * 120
812	S715	3690	269	15 * 120
813	S714	3675	124	15 * 120
814	S713	3660	269	15 * 120
815	S712	3645	124	15 * 120
816	S711	3630	269	15 * 120
817	S710	3615	124	15 * 120
818	S709	3600	269	15 * 120
819	S708	3585	124	15 * 120
820	S707	3570	269	15 * 120
821	S706	3555	124	15 * 120
822	S705	3540	269	15 * 120
823	S704	3525	124	15 * 120
824	S703	3510	269	15 * 120
825	S702	3495	124	15 * 120
826	S701	3480	269	15 * 120
827	S700	3465	124	15 * 120
828	S699	3450	269	15 * 120
829	S698	3435	124	15 * 120
830	S697	3420	269	15 * 120
831	S696	3405	124	15 * 120
832	S695	3390	269	15 * 120
833	S694	3375	124	15 * 120
834	S693	3360	269	15 * 120
835	S692	3345	124	15 * 120
836	S691	3330	269	15 * 120
837	S690	3315	124	15 * 120
838	S689	3300	269	15 * 120
839	S688	3285	124	15 * 120
840	S687	3270	269	15 * 120

No.	Name	X	Y	Bump size
841	S686	3255	124	15 * 120
842	S685	3240	269	15 * 120
843	S684	3225	124	15 * 120
844	S683	3210	269	15 * 120
845	S682	3195	124	15 * 120
846	S681	3180	269	15 * 120
847	S680	3165	124	15 * 120
848	S679	3150	269	15 * 120
849	S678	3135	124	15 * 120
850	S677	3120	269	15 * 120
851	S676	3105	124	15 * 120
852	S675	3090	269	15 * 120
853	S674	3075	124	15 * 120
854	S673	3060	269	15 * 120
855	S672	3045	124	15 * 120
856	S671	3030	269	15 * 120
857	S670	3015	124	15 * 120
858	S669	3000	269	15 * 120
859	S668	2985	124	15 * 120
860	S667	2970	269	15 * 120
861	S666	2955	124	15 * 120
862	S665	2940	269	15 * 120
863	S664	2925	124	15 * 120
864	S663	2910	269	15 * 120
865	S662	2895	124	15 * 120
866	S661	2880	269	15 * 120
867	S660	2865	124	15 * 120
868	S659	2850	269	15 * 120
869	S658	2835	124	15 * 120
870	S657	2820	269	15 * 120
871	S656	2805	124	15 * 120
872	S655	2790	269	15 * 120
873	S654	2775	124	15 * 120
874	S653	2760	269	15 * 120
875	S652	2745	124	15 * 120
876	S651	2730	269	15 * 120
877	S650	2715	124	15 * 120
878	S649	2700	269	15 * 120
879	S648	2685	124	15 * 120
880	S647	2670	269	15 * 120
881	S646	2655	124	15 * 120
882	S645	2640	269	15 * 120
883	S644	2625	124	15 * 120
884	S643	2610	269	15 * 120
885	S642	2595	124	15 * 120
886	S641	2580	269	15 * 120
887	S640	2565	124	15 * 120
888	S639	2550	269	15 * 120
889	S638	2535	124	15 * 120
890	S637	2520	269	15 * 120
891	S636	2505	124	15 * 120
892	S635	2490	269	15 * 120
893	S634	2475	124	15 * 120
894	S633	2460	269	15 * 120
895	S632	2445	124	15 * 120
896	S631	2430	269	15 * 120
897	S630	2415	124	15 * 120
898	S629	2400	269	15 * 120
899	S628	2385	124	15 * 120
900	S627	2370	269	15 * 120

No.	Name	X	Y	Bump size
901	S626	2355	124	15 * 120
902	S625	2340	269	15 * 120
903	S624	2325	124	15 * 120
904	S623	2310	269	15 * 120
905	S622	2295	124	15 * 120
906	S621	2280	269	15 * 120
907	S620	2265	124	15 * 120
908	S619	2250	269	15 * 120
909	S618	2235	124	15 * 120
910	S617	2220	269	15 * 120
911	S616	2205	124	15 * 120
912	S615	2190	269	15 * 120
913	S614	2175	124	15 * 120
914	S613	2160	269	15 * 120
915	S612	2145	124	15 * 120
916	S611	2130	269	15 * 120
917	S610	2115	124	15 * 120
918	S609	2100	269	15 * 120
919	S608	2085	124	15 * 120
920	S607	2070	269	15 * 120
921	S606	2055	124	15 * 120
922	S605	2040	269	15 * 120
923	S604	2025	124	15 * 120
924	S603	2010	269	15 * 120
925	S602	1995	124	15 * 120
926	S601	1980	269	15 * 120
927	S600	1965	124	15 * 120
928	S599	1950	269	15 * 120
929	S598	1935	124	15 * 120
930	S597	1920	269	15 * 120
931	S596	1905	124	15 * 120
932	S595	1890	269	15 * 120
933	S594	1875	124	15 * 120
934	S593	1860	269	15 * 120
935	S592	1845	124	15 * 120
936	S591	1830	269	15 * 120
937	S590	1815	124	15 * 120
938	S589	1800	269	15 * 120
939	S588	1785	124	15 * 120
940	S587	1770	269	15 * 120
941	S586	1755	124	15 * 120
942	S585	1740	269	15 * 120
943	S584	1725	124	15 * 120
944	S583	1710	269	15 * 120
945	S582	1695	124	15 * 120
946	S581	1680	269	15 * 120
947	S580	1665	124	15 * 120
948	S579	1650	269	15 * 120
949	S578	1635	124	15 * 120
950	S577	1620	269	15 * 120
951	S576	1605	124	15 * 120
952	S575	1590	269	15 * 120
953	S574	1575	124	15 * 120
954	S573	1560	269	15 * 120
955	S572	1545	124	15 * 120
956	S571	1530	269	15 * 120
957	S570	1515	124	15 * 120
958	S569	1500	269	15 * 120
959	S568	1485	124	15 * 120
960	S567	1470	269	15 * 120

No.	Name	X	Y	Bump size
961	S566	1455	124	15 * 120
962	S565	1440	269	15 * 120
963	S564	1425	124	15 * 120
964	S563	1410	269	15 * 120
965	S562	1395	124	15 * 120
966	S561	1380	269	15 * 120
967	S560	1365	124	15 * 120
968	S559	1350	269	15 * 120
969	S558	1335	124	15 * 120
970	S557	1320	269	15 * 120
971	S556	1305	124	15 * 120
972	S555	1290	269	15 * 120
973	S554	1275	124	15 * 120
974	S553	1260	269	15 * 120
975	S552	1245	124	15 * 120
976	S551	1230	269	15 * 120
977	S550	1215	124	15 * 120
978	S549	1200	269	15 * 120
979	S548	1185	124	15 * 120
980	S547	1170	269	15 * 120
981	S546	1155	124	15 * 120
982	S545	1140	269	15 * 120
983	S544	1125	124	15 * 120
984	S543	1110	269	15 * 120
985	S542	1095	124	15 * 120
986	S541	1080	269	15 * 120
987	S540	1065	124	15 * 120
988	S539	1050	269	15 * 120
989	S538	1035	124	15 * 120
990	S537	1020	269	15 * 120
991	S536	1005	124	15 * 120
992	S535	990	269	15 * 120
993	S534	975	124	15 * 120
994	S533	960	269	15 * 120
995	S532	945	124	15 * 120
996	S531	930	269	15 * 120
997	S530	915	124	15 * 120
998	S529	900	269	15 * 120
999	S528	885	124	15 * 120
1000	S527	870	269	15 * 120
1001	S526	855	124	15 * 120
1002	S525	840	269	15 * 120
1003	S524	825	124	15 * 120
1004	S523	810	269	15 * 120
1005	S522	795	124	15 * 120
1006	S521	780	269	15 * 120
1007	S520	765	124	15 * 120
1008	S519	750	269	15 * 120
1009	S518	735	124	15 * 120
1010	S517	720	269	15 * 120
1011	S516	705	124	15 * 120
1012	S515	690	269	15 * 120
1013	S514	675	124	15 * 120
1014	S513	660	269	15 * 120
1015	S512	645	124	15 * 120
1016	S511	630	269	15 * 120
1017	S510	615	124	15 * 120
1018	S509	600	269	15 * 120
1019	S508	585	124	15 * 120
1020	S507	570	269	15 * 120

No.	Name	X	Y	Bump size
1021	S506	555	124	15 * 120
1022	S505	540	269	15 * 120
1023	S504	525	124	15 * 120
1024	S503	510	269	15 * 120
1025	S502	495	124	15 * 120
1026	S501	480	269	15 * 120
1027	S500	465	124	15 * 120
1028	S499	450	269	15 * 120
1029	S498	435	124	15 * 120
1030	S497	420	269	15 * 120
1031	S496	405	124	15 * 120
1032	S495	390	269	15 * 120
1033	S494	375	124	15 * 120
1034	S493	360	269	15 * 120
1035	S492	345	124	15 * 120
1036	S491	330	269	15 * 120
1037	S490	315	124	15 * 120
1038	S489	300	269	15 * 120
1039	S488	285	124	15 * 120
1040	S487	270	269	15 * 120
1041	S486	255	124	15 * 120
1042	S485	240	269	15 * 120
1043	S484	225	124	15 * 120
1044	S483	210	269	15 * 120
1045	S482	195	124	15 * 120
1046	S481	180	269	15 * 120
1047	VTEST	165	124	15 * 120
1048	DUMMY23	150	269	15 * 120
1049	DUMMY24	-150	269	15 * 120
1050	TVCOMHI	-165	124	15 * 120
1051	S480	-180	269	15 * 120
1052	S479	-195	124	15 * 120
1053	S478	-210	269	15 * 120
1054	S477	-225	124	15 * 120
1055	S476	-240	269	15 * 120
1056	S475	-255	124	15 * 120
1057	S474	-270	269	15 * 120
1058	S473	-285	124	15 * 120
1059	S472	-300	269	15 * 120
1060	S471	-315	124	15 * 120
1061	S470	-330	269	15 * 120
1062	S469	-345	124	15 * 120
1063	S468	-360	269	15 * 120
1064	S467	-375	124	15 * 120
1065	S466	-390	269	15 * 120
1066	S465	-405	124	15 * 120
1067	S464	-420	269	15 * 120
1068	S463	-435	124	15 * 120
1069	S462	-450	269	15 * 120
1070	S461	-465	124	15 * 120
1071	S460	-480	269	15 * 120
1072	S459	-495	124	15 * 120
1073	S458	-510	269	15 * 120
1074	S457	-525	124	15 * 120
1075	S456	-540	269	15 * 120
1076	S455	-555	124	15 * 120
1077	S454	-570	269	15 * 120
1078	S453	-585	124	15 * 120
1079	S452	-600	269	15 * 120
1080	S451	-615	124	15 * 120

No.	Name	X	Y	Bump size
1081	S450	-630	269	15 * 120
1082	S449	-645	124	15 * 120
1083	S448	-660	269	15 * 120
1084	S447	-675	124	15 * 120
1085	S446	-690	269	15 * 120
1086	S445	-705	124	15 * 120
1087	S444	-720	269	15 * 120
1088	S443	-735	124	15 * 120
1089	S442	-750	269	15 * 120
1090	S441	-765	124	15 * 120
1091	S440	-780	269	15 * 120
1092	S439	-795	124	15 * 120
1093	S438	-810	269	15 * 120
1094	S437	-825	124	15 * 120
1095	S436	-840	269	15 * 120
1096	S435	-855	124	15 * 120
1097	S434	-870	269	15 * 120
1098	S433	-885	124	15 * 120
1099	S432	-900	269	15 * 120
1100	S431	-915	124	15 * 120
1101	S430	-930	269	15 * 120
1102	S429	-945	124	15 * 120
1103	S428	-960	269	15 * 120
1104	S427	-975	124	15 * 120
1105	S426	-990	269	15 * 120
1106	S425	-1005	124	15 * 120
1107	S424	-1020	269	15 * 120
1108	S423	-1035	124	15 * 120
1109	S422	-1050	269	15 * 120
1110	S421	-1065	124	15 * 120
1111	S420	-1080	269	15 * 120
1112	S419	-1095	124	15 * 120
1113	S418	-1110	269	15 * 120
1114	S417	-1125	124	15 * 120
1115	S416	-1140	269	15 * 120
1116	S415	-1155	124	15 * 120
1117	S414	-1170	269	15 * 120
1118	S413	-1185	124	15 * 120
1119	S412	-1200	269	15 * 120
1120	S411	-1215	124	15 * 120
1121	S410	-1230	269	15 * 120
1122	S409	-1245	124	15 * 120
1123	S408	-1260	269	15 * 120
1124	S407	-1275	124	15 * 120
1125	S406	-1290	269	15 * 120
1126	S405	-1305	124	15 * 120
1127	S404	-1320	269	15 * 120
1128	S403	-1335	124	15 * 120
1129	S402	-1350	269	15 * 120
1130	S401	-1365	124	15 * 120
1131	S400	-1380	269	15 * 120
1132	S399	-1395	124	15 * 120
1133	S398	-1410	269	15 * 120
1134	S397	-1425	124	15 * 120
1135	S396	-1440	269	15 * 120
1136	S395	-1455	124	15 * 120
1137	S394	-1470	269	15 * 120
1138	S393	-1485	124	15 * 120
1139	S392	-1500	269	15 * 120
1140	S391	-1515	124	15 * 120

No.	Name	X	Y	Bump size
1141	S390	-1530	269	15 * 120
1142	S389	-1545	124	15 * 120
1143	S388	-1560	269	15 * 120
1144	S387	-1575	124	15 * 120
1145	S386	-1590	269	15 * 120
1146	S385	-1605	124	15 * 120
1147	S384	-1620	269	15 * 120
1148	S383	-1635	124	15 * 120
1149	S382	-1650	269	15 * 120
1150	S381	-1665	124	15 * 120
1151	S380	-1680	269	15 * 120
1152	S379	-1695	124	15 * 120
1153	S378	-1710	269	15 * 120
1154	S377	-1725	124	15 * 120
1155	S376	-1740	269	15 * 120
1156	S375	-1755	124	15 * 120
1157	S374	-1770	269	15 * 120
1158	S373	-1785	124	15 * 120
1159	S372	-1800	269	15 * 120
1160	S371	-1815	124	15 * 120
1161	S370	-1830	269	15 * 120
1162	S369	-1845	124	15 * 120
1163	S368	-1860	269	15 * 120
1164	S367	-1875	124	15 * 120
1165	S366	-1890	269	15 * 120
1166	S365	-1905	124	15 * 120
1167	S364	-1920	269	15 * 120
1168	S363	-1935	124	15 * 120
1169	S362	-1950	269	15 * 120
1170	S361	-1965	124	15 * 120
1171	S360	-1980	269	15 * 120
1172	S359	-1995	124	15 * 120
1173	S358	-2010	269	15 * 120
1174	S357	-2025	124	15 * 120
1175	S356	-2040	269	15 * 120
1176	S355	-2055	124	15 * 120
1177	S354	-2070	269	15 * 120
1178	S353	-2085	124	15 * 120
1179	S352	-2100	269	15 * 120
1180	S351	-2115	124	15 * 120
1181	S350	-2130	269	15 * 120
1182	S349	-2145	124	15 * 120
1183	S348	-2160	269	15 * 120
1184	S347	-2175	124	15 * 120
1185	S346	-2190	269	15 * 120
1186	S345	-2205	124	15 * 120
1187	S344	-2220	269	15 * 120
1188	S343	-2235	124	15 * 120
1189	S342	-2250	269	15 * 120
1190	S341	-2265	124	15 * 120
1191	S340	-2280	269	15 * 120
1192	S339	-2295	124	15 * 120
1193	S338	-2310	269	15 * 120
1194	S337	-2325	124	15 * 120
1195	S336	-2340	269	15 * 120
1196	S335	-2355	124	15 * 120
1197	S334	-2370	269	15 * 120
1198	S333	-2385	124	15 * 120
1199	S332	-2400	269	15 * 120
1200	S331	-2415	124	15 * 120

No.	Name	X	Y	Bump size
1201	S330	-2430	269	15 * 120
1202	S329	-2445	124	15 * 120
1203	S328	-2460	269	15 * 120
1204	S327	-2475	124	15 * 120
1205	S326	-2490	269	15 * 120
1206	S325	-2505	124	15 * 120
1207	S324	-2520	269	15 * 120
1208	S323	-2535	124	15 * 120
1209	S322	-2550	269	15 * 120
1210	S321	-2565	124	15 * 120
1211	S320	-2580	269	15 * 120
1212	S319	-2595	124	15 * 120
1213	S318	-2610	269	15 * 120
1214	S317	-2625	124	15 * 120
1215	S316	-2640	269	15 * 120
1216	S315	-2655	124	15 * 120
1217	S314	-2670	269	15 * 120
1218	S313	-2685	124	15 * 120
1219	S312	-2700	269	15 * 120
1220	S311	-2715	124	15 * 120
1221	S310	-2730	269	15 * 120
1222	S309	-2745	124	15 * 120
1223	S308	-2760	269	15 * 120
1224	S307	-2775	124	15 * 120
1225	S306	-2790	269	15 * 120
1226	S305	-2805	124	15 * 120
1227	S304	-2820	269	15 * 120
1228	S303	-2835	124	15 * 120
1229	S302	-2850	269	15 * 120
1230	S301	-2865	124	15 * 120
1231	S300	-2880	269	15 * 120
1232	S299	-2895	124	15 * 120
1233	S298	-2910	269	15 * 120
1234	S297	-2925	124	15 * 120
1235	S296	-2940	269	15 * 120
1236	S295	-2955	124	15 * 120
1237	S294	-2970	269	15 * 120
1238	S293	-2985	124	15 * 120
1239	S292	-3000	269	15 * 120
1240	S291	-3015	124	15 * 120
1241	S290	-3030	269	15 * 120
1242	S289	-3045	124	15 * 120
1243	S288	-3060	269	15 * 120
1244	S287	-3075	124	15 * 120
1245	S286	-3090	269	15 * 120
1246	S285	-3105	124	15 * 120
1247	S284	-3120	269	15 * 120
1248	S283	-3135	124	15 * 120
1249	S282	-3150	269	15 * 120
1250	S281	-3165	124	15 * 120
1251	S280	-3180	269	15 * 120
1252	S279	-3195	124	15 * 120
1253	S278	-3210	269	15 * 120
1254	S277	-3225	124	15 * 120
1255	S276	-3240	269	15 * 120
1256	S275	-3255	124	15 * 120
1257	S274	-3270	269	15 * 120
1258	S273	-3285	124	15 * 120
1259	S272	-3300	269	15 * 120
1260	S271	-3315	124	15 * 120

No.	Name	X	Y	Bump size
1261	S270	-3330	269	15 * 120
1262	S269	-3345	124	15 * 120
1263	S268	-3360	269	15 * 120
1264	S267	-3375	124	15 * 120
1265	S266	-3390	269	15 * 120
1266	S265	-3405	124	15 * 120
1267	S264	-3420	269	15 * 120
1268	S263	-3435	124	15 * 120
1269	S262	-3450	269	15 * 120
1270	S261	-3465	124	15 * 120
1271	S260	-3480	269	15 * 120
1272	S259	-3495	124	15 * 120
1273	S258	-3510	269	15 * 120
1274	S257	-3525	124	15 * 120
1275	S256	-3540	269	15 * 120
1276	S255	-3555	124	15 * 120
1277	S254	-3570	269	15 * 120
1278	S253	-3585	124	15 * 120
1279	S252	-3600	269	15 * 120
1280	S251	-3615	124	15 * 120
1281	S250	-3630	269	15 * 120
1282	S249	-3645	124	15 * 120
1283	S248	-3660	269	15 * 120
1284	S247	-3675	124	15 * 120
1285	S246	-3690	269	15 * 120
1286	S245	-3705	124	15 * 120
1287	S244	-3720	269	15 * 120
1288	S243	-3735	124	15 * 120
1289	S242	-3750	269	15 * 120
1290	S241	-3765	124	15 * 120
1291	S240	-3780	269	15 * 120
1292	S239	-3795	124	15 * 120
1293	S238	-3810	269	15 * 120
1294	S237	-3825	124	15 * 120
1295	S236	-3840	269	15 * 120
1296	S235	-3855	124	15 * 120
1297	S234	-3870	269	15 * 120
1298	S233	-3885	124	15 * 120
1299	S232	-3900	269	15 * 120
1300	S231	-3915	124	15 * 120
1301	S230	-3930	269	15 * 120
1302	S229	-3945	124	15 * 120
1303	S228	-3960	269	15 * 120
1304	S227	-3975	124	15 * 120
1305	S226	-3990	269	15 * 120
1306	S225	-4005	124	15 * 120
1307	S224	-4020	269	15 * 120
1308	S223	-4035	124	15 * 120
1309	S222	-4050	269	15 * 120
1310	S221	-4065	124	15 * 120
1311	S220	-4080	269	15 * 120
1312	S219	-4095	124	15 * 120
1313	S218	-4110	269	15 * 120
1314	S217	-4125	124	15 * 120
1315	S216	-4140	269	15 * 120
1316	S215	-4155	124	15 * 120
1317	S214	-4170	269	15 * 120
1318	S213	-4185	124	15 * 120
1319	S212	-4200	269	15 * 120
1320	S211	-4215	124	15 * 120

No.	Name	X	Y	Bump size
1321	S210	-4230	269	15 * 120
1322	S209	-4245	124	15 * 120
1323	S208	-4260	269	15 * 120
1324	S207	-4275	124	15 * 120
1325	S206	-4290	269	15 * 120
1326	S205	-4305	124	15 * 120
1327	S204	-4320	269	15 * 120
1328	S203	-4335	124	15 * 120
1329	S202	-4350	269	15 * 120
1330	S201	-4365	124	15 * 120
1331	S200	-4380	269	15 * 120
1332	S199	-4395	124	15 * 120
1333	S198	-4410	269	15 * 120
1334	S197	-4425	124	15 * 120
1335	S196	-4440	269	15 * 120
1336	S195	-4455	124	15 * 120
1337	S194	-4470	269	15 * 120
1338	S193	-4485	124	15 * 120
1339	S192	-4500	269	15 * 120
1340	S191	-4515	124	15 * 120
1341	S190	-4530	269	15 * 120
1342	S189	-4545	124	15 * 120
1343	S188	-4560	269	15 * 120
1344	S187	-4575	124	15 * 120
1345	S186	-4590	269	15 * 120
1346	S185	-4605	124	15 * 120
1347	S184	-4620	269	15 * 120
1348	S183	-4635	124	15 * 120
1349	S182	-4650	269	15 * 120
1350	S181	-4665	124	15 * 120
1351	S180	-4680	269	15 * 120
1352	S179	-4695	124	15 * 120
1353	S178	-4710	269	15 * 120
1354	S177	-4725	124	15 * 120
1355	S176	-4740	269	15 * 120
1356	S175	-4755	124	15 * 120
1357	S174	-4770	269	15 * 120
1358	S173	-4785	124	15 * 120
1359	S172	-4800	269	15 * 120
1360	S171	-4815	124	15 * 120
1361	S170	-4830	269	15 * 120
1362	S169	-4845	124	15 * 120
1363	S168	-4860	269	15 * 120
1364	S167	-4875	124	15 * 120
1365	S166	-4890	269	15 * 120
1366	S165	-4905	124	15 * 120
1367	S164	-4920	269	15 * 120
1368	S163	-4935	124	15 * 120
1369	S162	-4950	269	15 * 120
1370	S161	-4965	124	15 * 120
1371	S160	-4980	269	15 * 120
1372	S159	-4995	124	15 * 120
1373	S158	-5010	269	15 * 120
1374	S157	-5025	124	15 * 120
1375	S156	-5040	269	15 * 120
1376	S155	-5055	124	15 * 120
1377	S154	-5070	269	15 * 120
1378	S153	-5085	124	15 * 120
1379	S152	-5100	269	15 * 120
1380	S151	-5115	124	15 * 120

No.	Name	X	Y	Bump size
1381	S150	-5130	269	15 * 120
1382	S149	-5145	124	15 * 120
1383	S148	-5160	269	15 * 120
1384	S147	-5175	124	15 * 120
1385	S146	-5190	269	15 * 120
1386	S145	-5205	124	15 * 120
1387	S144	-5220	269	15 * 120
1388	S143	-5235	124	15 * 120
1389	S142	-5250	269	15 * 120
1390	S141	-5265	124	15 * 120
1391	S140	-5280	269	15 * 120
1392	S139	-5295	124	15 * 120
1393	S138	-5310	269	15 * 120
1394	S137	-5325	124	15 * 120
1395	S136	-5340	269	15 * 120
1396	S135	-5355	124	15 * 120
1397	S134	-5370	269	15 * 120
1398	S133	-5385	124	15 * 120
1399	S132	-5400	269	15 * 120
1400	S131	-5415	124	15 * 120
1401	S130	-5430	269	15 * 120
1402	S129	-5445	124	15 * 120
1403	S128	-5460	269	15 * 120
1404	S127	-5475	124	15 * 120
1405	S126	-5490	269	15 * 120
1406	S125	-5505	124	15 * 120
1407	S124	-5520	269	15 * 120
1408	S123	-5535	124	15 * 120
1409	S122	-5550	269	15 * 120
1410	S121	-5565	124	15 * 120
1411	S120	-5580	269	15 * 120
1412	S119	-5595	124	15 * 120
1413	S118	-5610	269	15 * 120
1414	S117	-5625	124	15 * 120
1415	S116	-5640	269	15 * 120
1416	S115	-5655	124	15 * 120
1417	S114	-5670	269	15 * 120
1418	S113	-5685	124	15 * 120
1419	S112	-5700	269	15 * 120
1420	S111	-5715	124	15 * 120
1421	S110	-5730	269	15 * 120
1422	S109	-5745	124	15 * 120
1423	S108	-5760	269	15 * 120
1424	S107	-5775	124	15 * 120
1425	S106	-5790	269	15 * 120
1426	S105	-5805	124	15 * 120
1427	S104	-5820	269	15 * 120
1428	S103	-5835	124	15 * 120
1429	S102	-5850	269	15 * 120
1430	S101	-5865	124	15 * 120
1431	S100	-5880	269	15 * 120
1432	S99	-5895	124	15 * 120
1433	S98	-5910	269	15 * 120
1434	S97	-5925	124	15 * 120
1435	S96	-5940	269	15 * 120
1436	S95	-5955	124	15 * 120
1437	S94	-5970	269	15 * 120
1438	S93	-5985	124	15 * 120
1439	S92	-6000	269	15 * 120
1440	S91	-6015	124	15 * 120

No.	Name	X	Y	Bump size
1441	S90	-6030	269	15 * 120
1442	S89	-6045	124	15 * 120
1443	S88	-6060	269	15 * 120
1444	S87	-6075	124	15 * 120
1445	S86	-6090	269	15 * 120
1446	S85	-6105	124	15 * 120
1447	S84	-6120	269	15 * 120
1448	S83	-6135	124	15 * 120
1449	S82	-6150	269	15 * 120
1450	S81	-6165	124	15 * 120
1451	S80	-6180	269	15 * 120
1452	S79	-6195	124	15 * 120
1453	S78	-6210	269	15 * 120
1454	S77	-6225	124	15 * 120
1455	S76	-6240	269	15 * 120
1456	S75	-6255	124	15 * 120
1457	S74	-6270	269	15 * 120
1458	S73	-6285	124	15 * 120
1459	S72	-6300	269	15 * 120
1460	S71	-6315	124	15 * 120
1461	S70	-6330	269	15 * 120
1462	S69	-6345	124	15 * 120
1463	S68	-6360	269	15 * 120
1464	S67	-6375	124	15 * 120
1465	S66	-6390	269	15 * 120
1466	S65	-6405	124	15 * 120
1467	S64	-6420	269	15 * 120
1468	S63	-6435	124	15 * 120
1469	S62	-6450	269	15 * 120
1470	S61	-6465	124	15 * 120
1471	S60	-6480	269	15 * 120
1472	S59	-6495	124	15 * 120
1473	S58	-6510	269	15 * 120
1474	S57	-6525	124	15 * 120
1475	S56	-6540	269	15 * 120
1476	S55	-6555	124	15 * 120
1477	S54	-6570	269	15 * 120
1478	S53	-6585	124	15 * 120
1479	S52	-6600	269	15 * 120
1480	S51	-6615	124	15 * 120
1481	S50	-6630	269	15 * 120
1482	S49	-6645	124	15 * 120
1483	S48	-6660	269	15 * 120
1484	S47	-6675	124	15 * 120
1485	S46	-6690	269	15 * 120
1486	S45	-6705	124	15 * 120
1487	S44	-6720	269	15 * 120
1488	S43	-6735	124	15 * 120
1489	S42	-6750	269	15 * 120
1490	S41	-6765	124	15 * 120
1491	S40	-6780	269	15 * 120
1492	S39	-6795	124	15 * 120
1493	S38	-6810	269	15 * 120
1494	S37	-6825	124	15 * 120
1495	S36	-6840	269	15 * 120
1496	S35	-6855	124	15 * 120
1497	S34	-6870	269	15 * 120
1498	S33	-6885	124	15 * 120
1499	S32	-6900	269	15 * 120
1500	S31	-6915	124	15 * 120

No.	Name	X	Y	Bump size
1501	S30	-6930	269	15 * 120
1502	S29	-6945	124	15 * 120
1503	S28	-6960	269	15 * 120
1504	S27	-6975	124	15 * 120
1505	S26	-6990	269	15 * 120
1506	S25	-7005	124	15 * 120
1507	S24	-7020	269	15 * 120
1508	S23	-7035	124	15 * 120
1509	S22	-7050	269	15 * 120
1510	S21	-7065	124	15 * 120
1511	S20	-7080	269	15 * 120
1512	S19	-7095	124	15 * 120
1513	S18	-7110	269	15 * 120
1514	S17	-7125	124	15 * 120
1515	S16	-7140	269	15 * 120
1516	S15	-7155	124	15 * 120
1517	S14	-7170	269	15 * 120
1518	S13	-7185	124	15 * 120
1519	S12	-7200	269	15 * 120
1520	S11	-7215	124	15 * 120
1521	S10	-7230	269	15 * 120
1522	S9	-7245	124	15 * 120
1523	S8	-7260	269	15 * 120
1524	S7	-7275	124	15 * 120
1525	S6	-7290	269	15 * 120
1526	S5	-7305	124	15 * 120
1527	S4	-7320	269	15 * 120
1528	S3	-7335	124	15 * 120
1529	S2	-7350	269	15 * 120
1530	S1	-7365	124	15 * 120
1531	DUMMY25	-7380	269	15 * 120
1532	DUMMY26	-7395	124	15 * 120
1533	DUMMY27	-7560	269	15 * 120
1534	DUMMY28	-7575	124	15 * 120
1535	G480	-7590	269	15 * 120
1536	G478	-7605	124	15 * 120
1537	G476	-7620	269	15 * 120
1538	G474	-7635	124	15 * 120
1539	G472	-7650	269	15 * 120
1540	G470	-7665	124	15 * 120
1541	G468	-7680	269	15 * 120
1542	G466	-7695	124	15 * 120
1543	G464	-7710	269	15 * 120
1544	G462	-7725	124	15 * 120
1545	G460	-7740	269	15 * 120
1546	G458	-7755	124	15 * 120
1547	G456	-7770	269	15 * 120
1548	G454	-7785	124	15 * 120
1549	G452	-7800	269	15 * 120
1550	G450	-7815	124	15 * 120
1551	G448	-7830	269	15 * 120
1552	G446	-7845	124	15 * 120
1553	G444	-7860	269	15 * 120
1554	G442	-7875	124	15 * 120
1555	G440	-7890	269	15 * 120
1556	G438	-7905	124	15 * 120
1557	G436	-7920	269	15 * 120
1558	G434	-7935	124	15 * 120
1559	G432	-7950	269	15 * 120
1560	G430	-7965	124	15 * 120

No.	Name	X	Y	Bump size
1561	G428	-7980	269	15 * 120
1562	G426	-7995	124	15 * 120
1563	G424	-8010	269	15 * 120
1564	G422	-8025	124	15 * 120
1565	G420	-8040	269	15 * 120
1566	G418	-8055	124	15 * 120
1567	G416	-8070	269	15 * 120
1568	G414	-8085	124	15 * 120
1569	G412	-8100	269	15 * 120
1570	G410	-8115	124	15 * 120
1571	G408	-8130	269	15 * 120
1572	G406	-8145	124	15 * 120
1573	G404	-8160	269	15 * 120
1574	G402	-8175	124	15 * 120
1575	G400	-8190	269	15 * 120
1576	G398	-8205	124	15 * 120
1577	G396	-8220	269	15 * 120
1578	G394	-8235	124	15 * 120
1579	G392	-8250	269	15 * 120
1580	G390	-8265	124	15 * 120
1581	G388	-8280	269	15 * 120
1582	G386	-8295	124	15 * 120
1583	G384	-8310	269	15 * 120
1584	G382	-8325	124	15 * 120
1585	G380	-8340	269	15 * 120
1586	G378	-8355	124	15 * 120
1587	G376	-8370	269	15 * 120
1588	G374	-8385	124	15 * 120
1589	G372	-8400	269	15 * 120
1590	G370	-8415	124	15 * 120
1591	G368	-8430	269	15 * 120
1592	G366	-8445	124	15 * 120
1593	G364	-8460	269	15 * 120
1594	G362	-8475	124	15 * 120
1595	G360	-8490	269	15 * 120
1596	G358	-8505	124	15 * 120
1597	G356	-8520	269	15 * 120
1598	G354	-8535	124	15 * 120
1599	G352	-8550	269	15 * 120
1600	G350	-8565	124	15 * 120
1601	G348	-8580	269	15 * 120
1602	G346	-8595	124	15 * 120
1603	G344	-8610	269	15 * 120
1604	G342	-8625	124	15 * 120
1605	G340	-8640	269	15 * 120
1606	G338	-8655	124	15 * 120
1607	G336	-8670	269	15 * 120
1608	G334	-8685	124	15 * 120
1609	G332	-8700	269	15 * 120
1610	G330	-8715	124	15 * 120
1611	G328	-8730	269	15 * 120
1612	G326	-8745	124	15 * 120
1613	G324	-8760	269	15 * 120
1614	G322	-8775	124	15 * 120
1615	G320	-8790	269	15 * 120
1616	G318	-8805	124	15 * 120
1617	G316	-8820	269	15 * 120
1618	G314	-8835	124	15 * 120
1619	G312	-8850	269	15 * 120
1620	G310	-8865	124	15 * 120

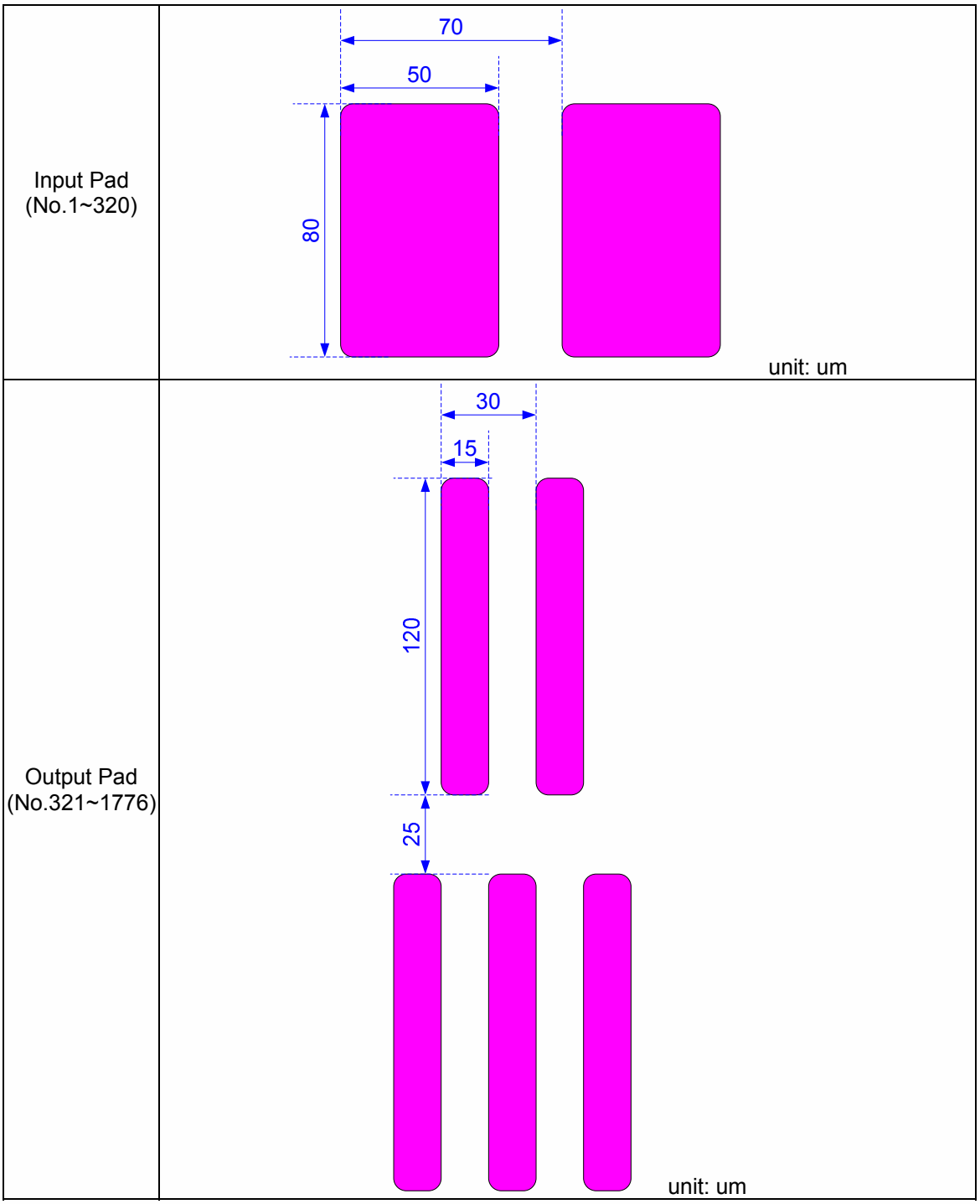
No.	Name	X	Y	Bump size
1621	G308	-8880	269	15 * 120
1622	G306	-8895	124	15 * 120
1623	G304	-8910	269	15 * 120
1624	G302	-8925	124	15 * 120
1625	G300	-8940	269	15 * 120
1626	G298	-8955	124	15 * 120
1627	G296	-8970	269	15 * 120
1628	G294	-8985	124	15 * 120
1629	G292	-9000	269	15 * 120
1630	G290	-9015	124	15 * 120
1631	G288	-9030	269	15 * 120
1632	G286	-9045	124	15 * 120
1633	G284	-9060	269	15 * 120
1634	G282	-9075	124	15 * 120
1635	G280	-9090	269	15 * 120
1636	G278	-9105	124	15 * 120
1637	G276	-9120	269	15 * 120
1638	G274	-9135	124	15 * 120
1639	G272	-9150	269	15 * 120
1640	G270	-9165	124	15 * 120
1641	G268	-9180	269	15 * 120
1642	G266	-9195	124	15 * 120
1643	G264	-9210	269	15 * 120
1644	G262	-9225	124	15 * 120
1645	G260	-9240	269	15 * 120
1646	G258	-9255	124	15 * 120
1647	G256	-9270	269	15 * 120
1648	G254	-9285	124	15 * 120
1649	G252	-9300	269	15 * 120
1650	G250	-9315	124	15 * 120
1651	G248	-9330	269	15 * 120
1652	G246	-9345	124	15 * 120
1653	G244	-9360	269	15 * 120
1654	G242	-9375	124	15 * 120
1655	G240	-9390	269	15 * 120
1656	G238	-9405	124	15 * 120
1657	G236	-9420	269	15 * 120
1658	G234	-9435	124	15 * 120
1659	G232	-9450	269	15 * 120
1660	G230	-9465	124	15 * 120
1661	G228	-9480	269	15 * 120
1662	G226	-9495	124	15 * 120
1663	G224	-9510	269	15 * 120
1664	G222	-9525	124	15 * 120
1665	G220	-9540	269	15 * 120
1666	G218	-9555	124	15 * 120
1667	G216	-9570	269	15 * 120
1668	G214	-9585	124	15 * 120
1669	G212	-9600	269	15 * 120
1670	G210	-9615	124	15 * 120
1671	G208	-9630	269	15 * 120
1672	G206	-9645	124	15 * 120
1673	G204	-9660	269	15 * 120
1674	G202	-9675	124	15 * 120
1675	G200	-9690	269	15 * 120
1676	G198	-9705	124	15 * 120
1677	G196	-9720	269	15 * 120
1678	G194	-9735	124	15 * 120
1679	G192	-9750	269	15 * 120
1680	G190	-9765	124	15 * 120

No.	Name	X	Y	Bump size
1681	G188	-9780	269	15 * 120
1682	G186	-9795	124	15 * 120
1683	G184	-9810	269	15 * 120
1684	G182	-9825	124	15 * 120
1685	G180	-9840	269	15 * 120
1686	G178	-9855	124	15 * 120
1687	G176	-9870	269	15 * 120
1688	G174	-9885	124	15 * 120
1689	G172	-9900	269	15 * 120
1690	G170	-9915	124	15 * 120
1691	G168	-9930	269	15 * 120
1692	G166	-9945	124	15 * 120
1693	G164	-9960	269	15 * 120
1694	G162	-9975	124	15 * 120
1695	G160	-9990	269	15 * 120
1696	G158	-10005	124	15 * 120
1697	G156	-10020	269	15 * 120
1698	G154	-10035	124	15 * 120
1699	G152	-10050	269	15 * 120
1700	G150	-10065	124	15 * 120
1701	G148	-10080	269	15 * 120
1702	G146	-10095	124	15 * 120
1703	G144	-10110	269	15 * 120
1704	G142	-10125	124	15 * 120
1705	G140	-10140	269	15 * 120
1706	G138	-10155	124	15 * 120
1707	G136	-10170	269	15 * 120
1708	G134	-10185	124	15 * 120
1709	G132	-10200	269	15 * 120
1710	G130	-10215	124	15 * 120
1711	G128	-10230	269	15 * 120
1712	G126	-10245	124	15 * 120
1713	G124	-10260	269	15 * 120
1714	G122	-10275	124	15 * 120
1715	G120	-10290	269	15 * 120
1716	G118	-10305	124	15 * 120
1717	G116	-10320	269	15 * 120
1718	G114	-10335	124	15 * 120
1719	G112	-10350	269	15 * 120
1720	G110	-10365	124	15 * 120
1721	G108	-10380	269	15 * 120
1722	G106	-10395	124	15 * 120
1723	G104	-10410	269	15 * 120
1724	G102	-10425	124	15 * 120
1725	G100	-10440	269	15 * 120
1726	G98	-10455	124	15 * 120
1727	G96	-10470	269	15 * 120
1728	G94	-10485	124	15 * 120
1729	G92	-10500	269	15 * 120
1730	G90	-10515	124	15 * 120
1731	G88	-10530	269	15 * 120
1732	G86	-10545	124	15 * 120
1733	G84	-10560	269	15 * 120
1734	G82	-10575	124	15 * 120
1735	G80	-10590	269	15 * 120
1736	G78	-10605	124	15 * 120
1737	G76	-10620	269	15 * 120
1738	G74	-10635	124	15 * 120
1739	G72	-10650	269	15 * 120
1740	G70	-10665	124	15 * 120

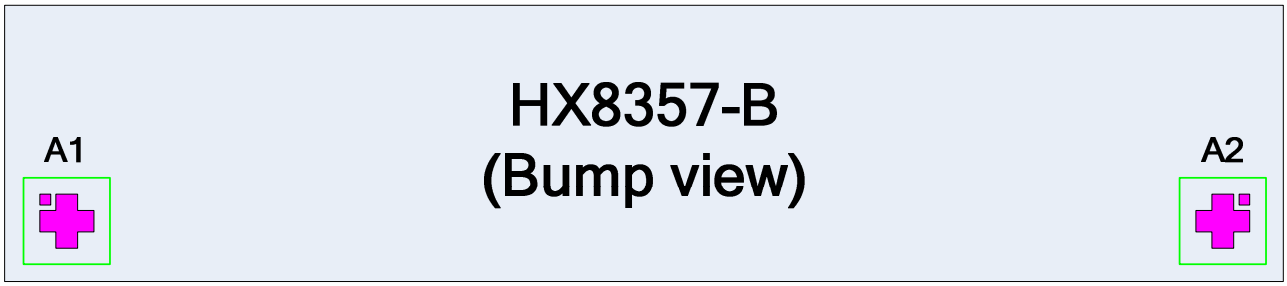
No.	Name	X	Y	Bump size
1741	G68	-10680	269	15 * 120
1742	G66	-10695	124	15 * 120
1743	G64	-10710	269	15 * 120
1744	G62	-10725	124	15 * 120
1745	G60	-10740	269	15 * 120
1746	G58	-10755	124	15 * 120
1747	G56	-10770	269	15 * 120
1748	G54	-10785	124	15 * 120
1749	G52	-10800	269	15 * 120
1750	G50	-10815	124	15 * 120
1751	G48	-10830	269	15 * 120
1752	G46	-10845	124	15 * 120
1753	G44	-10860	269	15 * 120
1754	G42	-10875	124	15 * 120
1755	G40	-10890	269	15 * 120
1756	G38	-10905	124	15 * 120
1757	G36	-10920	269	15 * 120
1758	G34	-10935	124	15 * 120
1759	G32	-10950	269	15 * 120
1760	G30	-10965	124	15 * 120
1761	G28	-10980	269	15 * 120
1762	G26	-10995	124	15 * 120
1763	G24	-11010	269	15 * 120
1764	G22	-11025	124	15 * 120
1765	G20	-11040	269	15 * 120
1766	G18	-11055	124	15 * 120
1767	G16	-11070	269	15 * 120
1768	G14	-11085	124	15 * 120
1769	G12	-11100	269	15 * 120
1770	G10	-11115	124	15 * 120
1771	G8	-11130	269	15 * 120
1772	G6	-11145	124	15 * 120
1773	G4	-11160	269	15 * 120
1774	G2	-11175	124	15 * 120
1775	DUMMY29	-11190	269	15 * 120
1776	DUMMY30	-11205	124	15 * 120

No.	Name	X	Y
A1	Alignment	-11300	-300
A2	Alignment	11300	-300

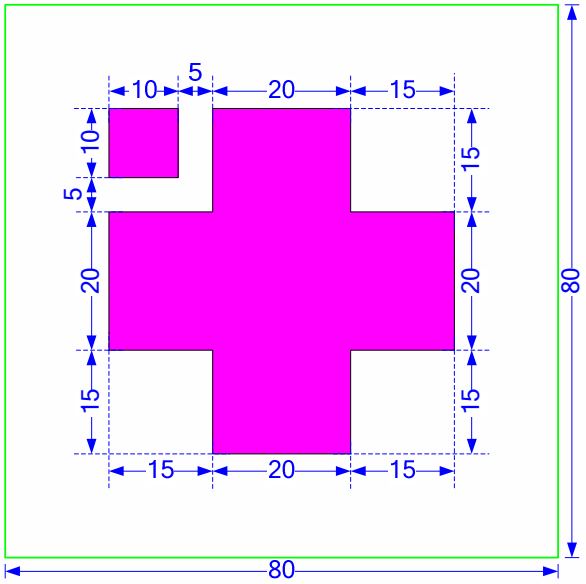
3.5 Bump Arrangement



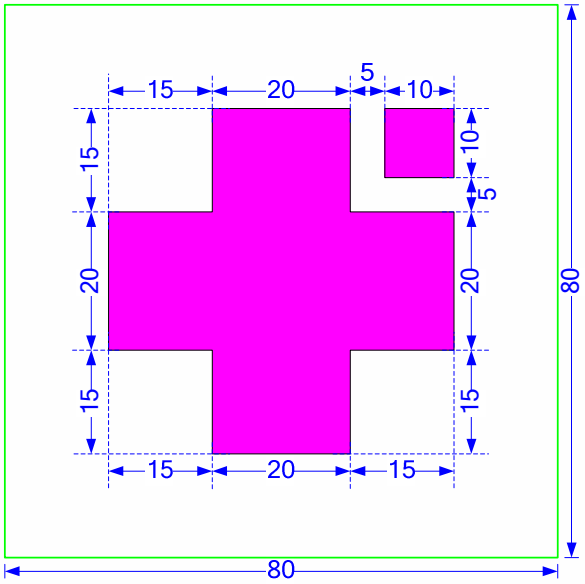
3.6 Alignment Mark



A1 (-11300, -300)



A2 (11300, -300)



unit: um

4. Interface Description

The HX8357-B supports MIPI interfaces: DBI (Display Bus Interface), DPI(Display Pixel Interface). Where DBI supports (18-/16-/9-/8-bit interface) Parallel Interface (Type-B) and Serial interface (Type-C). The interface mode can be selected by IM2-0 pins setting as show in table4.1.

IM2	IM1	IM0	Interface	Color mode
0	0	0	DBI Type-B 18-bit	262K
0	0	1	DBI Type-B 9-bit	262K
0	1	0	DBI Type-B 16-bit	65K / 262K
0	1	1	DBI Type-B 8-bit	65K / 262K
1	0	0	Inhibited	-
1	0	1	DBI Type-C Option 1(9 bits)	8 / 262K
1	1	0	Inhibited	-
1	1	1	DBI Type-C Option 3 (8 bits)	8 / 262K

Table 4.1: Interface Selection

The HX8357-B includes an index register (IR), which is stored the index data of internal control register and GRAM. When DCX =”L”, the command via DBI interface write into register. when DCX =”H”, GRAM data via R2Ch register can be written through data bus. There are two 16-bit bus control registers, which are used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM.

When data is read from the GRAM to the MPU, it is first read from GRAM to the read-data latch and then data is read to MPU through the read-data latch in next read operation. Therefore, the read data in data bus in first read operation is invalid, and the read data in data bus in second and the following read operation is valid.

Interface	RDX	WRX_SCL	DCX	DB17 –DB0 or other input pin
DBI Type-C Option 1	Unused	SCL	Unused	DB17 – DB0: 18 bit data bus DIN_SDA
DBI Type-C Option 3	Unused	SCL	DCX	DB17 – DB0: 18 bit data bus DIN_SDA
DBI Type-B 8-bit parallel	RDX	WRX	DCX	DB17 – DB8: Unused, DB7 – DB0 : 8 bit data bus
DBI Type-B 9-bit parallel	RDX	WRX	DCX	DB17 – DB9: Unused, DB8 – DB0: 9 bit data bus
DBI Type-B 16-bit parallel	RDX	WRX	DCX	DB17 – DB16: Unused, DB15 – DB0: 16 bit data bus
DBI Type-B 18-bit parallel	RDX	WRX	DCX	DB17 – DB0: 18 bit data bus

Table 4.2: Pin connection according of different interface

4.1 MIPI DBI-B Interface

The selection of DBI Type-B interface is by IM2 pin .When this pin is Low state (VSSD), the interface is use DBI system. And use IM1~IM0 pin to select DBI-B interface mode. The parallel interface timing diagram is described in Figure 4.1 and 4.2.

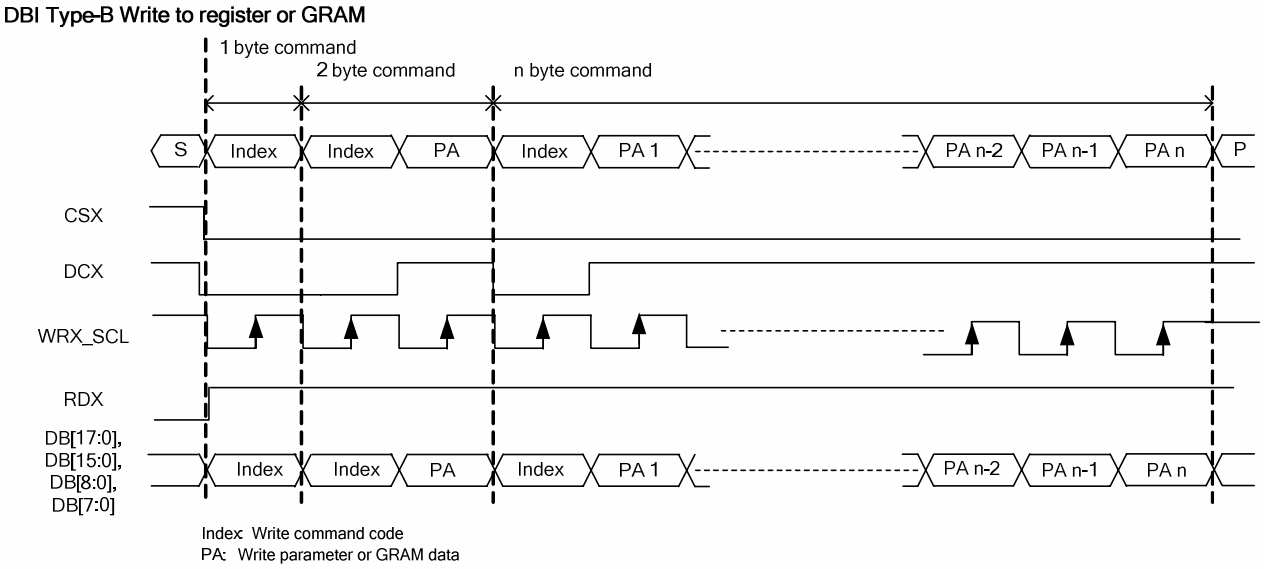


Figure 4.1: DBI-B System interface protocol, write to register or GRAM

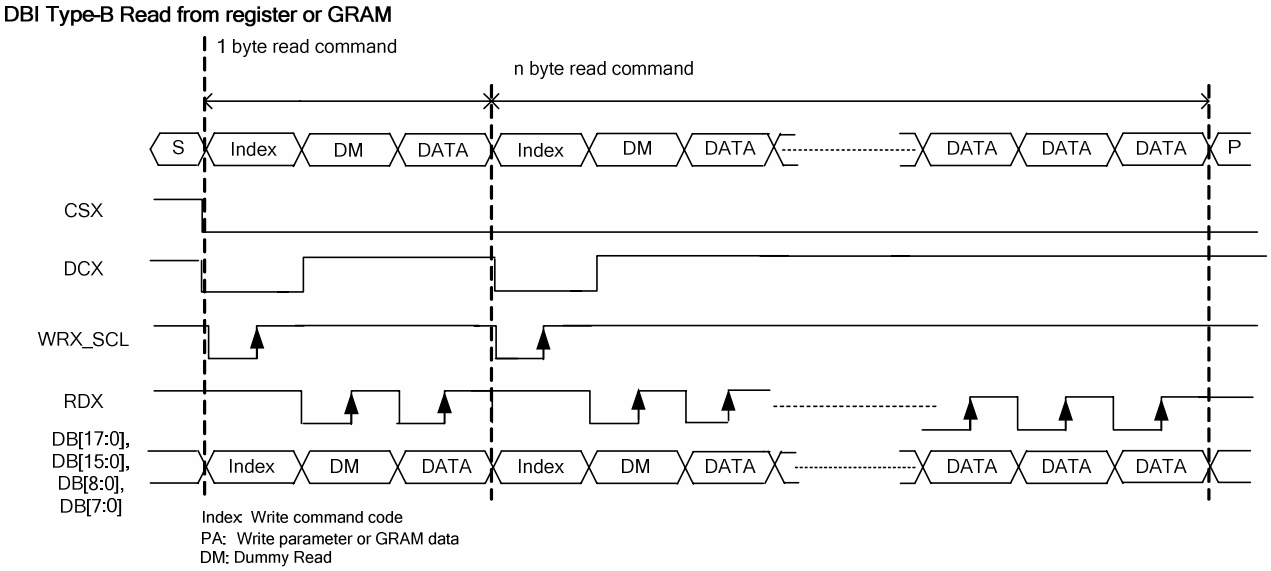


Figure 4.2: DBI-B System interface protocol, read from register or GRAM

4.1.1 DBI Type-B 18-bit Parallel Bus System Interface

The DBI-B system 18-bit bus parallel data transfer can be used by setting “IM2-0” pins to “000”. The Figure 4.3 is the example of interface with 18-bit DBI Type-B microcomputer system interface.

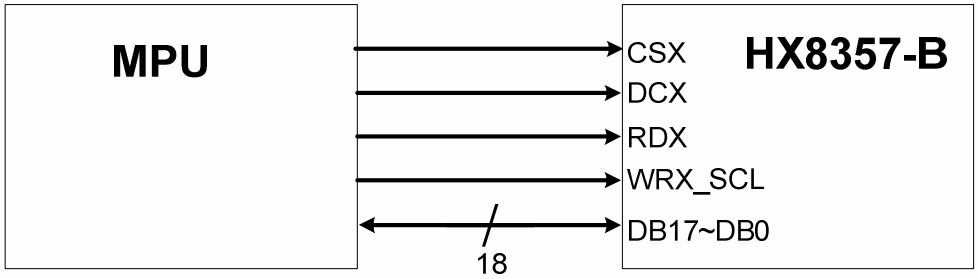


Figure 4.3: Example of DBI Type-B System 18-Bit Parallel Bus Interface

4.1.2 16-bit Parallel Bus System Interface

The DBI-B system 16-bit bus parallel data transfer can be used by setting “IM2-0”pins to “010”. The Figure 4.4 is the example of interface with 16-bit DBI Type-B microcomputer system interface.

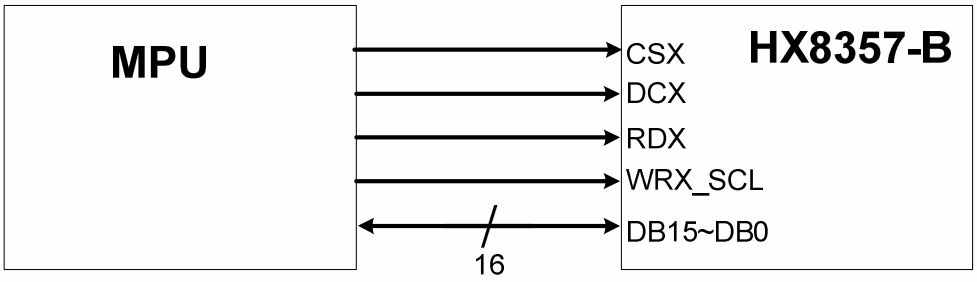


Figure 4.4: Example of DBI-B- System 16-bit bus Interface

4.1.3 9-bit Parallel Bus System Interface

The DBI Type-B system 9-bit bus parallel data transfer can be used by setting “IM2-0” pins to “001”. The Figure 4.5 is the example of interface with 9-bit DBI Type-B microcomputer system interface.

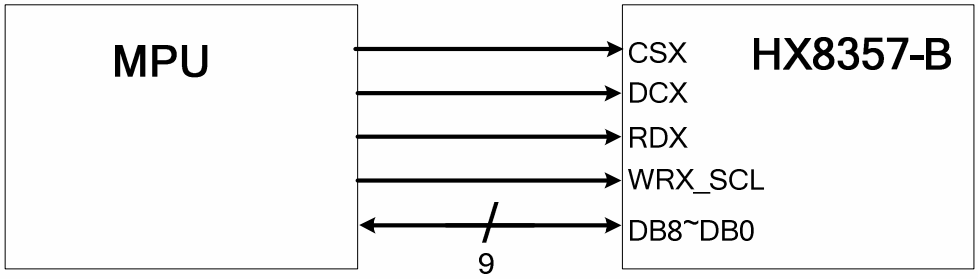


Figure 4.5: Example of DBI Type-B System 9-bit bus Interface

4.1.4 8-bit Parallel Bus System Interface

The DBI Type-B system 8-bit bus parallel data transfer can be used by setting “IM2-0” pins to “011”. The Figure 4.6 is the example of interface with 8-bit DBI Type-B microcomputer system interface.

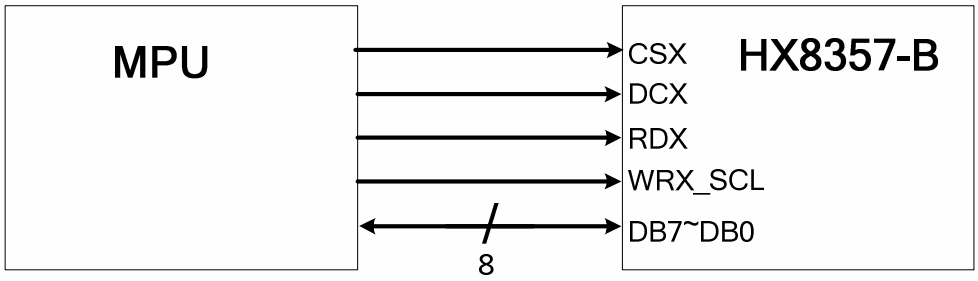


Figure 4.6: Example of DBI Type-B System 8-bit bus Interface

4.1.5 DBI Type-B Interface Data Color Coding

DBI Type-B Interface Data Color Coding for GRAM data ***Write***

- DBI Type-B 8-Bits Bus Interface (IM2, IM1, IM0="011")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3'h5	X	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixels/ 2-transfer)
		x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
3'h6	X	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixels/ 3-transfer)
		x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
		x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 4.3: DBI Type-B 8-Bits Interface GRAM Write Table

- DBI Type-B 9-Bits Bus Interface (IM2,IM1,IM0="001")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3'h6	X	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixels/ 2-transfer)
		x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 4.4: DBI Type-B 9-Bits Interface GRAM Write Set Table

- DBI Type-B 16-Bits Bus Interface (IM2,IM1,IM0="010")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3'h5	X	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color (1-pixels/ 1-transfer)
		x	x																	
3'h6	0	x	x	R05	R04	R03	R02	R01	R00	x	x	G05	G04	G03	G02	G01	G00	x	x	262K-Color (2-pixels/ 3-transfer)
		x	x	B05	B04	B03	B02	B01	B00	x	x	R15	R14	R13	R12	R11	R10	x	x	
		x	x	G15	G14	G13	G12	G11	G10	x	x	B15	B14	B13	B12	B11	B10	x	x	
	1	x	x	x	x	x	x	x	x	x	x	R05	R04	R03	R02	R01	R00	x	x	262K-Color (1-pixels/ 2-transfer)
		x	x	G05	G04	G03	G02	G01	G00	x	x	B05	B04	B03	B02	B01	B00	x	x	
		x	x	x	x	x	x	x	x	x	x	R15	R14	R13	R12	R11	R10	x	x	
				G15	G14	G13	G12	G11	G10	x	x	B15	B14	B13	B12	B11	B10	x	x	

Table 4.5: DBI Type-B 16-Bits Interface GRAM Write Table

- DBI Type-B 18-Bits Bus Interface (IM2,IM1,IM0="000")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3'h6	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color (1-pixels/ 1-transfer)

Table 4.6: DBI Type-B 18-Bits Interface GRAM Write Set Table

- DBI Type-B 16-Bits Data extend to 18-Bit

Register		GRAM Data																	
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3'h5	2'h0	R4	R3	R2	R1	R0	0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0
	2'h1	R4	R3	R2	R1	R0	1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1
	2'h2	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4

Table 4.7: DBI Type-B 16-Bits Data extend to 18-Bit

DBI Type-B Interface Data Color Coding for RAM data ***Read***

- DBI Type-B I 8-Bits Bus Interface (IM2, IM1, IM0="011")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
3'h5	X	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixels/ 2-transfer)
		x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
3'h6	X	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixels/ 3-transfer)
		x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
		x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 4.8: DBI Type-B 8-Bits Interface GRAM Read Table

- DBI Type-B 9-Bits Bus Interface (IM2, IM1, IM0="001")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
3'h6	X	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixels/ 2-transfer)
		x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 4.9: DBI Type-B 9-Bits Interface GRAM Read Set Table

- DBI Type-B 16-Bits Bus Interface (IM2, IM1, IM0="010")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
3'h5	X	x x	x x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color (1-pixels/ 1-transfer)
3'h6	0	x	x	R05	R04	R03	R02	R01	R00	x	x	G05	G04	G03	G02	G01	G00	x	x	262K-Color (2-pixels/ 3-transfer)
		x	x	B05	B04	B03	B02	B01	B00	x	x	R15	R14	R13	R12	R11	R10	x	x	
		x	x	G15	G14	G13	G12	G11	G10	x	x	B15	B14	B13	B12	B11	B10	x	x	
	1	x	x	x	x	x	x	x	x	x	x	R05	R04	R03	R02	R01	R00	x	x	262K-Color (1-pixels/ 2-transfer)
		x	x	G05	G04	G03	G02	G01	G00	x	x	B05	B04	B03	B02	B01	B00	x	x	
		x	x	x	x	x	x	x	x	x	x	R15	R14	R13	R12	R11	R10	x	x	
				G15	G14	G13	G12	G11	G10	x	x	B15	B14	B13	B12	B11	B10	x	x	

Table 4.10: DBI Type-B 16-Bits Interface GRAM Read Table

- DBI Type-B 18-Bits Bus Interface (IM2, IM1, IM0="000")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
3'h6	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color (1-pixels/ 1-transfer)

Table 4.11: DBI Type-B 18-Bits Interface GRAM Read Set Table

4.2 Serial Data Transfer Interface (MIPI DBI Type-C)

The HX8357-B supports two type serial data transfer interface, the interface selection by setting IM2-0 pins, The IM2-0 set “101” is select 3 wire option1 serial bus. The IM2-0 is set “111” when select 4 wire option3 serial bus.

The 3 wire serial bus is use: chip select line (CSX), serial input/output data (SDA) and the serial transfer clock line (WRX_SCL).The 4 wire serial bus is use: chip select line (CSX), data/command select (DCX), serial input/output data (DIN_SDA, DOUT) and the serial transfer clock line (WRX_SCL).

4.2.1 Serial data write mode

The 3-Pin serial data packet contains a control bit DCX and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control signal DCX is transferred by DCX pin. If DCX is low, the transmission byte is command byte. If DCX is high, the transmission byte is stored in to command register or GRAM. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or serial input/output data (DIN_SDA) have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

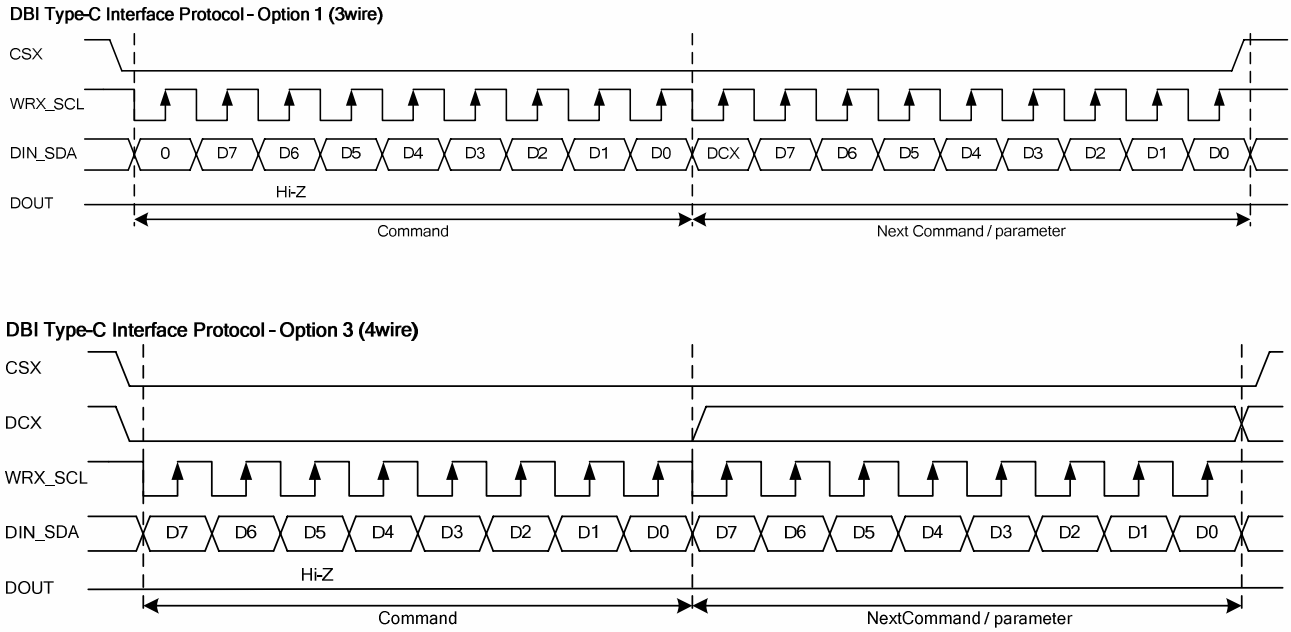


Figure 4.7: DBI Type-C -- Serial Interface protocol 3 wire/4 wire, write mode

4.2.2 Serial data read mode

The micro-controller first has to send a command and then the following byte is transmitted in the opposite direction. The 3-wire serial read data format which just needs 8-bit.

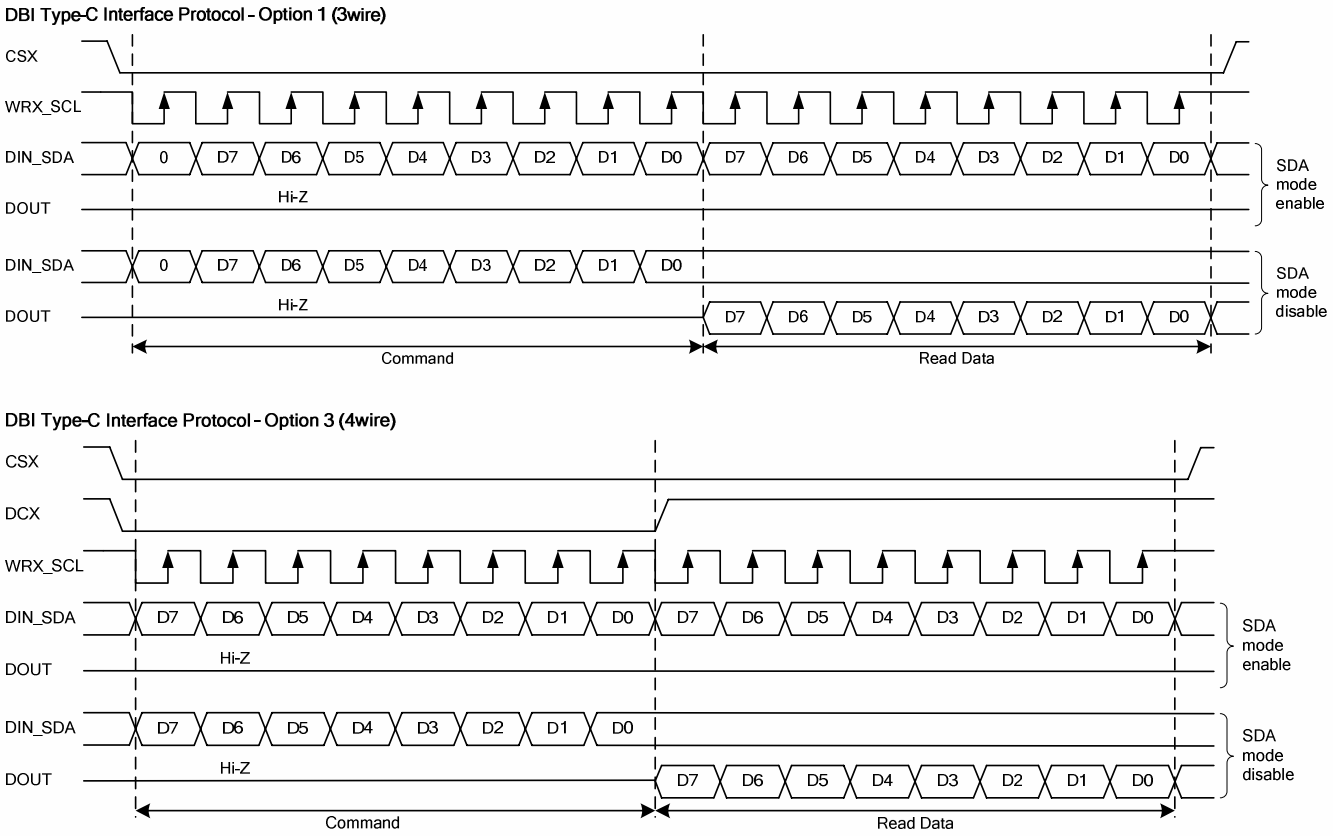


Figure 4.8: Type-C -- Serial Interface protocol 3 wire/4 wire read mode

4.2.3 DBI Type-C Interface Data Color Coding

- DBI Type-C 3/4-wire serial bus Interface (IM2, IM1, IM0="101" or "111")

Register		D7	D6	D5	D4	D3	D2	D1	D0	Command
Set_pixel_format	DFM	0	0	1	0	1	1	0	0	**2CH**
3'h1	0	X	X	R00	G00	B00	R10	G10	B10	8-Color (1-pixels/ 1-transfer)
	1	X	R00	G00	B00	X	R10	G10	B10	
3'h6	X	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixels/ 3-transfer)
		G5	G4	G3	G2	G1	G0	x	x	
		B5	B4	B3	B2	B1	B0	x	x	

Table 4.12: DBI Type-C Interface GRAM write Table

- DBI TYPE-C 3-Bits Data extend to 18-Bit

Register		GRAM Data																	
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3'h1	XX	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0

Table 4.13: DBI Type-C 3-Bits Data extend to 18-Bit

4.2.4 Break and Pause Sequences

If there is a break on data transmission when transmit a command before a whole byte has been completed, then the display module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following figure.

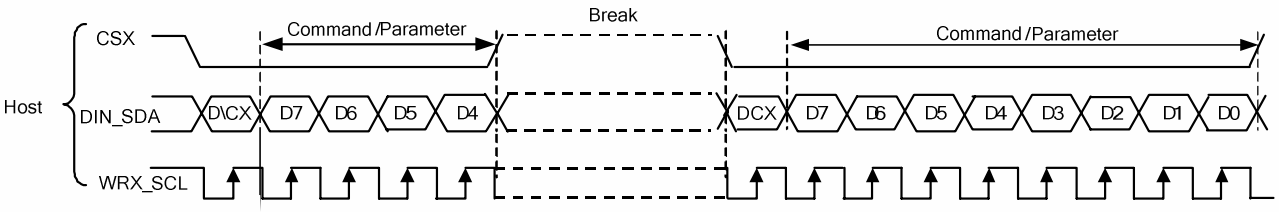


Figure 4.9: Display Module Data Transfer Recovery

If a one or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than retransmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

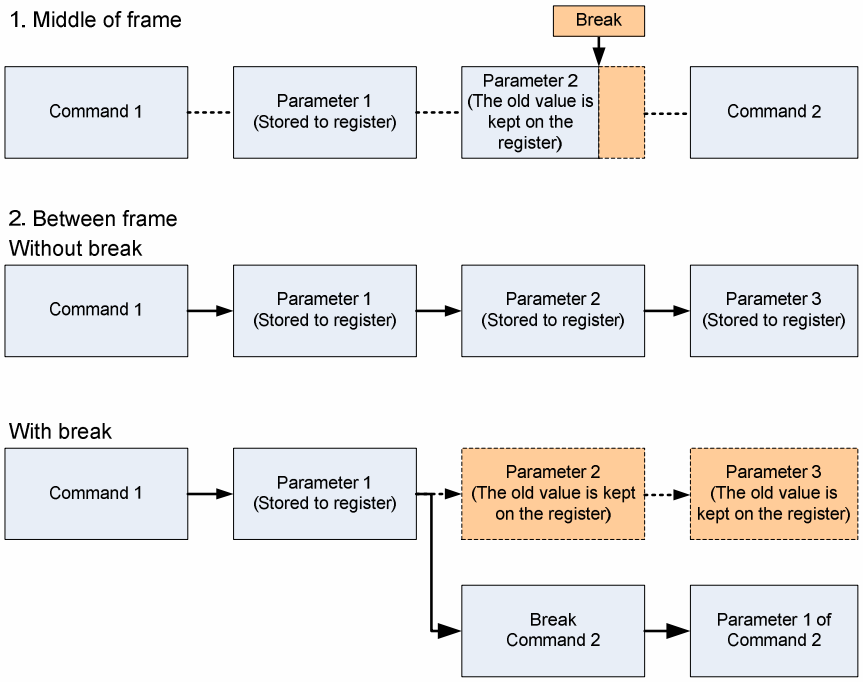


Figure 4.10: Break during parameter

The host processor can pause a write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

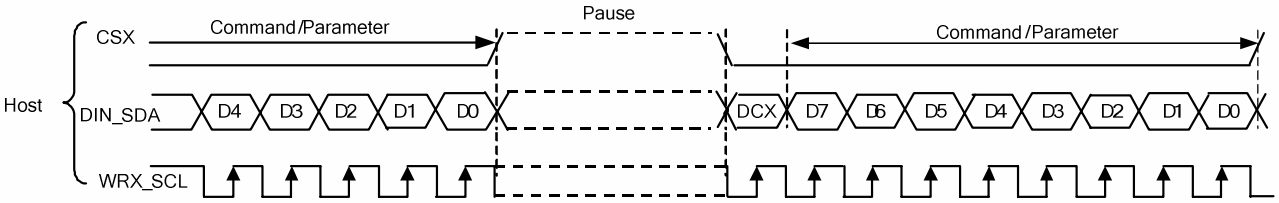


Figure 4.11: Display Module Data Transfer Pause

There are 4 cases where there is possible to see this kind of pause:

a. Command – Pause – Command
b. Command – Pause – Parameter
c. Parameter – Pause – Command
d. Parameter – Pause – Parameter

4.3 MIPI DPI interface (Display Pixel Interface)

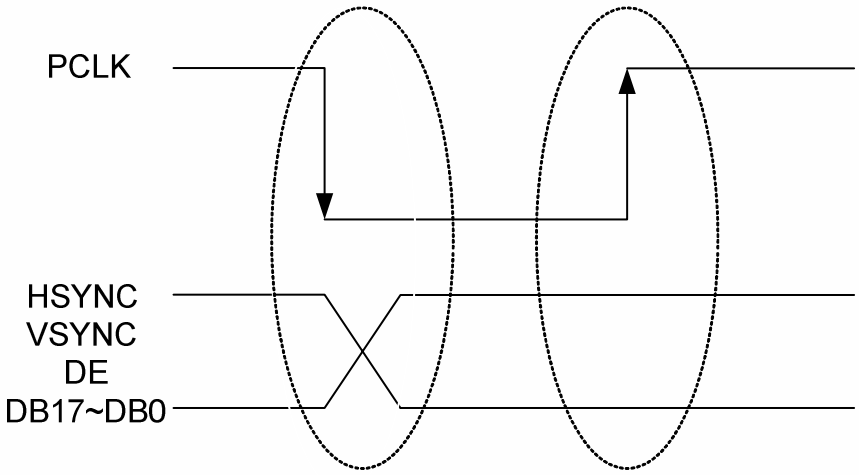
The HX8357-B uses 16 or 18-bit parallel RGB interface which includes: HSYNC, VSYNC, DE, PCLK, DB17~DB0. The interface is active after Power On sequence. Pixel clock (PCLK) is running all the time without stopping and it is used to entering HSYNC, VSYNC, DE and DB17~DB0 –lines states when there is a rising edge of the PCLK. The PCLK cannot be used as continue internal clock for other functions of the display module e.g. Sleep In –mode etc. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display.

This is negative ('-', '0', low) active and its state is read to the display module by a rising edge of the PCLK-line. Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame.

This is negative ('-', '0', low) active and its state is read to the display module by a rising edge of the PCLK-line. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display.

This is positive ('+', '1', high) active and its state is read to the display module by a rising edge of the PCLK-line. DB17~DB0 (18 bit: R5-R0, G5-G0 and B5-B0; 16 bit: R4- R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (when DE =1 and there is a rising edge of PCLK). DB17~DB0 – lines can be set to "0" (low) or "1" (high). These lines are read by a rising edge of the PCLK-line.

The pixel clock cycle is described in the following figure.



Note: PCLK is an unsynchronized signal (It can be stopped).

Figure 4.12: PCLK cycle

General Timing Diagram

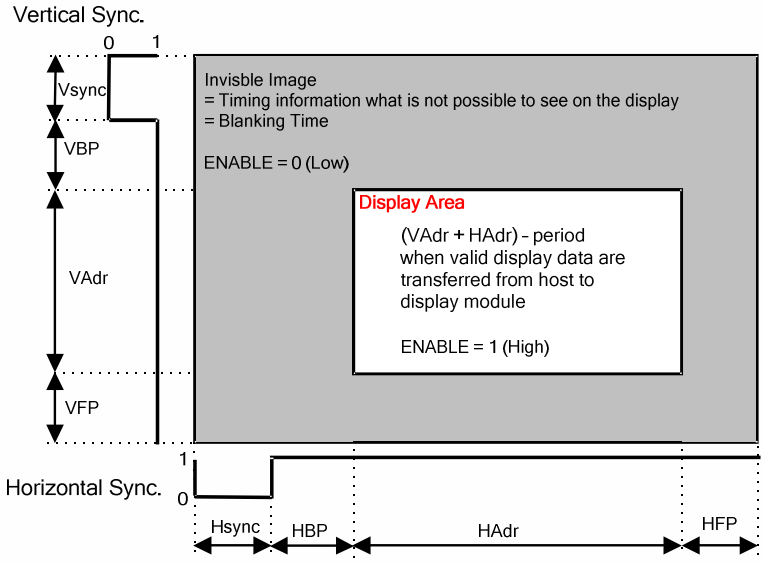


Figure 4.13: General Timing Diagram

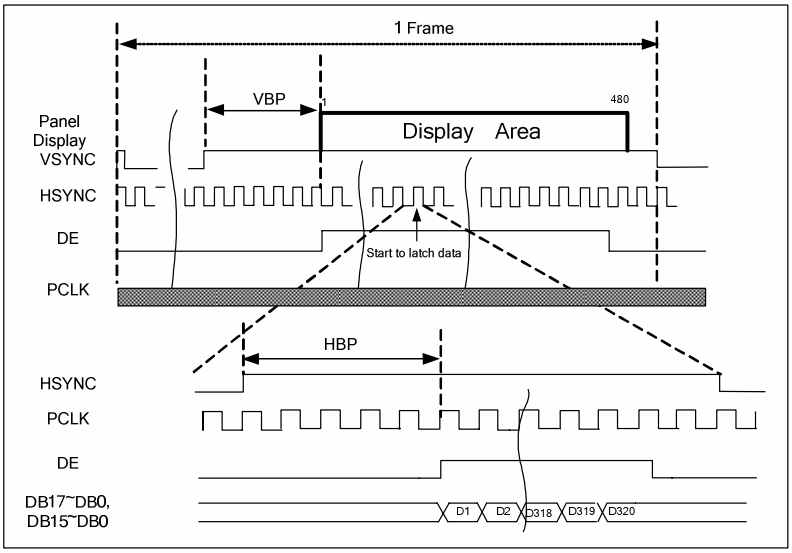


Figure 4.14: DPI (320RGBx480) timing diagram

The image information must be correct on the display, when the timings are in range on the interface. However, the image information can be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range interface timings.

The MIPI DPI interface includes two types which are 16-/18-bit data format by register 3Ah (set_pixel_format) to select.

4.3.1 16 bit/pixel Color Order on the DPI I/F

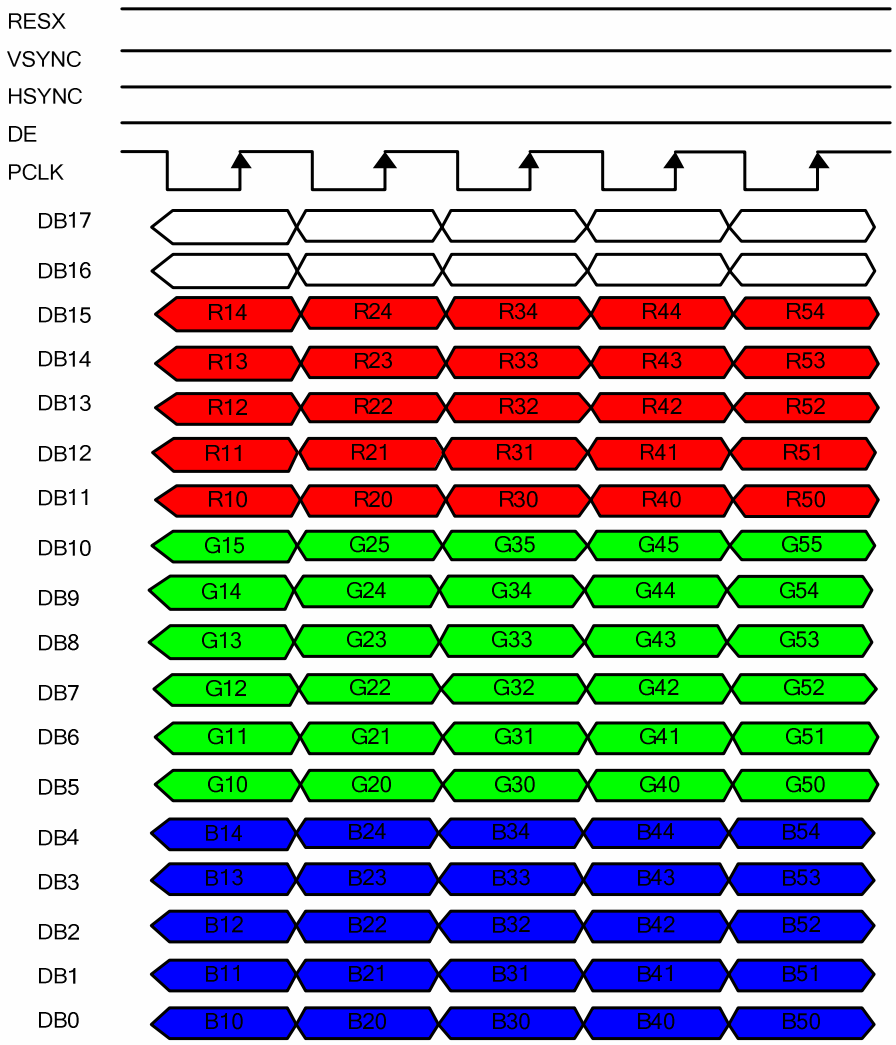


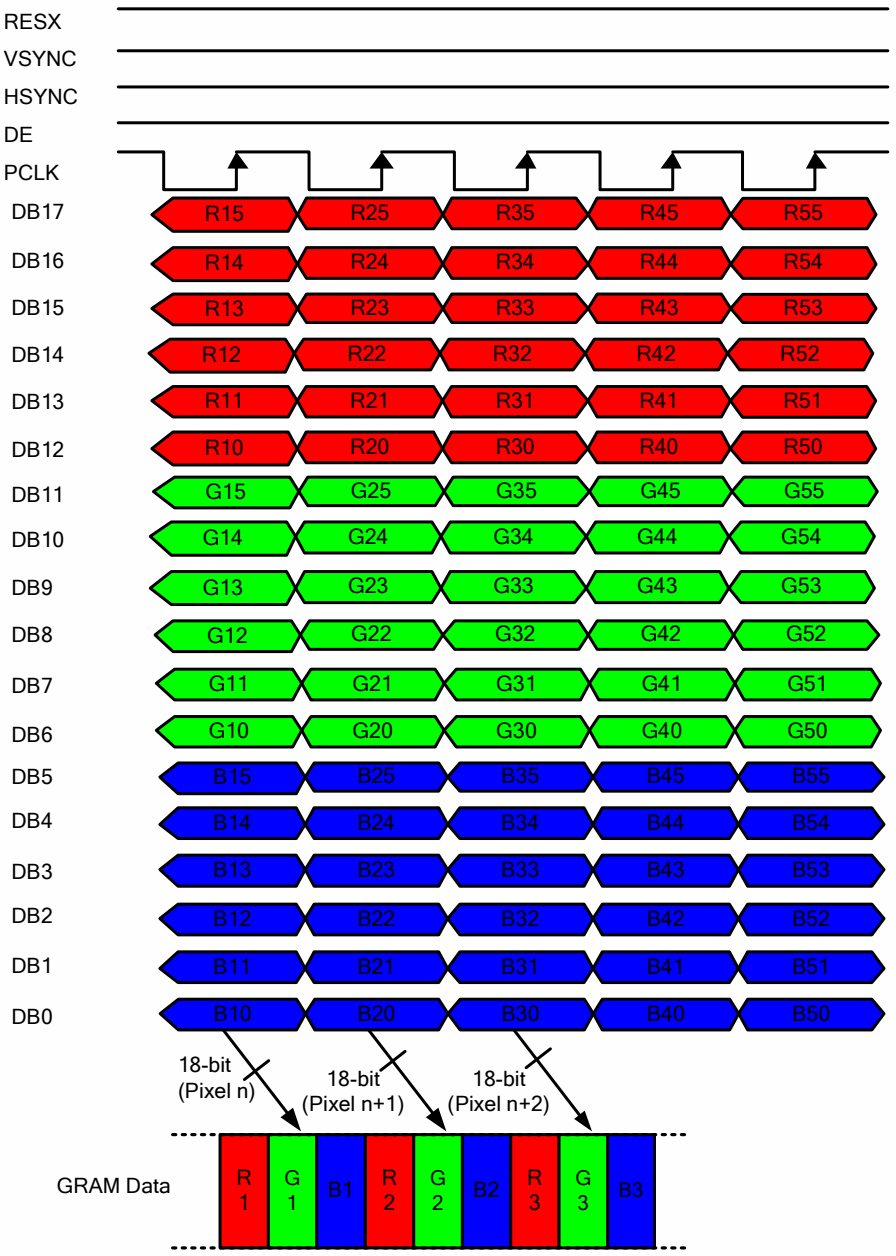
Figure 4.15: 16 bit/pixel 65k Color Order on the DPI I/F

- DPI 16-Bits Data extend to 18-Bit

Register		GRAM Data / Display data																	
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3'h5	2'h0	R4	R3	R2	R1	R0	0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0
	2'h1	R4	R3	R2	R1	R0	1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1
	2'h2	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4

Table 4.14: DPI 16-Bits Data extend to 18-Bit

4.3.2 18 bit/pixel Color Order on the DPI I/F



Note: The Data order is as follows, MSB = DB17, LSB = DB0 and Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data.

Figure 4.16: 18 bit/pixel -- 262k Color Order on the DPI I/F

4.3.3 Shutdown and Color Mode Signals

The HX8357-B is support hardware pin control function on DPI interface. If use this function, some OTP data need program for display quality, example Gamma setting, VCOM setting and Power voltage setting.

4.3.3.1 Shutdown for DPI interface hardware control

The Shutdown signal, SD, is used to turn on or turn off the display module. When SD is asserted high, the host processor should stop the video stream data to the display module to reduce interface signal power consumption.

PCLK may also be turned off to further reduce power consumption. The display module may reduce its power consumption by switching off its internal circuits. The control interface shall remain powered on.

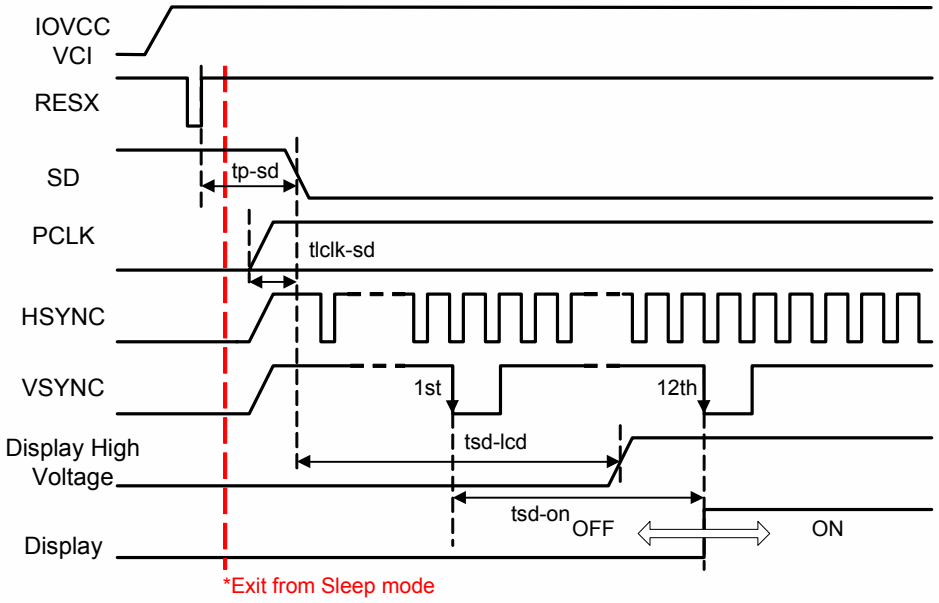


Figure 4.17: Power on and Shutdown Recovery Sequence

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RESX off to falling edge of SD	tp-sd	-	5	-	-	ms
PCLK input to the falling edge of SD	tclk-sd	-	1	-	-	PCLK
Falling edge of SD to display start	tsd-on	-	-	12	-	Vertical period

Table 4.15: AC timing for power-on sequence and recovery sequence from shutdown

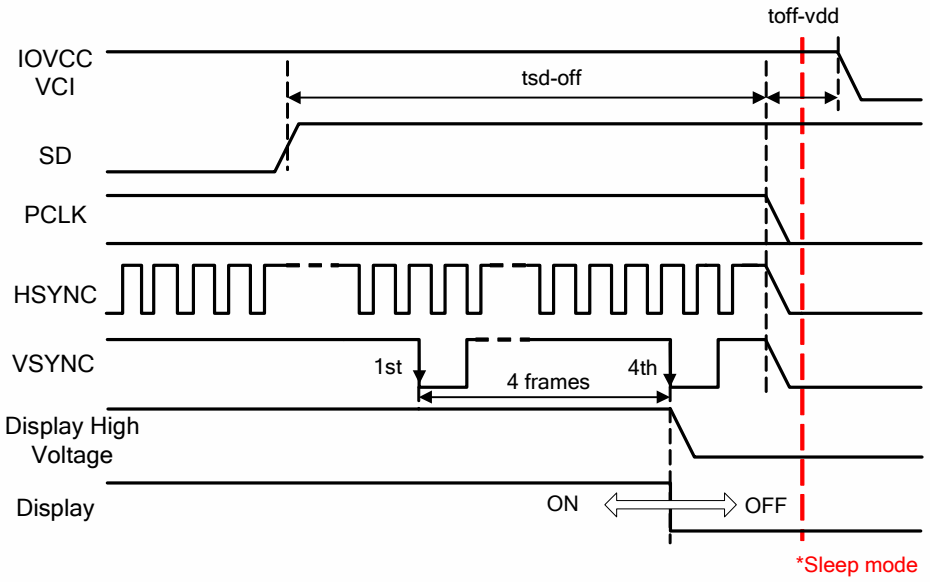


Figure 4.18: Power off and Shutdown Sequence

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Rising edge of SD to display off	tsd-off	-	4	-	-	Vertical period
Input-signal-off to IOVCC/VCI off	toff-vdd	-	0	-	-	s

Table 4.16: AC timing for power-off sequence and shutdown sequence

Color mode for DPI interface hardware control

The Color Mode signal, CM, is used to change the displayed number of colors. When CM is asserted high, the display module shall show the image data using eight colors, MSB for each R, G, and B color components. All unnecessary circuits on the display module may be stopped at the same time to reduce display module power consumption.

Transition from full-color mode to 8-color mode shall occur on the VSYNC following a low-to-high transition on CM.

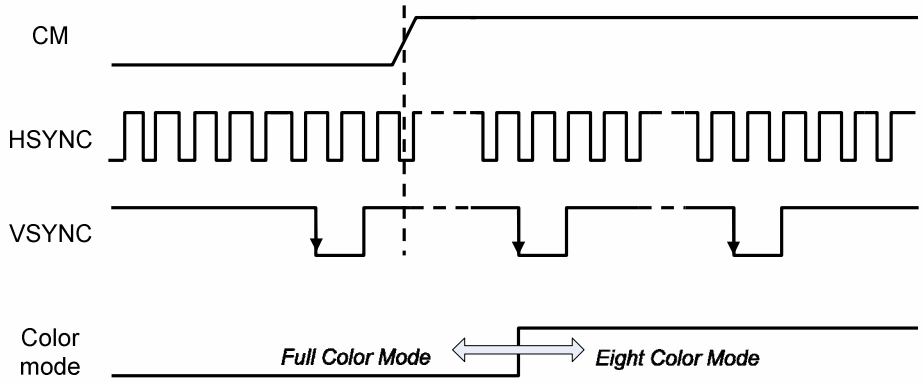


Figure 4.19: Full-color to 8-color Mode Transition Sequence

Transition from 8-color mode to full-color mode shall occur on the Vsync following a high-to-low transition on CM.

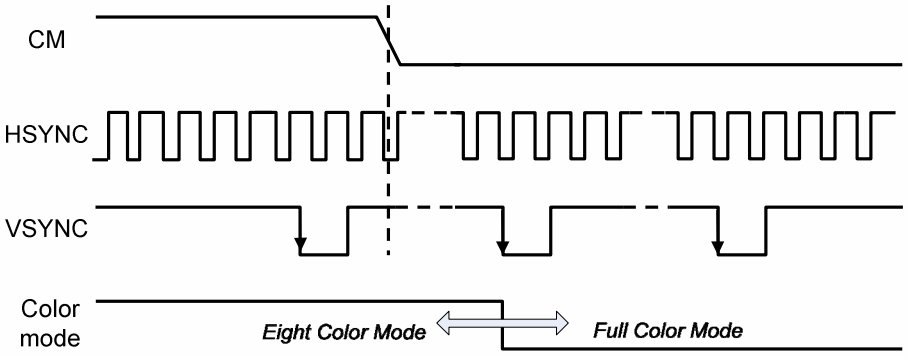


Figure 4.20: 8-color to Full-color Mode Transition Sequence

5. Function Description

5.1 Display Data GRAM

The display data RAM stores display dots and consists of 2,764,800 bits (320x18x480 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory

5.1.1 Address Counter (AC)

The HX8357-B contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range:

MX	MY	MV	X Range	Y Range	Panel Resolution
X	X	0	0~319d	0~479d	320RGB x480 dot
		1	0~479d	0~319d	

Table 5.1: Addresses Counter Range

Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data is written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the Column address register (start: SC, end: EC) or the Row address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

5.1.2 MCU to Memory Write/Read Direction

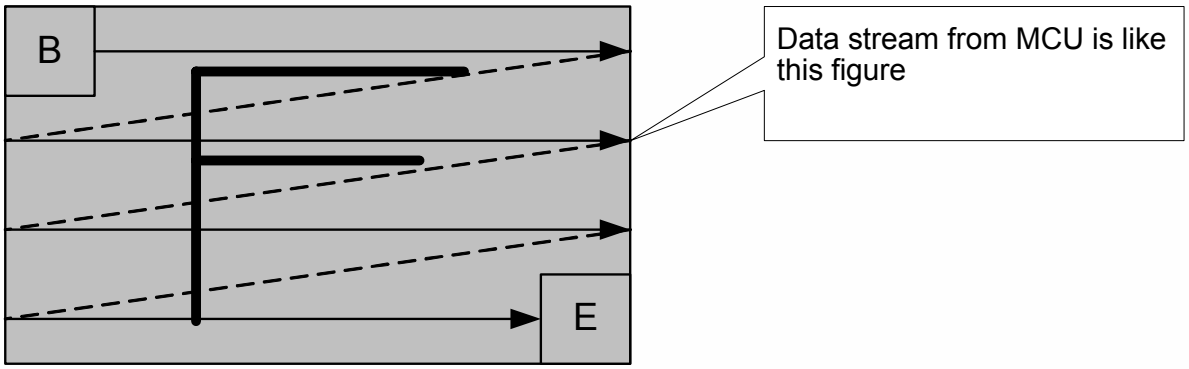


Figure 5.1: MCU to Memory Write/Read Direction

The data is written in the order as illustrated above. The counter that dictates which physical memory the data is to be written is controlled by “Memory Access Control” Command, Bits MY, MX, MV as described below.

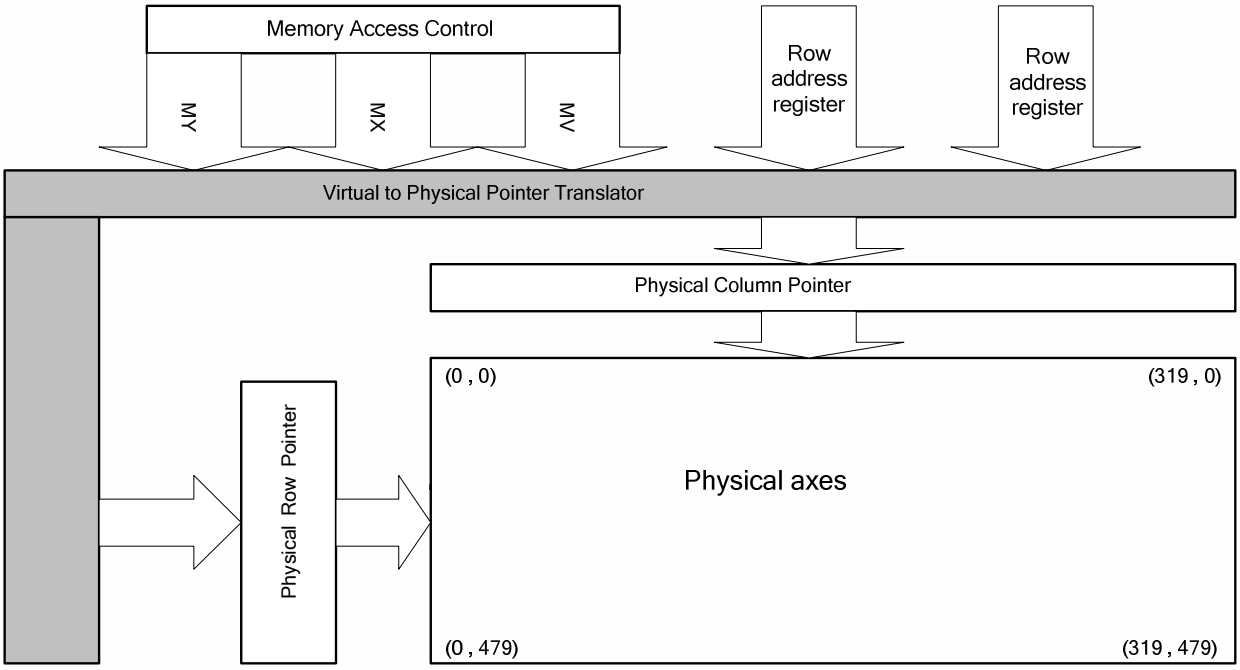


Figure 5.2: MY, MX, MV Setting of GRAM control

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (479-Physical Row Pointer) with SC
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (479-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (479-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (479-Physical Row Pointer)	Direct to (319-Physical Column Pointer)

Table 5.2: MY, MX, MV Setting of GRAM address mapping

The following figure depicts the update method set by MV, MX and MY bit.

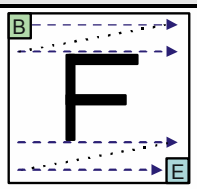
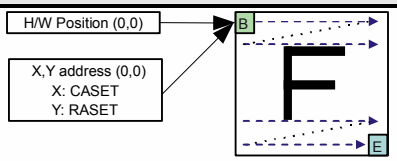
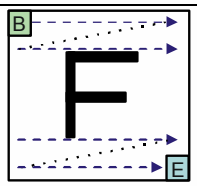
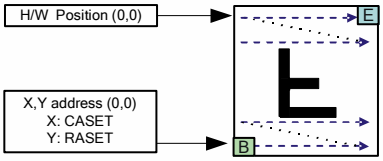
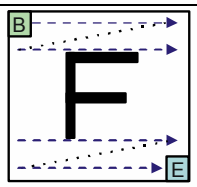
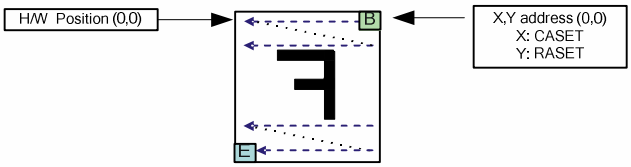
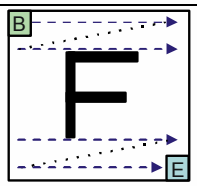
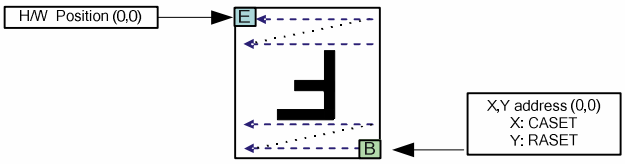
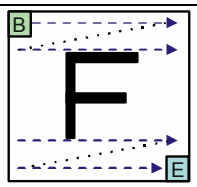
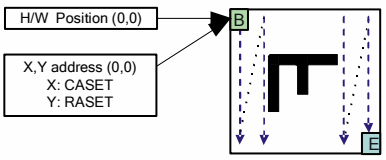
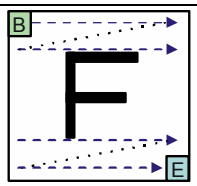
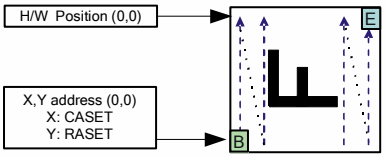
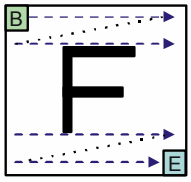
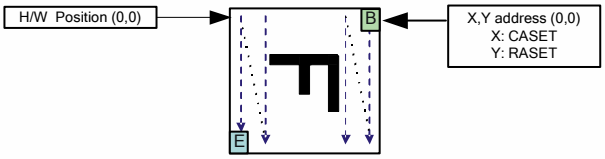
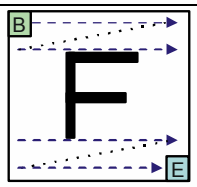
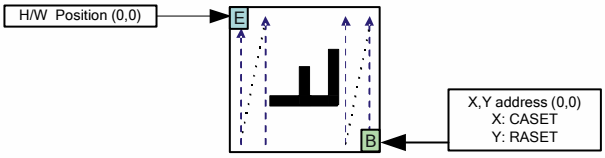
Display Data Direction	Memory Access Control			Image in the Host	Image in the Driver (GRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 5.3: Address Direction Settings

5.1.3 Source, Gate and Memory Map

Source Out		S1	S2	S3	S4	S5	S6	----------	S955	S956	S957	S958	S959	S960		
								RGB Order								
RA								—— :BGR=0							SA	
MY=0	MY=1							----- :BGR=1							ML=0	ML=1
0	479	R0 5-0	G0 5-0	B0 5-0	R1 5-0	G1 5-0	B1 5-0	–	R318 5-0	G318 5-0	B318 5-0	R319 5-0	G319 5-0	B319 5-0	0	479
1	478							–							1	478
2	477							–							2	477
3	476							–							3	476
4	475							–							4	475
5	474							–							5	474
6	473							–							6	473
7	472							–							7	472
8	471							–							8	471
9	470							–							9	470
10	469							–							10	469
11	468							–							11	468
:	:	:	:	:	:	:	:	--	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
472	7							–							472	7
473	6							–							473	6
474	5							–							474	5
475	4							–							475	4
476	3							–							476	3
477	2							–							477	2
478	1							–							478	1
479	0							–				RN 5-0	GN 5-0	BN 5-0	479	0
CA	MX=0	0			1				318			319				
	MX=1	319			318				1			0				

Note: **RA** = Row Address.
CA = Column Address.
SA = Scan Address.
MX = Mirror X-axis (Column address direction parameter), D6 parameter of Memory Access Control (R36h) command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of Memory Access Control (R36h) command
ML = Scan direction parameter, D4 parameter of Memory Access Control (R36h) command
BGR = Red, Green and Blue pixel position change, D3 parameter of Memory Access Control (R36h) command

Figure 5.4: Memory Map - 320RGBx480 dot

5.1.4 Fully Display, Partial Display, Vertical Scrolling Display

5.1.4.1 Fully Display

Example: (1) 320RGBx480 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x13Fh (R2Ah) and SP=0x000h, EP=0x1DFh (R2Bh), ML=0.

GRAM	00h DB---DB 17 --- 0	01h DB---DB 17 --- 0	---------	13Eh DB---DB 17 --- 0	13Fh DB---DB 17 --- 0
000h	000000H	000001H	---------	00013EH	00013FH
001h	001000H	001001H	---------	00113EH	00113FH
002h	002000H	002001H	---------	00213EH	00213FH
003h	003000H	003001H	---------	00313EH	00313FH
004h	004000H	004001H	---------	00413EH	00413FH
005h	005000H	005001H	---------	00513EH	00513FH
⋮	⋮	⋮	---------	⋮	⋮
1DAh	1DA000H	1DA001H	---------	1DA13EH	1DA13FH
1DBh	1DB000H	1DB001H	---------	1DB13EH	1DB13FH
1DCh	1DC000H	1DC001H	---------	1DC13EH	1DC13FH
1DDh	1DD000H	1DD001H	---------	1DD13EH	1DD13FH
1DEh	1DE000H	1DE001H	---------	1DE13EH	1DE13FH
1DFh	1DF000H	1DF001H	---------	1DF13EH	1DF13FH

Table 5.3: Memory map of full display

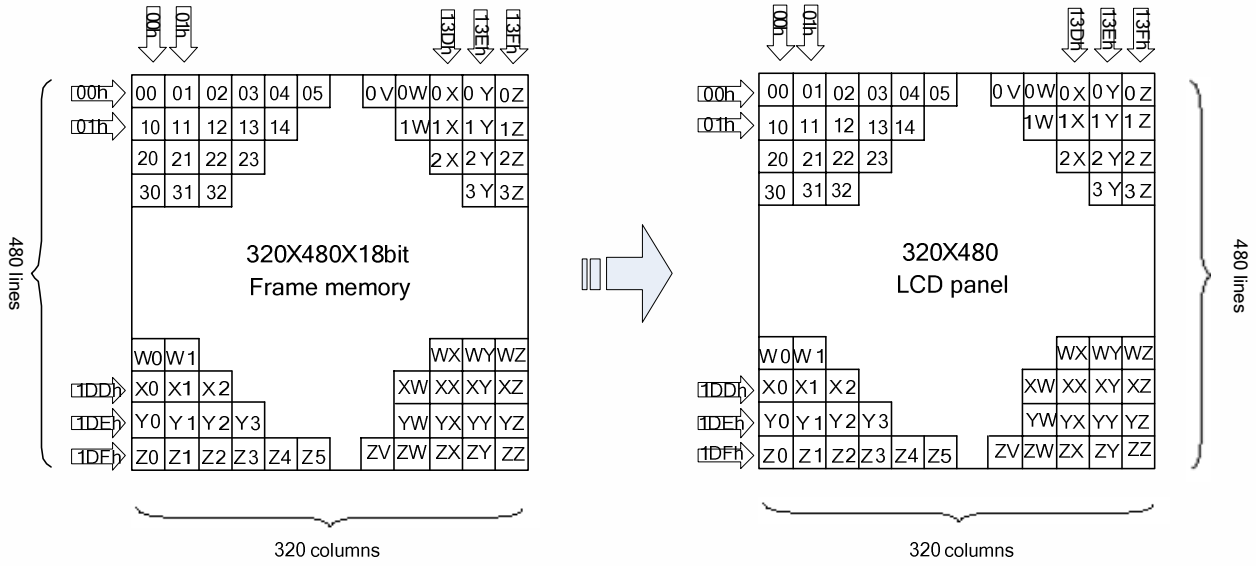


Figure 5.5: Memory map of full display

5.1.4.2 Partial Display

Example: (1) 320RGBx480 dot display mode.
(2) PLTON instruction (R12h).
(3) SR[15:0]=0002h, ER[15:0]=01DBh, ML=0.

GRAM	00h DB---DB 17 --- 0	01h DB---DB 17 --- 0	-------- ---------	13Eh DB---DB 17 --- 0	13Fh DB---DB 17 --- 0
000h	000000H	000001H	---------	00013EH	00013FH
001h	001000H	001001H	---------	00113EH	00113FH
002h	002000H	002001H	---------	00213EH	00213FH
003h	003000H	003001H	---------	00313EH	00313FH
004h	004000H	004001H	---------	00413EH	00413FH
005h	005000H	005001H	---------	00513EH	00513FH
⋮	⋮	⋮	---------	⋮	⋮
1DAh	1DA000H	1DA001H	---------	1DA13EH	1DA13FH
1DBh	1DB000H	1DB001H	---------	1DB13EH	1DB13FH
1DCh	1DC000H	1DC001H	---------	1DC13EH	1DC13FH
1DDh	1DD000H	1DD001H	---------	1DD13EH	1DD13FH
1DEh	1DE000H	1DE001H	---------	1DE13EH	1DE13FH
1DFh	1DF000H	1DF001H	---------	1DF13EH	1DF13FH

	LCD panel S/G pins	Pixel 1	Pixel 2	---------	Pixel319	Pixel320
Non-display area	**G1**	000000H	000001H	---------	00013EH	00013FH
	G2	001000H	001001H	---------	00113EH	00113FH
Display area -> 234 lines	**G3**	002000H	002001H	---------	00213EH	00213FH
	G4	003000H	003001H	---------	00313EH	00313FH
	G5	004000H	004001H	---------	00413EH	00413FH
	G6	005000H	005001H	---------	00513EH	00513FH
	⋮	⋮	⋮	---------	⋮	⋮
	G475	1DA000H	1DA001H	---------	1DA13EH	1DA13FH
	G476	1DB000H	1DB001H	---------	1DB13EH	1DB13FH
Non-display area	**G477**	1DC000H	1DC001H	---------	1DC13EH	1DC13FH
	G478	1DD000H	1DD001H	---------	1DD13EH	1DD13FH
	G479	1DE000H	1DE001H	---------	1DE13EH	1DE13FH
	G480	1DF000H	1DF001H	---------	1DF13EH	1DF13FH

Table 5.4: Memory map of partial display

5.1.4.3 Vertical Scrolling Display

The vertical scrolling display is specified by VSCRDEF instruction (R33h) and VSCRSADD instruction (R37h).

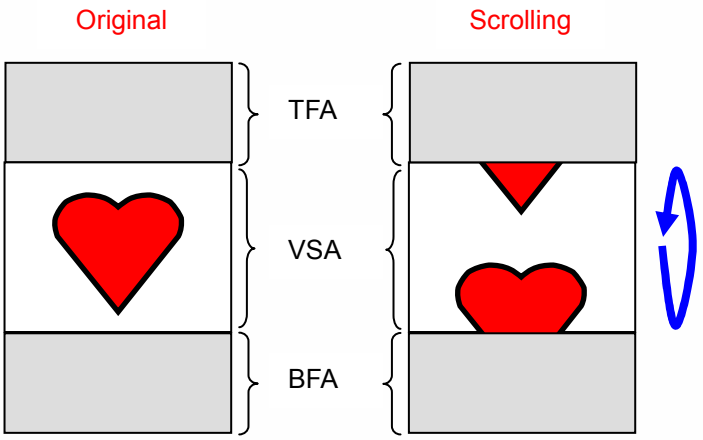


Figure 5.6: Vertical scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=Panel total scan lines. In this case, scrolling is applied as shown below.

Example 1: (1) 320RGBx480 dot display mode.
(2) TFA=2, VSA=478, BFA=0 when MADCTL B4=0
(3) VSCRSADD=03h

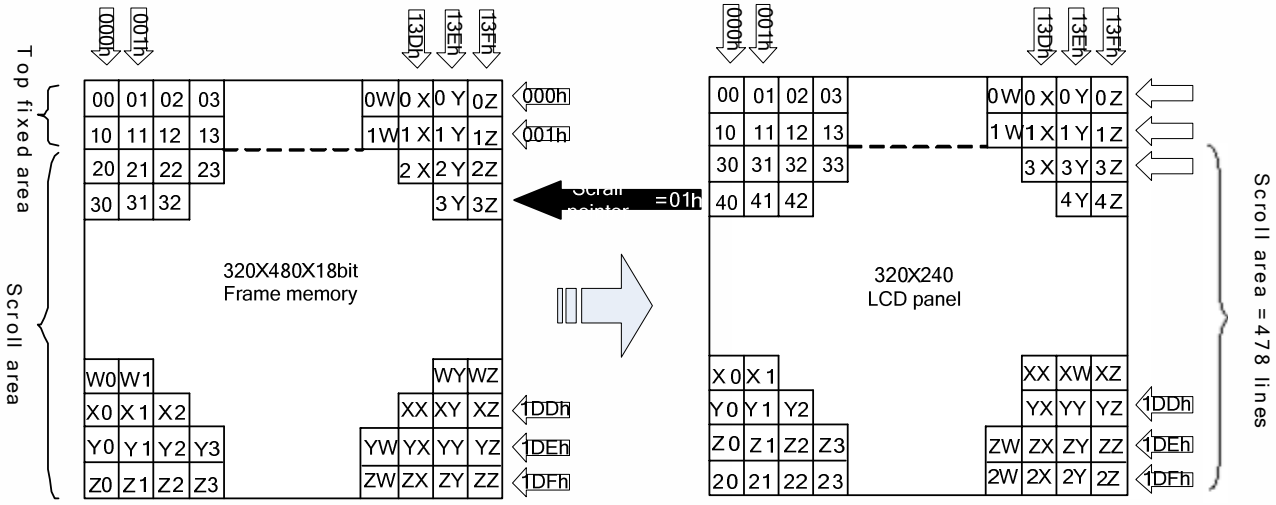


Figure 5.7: Memory map of vertical scrolling example 1

Example 2: (1) 320RGBx480 dot display mode.
(2) TFA=2, VSA=476, BFA=2 when MADCTL B4=0
(3) VSCRSADD=03h

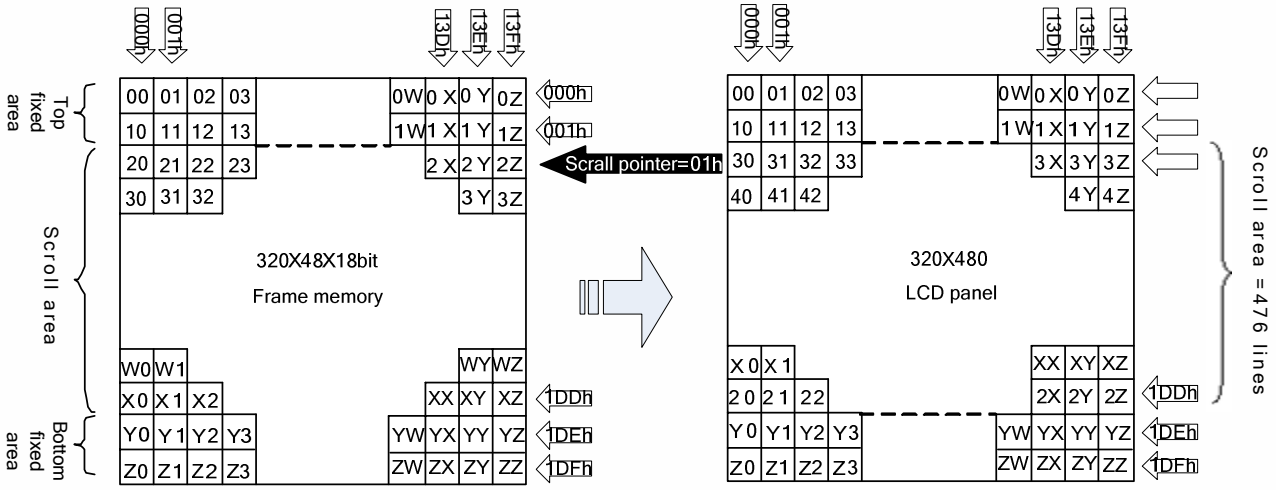


Figure 5.8: Memory map of vertical scrolling example 2

Example 3: (1) 320RGBx480 dot display mode.
(2) TFA=2, VSA=476, BFA=2 when MADCTL B4=0
(3) VSCRSADD=04h

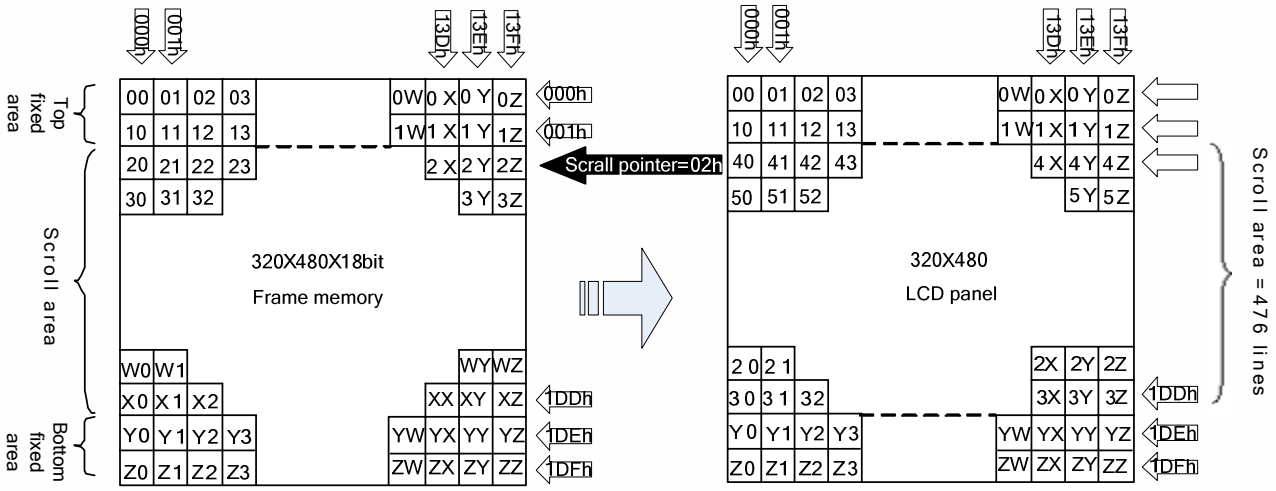


Figure 5.9: Memory map of vertical scrolling example 3

Vertical **Scroll Example**

There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA ≠ Panel scan lines
N/A. Do not set TFA + VSA + BFA≠Panel scan lines. In that case, unexpected picture will be shown.
Case 2: TFA + VSA + BFA = Panel scan lines (Scrolling)

Example 1: (1) 320RGBx480 dot display mode.
(2) When TFA=0, VSA=480, BFA=0 and VSCRSADD=40. MADCTL parameter B4=”0”

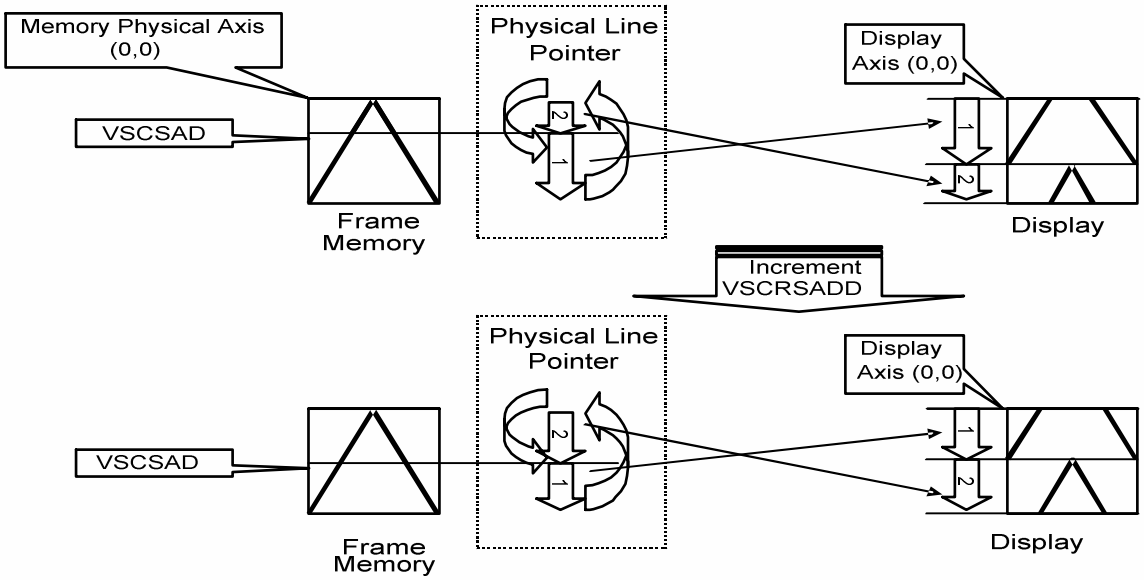


Figure 5.10: Display of Vertical Scroll Example 1

Example 2: (1) 320RGBx480 dot display mode.
(2) TFA=60, VSA=420, BFA=0 and VSCRSADD =160. MADCTRL parameter B4=”1”

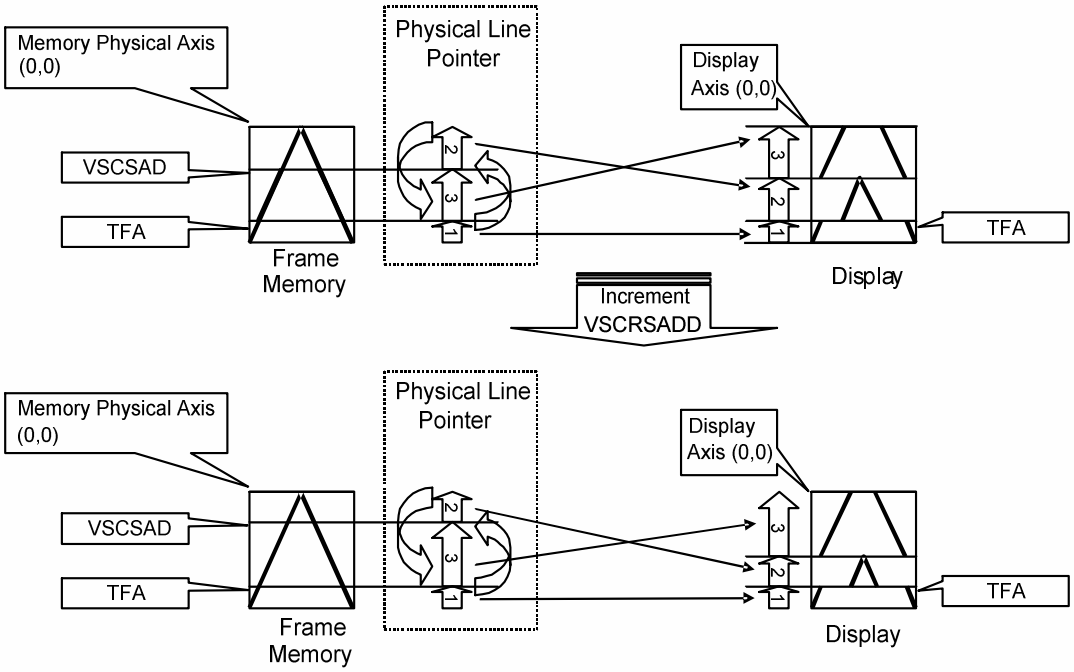


Figure 5.11: Display of Vertical Scroll Example 2

5.2 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.2.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

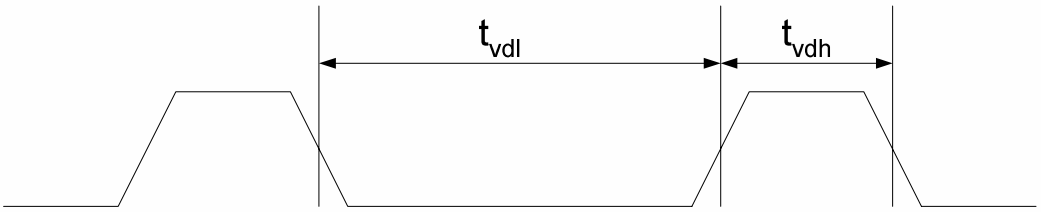


Figure 5.12: Tearing Effect Output signal mode 1

tvdh= The LCD display is not updated from the Frame Memory
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Under Mode1, the TE output timing will be defined by TSEL[15:0] setting.

Ex: 1. TSEL[15:0]=0, then TE signal will output after last Line finished.
TSEL[15:0]=2, then TE signal will output at second Line start.

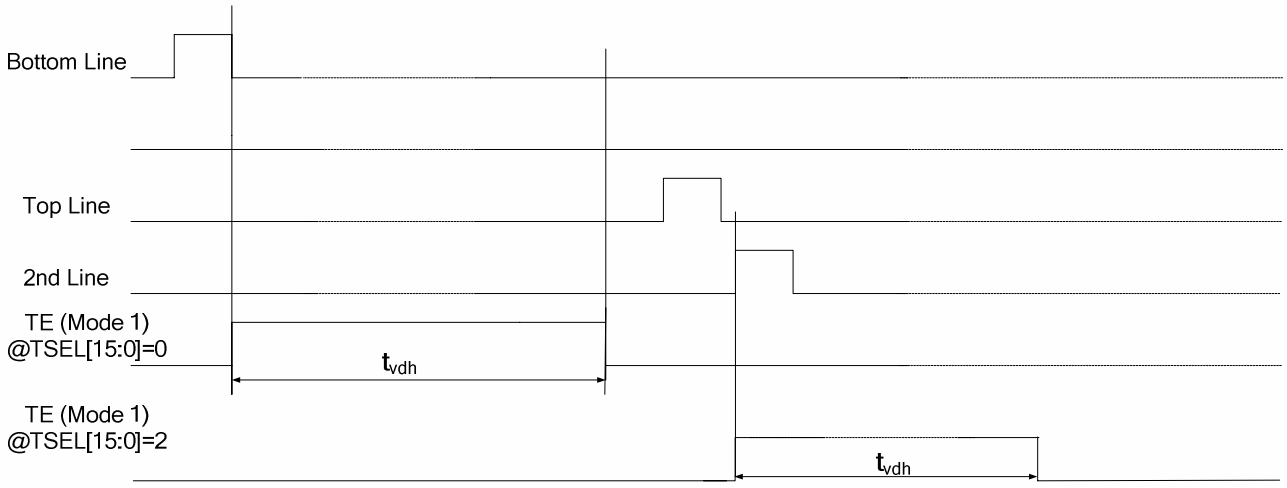


Figure 5.13: TE Delay Output

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync pulses per field.

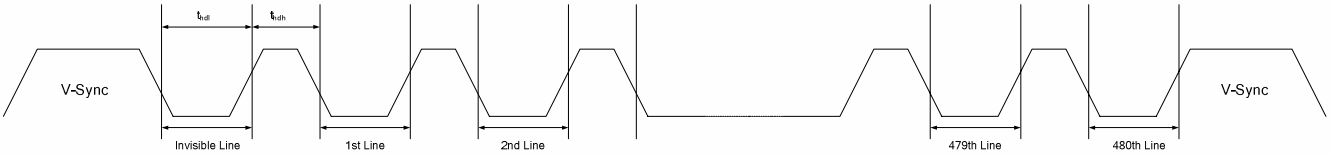


Figure 5.14: Tearing Effect Output signal mode 2

thdh= The LCD display is not updated from the Frame Memory
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Under Mode2, the H-sync pulse output amount will be defined by TSEL[15:0] setting.

Ex: TSEL[15:0]=0, then TE signal will output 480 H-sync.
TSEL[15:0]=1, then TE signal will output 480 H-sync.
TSEL[15:0]=2, then TE signal will output 479 H-sync.

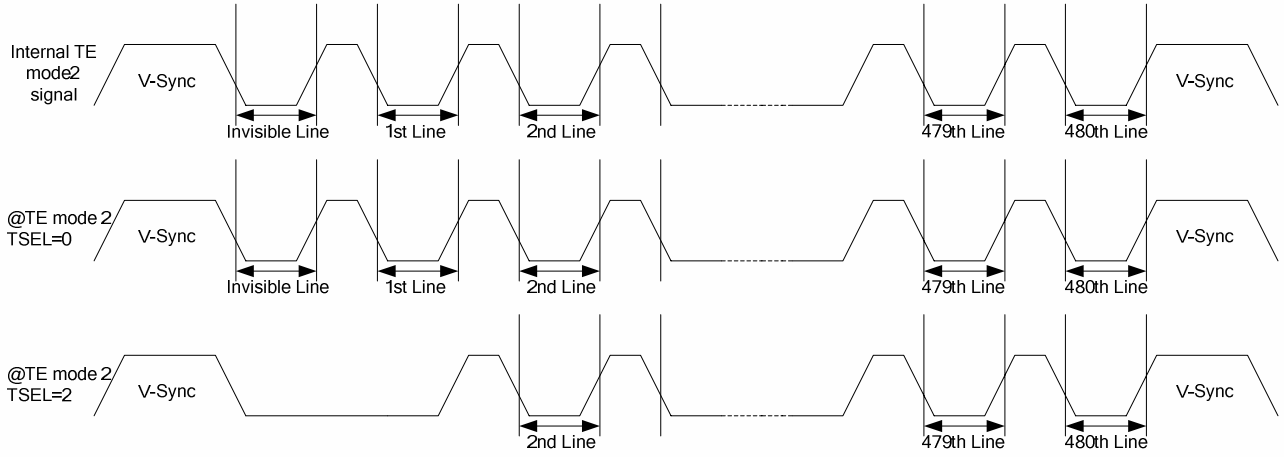
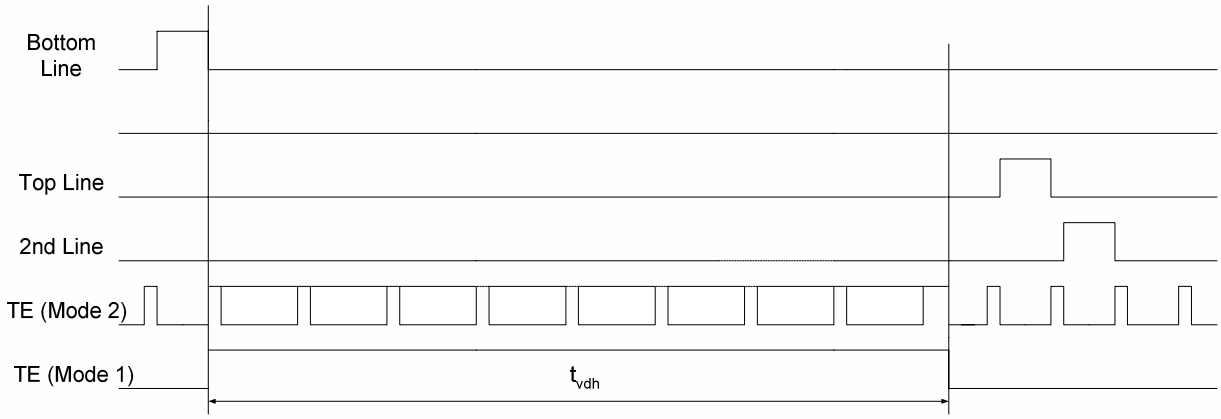


Figure 5.15: TE Output for TELINE setting



Note: During Sleep in Mode, the Tearing Output Pin is active Low

Figure 5.16: Tearing Effect Output signal

5.2.2 Tearing Effect Line Timing

The Tearing Effect signal is described below:

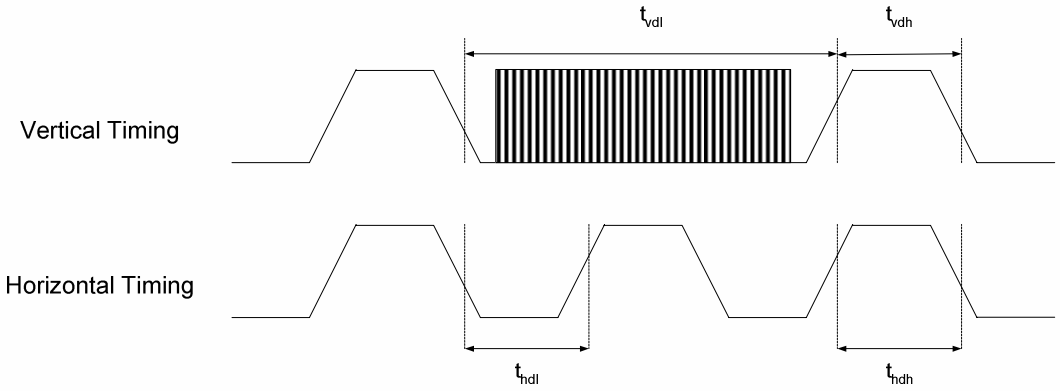


Figure 5.17: Tearing Effect Line Timing

Idle Mode Off (Frame Rate = TBDHz)

Symbol	Parameter	Min.	Max.	Unit	description
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: The timings in Table 5.5 apply when MADCTL ML=0 and ML=1

Table 5.5: AC characteristics of Tearing Effect Signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

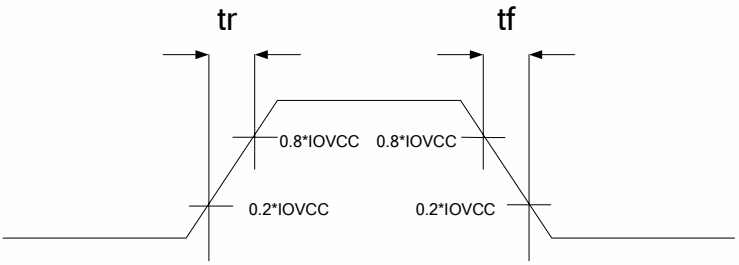


Figure 5.18: Rise and fall times of TE signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

Example 1: MPU's Write is faster than Panel's Read.

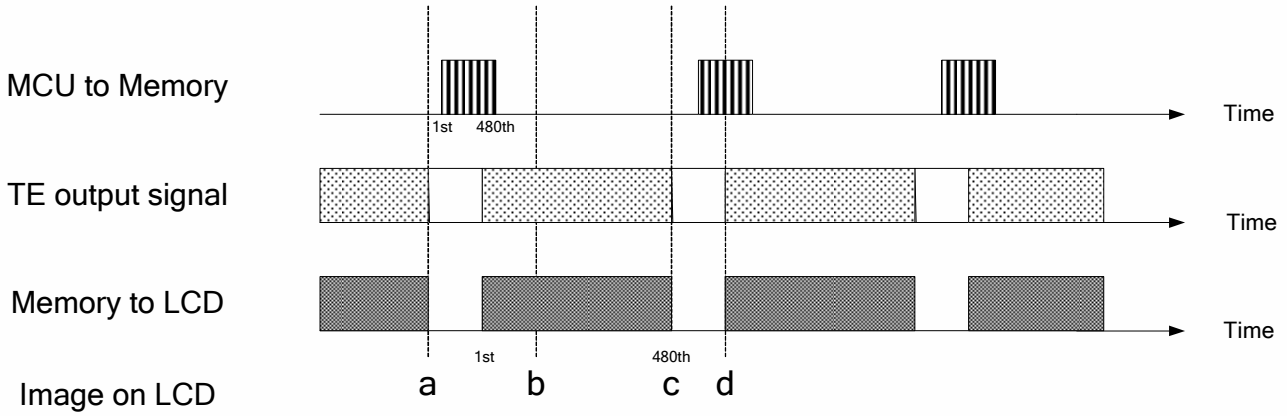


Figure 5.19: Tearing Effect - Example 1-1

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

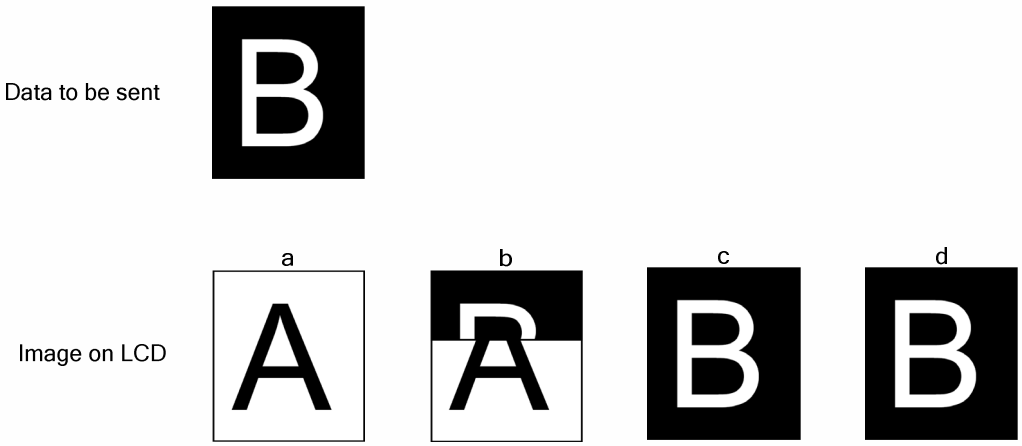


Figure 5.20: Tearing Effect - Example 1-2

Example 2: MPU's Write is slower than Panel's Read.

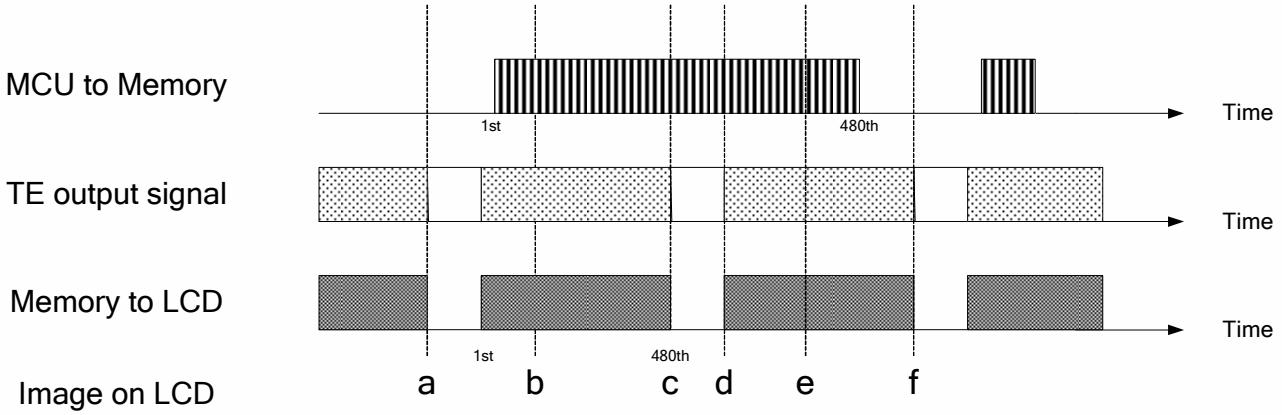


Figure 5.21: Tearing Effect - Example 2-1

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.

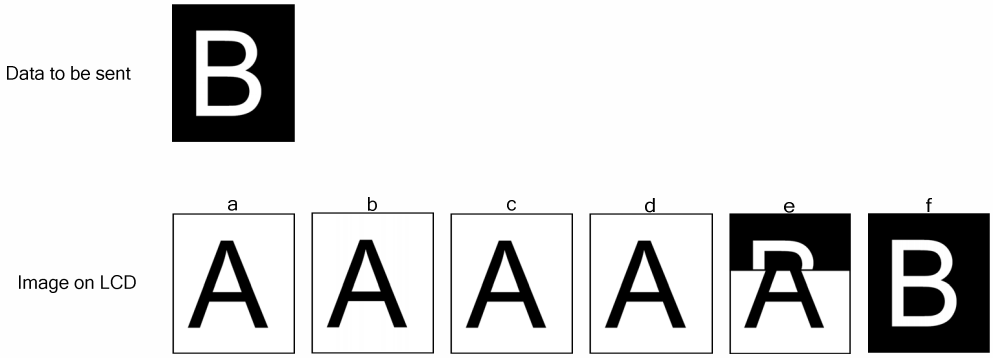


Figure 5.22: Tearing Effect - Example 2-2

5.3 Oscillator

The HX8357-B can oscillate an internal R-C oscillator with an internal oscillation resistor (Rf). The oscillation frequency is changed according to the UADJ[3:0] internal register. Please refer to Set OSC control register (RC5h). The default frequency is 5.2MHz.

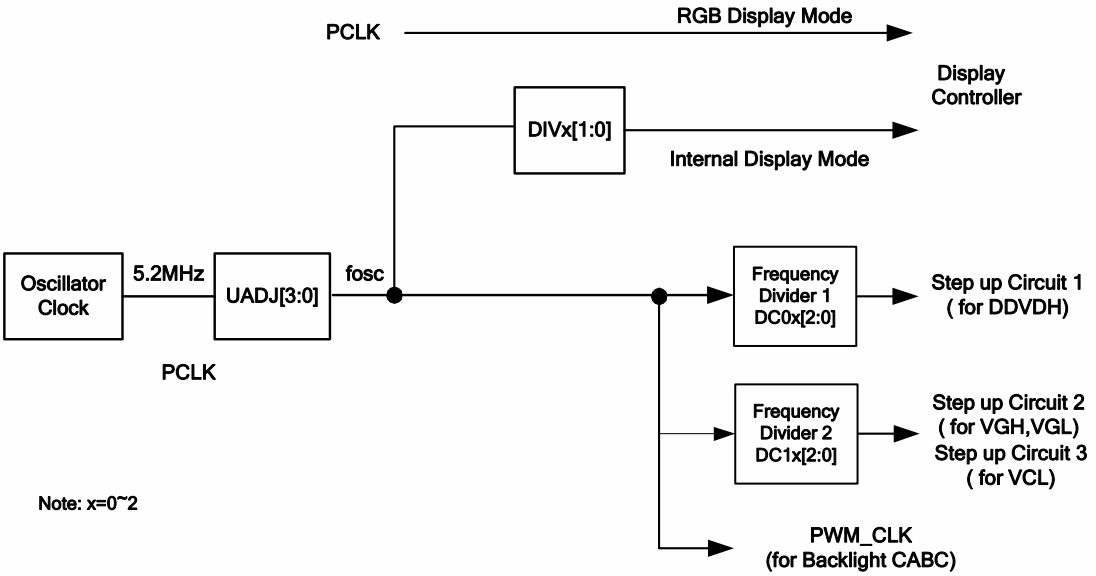


Figure 5.23: Oscillation Circuit

5.4 Source Driver

The HX8357-B contains a 960 channels of source driver (S1~S960) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 960 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.5 Gate Driver

The HX8357-B contains a 480 gate channels of gate driver (G1~G480) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.6 LCD Power Generation Circuit

5.6.1 LCD Power Generation Scheme

The boost voltage generated is shown as below.

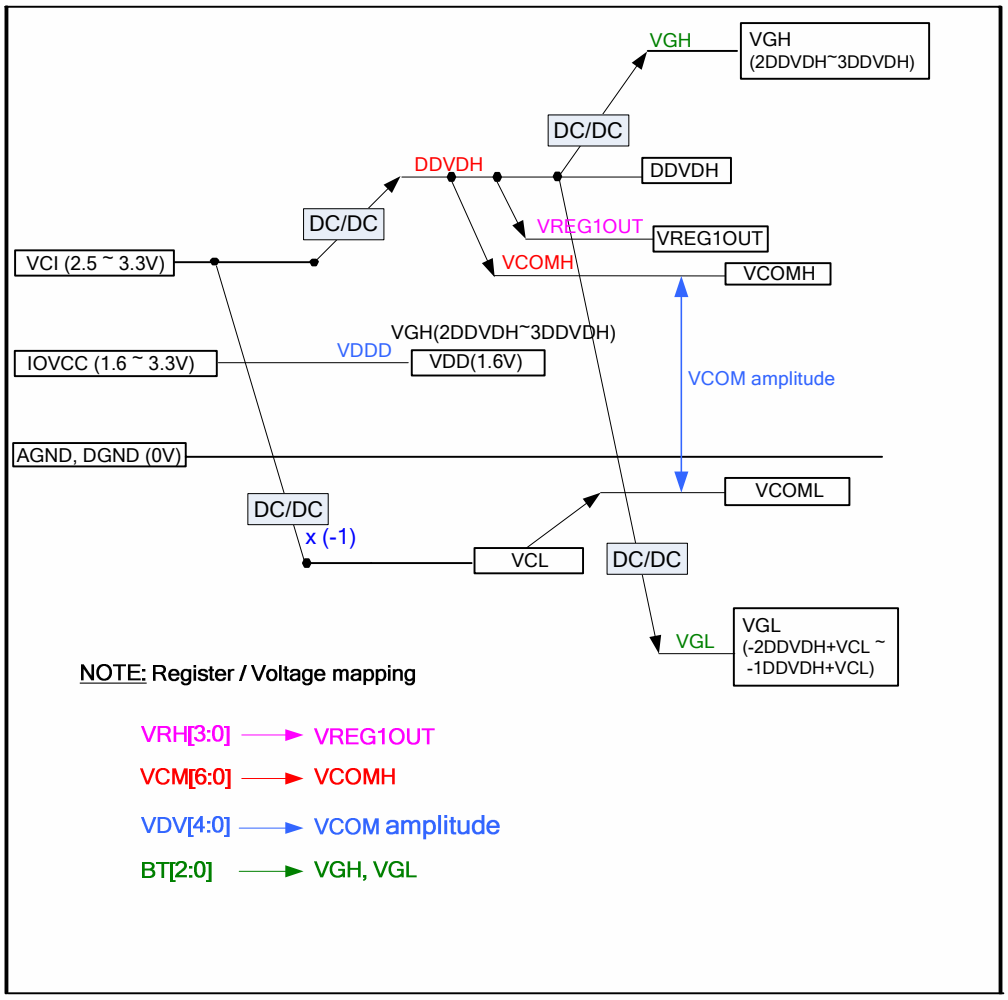
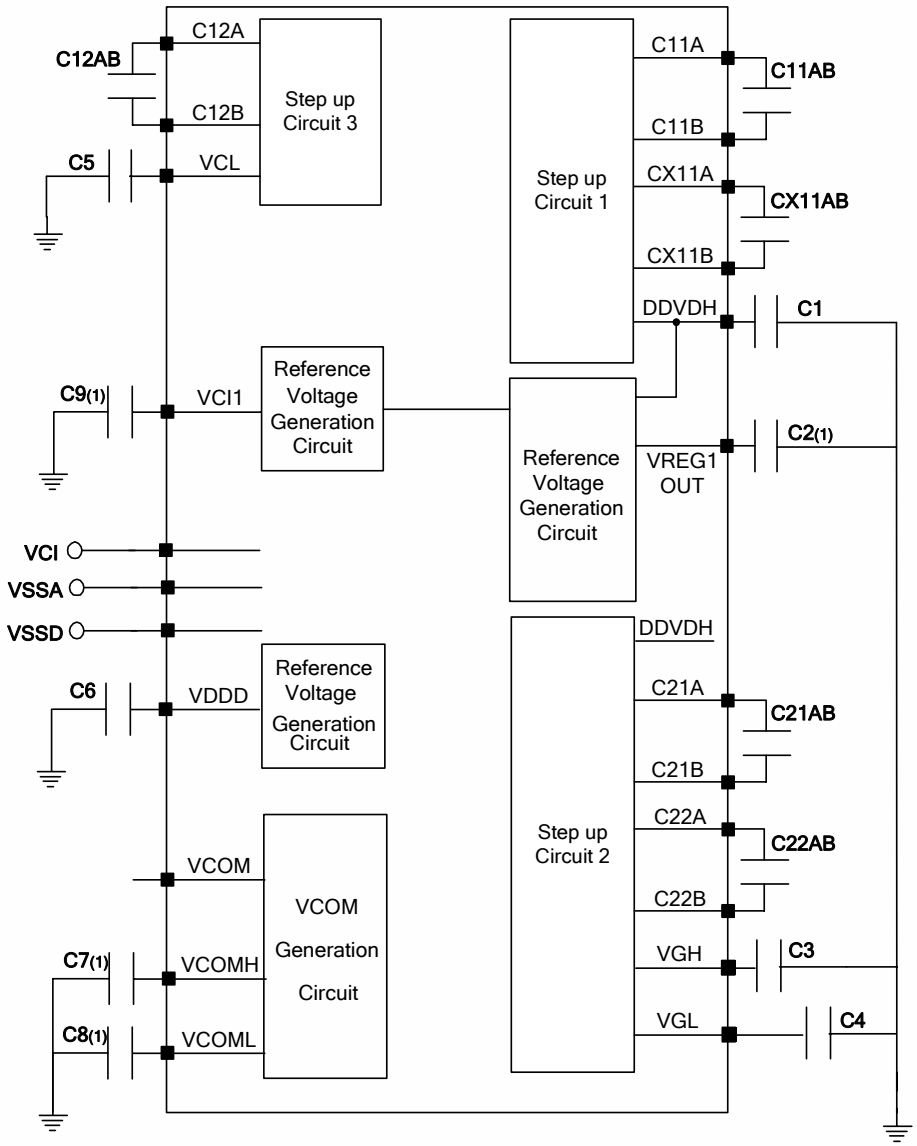


Figure 5.24: LCD Power Generation Scheme

5.6.2 Various Boosting Steps



Note: If Display quality normal, the C2, C7, C8 and C9 can remove.

Figure 5.25: Various Boosting Steps

Specification of Connected Passive Component

Capacitor	Recommended voltage	Capacity	Note
C1 (DDVDH)	10V	1μF (B characteristics)	-
C2 (VREG1OUT)	10V	1μF (B characteristics)	(1)
C3 (VGH)	25V	1μF (B characteristics)	-
C4 (VGL)	16V	1μF (B characteristics)	-
C5 (VCL)	6V	1μF (B characteristics)	-
C6(VDD)	6V	1μF (B characteristics)	-
C7 (VCOMH)	10V	1μF (B characteristics)	(1)
C8(VCOML)	6V	1μF (B characteristics)	(1)
C9(VCI1)	6V	1μF (B characteristics)	(1)
C11AB (C11A/B)	6V	1μF (B characteristics)	-
CX11AB (CX11A/B)	6V	1μF (B characteristics)	-
C12AB (C12A/B)	6V	1μF (B characteristics)	-
C21AB (C21A/B)	10V	1μF (B characteristics)	-
C22AB (C22A/B)	10V	1μF (B characteristics)	-

Note: If Display quality normal, the C2, C7, C8 and C9 can remove.

Table 5.6: The adoptability of Capacitor

5.7 Gamma Characteristic Correction Function

The HX8357-B incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 64 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

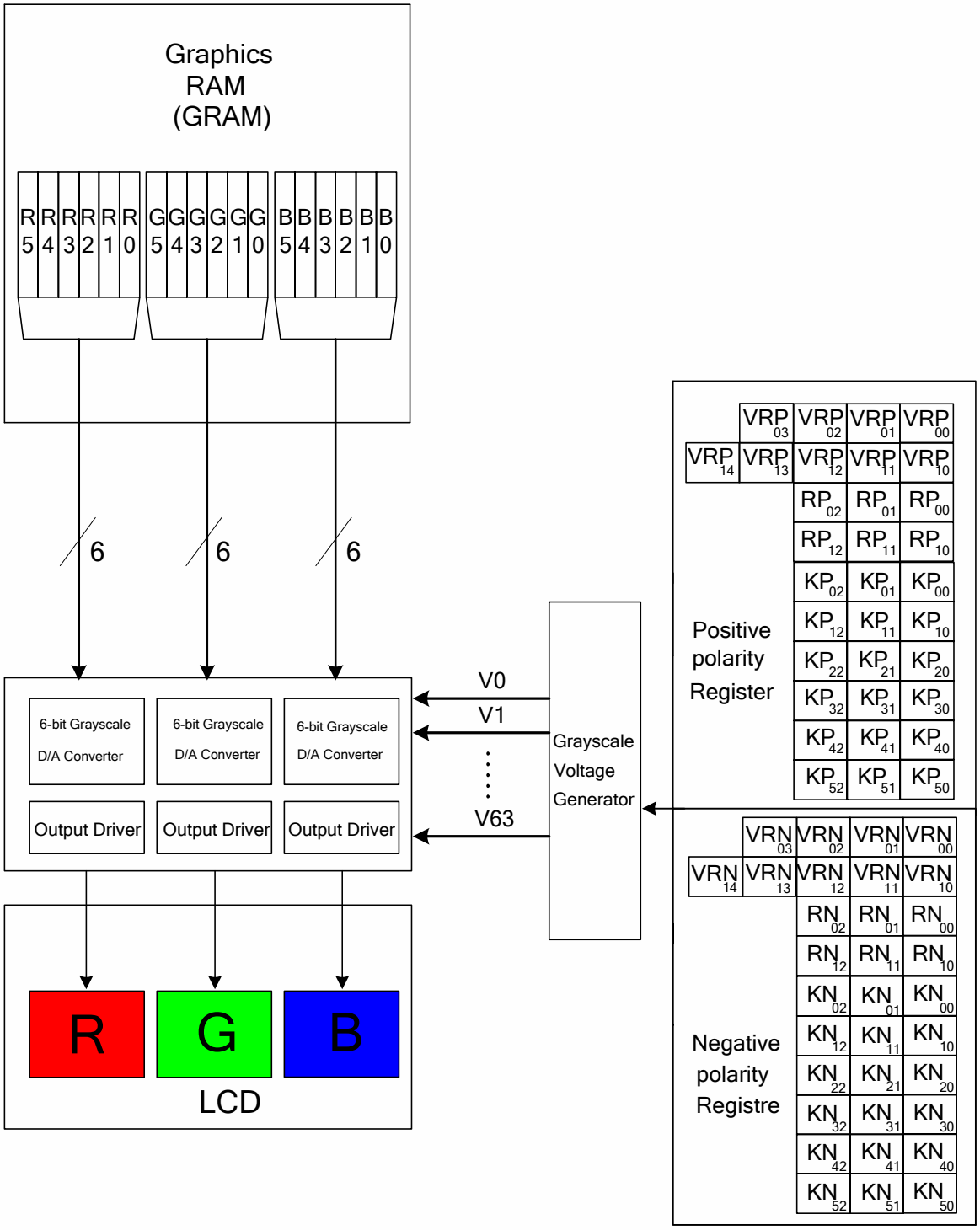


Figure 5.26: Grayscale Control

5.7.1 Structure of Grayscale Voltage Generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62, 63) for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltages injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel used.

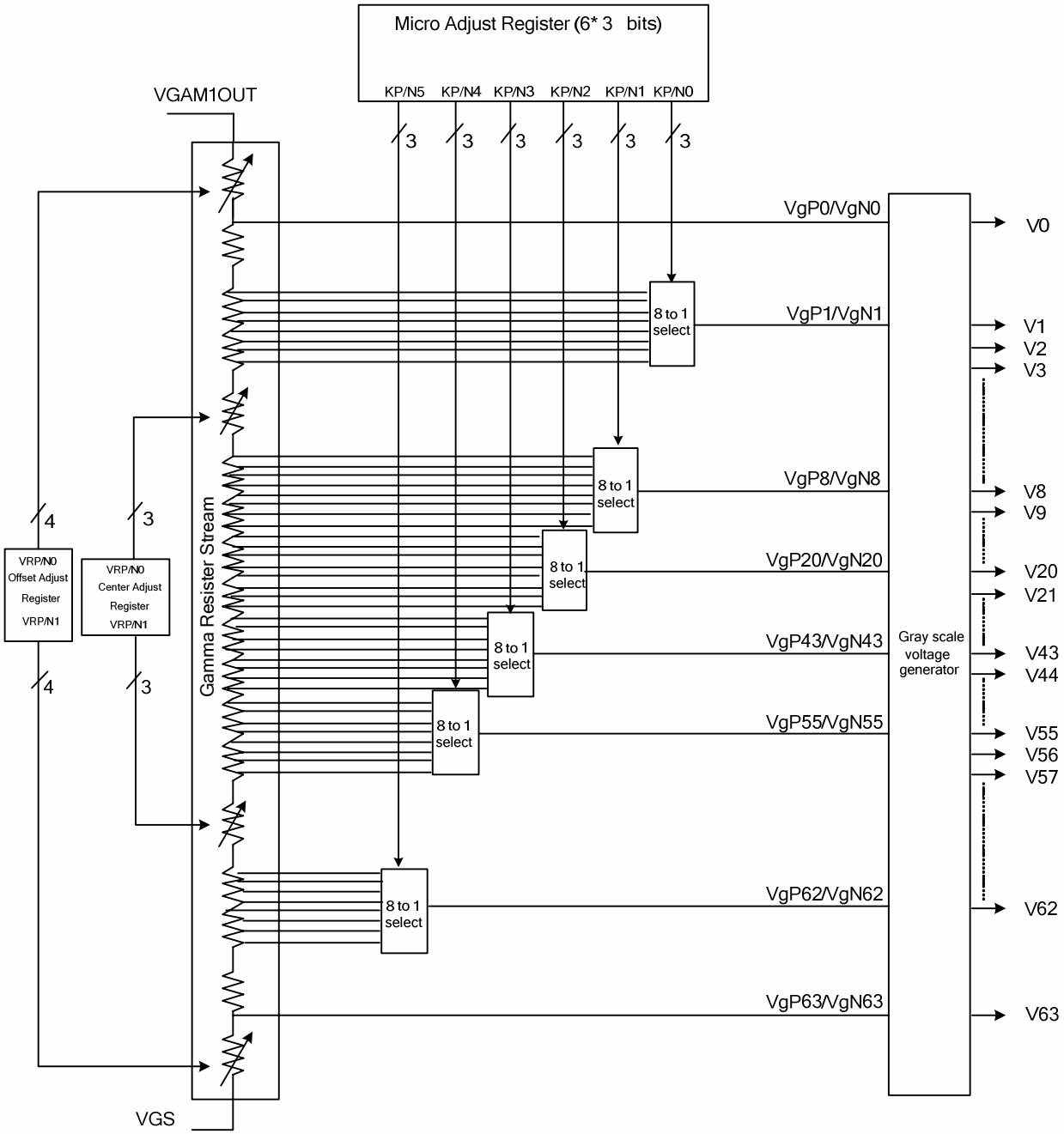


Figure 5.27: Structure of Grayscale Voltage Generator

5.7.2 Gamma-Characteristics Adjustment Register

This HX8357-B has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

A. Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

B. Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

C. Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (KP/N0~5), each of which has 8 inputs and generate one reference voltage output (VgP/N) 1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	RP0 2-0	RN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	RP1 2-0	RN1 2-0	Variable resistor (VRCP/N1) for center adjustment
Macro Adjustment	KP0 2-0	KN0 2-0	8-to-1 selector (voltage level of grayscale 1)
	KP1 2-0	KN1 2-0	8-to-1 selector (voltage level of grayscale 8)
	KP2 2-0	KN2 2-0	8-to-1 selector (voltage level of grayscale 20)
	KP3 2-0	KN3 2-0	8-to-1 selector (voltage level of grayscale 43)
	KP4 2-0	KN4 2-0	8-to-1 selector (voltage level of grayscale 55)
	KP5 2-0	KN5 2-0	8-to-1 selector (voltage level of grayscale 62)
Offset Adjustment	VRP0 3-0	VRN0 3-0	Variable resistor (VROP/N0) for offset adjustment
	VRP1 4-0	VRN1 4-0	Variable resistor (VROP/N1) for offset adjustment

Table 5.7: Gamma-Adjustment Registers

5.7.3 Gamma resister stream and 8 to 1 Selector

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. (VgP/N) 0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has pin (VGS) to connect a variable resistor outside the chip for the variation between panels if needed.

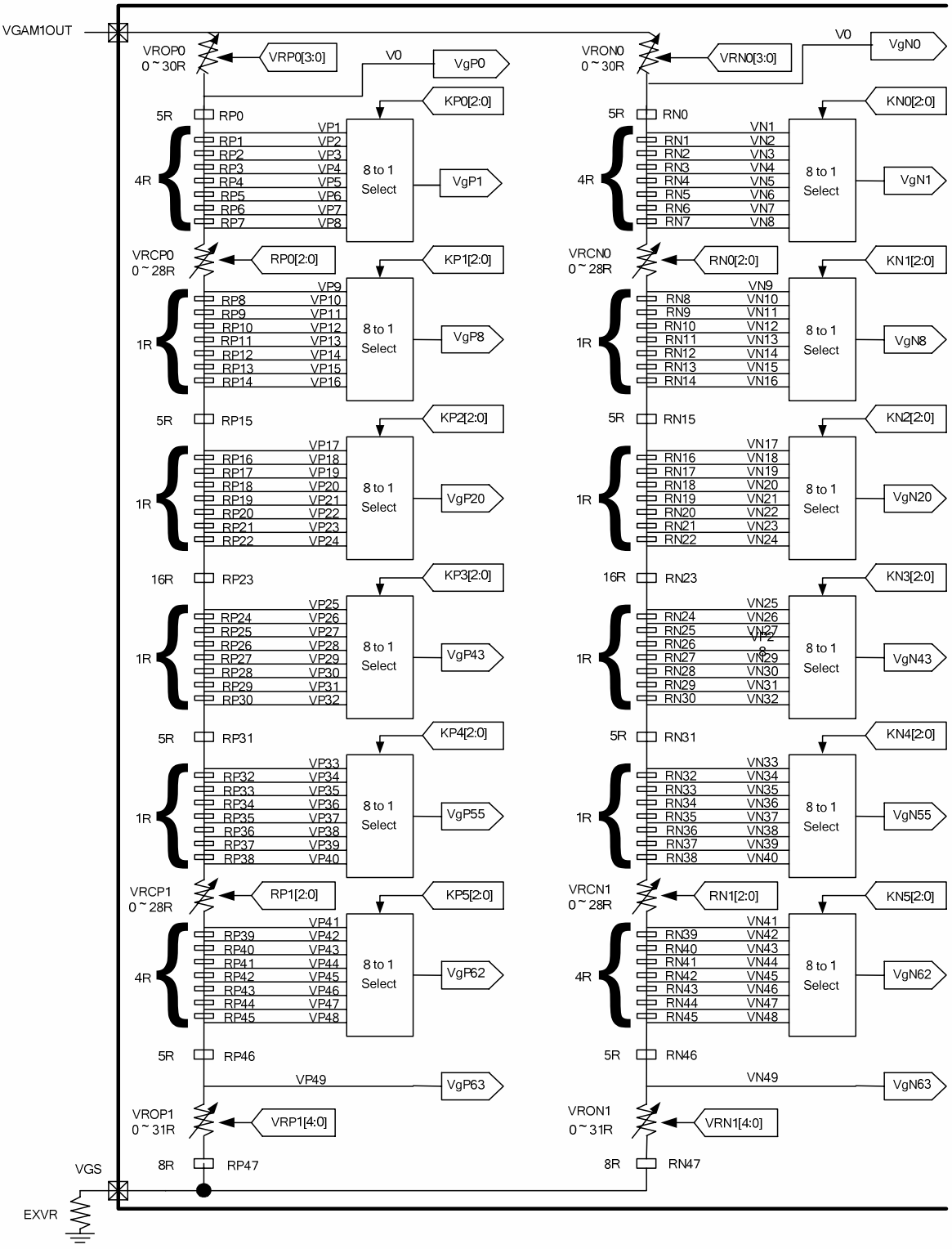


Figure 5.28: Gamma Resister Stream and Gamma Reference Voltage

A. Variable resister

There are two types of variable resistors, one is for center adjustment, and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 3-0	Resistance VRO(P/N)0
0000	0R
0001	2R
0010	4R
•	•
•	•
1101	26R
1110	28R
1111	30R

Table 5.8: Offset Adjustment 0

Value in Register VR(P/N)1 4-0	Resistance VRO(P/N)1
00000	0R
00001	1R
00010	2R
•	•
•	•
11101	29R
11110	30R
11111	31R

Table 5.9: Offset Adjustment 1

Value in Register R(P/N)0/1 2-0	Resistance VRC(P/N)0/1
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 5.10: Center Adjustment

B. 8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream. It outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. These six 8 to 1 selectors and the relationship are shown below.

Value in Register	Voltage level					
K(P/N) 2-0	Vg(P/N) 1	Vg(P/N) 8	Vg(P/N) 20	Vg(P/N) 43	V(P/N) 55	V(P/N) 62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 5.11: Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgP0	-	VGAM1OUT-VD*VROP0 /sumRP	VP0
VgP1	KP0 2-0=000	VGAM1OUT-VD((VROP0+5R) /sumRP	VP1
	KP0 2-0=001	VGAM1OUT-VD((VROP0+9R) /sumRP	VP2
	KP0 2-0=010	VGAM1OUT-VD((VROP0+13R) /sumRP	VP3
	KP0 2-0=011	VGAM1OUT-VD((VROP0+17R) /sumRP	VP4
	KP0 2-0=100	VGAM1OUT-VD((VROP0+21R) /sumRP	VP5
	KP0 2-0=101	VGAM1OUT-VD((VROP0+25R) /sumRP	VP6
	KP0 2-0=110	VGAM1OUT-VD((VROP0+29R) /sumRP	VP7
	KP0 2-0=111	VGAM1OUT-VD((VROP0+33R) /sumRP	VP8
VgP8	KP1 2-0=000	VGAM1OUT-VD((VROP0+33R+VRCP0) /sumRP	VP9
	KP1 2-0=001	VGAM1OUT-VD((VROP0+34R+VRCP0) /sumRP	VP10
	KP1 2-0=010	VGAM1OUT-VD((VROP0+35R+VRCP0) /sumRP	VP11
	KP1 2-0=011	VGAM1OUT-VD((VROP0+36R+VRCP0) /sumRP	VP12
	KP1 2-0=100	VGAM1OUT-VD((VROP0+37R+VRCP0) /sumRP	VP13
	KP1 2-0=101	VGAM1OUT-VD((VROP0+38R+VRCP0) /sumRP	VP14
	KP1 2-0=110	VGAM1OUT-VD((VROP0+39R+VRCP0) /sumRP	VP15
	KP1 2-0=111	VGAM1OUT-VD((VROP0+40R+VRCP0) /sumRP	VP16
VgP20	KP2 2-0=000	VGAM1OUT-VD((VROP0+45R+VRCP0) /sumRP	VP17
	KP2 2-0=001	VGAM1OUT-VD((VROP0+46R+VRCP0) /sumRP	VP18
	KP2 2-0=010	VGAM1OUT-VD((VROP0+47R+VRCP0) /sumRP	VP19
	KP2 2-0=011	VGAM1OUT-VD((VROP0+48R+VRCP0) /sumRP	VP20
	KP2 2-0=100	VGAM1OUT-VD((VROP0+49R+VRCP0) /sumRP	VP21
	KP2 2-0=101	VGAM1OUT-VD((VROP0+50R+VRCP0) /sumRP	VP22
	KP2 2-0=110	VGAM1OUT-VD((VROP0+51R+VRCP0) /sumRP	VP23
	KP2 2-0=111	VGAM1OUT-VD((VROP0+52R+VRCP0) /sumRP	VP24
VgP43	KP3 2-0=000	VGAM1OUT-VD((VROP0+68R+VRCP0) /sumRP	VP25
	KP3 2-0=001	VGAM1OUT-VD((VROP0+69R+VRCP0) /sumRP	VP26
	KP3 2-0=010	VGAM1OUT-VD((VROP0+70R+VRCP0) /sumRP	VP27
	KP3 2-0=011	VGAM1OUT-VD((VROP0+71R+VRCP0) /sumRP	V2P8
	KP3 2-0=100	VGAM1OUT-VD((VROP0+72R+VRCP0) /sumRP	VP29
	KP3 2-0=101	VGAM1OUT-VD((VROP0+73R+VRCP0) /sumRP	VP30
	KP3 2-0=110	VGAM1OUT-VD((VROP0+74R+VRCP0) /sumRP	VP31
	KP3 2-0=111	VGAM1OUT-VD((VROP0+75R+VRCP0) /sumRP	VP32
VgP55	KP4 2-0=000	VGAM1OUT-VD((VROP0+80R+VRCP0) /sumRP	VP33
	KP4 2-0=001	VGAM1OUT-VD((VROP0+81R+VRCP0) /sumRP	VP34
	KP4 2-0=010	VGAM1OUT-VD((VROP0+82R+VRCP0) /sumRP	VP35
	KP4 2-0=011	VGAM1OUT-VD((VROP0+83R+VRCP0) /sumRP	VP36
	KP4 2-0=100	VGAM1OUT-VD((VROP0+84R+VRCP0) /sumRP	VP37
	KP4 2-0=101	VGAM1OUT-VD((VROP0+85R+VRCP0) /sumRP	VP38
	KP4 2-0=110	VGAM1OUT-VD((VROP0+86R+VRCP0) /sumRP	VP39
	KP4 2-0=111	VGAM1OUT-VD((VROP0+87R+VRCP0) /sumRP	VP40
VgP62	KP5 2-0=000	VGAM1OUT-VD((VROP0+87R+VRCP0+VRCP1) /sumRP	VP41
	KP5 2-0=001	VGAM1OUT-VD((VROP0+91R+VRCP0+VRCP1) /sumRP	VP42
	KP5 2-0=010	VGAM1OUT-VD((VROP0+95R+VRCP0+VRCP1) /sumRP	VP43
	KP5 2-0=011	VGAM1OUT-VD((VROP0+99R+VRCP0+VRCP1) /sumRP	VP44
	KP5 2-0=100	VGAM1OUT-VD((VROP0+103R+VRCP0+VRCP1) /sumRP	VP45
	KP5 2-0=101	VGAM1OUT-VD((VROP0+107R+VRCP0+VRCP1) /sumRP	VP46
	KP5 2-0=110	VGAM1OUT-VD((VROP0+111R+VRCP0+VRCP1) /sumRP	VP47
	KP5 2-0=111	VGAM1OUT-VD((VROP0+115R+VRCP0+VRCP1) /sumRP	VP48
VgP63	-	VGAM1OUT-VD((VROP0+120R+VRCP0+VRCP1) /sumRP	VP49

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1.
SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1.
VD=(VGAM1OUT-VGS).
[sumRP× (sumRN/ (sumRP+sumRN))]/ [sumRP×sumRN/ (sumRP+sumRN) +EXVR]

Table 5.12: Voltage Calculation Formula (Positive Polarity)

Grayscale Voltage	Formula
V0	VgP0
V1	VgP1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VgP8
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINP3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINP4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINP5
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VINP6
V63	VINP7

Table 5.13: Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN0	-	VGAM1OUT-VD*VRON0 /sumRN	VN0
VgN1	KN0 2-0=000	VGAM1OUT-VD((VRON0+5R) /sumRN	VN1
	KN0 2-0=001	VGAM1OUT-VD((VRON0+9R) /sumRN	VN2
	KN0 2-0=010	VGAM1OUT-VD((VRON0+13R) /sumRN	VN3
	KN0 2-0=011	VGAM1OUT-VD((VRON0+17R) /sumRN	VN4
	KN0 2-0=100	VGAM1OUT-VD((VRON0+21R) /sumRN	VN5
	KN0 2-0=101	VGAM1OUT-VD((VRON0+25R) /sumRN	VN6
	KN0 2-0=110	VGAM1OUT-VD((VRON0+29R) /sumRN	VN7
	KN0 2-0=111	VGAM1OUT-VD((VRON0+33R) /sumRN	VN8
VgN8	KN1 2-0=000	VGAM1OUT-VD((VRON0+33R+VRCN0) /sumRN	VN9
	KN1 2-0=001	VGAM1OUT-VD((VRON0+34R+VRCN0) /sumRN	VN10
	KN1 2-0=010	VGAM1OUT-VD((VRON0+35R+VRCN0) /sumRN	VN11
	KN1 2-0=011	VGAM1OUT-VD((VRON0+36R+VRCN0) /sumRN	VN12
	KN1 2-0=100	VGAM1OUT-VD((VRON0+37R+VRCN0) /sumRN	VN13
	KN1 2-0=101	VGAM1OUT-VD((VRON0+38R+VRCN0) /sumRN	VN14
	KN1 2-0=110	VGAM1OUT-VD((VRON0+39R+VRCN0) /sumRN	VN15
	KN1 2-0=111	VGAM1OUT-VD((VRON0+40R+VRCN0) /sumRN	VN16
VgN20	KN2 2-0=000	VGAM1OUT-VD((VRON0+45R+VRCN0) /sumRN	VN17
	KN2 2-0=001	VGAM1OUT-VD((VRON0+46R+VRCN0) /sumRN	VN18
	KN2 2-0=010	VGAM1OUT-VD((VRON0+47R+VRCN0) /sumRN	VN19
	KN2 2-0=011	VGAM1OUT-VD((VRON0+48R+VRCN0) /sumRN	VN20
	KN2 2-0=100	VGAM1OUT-VD((VRON0+49R+VRCN0) /sumRN	VN21
	KN2 2-0=101	VGAM1OUT-VD((VRON0+50R+VRCN0) /sumRN	VN22
	KN2 2-0=110	VGAM1OUT-VD((VRON0+51R+VRCN0) /sumRN	VN23
	KN2 2-0=111	VGAM1OUT-VD((VRON0+52R+VRCN0) /sumRN	VN24
VgN43	KN3 2-0=000	VGAM1OUT-VD((VRON0+68R+VRCN0) /sumRN	VN25
	KN3 2-0=001	VGAM1OUT-VD((VRON0+69R+VRCN0) /sumRN	VN26
	KN3 2-0=010	VGAM1OUT-VD((VRON0+70R+VRCN0) /sumRN	VN27
	KN3 2-0=011	VGAM1OUT-VD((VRON0+71R+VRCN0) /sumRN	VNP8
	KN3 2-0=100	VGAM1OUT-VD((VRON0+72R+VRCN0) /sumRN	VN29
	KN3 2-0=101	VGAM1OUT-VD((VRON0+73R+VRCN0) /sumRN	VN30
	KN3 2-0=110	VGAM1OUT-VD((VRON0+74R+VRCN0) /sumRN	VN31
	KN3 2-0=111	VGAM1OUT-VD((VRON0+75R+VRCN0) /sumRN	VN32
VgN55	KN4 2-0=000	VGAM1OUT-VD((VRON0+80R+VRCN0) /sumRN	VN33
	KN4 2-0=001	VGAM1OUT-VD((VRON0+81R+VRCN0) /sumRN	VN34
	KN4 2-0=010	VGAM1OUT-VD((VRON0+82R+VRCN0) /sumRN	VN35
	KN4 2-0=011	VGAM1OUT-VD((VRON0+83R+VRCN0) /sumRN	VN36
	KN4 2-0=100	VGAM1OUT-VD((VRON0+84R+VRCN0) /sumRN	VN37
	KN4 2-0=101	VGAM1OUT-VD((VRON0+85R+VRCN0) /sumRN	VN38
	KN4 2-0=110	VGAM1OUT-VD((VRON0+86R+VRCN0) /sumRN	VN39
	KN4 2-0=111	VGAM1OUT-VD((VRON0+87R+VRCN0) /sumRN	VN40
VgN62	KN5 2-0=000	VGAM1OUT-VD((VRON0+87R+VRCN0+VRCN1) /sumRN	VN41
	KN5 2-0=001	VGAM1OUT-VD((VRON0+91R+VRCN0+VRCN1) /sumRN	VN42
	KN5 2-0=010	VGAM1OUT-VD((VRON0+95R+VRCN0+VRCN1) /sumRN	VN43
	KN5 2-0=011	VGAM1OUT-VD((VRON0+99R+VRCN0+VRCN1) /sumRN	VN44
	KN5 2-0=100	VGAM1OUT-VD((VRON0+103R+VRCN0+VRCN1)/sumRN	VN45
	KN5 2-0=101	VGAM1OUT-VD((VRON0+107R+VRCN0+VRCN1)/sumRN	VN46
	KN5 2-0=110	VGAM1OUT-VD((VRON0+111R+VRCN0+VRCN1)/sumRN	VN47
	KN5 2-0=111	VGAM1OUT-VD((VRON0+115R+VRCN0+VRCN1)/sumRN	VN48
VgN63	-	VGAM1OUT-VD((VRON0+120R+VRCN0+VRCN1)/sumRN	VN49

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1;
SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1
VD = (VGAM1OUT-VGS) [sumRP(sumRN/(sumRP+sumRN))]/[sumRP(sumRN/(sumRP+sumRN)+EXVR)

Table 5.14: Voltage Calculation Formula (Negative Polarity)

Grayscale Voltage	Formula
V0	VgN0
V1	VIgN1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VgN8
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VgN20
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VgN43
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VgN55
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VgN62
V63	VgN63

Table 5.15: Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

Relationship between GRAM Data and Output Level.

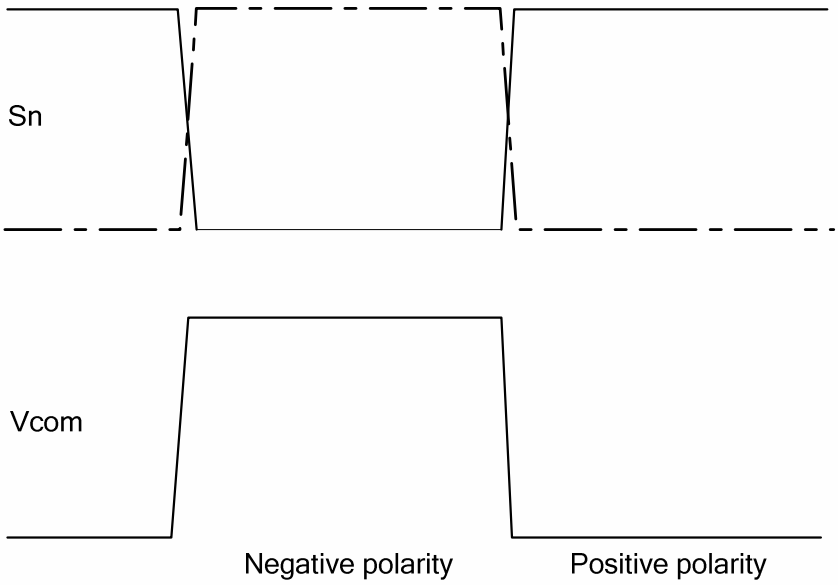
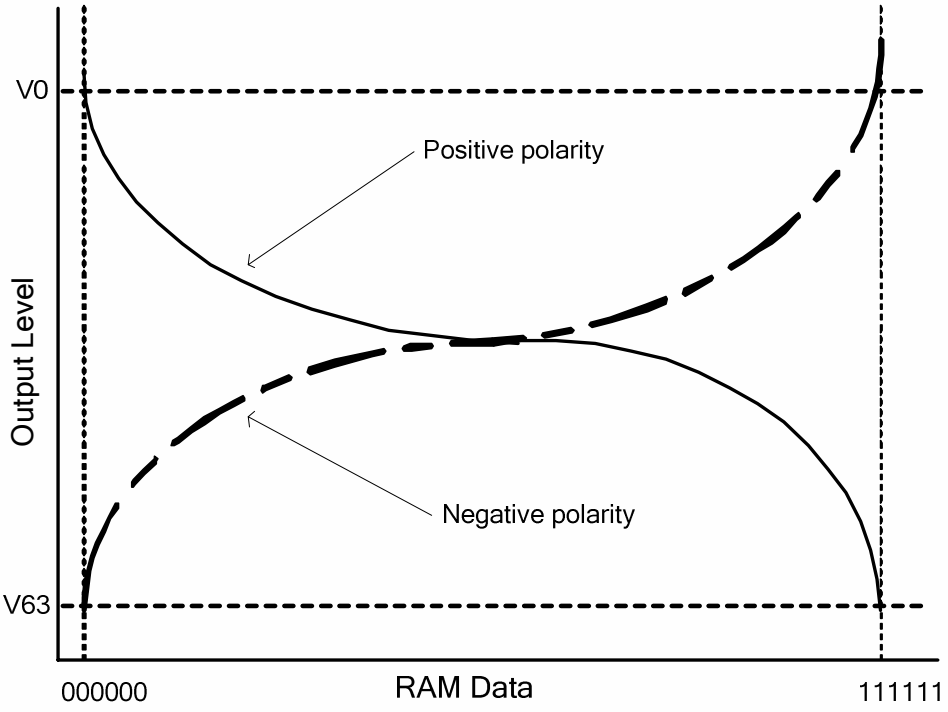


Figure 5.29: Relationship between Source Output and Vcom



(Same characteristic for each RGB)

Figure 5.30: Relationships between GRAM Data and Output Level

5.8 Power Flow Chart for Different Power Modes

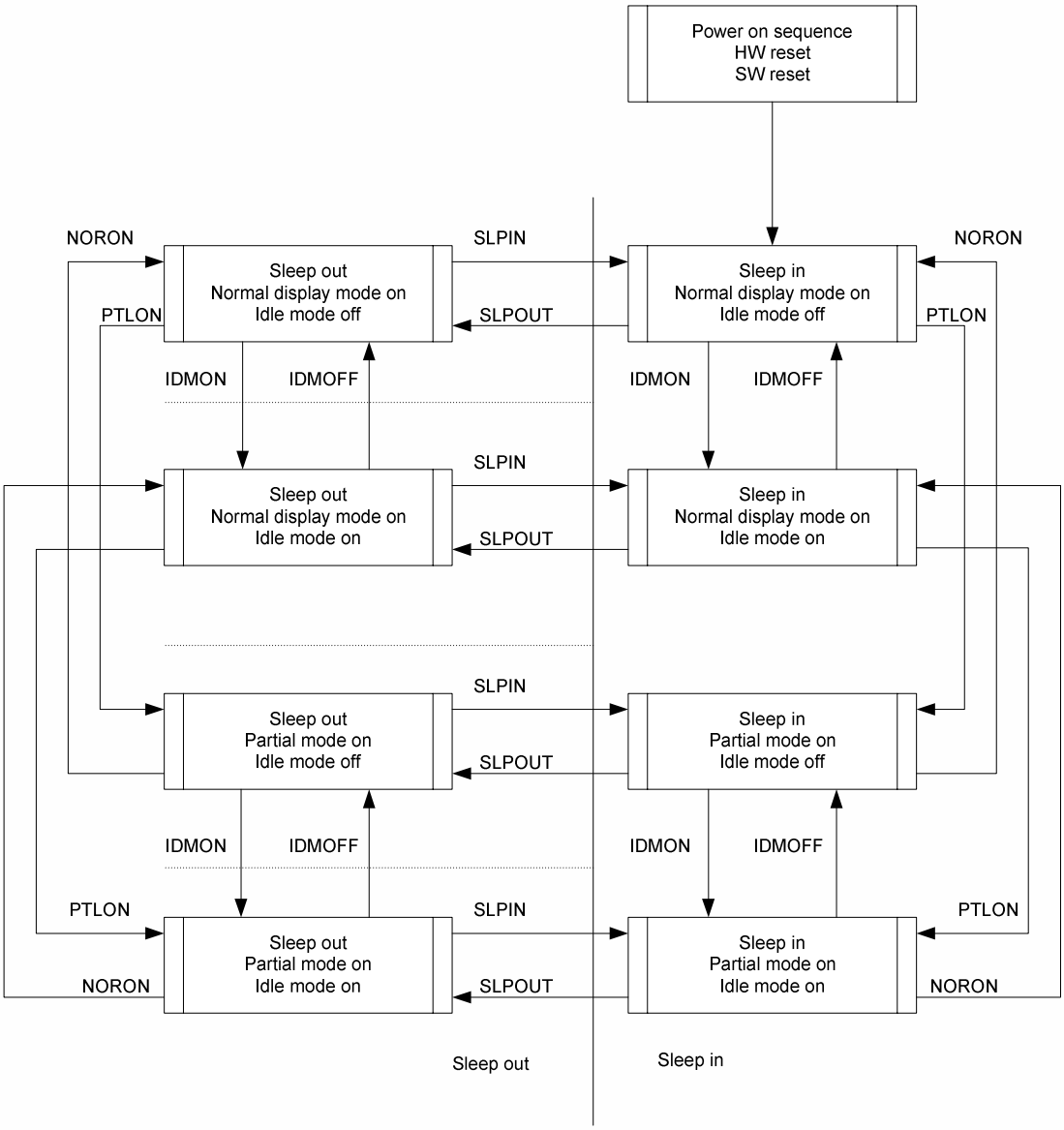


Figure 5.31: Power Flow Chart for Different Power Modes

Mode		Meaning	Other word
Display Mode	Normal Mode	Driving Mode for Fully Display ”Partial Mode Off” and “Scroll Mode Off”	Normal Mode On Normal Display Mode On
	Partial Mode	Driving Mode for Partial Display	Partial Mode On
Color Mode	Idle Mode On	8 Color Mode	-
	Idle Mode Off	Full Color Mode	-

Table 5.16: Mode definition

5.9 Input / Output Pin State

5.9.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
CABC_ON, CABC_PWM	Low	Low	Low
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Table 5.17: Characteristics of Output or Bi-directional (I/O) Pins

5.9.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	Section 7.12	Input valid	Input valid	Input valid	Section 7.12
CSX	Input valid	Input valid	Input valid	Input valid	Input valid
DCX	Input valid	Input valid	Input valid	Input valid	Input valid
WRX_SCL	Input valid	Input valid	Input valid	Input valid	Input valid
RDX	Input valid	Input valid	Input valid	Input valid	Input valid
DB17 to DB0 DIN_SDA	Input valid	Input valid	Input valid	Input valid	Input valid
HSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
VSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
PCLK	Input valid	Input valid	Input valid	Input valid	Input valid
DE	Input valid	Input valid	Input valid	Input valid	Input valid
IMO2, IM1, IM0, SD, CM	Input valid	Input valid	Input valid	Input valid	Input valid
TEST3-1	Low	Low	Low	Low	Low

Table 5.18: Characteristics of Input Pins

5.9.3 Sleep Out –Command and Self-Diagnostic functions of The Display Module

5.9.4 Register loading Detection

Sleep Out-command (See section 6.2.13 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command 6.2.9 “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).
The flow chart for this internal function is following:

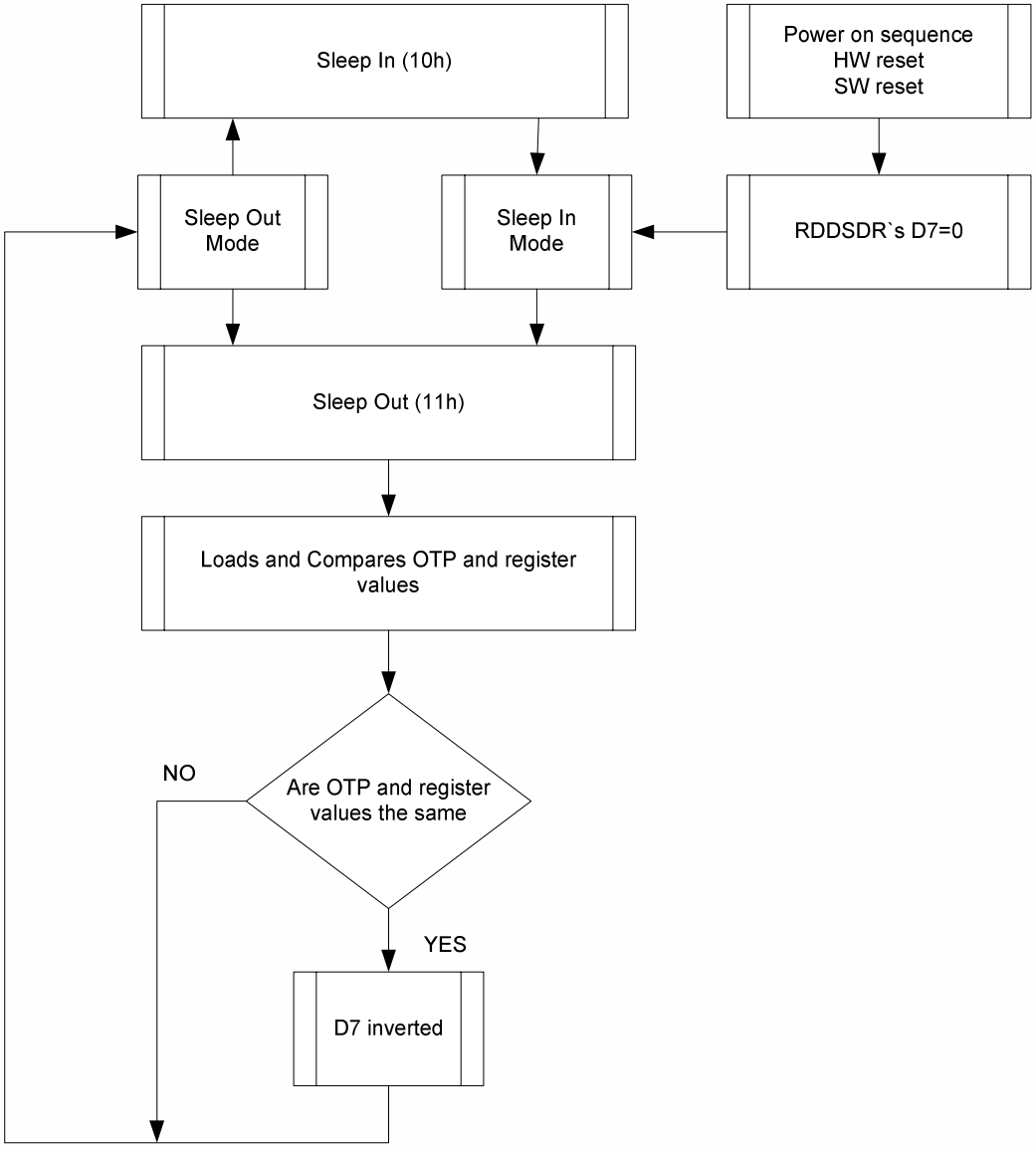


Figure 5.32: Sleep Out Flow Chart – Command and Self-Diagnostic Functions

5.9.5 Functionality Detection

Sleep Out-command (See section 6.2.13 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command 6.2.11 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is following:

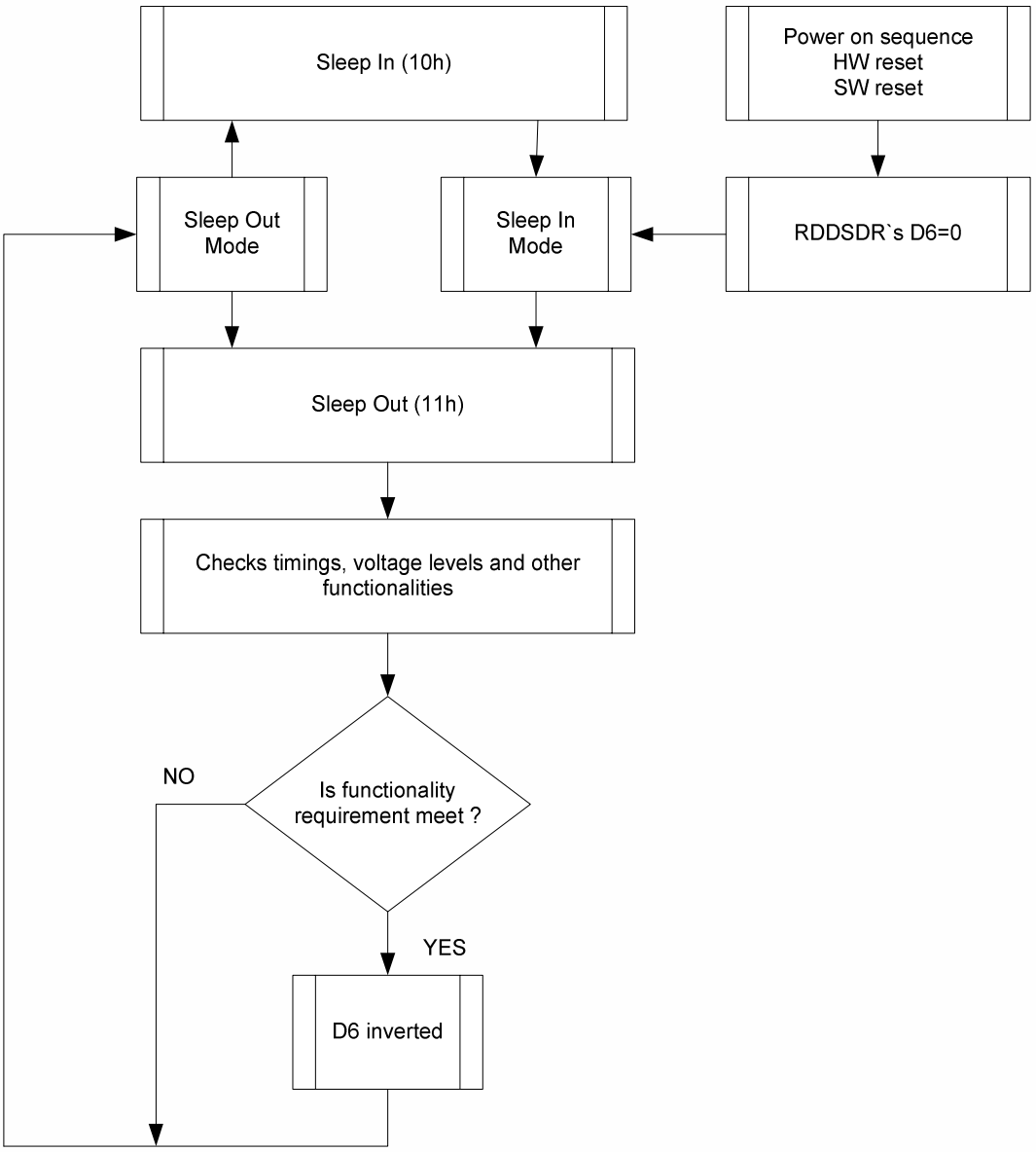


Figure 5.33: Sleep Out Flow Chart Internal Function Detection

5.10 Power On/Off Sequence

IOVCC and VCI can be applied in any order. IOVCC and VCI can be powered down in any order. During power off, if LCD is in the Sleep Out mode, IOVCC and VCI must be powered down minimum 120msec after RESX has been released. During power off, if LCD is in the Sleep In mode, IOVCC and VCI can be powered down minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power on Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence. If RESX line is not held stable by host during Power on Sequence as defined in Sections 7.12.1 and 7.12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power on Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The power on/off sequence is illustrated below.

5.10.1 Case 1 – RESX line is held High or Unstable by Host at Power On

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both IOVCC and VCI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

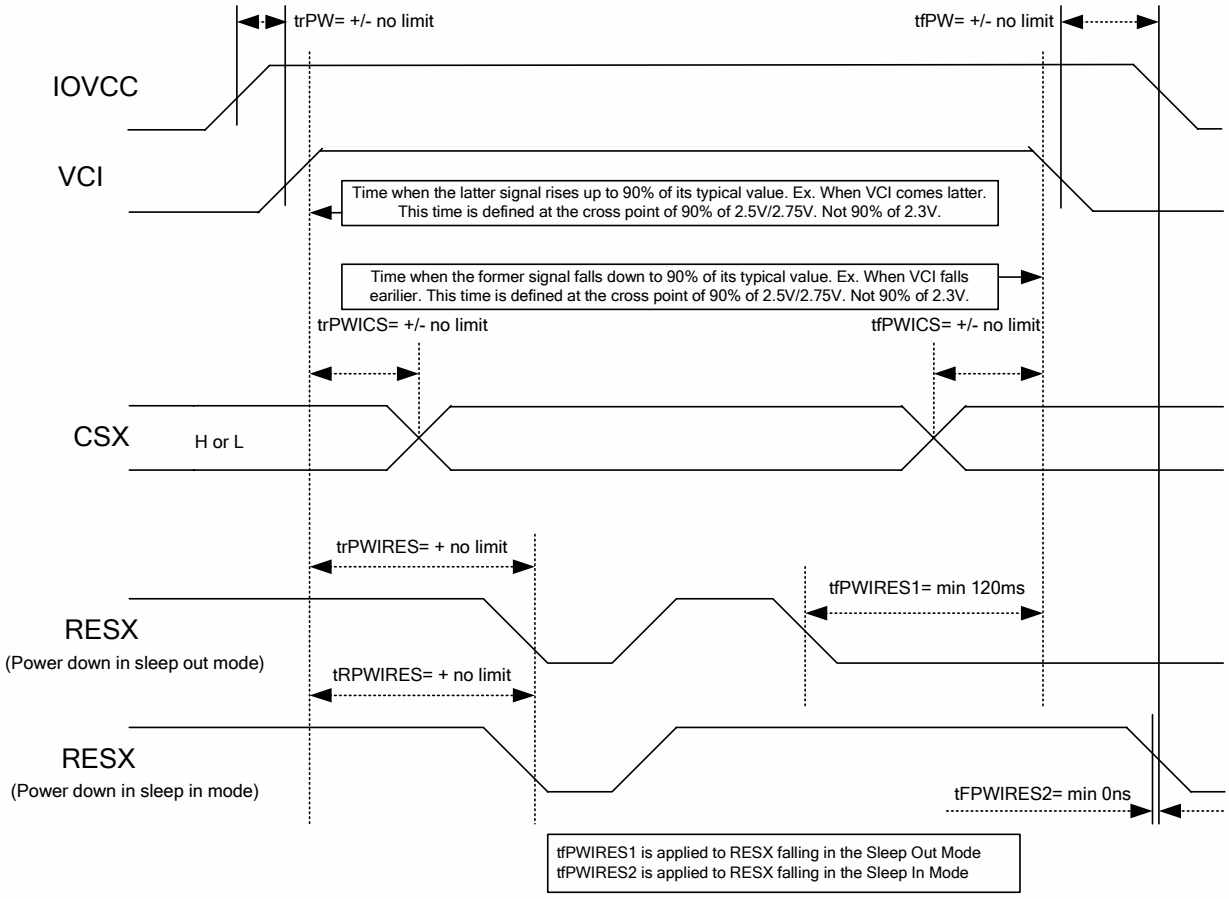


Figure 5.34: Case 1 –RESX line is held High or Unstable by Host at Power On

5.10.2 Case 2 – RESX line is held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both IOVCC and VCI have been applied.

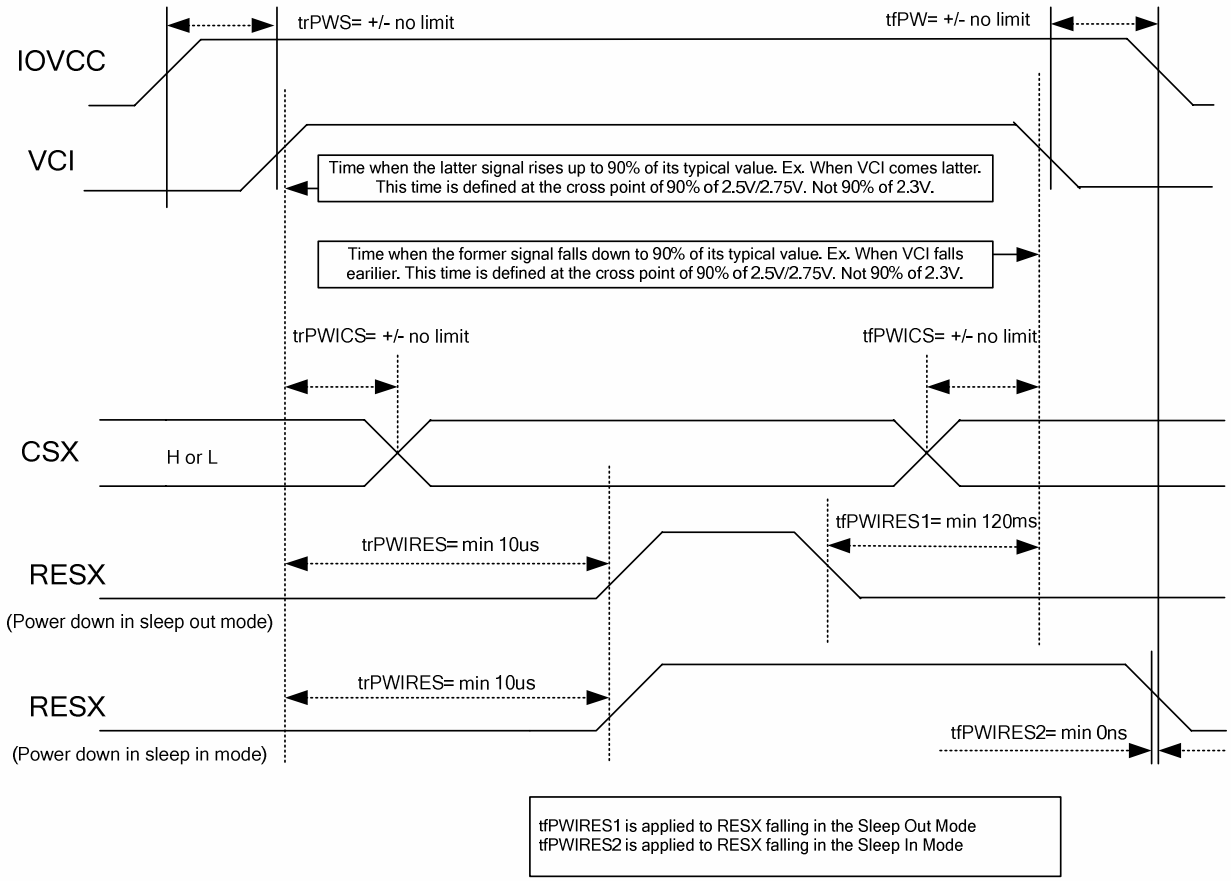


Figure 5.35: Case 2 – RESX line is held Low by Host at Power On

5.11 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power on Sequence” powers it

5.12 Deep standby mode enter/exit flow

A. Enter deep standby mode

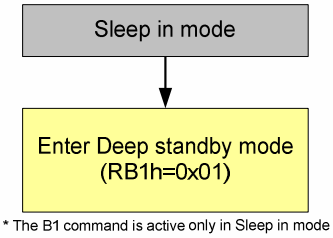


Figure 5.36: Enter deep standby mode flow

B. Exit deep standby mode

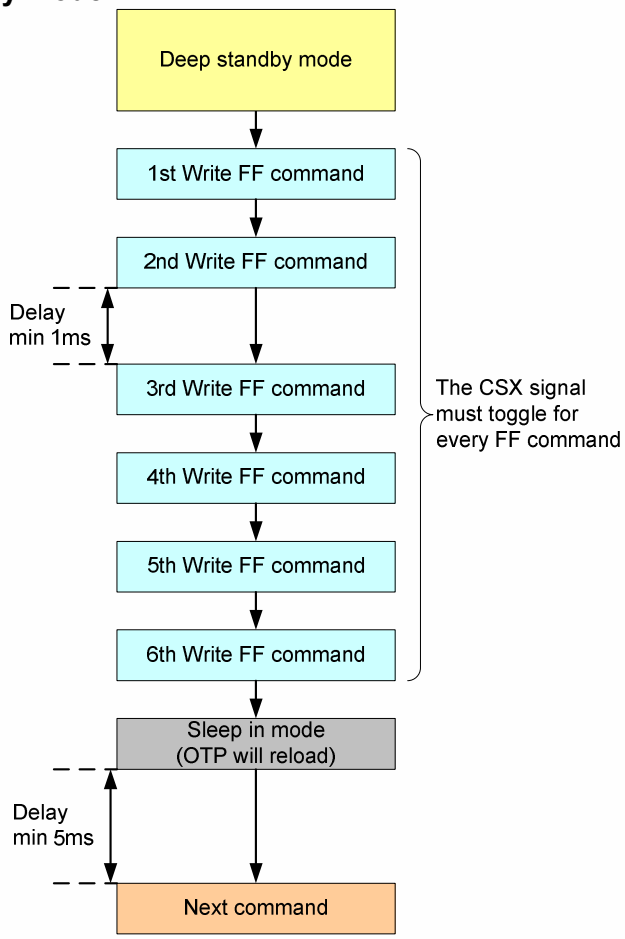


Figure 5.37: Exit Deep standby mode flow

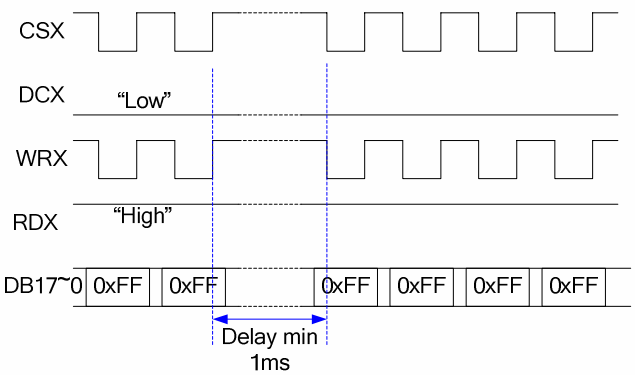


Figure 5.38: Exit Deep standby mode control signals

5.13 Content Adaptive Brightness Control (CABC) Function

The general block diagram of the CABC and the brightness control is illustrated below:

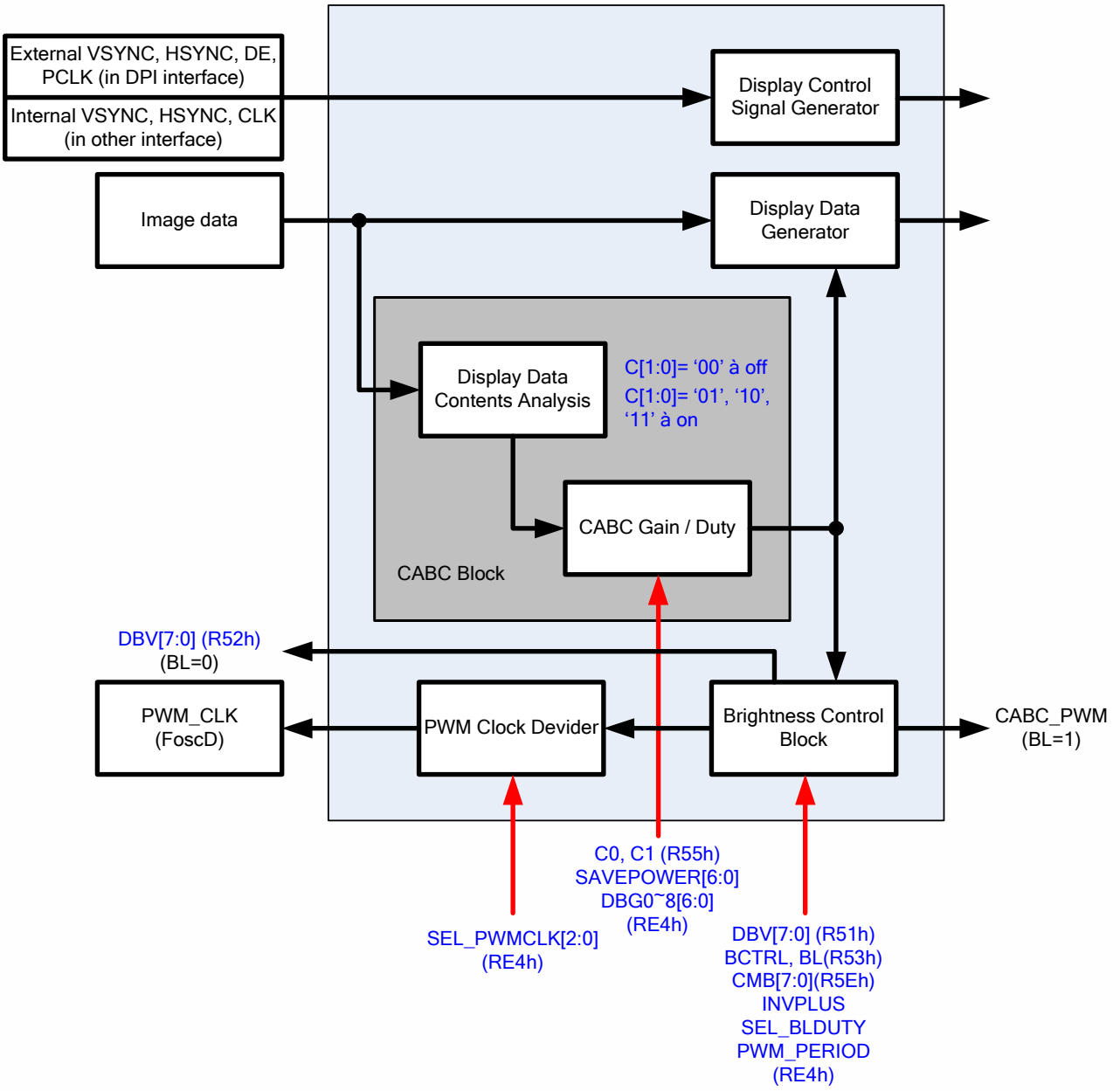


Figure 5.39: Block diagram of the CABC

5.13.1 Module Architectures

HX8357-B can support two module architectures for CABC operation. The **BL** bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- Architecture I

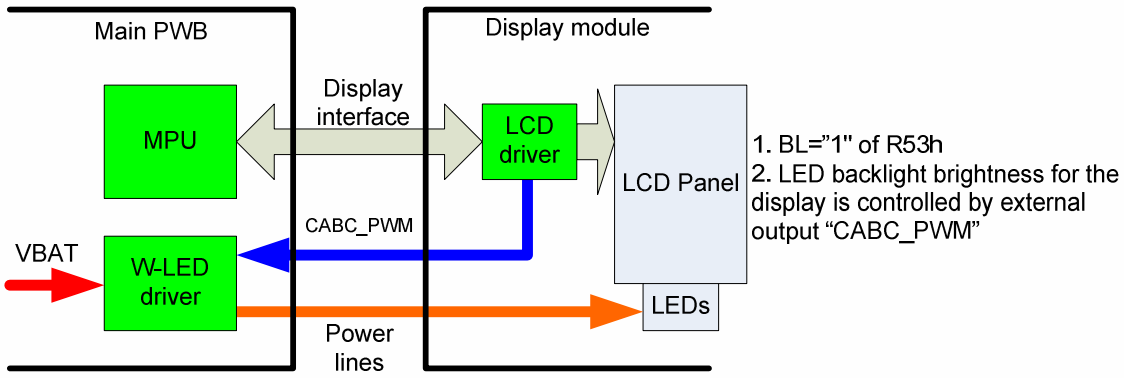


Figure 5.40: Module architecture I

- Architecture II

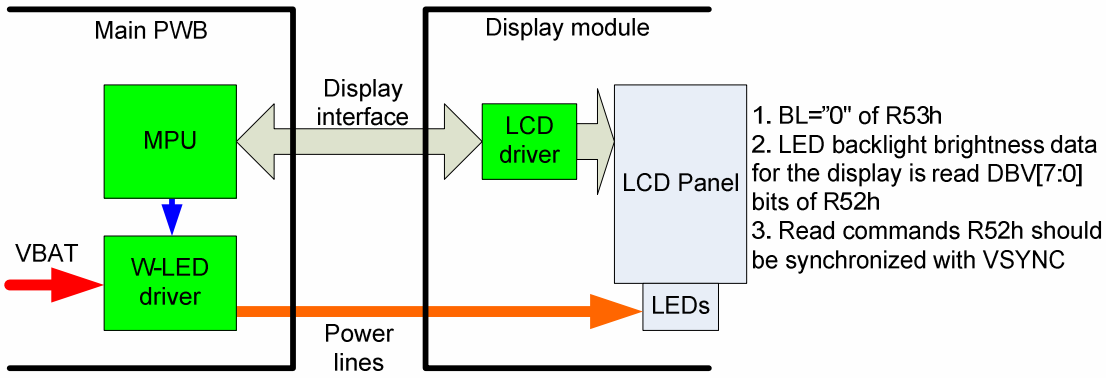


Figure 5.41: Module architecture II

5.13.2 CABC Block

There are DBG0~8[6:0] register bits in CABC block to define the “CABC gain”/ “CABC duty” table. Every DBGx[6:0] has 33 gain/duty value setting.

After one-frame display data content analysis, LSI will generate one CABC gain / CABC duty value calculated from DBG0~8[6:0] register bits setting (by using interpolated method) for display data generating and for backlight PWM pulse generating.

Please note that the CABC gain / CABC duty value calculated by the LSI is one of the 33 gain/duty value setting in DBGxx[6:0].

Please note that: Duty (valid level period (LED on) / one complete period) = 1/ gain.

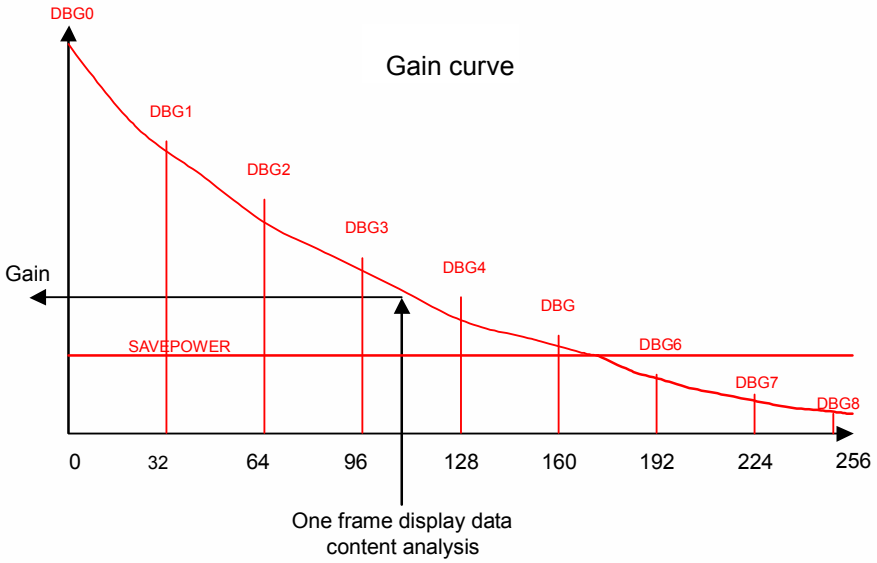


Figure 5.42: CABC Gain / CABC Duty Generation

For power saving of backlight module, there are **SAVEPOWER[6:0]** bits to define the “minimum gain”/ “maximum duty” of CABC block output. If the CABC gain/duty after one-frame display data contents analysis is smaller (gain)/larger(duty) than **SAVEPOWER[6:0]** bits setting, the CABC block will output CABC gain/duty equal to **SAVEPOWER[6:0]** and ignore the result of display data contents analysis.

5.13.3 Brightness Control Block

There is an external output signal from brightness block, CABC_PWM, to control the LED driver IC in order to control display brightness. The CABC_PWM output active polarity is defined by **INVPULS** bit of RCCh.

The CABC_PWM output period is controlled by **SEL_PWMCLK[2:0]** and **PWM_PERIOD[7:0]** bits of RE4h setting.

For ex: PWM CLK is 5.5MHz (period 180ns), SEL_PWMCLK=110(divide by 64),
and PWM_PERIOD=00h.
➔ CABC_PWM period = 180ns x 64 x (1x255) = 2.94 ms

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM duty is calculated as DBV[7:0]/255 x CABC duty(generated after one-frame display data content analysis).

For ex: CABC_PWM period = 2.94 ms, and DBV[7:0](R51h) = '228_{DEC}' and CABC duty is 74%. Then CABC_PWM duty = (228) / 255 x 74.42% ≡ 66.54%. Correspond to the CABC_PWM period = 2.94 ms, the high-level of CABC_PWM (high effective) = 1.96ms, and the low-level of CABC_PWM = 0.99ms.

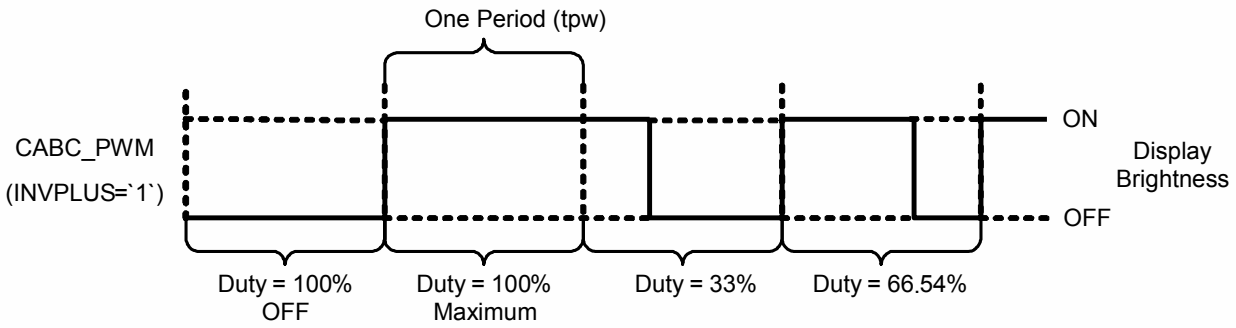


Figure 5.43: CABC_PWM Output Duty

Symbol	Parameter	Min.	Max.	Unit	Description
tpw	Pulse width	0.0333	8.33	ms	-

Note: The signal rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Table 5.19: CABC_PWM timing table

When Architecture II module is used (**BL**='0') with the example below, the CABC_PWM is always output low(**INVPULS='1'**) and the CABV[7:0](R52h) will be read a value as 169_{DEC}((169)/255≡ 66.27%).

5.13.4 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (**CMB[7:0]** bits of R5Eh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

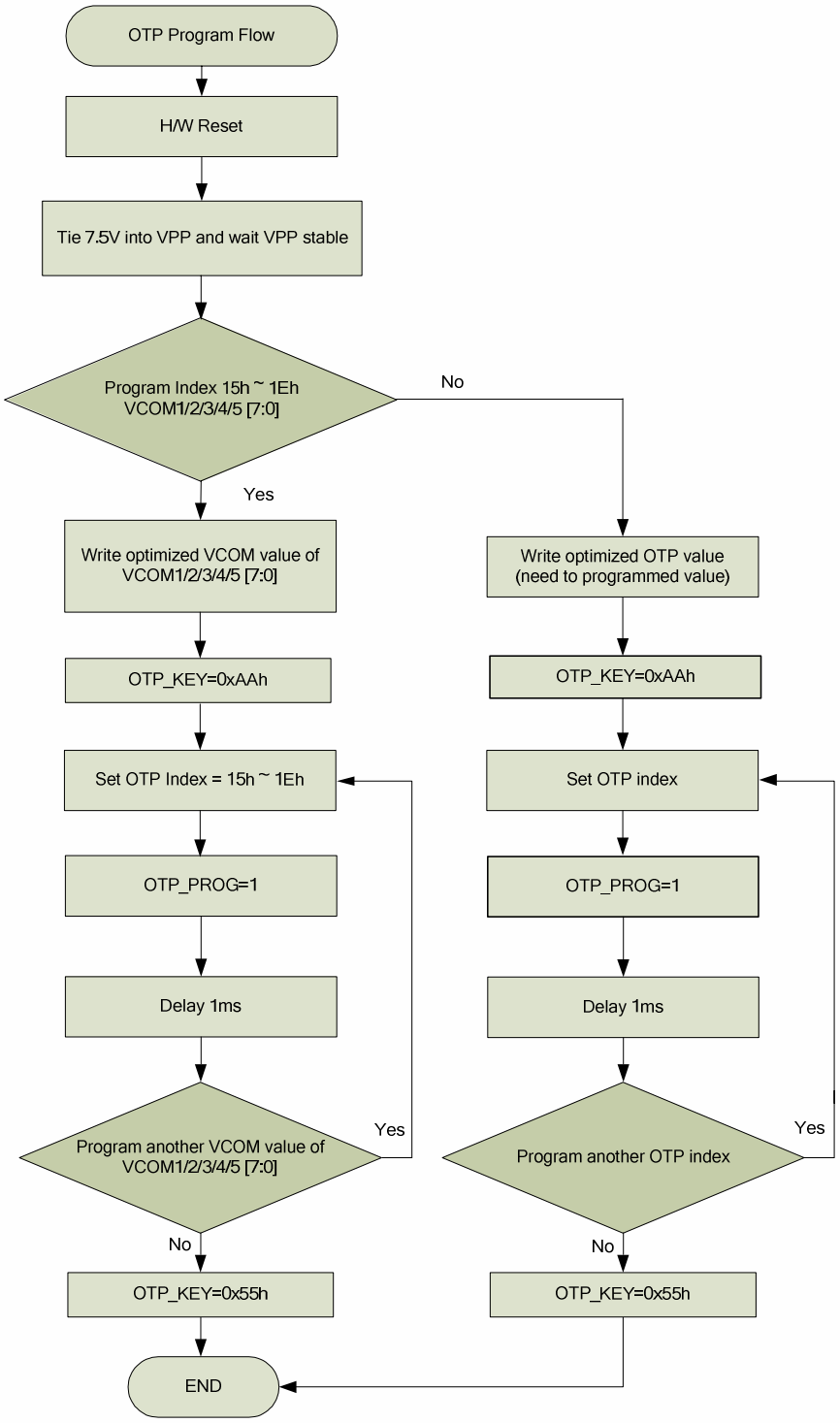
When display brightness is turned off (**BCTRL='0'** of R53h), CABC minimum brightness setting is ignored. "**CMB[7:0],** Read CABC minimum brightness (R5Fh) "always read the setting value of "**CMB[7:0],** Write CABC minimum brightness (R5Eh)"

5.14 OTP Programming

5.14.1 OTP Table

OTP_INDEX (HEX)	Ref. Command	B7	B6	B5	B4	B3	B2	B1	B0
0		VALID_ID1	VALID_ID2	VALID_ID3	VALID_ID4	VALID_ID5			
1	ID-1(E0)	ID11							
2		ID12							
3		ID13							
4		ID14							
5	ID-2(E0)	ID21							
6		ID22							
7		ID23							
8		ID24							
9	ID-3(E0)	ID31							
A		ID32							
B		ID33							
C		ID34							
D	ID-4(E0)	ID41							
E		ID42							
F		ID43							
10		ID44							
11	ID-5(E0)	ID51							
12		ID52							
13		ID53							
14		ID54							
15	VCOM1(D1)	VALID_VCM1	VCM1[6:0]						
16		-	-	-	VDV1[4:0]				
17	VCOM2(D1)	VALID_VCM2	VCM2[6:0]						
18		-	-	-	VDV2[4:0]				
19	VCOM3(D1)	VALID_VCM3	VCM3[6:0]						
1A		-	-	-	VDV3[4:0]				
1B	VCOM4(D1)	VALID_VCM4	VCM4[6:0]						
1C		-	-	-	VDV4[4:0]				
1D	VCOM5(D1)	VALID_VCM5	VCM5[6:0]						
1E		-	-	-	VDV5[4:0]				
30	SETOSC(C5)	VALID_OSC	-	-	-	-	UADJ[2:0]		
35	SETGAMMA(C8)	VALID_GAMMA	KP1[2:0]			–	KP0[2:0]		
36		-	KP3[2:0]			–	KP2[2:0]		
37		-	KP5[2:0]			–	KP4[2:0]		
38		-	RP1[2:0]			–	RP0[2:0]		
39		-	–	–	–	VRP0[3:0]			
3A		-	–	–	VRP1[4:0]				
3B		-	KN1[2:0]			–	KN0[2:0]		
3C		-	KN3[2:0]			–	KN2[2:0]		
3D		-	KN5[2:0]			–	KN4[2:0]		
3E		-	RN1[2:0]			–	RN0[2:0]		
3F		-	–	–	–	VRN0[3:0]			
40		-	–	–	VRN1[4:0]				

5.14.2 OTP Programming flow



OTP_KEY[7:0](8'h00)	Description	Note
AAh	Enter OTP Program mode	
55h	Leave OTP Program mode	
Other value	Invalid	1. If OTP is in OTP program mode, then keep OTP program mode. 2. If OTP is in non-OTP program mode, then keep non-OTP program mode. 3. OTP_KEY[7:0] can be ignored when user want to do OTP program.

Figure 5.44: OTP Programming Sequence

5.14.3 Programming sequence

<table>
<tr><th>Step</th><th>Operation</th></tr>
<tr><td>1</td><td>Power on and reset the module</td></tr>
<tr><td>2</td><td>Connect external power 7.5V to VPP pin</td></tr>
<tr><td>3</td><td>Wait 100ms for VPP stable</td></tr>
<tr><td>4</td><td>Write optimized value to related register
<table>
<tr><th>Command</th><th>Register</th><th>Description</th></tr>
<tr><td>ID1 (E0h)</td><td>ID1[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>ID2 (E0h)</td><td>ID2[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>ID3 (E0h)</td><td>ID3[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>ID4 (E0h)</td><td>ID4[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>ID5 (E0h)</td><td>ID5[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>VCOM1 (D1h)</td><td>VCM1[6:0], VDV1[4:0]</td><td>VCOMH and VCOM amplitude setting.</td></tr>
<tr><td>VCOM2 (D1h)</td><td>VCM2[6:0], VDV2[4:0]</td><td>VCOMH and VCOM amplitude setting.</td></tr>
<tr><td>VCOM3 (D1h)</td><td>VCM3[6:0], VDV3[4:0]</td><td>VCOMH and VCOM amplitude setting.</td></tr>
<tr><td>VCOM4 (D1h)</td><td>VCM4[6:0], VDV4[4:0]</td><td>VCOMH and VCOM amplitude setting.</td></tr>
<tr><td>VCOM5 (D1h)</td><td>VCM5[6:0], VDV5[4:0]</td><td>VCOMH and VCOM amplitude setting.</td></tr>
<tr><td>GAMMA(C8h)</td><td>Gamma value</td><td>Set gamma parameter</td></tr>
</table></td></tr>
<tr><td>5</td><td>Set OTP_KEY[7:0] (RE3h)=0xAAh to enter OTP program mode.</td></tr>
<tr><td>6</td><td>Specify OTP_index
<table>
<tr><th>OTP_index
(Write – For Program)</th><th>OTP_index
(Read – For get OTP value)</th><th>Parameter</th></tr>
<tr><td>0x00h</td><td>0x00h</td><td>VALID_ID1, VALID_ID2, VALID_ID3, VALID_ID4, VALID_ID5</td></tr>
<tr><td>0x01h</td><td>0x01h</td><td rowspan="4">ID1[7:0]</td></tr>
<tr><td>0x02h</td><td>0x02h</td></tr>
<tr><td>0x03h</td><td>0x03h</td></tr>
<tr><td>0x04h</td><td>0x04h</td></tr>
<tr><td>0x15h</td><td>0x15h</td><td rowspan="2">VALID_VCM1, VCM1[6:0], VDV1[4:0]</td></tr>
<tr><td>0x16h</td><td>0x16h</td></tr>
<tr><td>0x35h ~ 0x40h</td><td>0x35h ~ 0x40h</td><td>VALID_GAMMA, Gamma value</td></tr>
</table></td></tr>
<tr><td>7</td><td>Set OTP_Mask=0x00h, programming the entire bit of one parameter.</td></tr>
<tr><td>8</td><td>Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.</td></tr>
<tr><td>9</td><td>Wait 1 ms</td></tr>
<tr><td>10</td><td>Complete programming one parameter to OTP.
If continue to programming other parameter, return to step (5). Otherwise, set OTP_KEY[7:0]=0x55h to leave OTP program mode and power off the module and remove the external power on PVSS pin.</td></tr>
</table>

Note: Set OTP_KEY[7:0] can be ignored when user want to do OTP program.

5.14.4 OTP Read flow

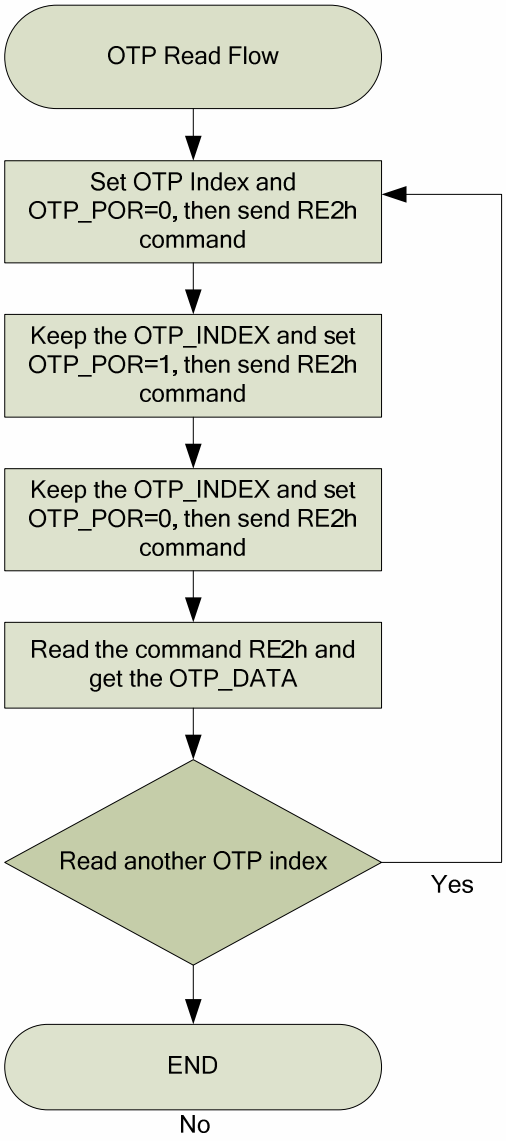
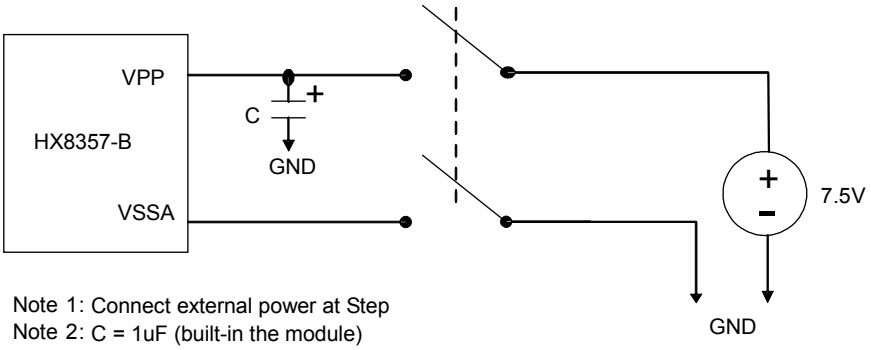


Figure 5.45: OTP Read Sequence

5.14.5 Programming circuitry



Note 1: Connect external power at Step
Note 2: C = 1uF (built-in the module)

6. Command

6.1 Standard Command List

(Hex)	Operation Code	DCX	WRX	RDX	D17 ~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Display mod Implementation Requirement	
															DM[1:0]	
															00,01,10	11
00	NOP	0	↑	1	-	0	0	0	0	0	0	0	0	No Operation	Y	Y
01	SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	Software reset	Y	Y
06	RDRED	0	↑	1	-	0	0	0	0	0	1	1	0	Read Red	N	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	R7	R6	R5	R4	R3	R2	R1	R0	-		
07	RDGREN	0	↑	1	-	0	0	0	0	0	1	1	1	Read Green	N	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	G7	G6	G5	G4	G3	G2	G1	G0	-		
08	RDBLUE	0	↑	1	-	0	0	0	0	1	0	0	0	Read Blue	N	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	B7	B6	B5	B4	B3	B2	B1	B0	-		
0A	RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	Read Display Power Mode	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	D[7:0]								-		
0B	RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	Read Display MADCTL	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	D[7:0]								-		
0C	RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	Read Display Pixel Format	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	x	D6	D5	D4	x	D2	D1	D0	-		
0D	RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	Read Display Image Mode	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	D[7:0]								-		
0E	RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	Read Display Signal Mode	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	D[7:0]								-		
0F	RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	Read Display Self-Diagnostic Result	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	D[7:0]								-		
10	SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	Sleep in and charge-pump off	Y	Y
11	SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	Sleep out and charge-pump on	Y	Y
12	PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	Partial Mode On	Y	N
13	NORON	0	↑	1	-	0	0	0	1	0	0	1	1	Normal Display Mode On	Y	N

(Hex)	Operation Code	DCX	WRX	RDX	D17 ~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Display mod Implementation Requirement	
															DM[1:0]	
															00,01,10	11
20	INVOFF	0	↑	1	-	0	0	1	0	0	0	0	1	Display Inversion off	Y	Y
21	INVON	0	↑	1	-	0	0	1	0	0	0	1	0	Display Inversion on	Y	Y
28	DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	Display off	Y	Y
29	DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	Display on	Y	Y
2A	CASET	0	↑	1	-	0	0	1	0	1	0	1	0	Column Address Set	Y	N
		1	↑	1	-	SC[15:8] (8'b0)								Column address start		
		1	↑	1	-	SC[7:0] (8'b0)								Column address start		
		1	↑	1	-	EC[15:8] (8'b0000_0001)								Column address end		
		1	↑	1	-	EC[7:0] (8'b0011_1111)								Column address end		
2B	PASET	0	↑	1	-	0	0	1	0	1	0	1	1	Row address set	Y	N
		1	↑	1	-	SP[15:8] (8'b0)								Row address start		
		1	↑	1	-	SP[7:0] (8'b0)								Row address start		
		1	↑	1	-	EP[15:8] (8'b0000_0001)								Row address end		
		1	↑	1	-	EP[7:0] (8'b1101_1111)								Row address end		
2C	RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	Memory write	Y	N
		1	↑	1	-	Write data								-		
2E	RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	Memory read	Y	N
		1	↑	1	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	Read data								-		
30	PLTAR	0	↑	1	-	0	0	1	1	0	0	0	0	Partial address set	Y	N
		1	↑	1	-	SR[15:8] (8'b0)								Start row		
		1	↑	1	-	SR[7:0] (8'b0)								Start row		
		1	↑	1	-	ER[15:8] (8'b0000_0001)								End row		
		1	↑	1	-	ER[7:0] (8'b1101_1111)								End row		
33	VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	Vertical Scrolling Definition)	Y	N
		1	↑	1	-	TFA[15:8] (8'b0)								Top Fixed Area		
		1	↑	1	-	TFA[7:0] (8'b0)								Top Fixed Area		
		1	↑	1	-	VSA[15:8] (8'b0000_0001)								Height of the Vertical Scrolling Area		
		1	↑	1	-	VSA[7:0] (8'b1101_1111)								Height of the Vertical Scrolling Area		
		1	↑	1	-	BFA[15:8] (8'b0)								Bottom Fixed Area		
		1	↑	1	-	BFA[7:0] (8'b0)								Bottom Fixed Area		

(Hex)	Operation Code	DCX	WRX	RDX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Display mod Implementation Requirement	
															DM[1:0]	
															00,01,10	11
34	TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	Tearing Effect line off	Y	N
35	TEON	0	↑	1	-	0	0	1	1	0	1	0	1	Tearing Effect Line ON	Y	N
		0	↑	1	-	-	-	-	-	-	-	-	TEMODE	-		
36	MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	Memory Access Control)	Y	Y
		1	↑	1	-	MY (0)	MX (0)	MV (0)	ML (0)	BGR (0)	0	SS (0)	GS (0)	-		
37	VSCRSADD	0	↑	1	-	0	0	1	1	0	1	1	1	Vertical Scrolling Start Address	Y	N
		1	↑	1	-	VSP[15:8] (8'b0)								-		
		1	↑	1	-	VSP[7:0] (8'b0)								-		
38	IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	Idle mode off	Y	N
39	IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	Idle mode on	Y	N
3A	COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	Interface Pixel Format	Y	Y
		1	↑	1	-	0	D[6:4]			0	D[2:0]			-		
3C	RAMWRCON	0	↑	1	-	0	0	1	1	1	1	0	0	Memory write	Y	N
		1	↑	1	-	Write data								-		
3E	RAMRDCON	0	↑	1	-	0	0	1	1	1	1	1	0	Memory read	Y	N
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	Read data								-		
44	TESL	0	↑	1	-	0	1	0	0	0	1	0	0	Set tear scan line	Y	N
		1	↑	1	-	TELINE[15:8] (8'b0)								-		
		1	↑	1	-	TELINE[7:0] (8'b0)								-		
45	GETSL	0	↑	1	-	0	1	0	0	0	1	0	1	Get the current scan line.	Y	N
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	SL[15:8]								-		
		1	1	↑	-	SL[7:0]								-		
A1	Read_DDB_ start	0	↑	1	-	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	ID1								The five bytes always output		
		1	1	↑	-	ID2										
		1	1	↑	-	ID3										
		1	1	↑	-	ID4										
		1	1	↑	-	8'hFF										

CABC command list

(Hex)	Operation Code	DCX	WRX	RDX	D17~ D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Display mod Implementation Requirement	
															DM[1:0]	
															00,01,10	11
51	WRDISBV	0	↑	1	-	-	-	-	-	-	-	-	-	Write Display Brightness Value	Y	Y
		0	↑	1	-	DBV[7:0] (8'b0)								-		
52	RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	Read Display Brightness Value	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	DBV[7:0]								-		
53	WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	Write Control Display	Y	Y
		1	↑	1	-	-	-	BCTRL (0)	-	DD (0)	BL (0)	-	-	-		
54	RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	Read Control Value Display	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0	-		
55	WRCABC	0	↑	1	-	0	1	0	1	0	1	0	1	-	Y	Y
		1	↑	1	-	-	-	-	-	-	-	CABC[1:0](00)		Write Adaptive Brightness Control		
56	RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	Read Content Adaptive Brightness Control	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	-	-	-	-	-	-	CABC[1:0]		-		
5E	WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	Write CABC minimum brightness	Y	Y
		1	↑	1	-	CMB[7:0]								-		
5F	RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	Read CABC minimum brightness	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	CMB[7:0]								-		
68	RDABCSDR	0	↑	1	-	0	1	1	0	1	0	0	0	Read Automatic Brightness Control Self-Diagnostic Result	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	-	-	-	-	-	-	-	-	-		

User Define Command List Table

(Hex)	Operation Code	DCX	WRX	RDX	D17 ~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
B0	SETEXTC	0	↑	1	-	1	0	1	1	0	0	0	0	Set extended command
		1	↑	1	-	0	0	0	0	0	0	EXTC[1:0]		-
B1	SETDPSTB	0	↑	1	-	1	0	1	1	0	0	0	1	Set Deep standby mode
		1	↑	1	-	0	0	0	0	0	0	0	DP_STB	-
B3	SETGRAM	0	↑	1	-	1	0	1	1	0	0	1	1	Set GRAM access and Interface
		1	↑	1	-	0	0	0	0	0	0	0	0	-
		1	↑	1	-	0	0	0	0	0	TEI[2:0]			-
		1	↑	1	-	0	0	0	0	DENC[3:0]				-
		1	↑	1	-	0	0	EPF[1:0]		0	0	0	DFM	-
B4	SETDISPLAY	0	↑	1	-	1	0	1	1	0	1	0	0	Set Display mode and GRAM write mode
		1	↑	1	-	0	0	0	RM	0	0	DM[1:0]		-
BF	GETDEVICEID	0	↑	1	-	1	0	1	1	1	1	1	1	Read Device ID
		1	1	↑	-	MIPI Alliance code								0x01
		1	1	↑	-	MIPI Alliance code								0x62
		1	1	↑	-	Device ID								0x83
		1	1	↑	-	Device ID								0x57
		1	1	↑	-	1	1	1	1	1	1	1	1	0xFF
C0	SETPANEL	0	↑	1	-	1	1	0	0	0	0	0	0	Set Panel Driving
		1	↑	1	-	0	0	0	REV	SM	GS	0	0	-
		1	↑	1	-	0	0	NL[5:0]						-
		1	↑	1	-	0	SCN[6:0]							-
		1	↑	1	-	0	0	0	NDL	0	PTS[2:0]			-
		1	↑	1	-	0	0	0	PTG	ISC[3:0]				-
C1	SETNORTIME	0	↑	1	-	0	0	0	0	1	0	1	1	Set display timing for Normal mode
		1	↑	1	-	0	0	0	BC0	0	0	DIV0[1:0]		-
		1	↑	1		0	0	0	RTN0[4:0]					-
		1	↑	1	-	FP0[3:0]				BF0[3:0]				-
C2	SETPARTIME	0	↑	1	-	1	1	0	0	0	0	1	0	Set display timing for Partial mode
		1	↑	1	-	0	0	0	BC1	0	0	DIV1[1:0]		-
		1	↑	1		0	0	0	RTN1[4:0]					-
		1	↑	1	-	FP1[3:0]				BF1[3:0]				-
C3	SETIDLTIME	0	↑	1	-	1	1	0	0	0	0	1	1	Set display timing for Idle mode
		1	↑	1	-	0	0	0	BC2	0	0	DIV2[1:0]		-
		1	↑	1		0	0	0	RTN2[4:0]					-
		1	↑	1	-	FP2[3:0]				BF2[3:0]				-
C5	SETOSC	0	↑	1	-	1	1	0	0	0	1	0	1	Set display frame
		1	↑	1	-	0	0	0	0	UADJ[3:0]				-
C6	SETRGB	0	↑	1	-	1	1	0	0	0	0	0	0	Set RGB Interface
		1	↑	1	-	SDA_EN	0	0	VPL	HPL	0	EPL	DPL	-

(Hex)	Operation Code	DCX	WRX	RDX	D17 ~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
C8	SETGAMMA	0	↑	1	-	1	1	0	0	1	0	0	0	Set Gamma curve
		1	↑	1	-	0	KP12	KP11	KP10	0	KP02	KP01	KP00	-
		1	↑	1	-	0	KP32	KP31	KP30	0	KP22	KP21	KP20	-
		1	↑	1	-	0	KP52	KP51	KP50	0	KP42	KP41	KP40	-
		1	↑	1	-	0	RP12	RP11	RP10	0	RP02	RP01	RP00	-
		1	↑	1	-	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00	-
		1	↑	1	-	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	-
		1	↑	1	-	0	KN12	KN11	KN10	0	KN02	KN01	KN00	-
		1	↑	1	-	0	KN32	KN31	KN30	0	KN22	KN21	KN20	-
		1	↑	1	-	0	KN52	KN51	KN50	0	KN42	KN41	KN40	-
		1	↑	1	-	0	RN12	RN11	RN10	0	RN02	RN01	RN00	-
		1	↑	1	-	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00	-
		1	↑	1	-	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	-
D0	SETPOWER	0	↑	1	-	1	1	0	1	0	0	0	0	Set Power
		1	↑	1	-	0	AP[2:0]			0	VC[2:0]			-
		1	↑	1	-	0	PON	0	0	0	BT[2:0]			-
		1	↑	1	-	0	0	0	0	VRH[3:0]				-
D1	SETVCOM	0	↑	1	-	1	1	0	1	0	0	0	1	Set VCOM
		1	↑	1	-	0	VCM[6:0]							-
		1	↑	1	-	0	0	0	VDV[4:0]					-
D2	SETNORPOW	0	↑	1	-	1	1	0	1	0	0	1	0	Set Power of Normal mode
		1	↑	1	-	0	0	0	0	0	SAP0[2:0]			-
		1	↑	1	-	0	DC10[2:0]				DC00[2:0]			-
D3	SETPARPOW	0	↑	1	-	1	1	0	1	0	0	1	1	Set Power of Partial mode
		1	↑	1	-	0	0	0	0	0	SAP1[2:0]			-
		1	↑	1	-	0	DC11[2:0]				DC01[2:0]			-
D4	SETIDLPOW	0	↑	1	-	1	1	0	1	0	1	0	0	Set Power of Idle mode
		1	↑	1	-	0	0	0	0	0	SAP2[2:0]			-
		1	↑	1	-	0	DC12[2:0]				DC02[2:0]			-
E0	SETID	0	↑	1	-	1	1	1	0	0	0	0	0	Set ID
		1	↑	1	-	ID1								-
		1	↑	1	-	ID2								-
		1	↑	1	-	ID3								-
		1	↑	1	-	ID4								-
E2	SETOTP	0	↑	1	-	1	1	1	0	0	0	1	0	Set OTP
		1	↑	1	-	OTP_MASK[7:0]								-
		1	↑	1	-	OTP_INDEX[7:0]								-
		1	↑	1	-	OTP_LOAD_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM[1:0]		VPP_SEL	OTP_PROG	-
		1	↑	1	-	OTP_DATA[7:0]								-
E3	SETOTPKEY	0	↑	1	-	1	1	1	0	0	0	1	1	Set OTP Key
		1	↑	1	-	OTP_KEY[7:0]								-
E4	SETCABC	0	↑	1	-	1	1	1	0	0	1	0	0	Set CABC Control
		1	↑	1	-	0	SEL_PWMCLK[2:0]			SEL_GAIN [1:0]		INVPULS (1)	SEL_BLDUTY (1)	-
		1	↑	1	-	PWM_PERIOD[7:0]								-
		1	↑	1	-	0	DIM_FRAME[6:0]							-

(Hex)	Operation Code	DCX	WRX	RDX	D17 ~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
E9	SETPANEL	0	↑	1	-	1	1	1	0	1	0	0	1	Set Panel related register
		1	↑	1	-	0	0	0	0	SS_PANEL	0	0	BGR_PANEL	-
EE	SETEQ	0	↑	1	-	1	1	1	0	1	1	1	0	Set EQ function
		1	↑	1	-	EQVCI_M1[7:0]								-
		1	↑	1	-	EQGND_M1[7:0]								-
		1	↑	1	-	EQVCI_M0[7:0]								-
		1	↑	1	-	EQGND_M0[7:0]								-

6.2 Command Description

6.2.1 NOP

00H	NOP (No Operation)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	0	0	0	0	0	0	00
Parameter	No Parameter												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart

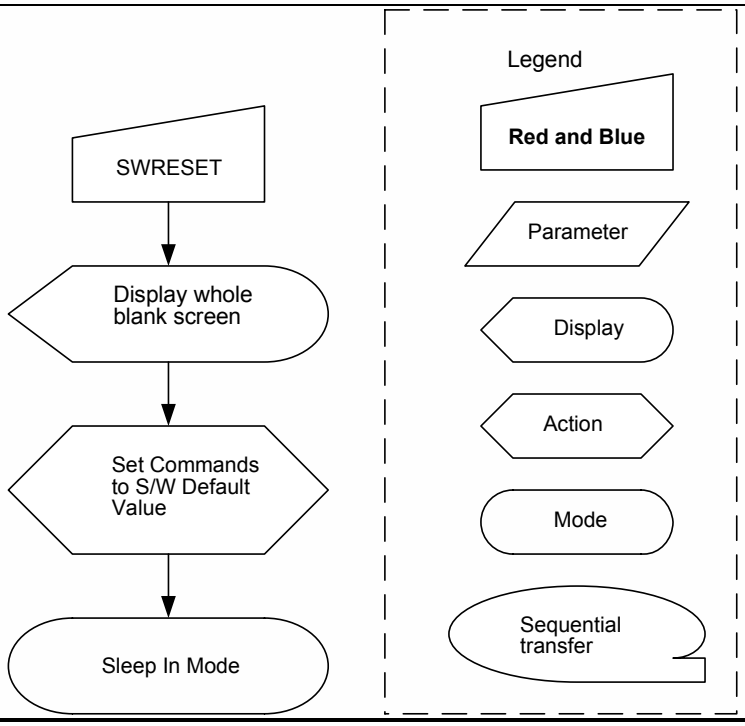
6.2.2 Software Reset (01h)

01 H	SWRESET (Software Reset)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	0	0	0	0	0	0	1	01
Parameter	No Parameter												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command It will be necessary to wait 5msec before sending new command following software reset.												
Restriction	The display module loads all display suppliers' factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default	Status	Default Value
	Power On Sequence	N/A
	S/W Reset	N/A
	H/W Reset	N/A

Flow Chart



6.2.3 Get_red_channel (06h)

06 H	RDRED (Read Red Colour)												
	DCX	**NRD**	**NWR**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	0	0	0	1	1	0	06
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	R7	R6	R5	R4	R3	R2	R1	R0	xx
Description	The first parameter is telling red colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'.												
Restriction	The command is active when DM[1:0]="11"												

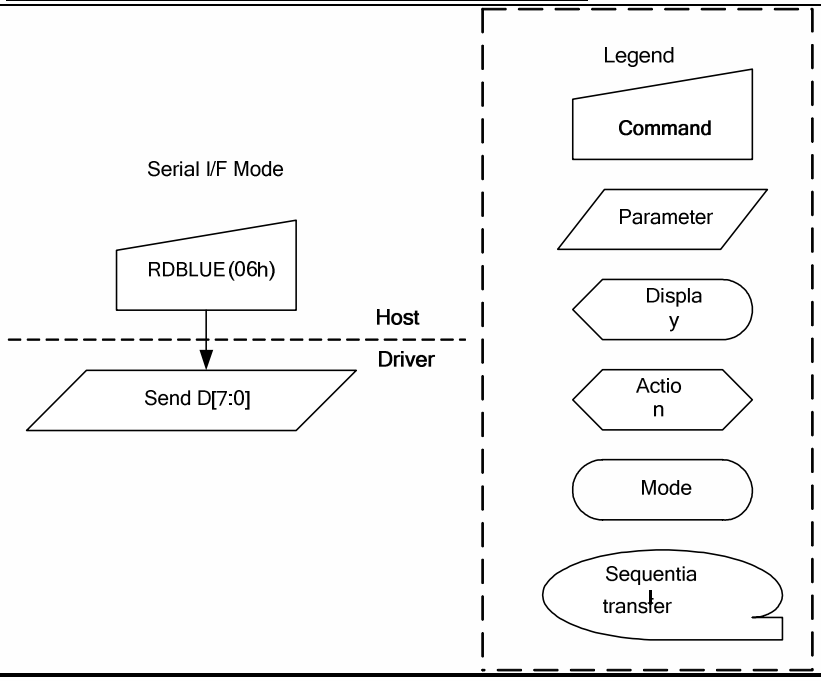
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.4 Get_green_channel (07h)

07 H	RDGREEN (Read Green Colour)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	0	0	0	1	1	1	01
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	G7	G6	G5	G4	G3	G2	G1	G0	xx
Description	The first parameter is telling green colour value of the first pixel of the frame when there is used DPI I/F. 16 and 18 bit formats: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'.												
Restriction	The command is active when DM[1:0]="11"												

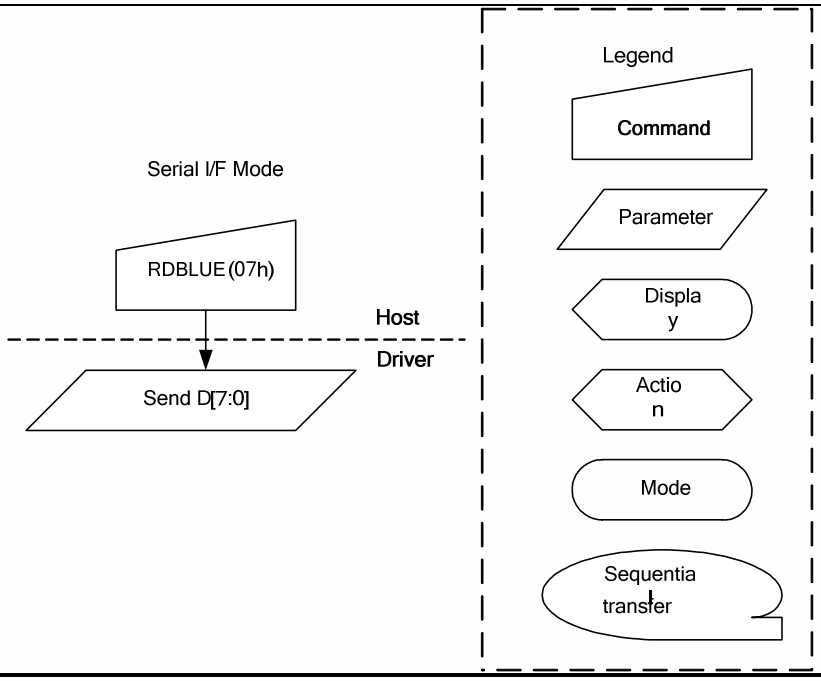
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

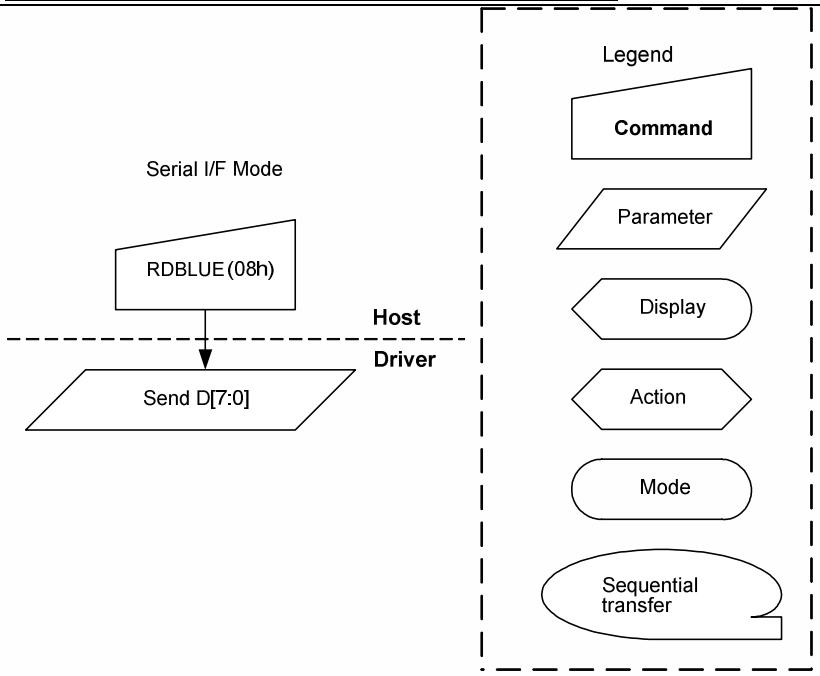
Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



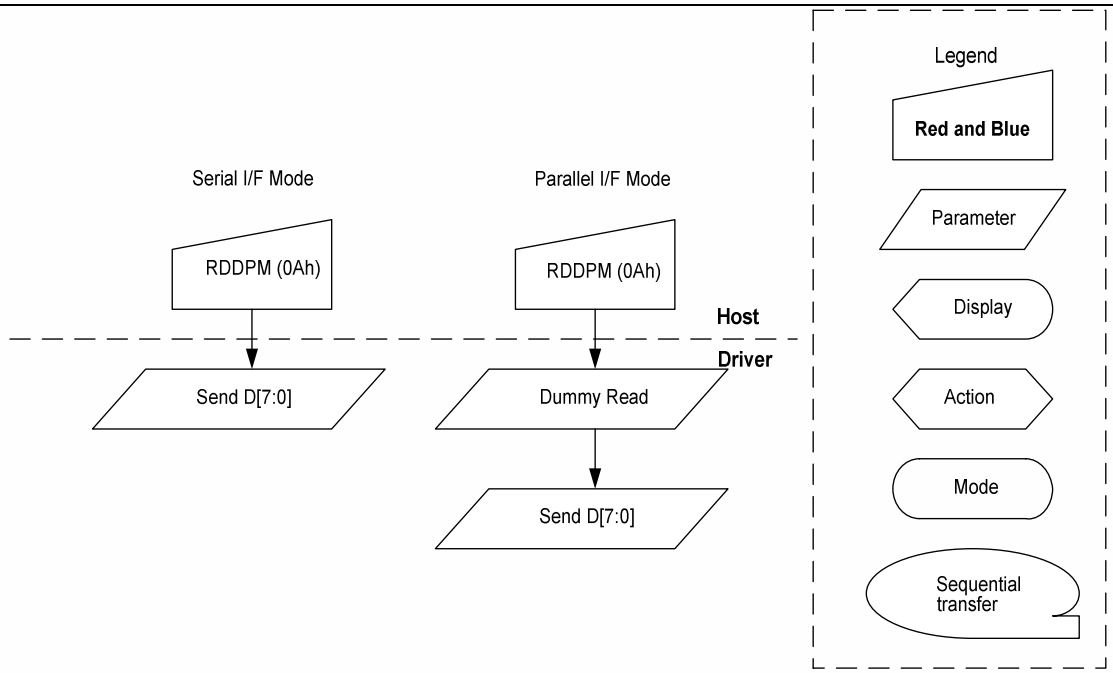
6.2.5 Get_blue_channel (08h)

08 H	RDBLUE (Read Blue Colour)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	0	0	1	0	0	0	08
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	B7	B6	B5	B4	B3	B2	B1	B0	xx
Description	The first parameter is telling blue colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'.												
Restriction	The command is active when DM[1:0]="11"												
Register Availability	Status: Availability Sleep Out: Yes Sleep In: Yes												
Default	Status: Default Value Power On Sequence: 00h S/W Reset: 00h H/W Reset: 00h												
Flow Chart													

6.2.6 Get_power_mode (0Ah)

<table>
<tr><td>0A H</td><td colspan="13">RDDPM (Read Display Power Mode)</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17~D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Dummy read</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><td>Bit</td><td>Description</td><td>Comment</td></tr>
<tr><td>D7</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D6</td><td>Idle Mode On/Off</td><td></td></tr>
<tr><td>D5</td><td>Partial Mode On/Off</td><td></td></tr>
<tr><td>D4</td><td>Sleep In/Out</td><td></td></tr>
<tr><td>D3</td><td>Display Normal Mode On/Off</td><td></td></tr>
<tr><td>D2</td><td>Display On/Off</td><td></td></tr>
<tr><td>D1</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
</table>
Bits D7 for future use and are set to ‘0’.
Bit D6 – Idle Mode On/Off
‘0’ = Idle Mode Off.
‘1’ = Idle Mode On.
Bit D5 – Partial Mode On/Off
‘0’ = Partial Mode Off.
‘1’ = Partial Mode On.
Bit D4 – Sleep In/Out
‘0’ = Sleep In Mode.
‘1’ = Sleep Out Mode.
Bit D3 – Display Normal Mode On/Off
‘0’ = Display Normal Mode Off.
‘1’ = Display Normal Mode On.
Bit D2 – Display On/Off
‘0’ = Display is Off.
‘1’ = Display is On.</td></tr>
<tr><td>Restrictions</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>08HEX</td></tr>
<tr><td>S/W Reset</td><td>08HEX</td></tr>
<tr><td>H/W Reset</td><td>08HEX</td></tr>
</table></td></tr>
</table>

Flow Chart



6.2.7 Read Display MADCTL (0Bh)

0B H	RDDMADCTL (Read Display MADCTL)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	0	1	1	0B
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	D7	D6	D5	D4	D3	0	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	
D6	Column Address Order	
D5	Page/Column Order	
D4	Line Address Order	
D3	RGB/BGR Order	
D2	Reserved	Set to '0'
D1	Flip Horizontal	
D0	Flip Vertical	

Bit D7 – Page Address Order
'0' = Top to Bottom (When MADCTL B7='0').
'1' = Bottom to Top (When MADCTL B7='1').

Bit D6 – Column Address Order
'0' = Left to Right (When MADCTL B6='0').
'1' = Right to Left (When MADCTL B6='1').

Bit D5 – Page/Column Order
'0' = Normal (When MADCTL B5='0').
'1' = Rotation (When MADCTL B5='1').
Note: For Bits D7 to D5, also refer to Section 5.1.3 MCU to memory write/read direction.

Bit D4 – Line Address Order
'0' = LCD Refresh Top to Bottom (When MADCTL B4='0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4='1').

Bit D3 – RGB/BGR Order
'0' = RGB (When MADCTL B3='0').
'1' = BGR (When MADCTL B3='1').
Note: For Bits D4 and D3 also refer to 9.2.29 Set_address_mode (36h).

Bit D2 is for future use and is set to '0'.

Bit D1 – Flip Horizontal
This bit flips the image shown on the display device left to right. No change is made to the frame memory.
'0' = Normal
'1' = Flipped

Bit D0 – Flip Vertical
This bit flips the image shown on the display device top to bottom. No change is made to the frame memory.
'0' = Normal

Restrictions

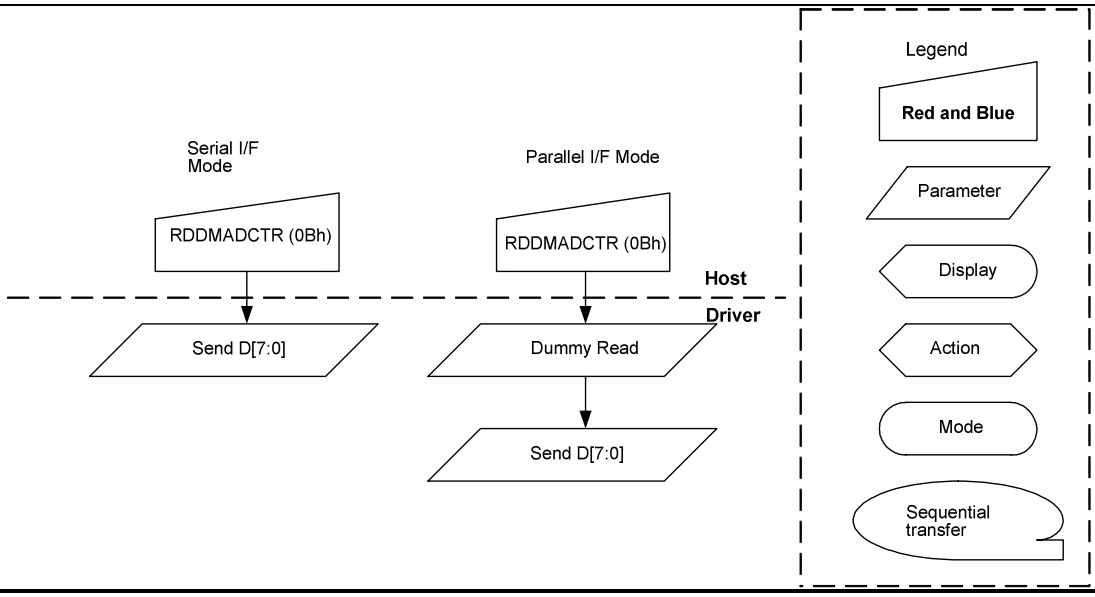
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00HEX
S/W Reset	No Change

Flow Chart



6.2.8 Get_pixel_format (0Ch)

0C H	RDDCOLMOD (Read Display COLMOD)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	0	0	1	1	0	0	0C
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1		-	D6	D5	D4	-	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Reserved	Set to '0'
D6	DPI Interface Pixel format	
D5		
D4		
D3	Reserved	Set to '0'
D2	DBI Interface Pixel format	
D1		
D0		

Bits D6, D5, D4 – DPI Interface Colour Pixel Format Definition
Bits D2, D1, D0 – DBI Interface Colour Pixel Format Definition.
See section "6.2.33 Set_pixel_format (3Ah)".

Interface Colour Format	D6/D2	D5/D1	D4/D0
Not Defined	0	0	0
3 bit/pixel	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
Not Defined	1	1	1

If a particular interface, either DBI or DPI, is not used then the corresponding bits in the

Restrictions

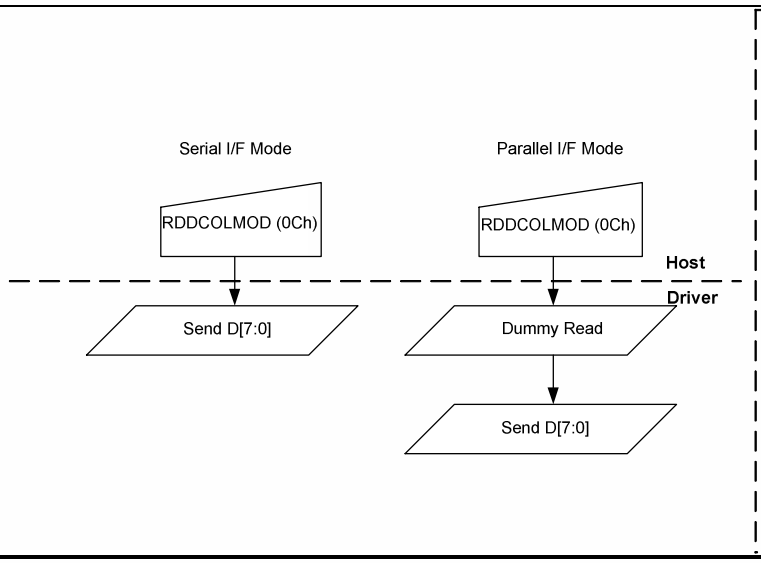
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	66HEX
S/W Reset	66HEX

Flow Chart



6.2.9 Get_display_mode (0Dh)

0D H	RDDIM (Read Display Image Mode)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	0	1	0D
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	D7	0	D5	0	0	D2	D1	D0	xx
Description	This command indicates the current status of the display as described in the table below: Bit D7 – Vertical Scrolling On/Off '0' = Vertical Scrolling is Off. '1' = Vertical Scrolling is On. Bit D6 – Horizontal Scrolling Status This bit is not applicable for this project, so it is set to '0' Bit D5 – Inversion On/Off '0' = Inversion is Off. '1' = Inversion is On. Bit D4 – Reserved Bit D3 – Reserved Bits D2, D1, D0 – Gamma Curve Selection These bit are not applicable for this project, so they are set to '000'												
Restrictions													

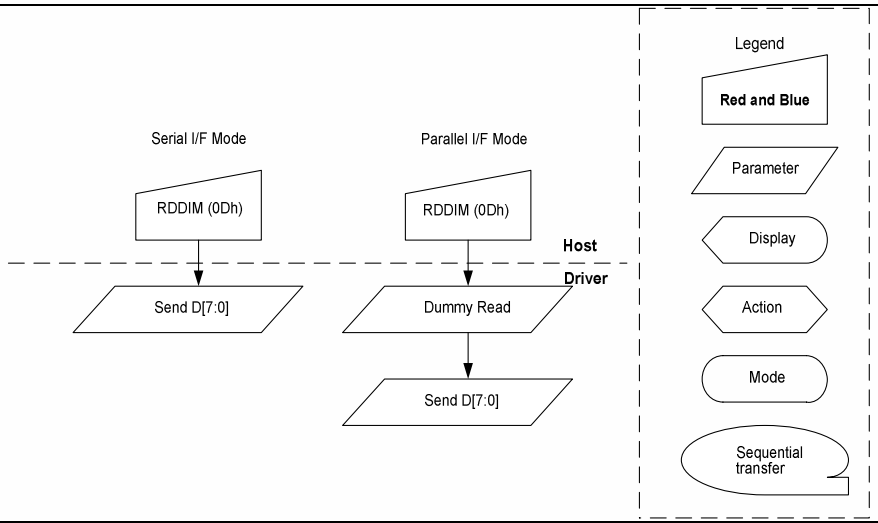
Register Availability

status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00HEX
S/W Reset	00HEX
H/W Reset	00HEX

Flow Chart



6.2.10 Get_signal_mode (0Eh)

0E H	RDDSM (Read Display Signal Mode)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	0	0	1	1	1	0	0E
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	D7	D6	0	0	0	0	0	0	xx
Description	This command indicates the current status of the display as described in the table below: Bit D7 – Tearing Effect Line On/Off '0' = Tearing Effect Line Off. '1' = Tearing Effect On. Bit D6 – Tearing Effect Line Output Mode, see section 7.1 for mode definitions. '0' = Mode 1. '1' = Mode 2. D5 are D0 – are for future use and are set to '0'.												
Restrictions													

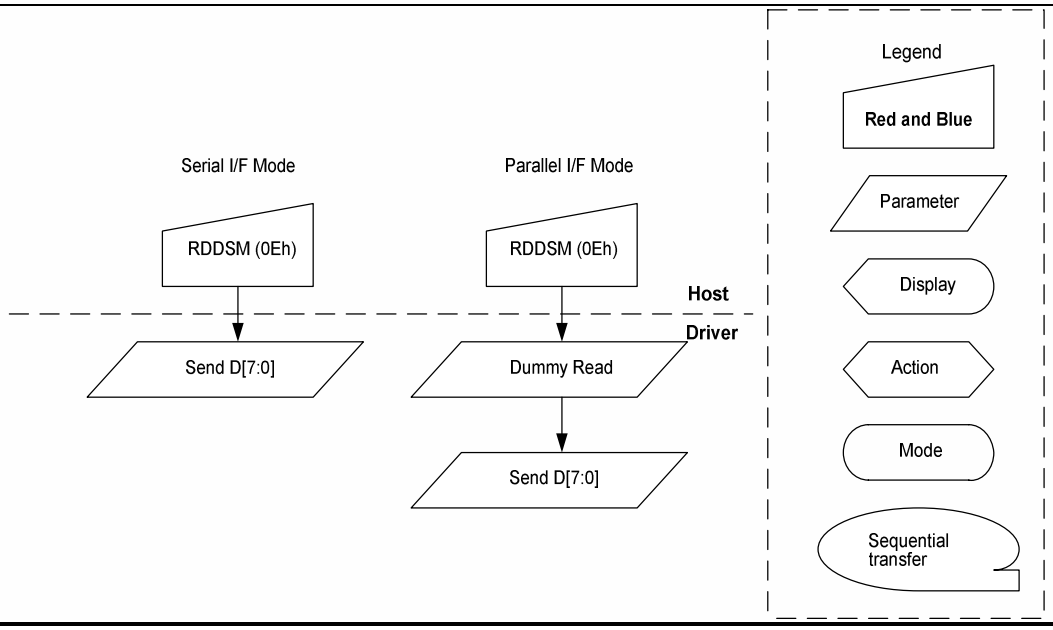
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default Value
Power On Sequence	00HEX
S/W Reset	00HEX

Flow Chart



6.2.11 Get_diagnostic_result (0Fh)

0F H	RDDSDR (Read Display Self-Diagnostic Result)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	0	0	1	1	1	1	0F
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	1	1	-	D7	D6	D5	D4	0	0	0	0	xx

Description

The display module returns the self-diagnostic results following a Sleep Out command. See section 7.10 for a description of the status results.
Bit D7 – Register Loading Detection
Bit D6 – Functionality Detection
Bit D5 – Chip Attachment Detection
Set to '0' if feature unimplemented.
Bit D4 – Display Glass Break Detection
Set to '0' if feature unimplemented.
Bits D[3:0] – Reserved
Set to '0'.

Restrictions

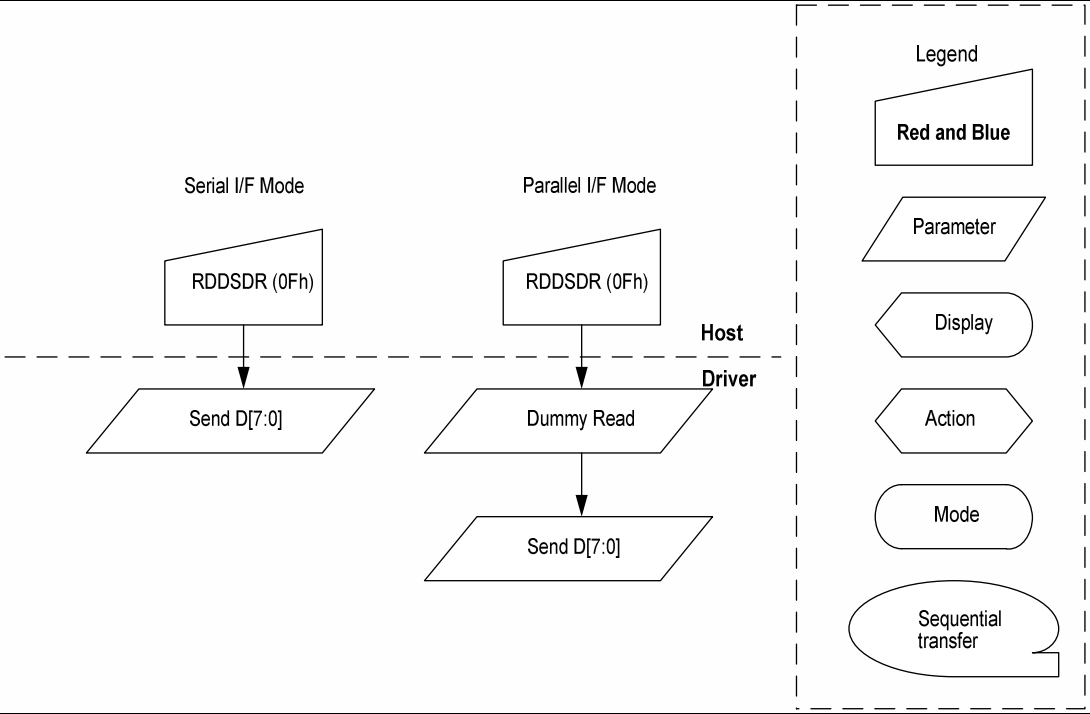
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

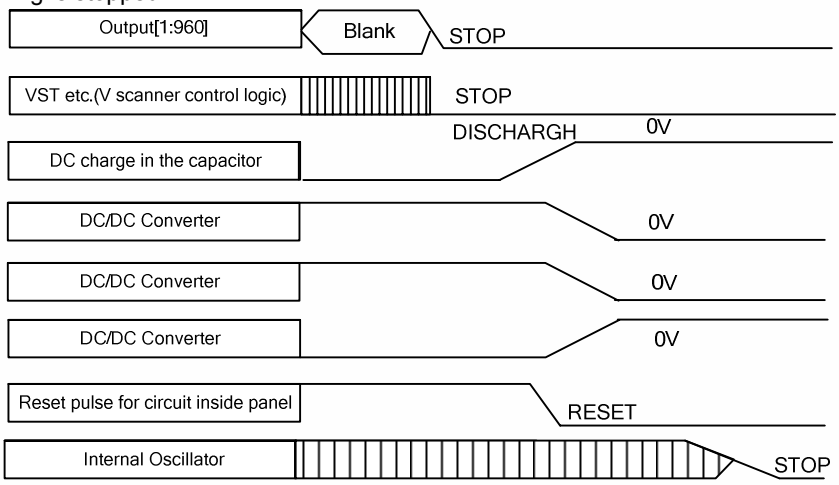
Default

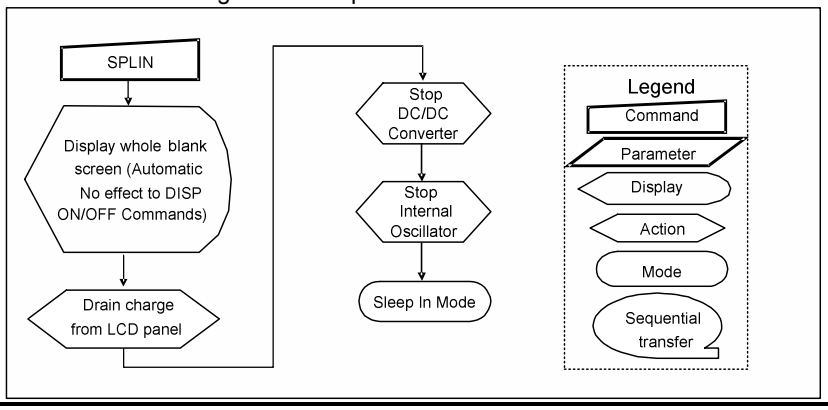
Status	Default Value
Power On Sequence	00HEX
S/W Reset	00HEX
H/W Reset	00HEX

Flow Chart



6.2.12 Enter_sleep_mode (10h)

<table>
<tr><td>10 H</td><td colspan="13">SLPIN (Sleep In)</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17~D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.
 

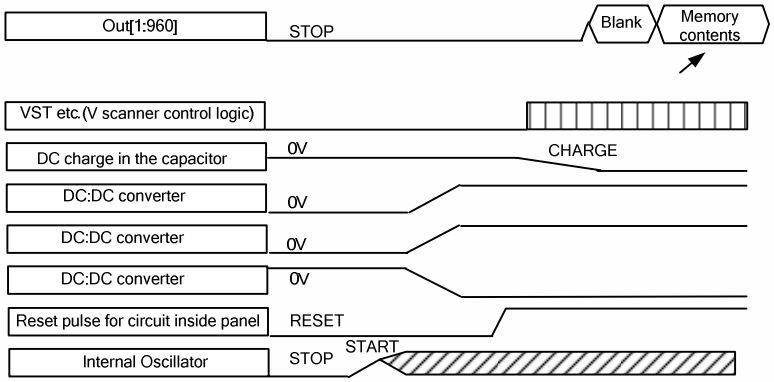
MCU interface and memory are still working and the memory keeps its contents.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>Sleep in mode</td></tr><tr><td>S/W Reset</td><td>Sleep in mode</td></tr><tr><td>H/W Reset</td><td>Sleep in mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">It takes 120msec to get into Sleep In mode after SLPIN command issued.
 
</td></tr>
</table>

6.2.13 Exit_sleep_omde (11h)

11 H	SLPOUT (Sleep Out)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	0	1	11
Parameter	No Parameter												

Description

This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.



Restriction

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.
The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Register Availability

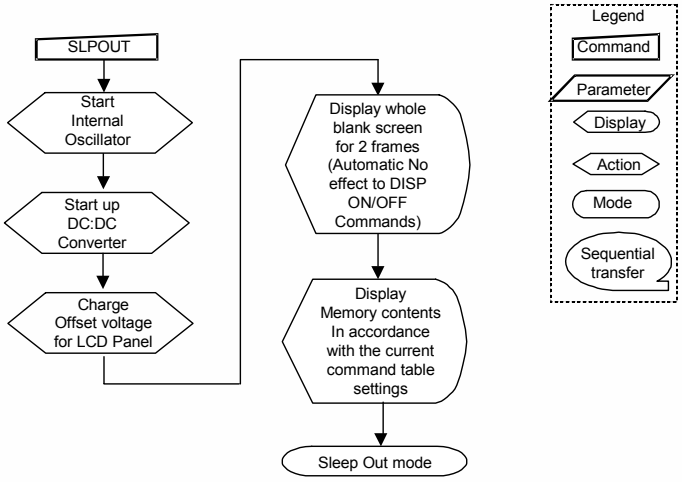
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart

It takes 120msec to become Sleep Out mode after SLPOUT command issued.



6.2.14 Enter_partial_mode (12h)

12 H	PTLON (Partial Mode On)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	0	1	0	0	1	0	12
Parameter	No Parameter												
Description	This command turns on partial mode The partial mode window is described by the “Set_partial_area” command (30H). To leave Partial mode, the “Enter_norma_mode” command (13H) should be written.												
Restrictions	This command has no effect when Partial mode is active.												
Register Availability	Status	Availability											
	Normal Mode On, Idle Mode Off, Sleep Out	Yes											
	Normal Mode On, Idle Mode On, Sleep Out	Yes											
	Partial Mode On, Idle Mode Off, Sleep Out	Yes											
	Partial Mode On, Idle Mode On, Sleep Out	Yes											
Default	Status	Default Value											
	Power On Sequence	Normal Mode On											
	S/W Reset	Normal Mode On											
	H/W Reset	Normal Mode On											
Flow Chart	See Partial Area (30h)												

6.2.15 Enter_normal_mode (13h)

13 H	NORON (Normal Display Mode On)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	0	1	0	0	1	1	13
Parameter	No Parameter												
Description	This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off.												
Restriction	This command has no effect when Normal Display mode is active.												

Register Availability

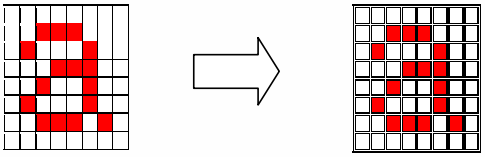
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart: See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.

6.2.16 Exit_inversion_mode (20h)

20 H	INVOFF (Display Inversion Off)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	0	0	0	0	0	20
Parameter	No Parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) (Example) Memory → Display 												
Restriction	This command has no effect when module is already in inversion off mode.												

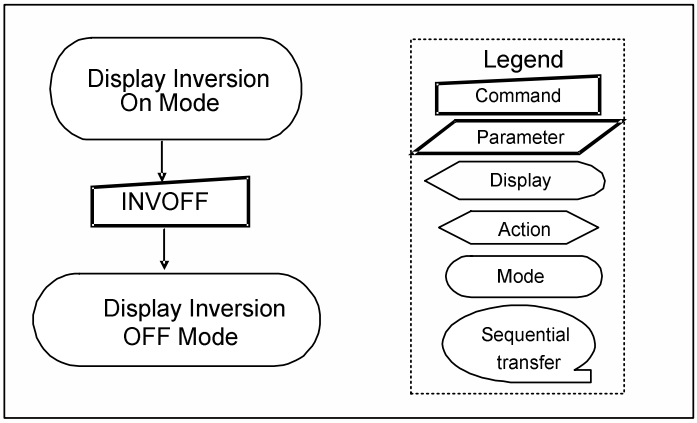
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

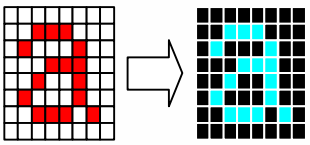
Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



6.2.17 Enter_inversion_mode (21h)

21 H	INVON (Display Inversion On)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	0	0	0	0	1	21
Parameter	No Parameter												
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) memory display 												
Restriction	This command has no effect when module is already in inversion on mode.												

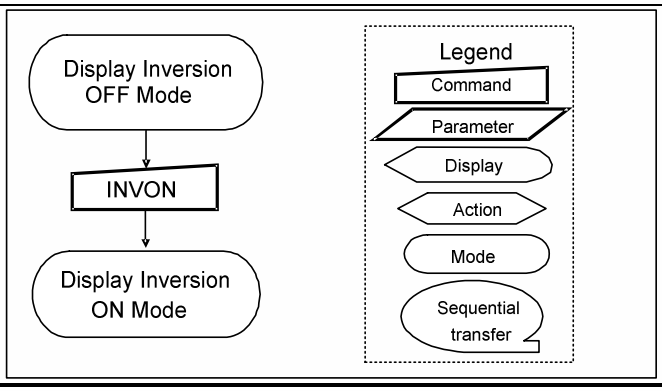
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

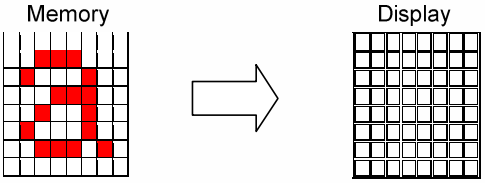
Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



6.2.18 Set_display_off (28h)

28H	DISPOFF (Display Off)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	0	0	28
Parameter	No Parameter												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Example Memory → Display 												
Restriction	This command has no effect when module is already in display off mode.												

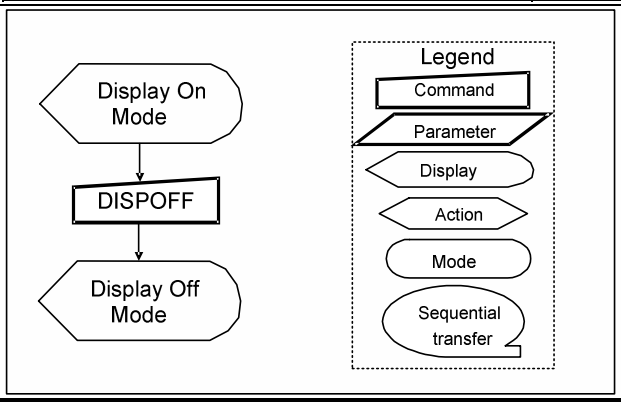
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

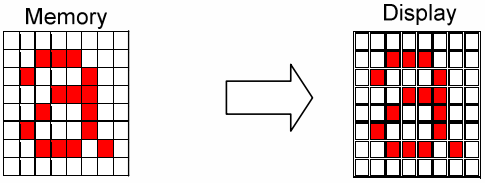
Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



6.2.19 Set_display_on (29h)

29 H	DISPON (Display On)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	0	1	0	0	1	29
Parameter	No Parameter												
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 												
Restriction	This command has no effect when module is already in display on mode.												

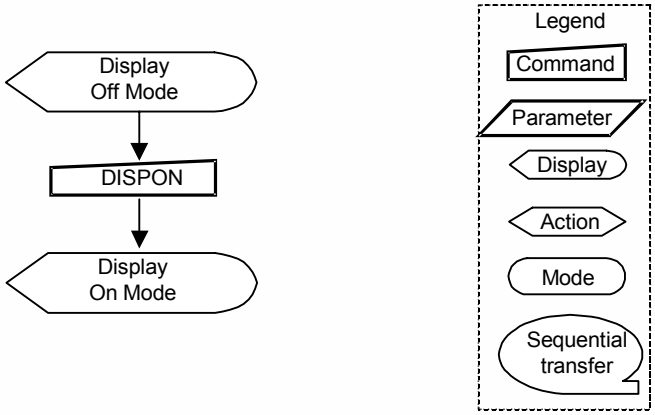
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



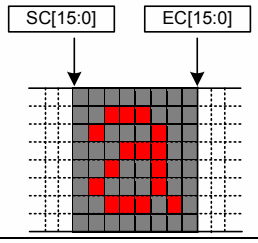
6.2.20 Set_clumn_address (2Ah)

2A H	CASET (Column Address Set)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	0	1	0	1	0	2A
1st parameter	1	1	↑	-	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	00..
2nd parameter	1	1	↑	-	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	Note 1
3rd parameter3rd	1	1	↑	-	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	00..
4th parameter4th	1	1	↑	-	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	Note 1

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

(Example)



Restriction

SC[15:0] always must be equal to or less than EC[15:0]
Note 1: When SC[15:0] or EC[15:0] is greater than horizontal line (when MADCTL's B5=0) or vertical line (when MADCTL's B5=1), data of out of range will be ignored.

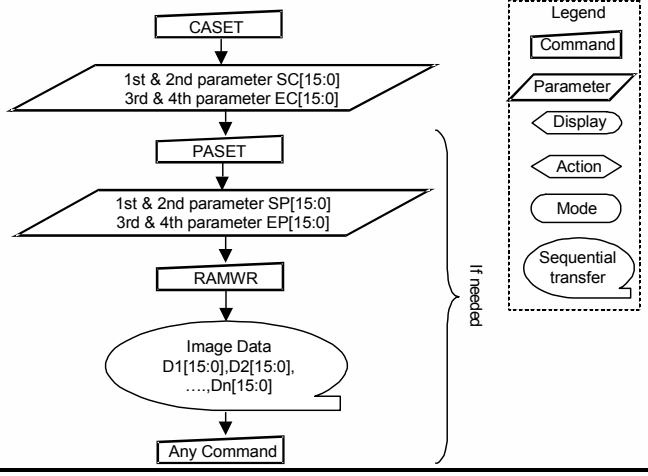
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
Power On Sequence	SC[15:0]=0000	The frame memory Column addresses corresponding to the last vertical line.
S/W Reset	When MADCTL's B5=0:	When MADCTL's B5=0:
	SC[15:0]=0000	The frame memory column addresses corresponding to the last vertical line.
	When MADCTL's B5=1:	When MADCTL's B5=1:
	SC[15:0]=0000	The frame memory column addresses corresponding to the last horizontal line.
H/W Reset	SC[15:0]=0000	The frame memory column addresse corresponding to the last horizontal line.

Flow Chart



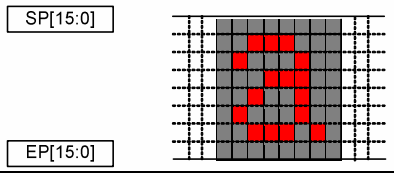
6.2.21 Set_page_address (2Bh)

2B H	PASET (Page Address Set)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	1	1	2B
1st parameter	1	1	↑	-	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	00 ...
2nd parameter	1	1	↑	-	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Note 1
3rd parameter	1	1	↑	-	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	00 ...
4th parameter	1	1	↑	-	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	Note 1

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.
Each value represents one Page line in the Frame Memory.

(Example)



Restriction

SP[15:0] always must be equal to or less than EP[15:0]
Note 1: When SP[15:0] or EP[15:0] is greater than vertical line (When MADCTL's B5=0) or horizontal line (When MADCTL's B5=1), data of out of range will be ignored.

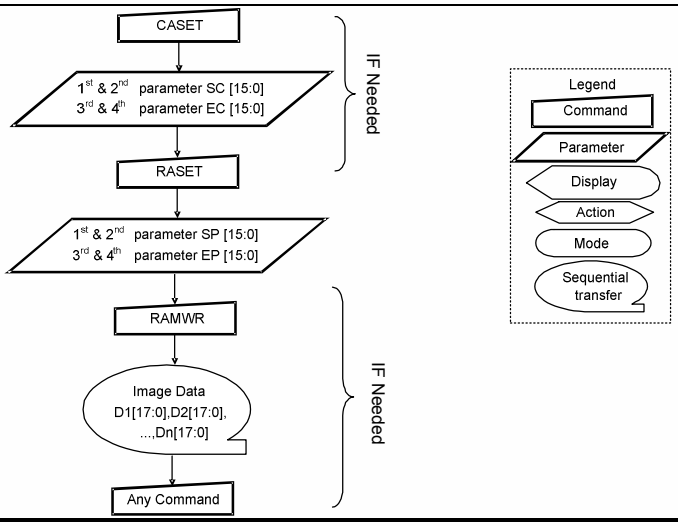
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default Value	
Power On Sequence	SP[15:0]=0000	The frame memory page addresses corresponding to the last horizontal line.
S/W Reset	When MADCTL's B5=0:	When MADCTL's B5=0:
	SP[15:0]=0000	The frame memory page addresses corresponding to the last horizontal line.
	When MADCTL's B5=1:	When MADCTL's B5=1:
	SP[15:0]=0000	The frame memory page addresses corresponding to the last vertical line.
H/W Reset	SP[15:0]=0000	The frame memory page addresses corresponding to the last horizontal line.

Flow Chart



6.2.22 Write_memory_start (2Ch)

2C H	RAMWR (Memory Write)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	0	1	1	0	0	2C
1st parameter	1	1	↑	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	1	↑	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
Nth parameter	1	1	↑	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. Then D[7:0] is stored in frame memory and the column register. Sending any other command can stop frame Write.												
Restriction	In all colour modes, there is no restriction on length of parameters.												

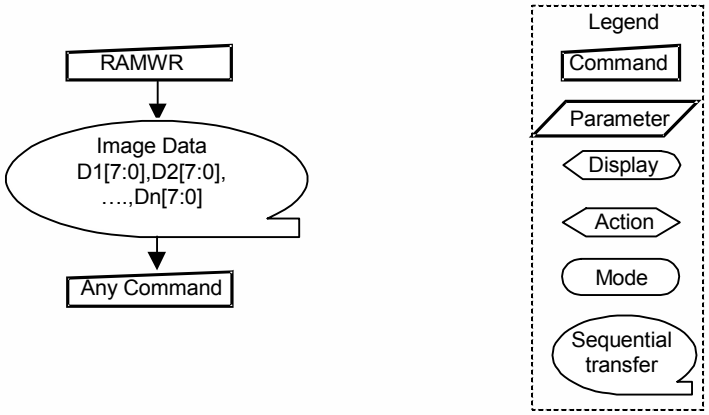
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared

Flow Chart



6.2.23 Raed_memory_start (2Eh)

2E H	RAMRD (Memory Read)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	0	1	1	1	0	2E
1st parameter	1	↑	1	-	X	X	X	X	X	X	X	X	Dummy read
2nd parameter	1	↑	1	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	↑	1	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
(n+1)th parameter	1	↑	1	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF
Description	This command is used to transfer data from frame memory to MCU. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. Frame Read can be stopped by sending any other command.												
Restriction	In all colour modes, the Frame Read is always 24bit so there is no restriction on length of parameters. Note – Memory Read is only possible via the Parallel Interface.												

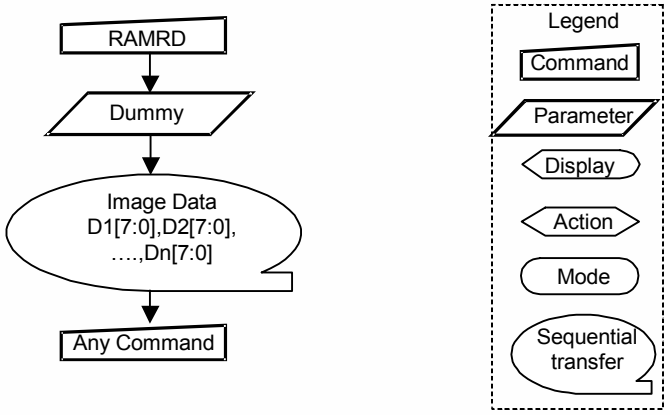
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



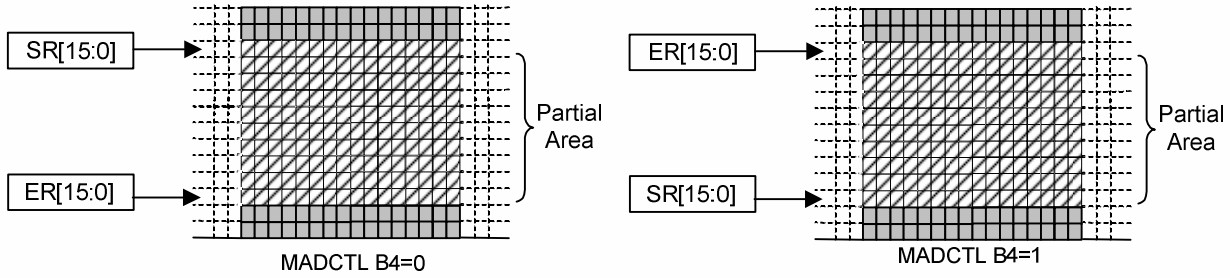
6.2.24 Set_partial_area (30h)

30 H	PLTAR (Partial Area)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	1	0	0	0	0	30
1st Parameter	1	1	↑	-	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	xx
2nd Parameter	1	1	↑	-	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	xx
3rd Parameter	1	1	↑	-	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	xx
4th Parameter	1	1	↑	-	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	xx

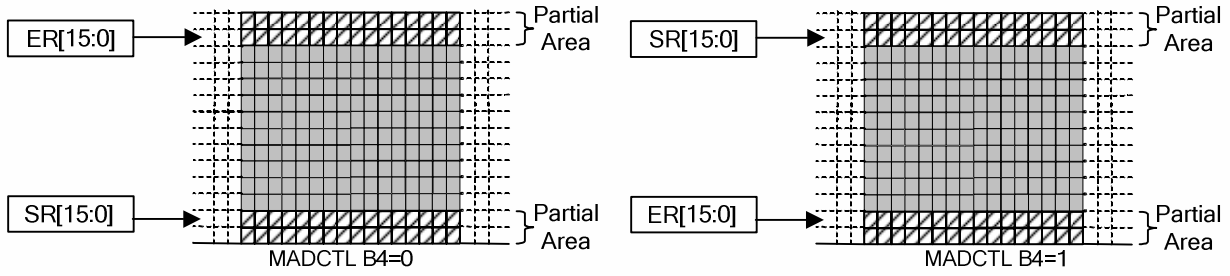
Description

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

If End Row>Start Row



If End Row<Start Row



If End Row = Start Row then the Partial Area will be one row.

Restriction

SR[15:0] and ER[15:0] cannot exceed the last vertical line number.

Register Availability

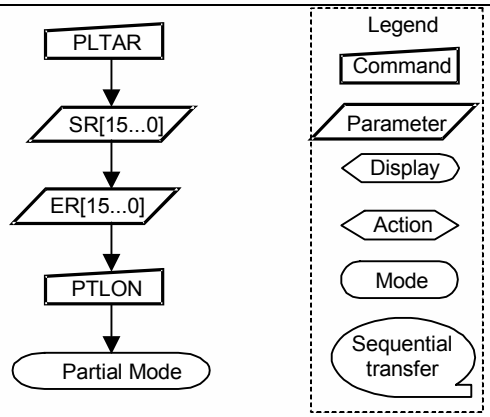
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

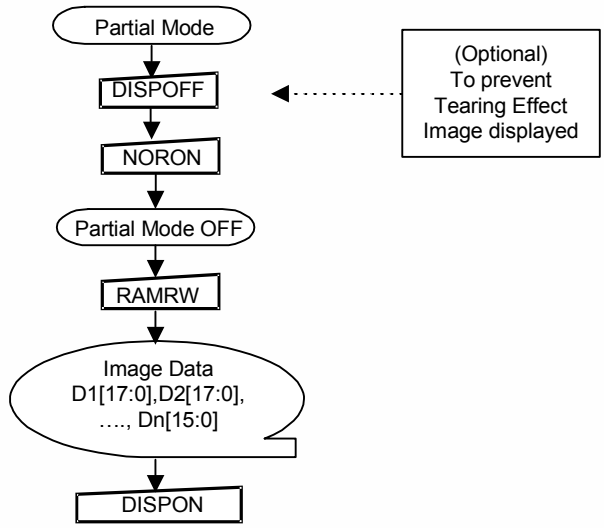
Status	Default Value	
Power On Sequence	SR[15..0]=00	ER[15..0]= Vertical line number
S/W Reset	SR[15..0]=00	ER[15..0]= Vertical line number
H/W Reset	SR[15..0]=00	ER[15..0]= Vertical line number

Flow Chart

1. To Enter Partial Mode:-



2. To Leave Partial Mode



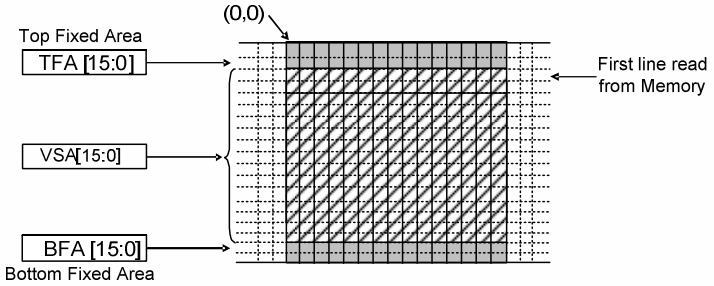
6.2.25 Set_scroll_area (33h)

33 H	VSCRDEF (Vertical Scrolling Definition)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	-	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	xx
2nd parameter	1	1	↑	-	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	xx
3rd parameter	1	1	↑	-	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	xx
4th parameter	1	1	↑	-	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	xx
5th parameter	1	1	↑	-	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	xx
6th parameter	1	1	↑	-	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	xx

Description

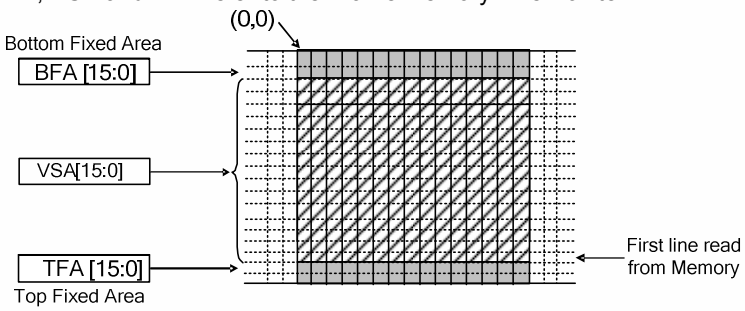
When MADCTL B4=0
The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from top of the Frame Memory and Display).
The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.
The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



When MADCTL B4=1
The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from bottom of the Frame Memory and Display).
The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.
The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Restriction

The condition is (TFA+VSA+BFA)= Vertical line number, otherwise Scrolling mode is undefined.
In Vertical Scroll Mode, MADCTL B5 should be set to '0' – this only affects the Frame Memory Write.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes

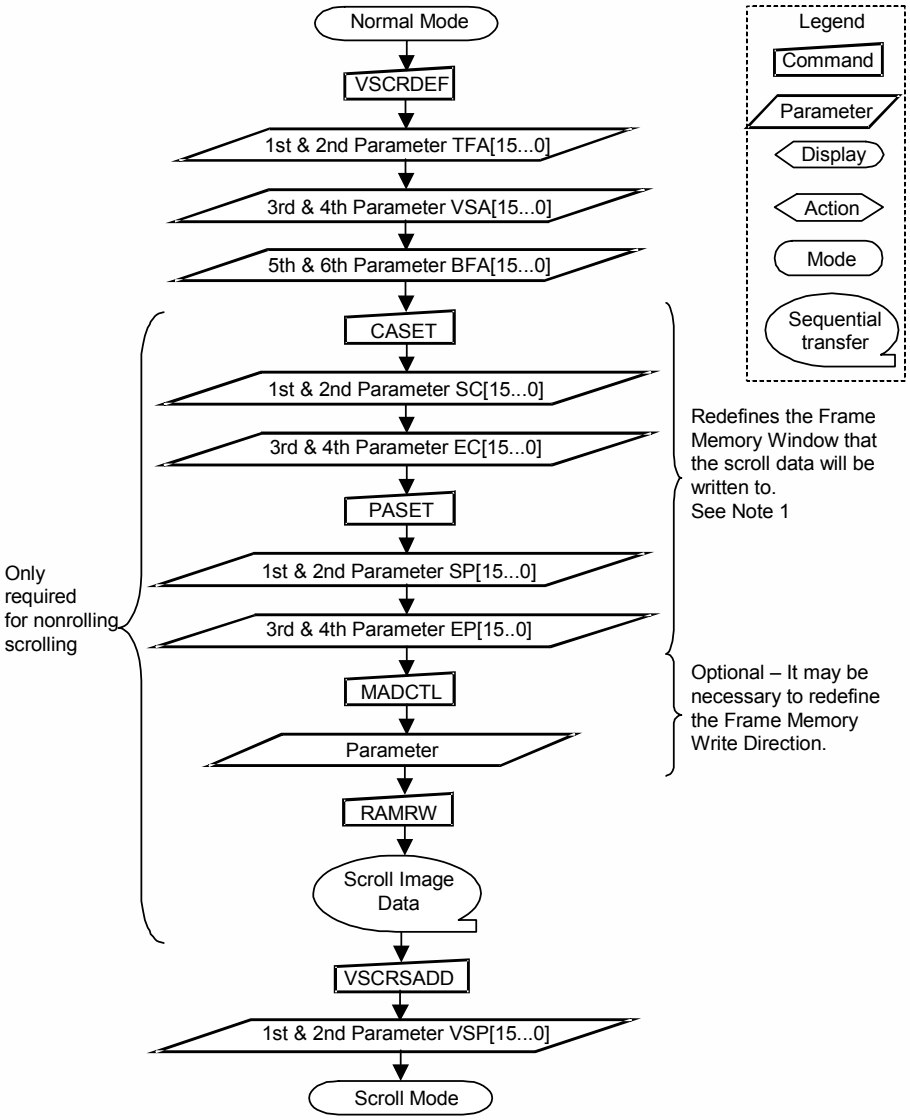
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value		
Power On Sequence	TFA[15..0]=0000	VSA[15..0]= The frame memory page address corresponding to the last horizontal line.	BFA[15..0]=0000
S/W Reset	TFA[15..0]=0000	VSA[15..0]= The frame memory page address corresponding to the last horizontal line.	BFA[15..0]=0000
H/W Reset	TFA[15..0]=0000	VSA[15..0]= The frame memory page address corresponding to the last	BFA[15..0]=0000

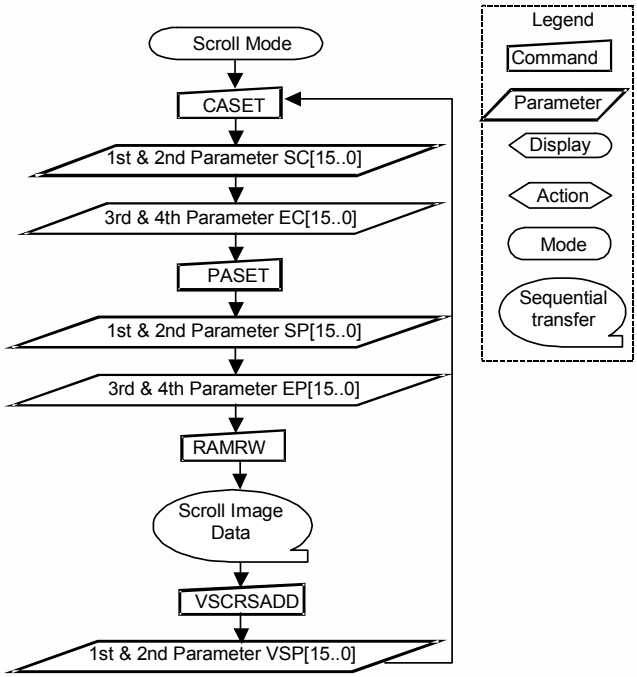
Flow Charts

1.To enter Vertical Scroll Mode:

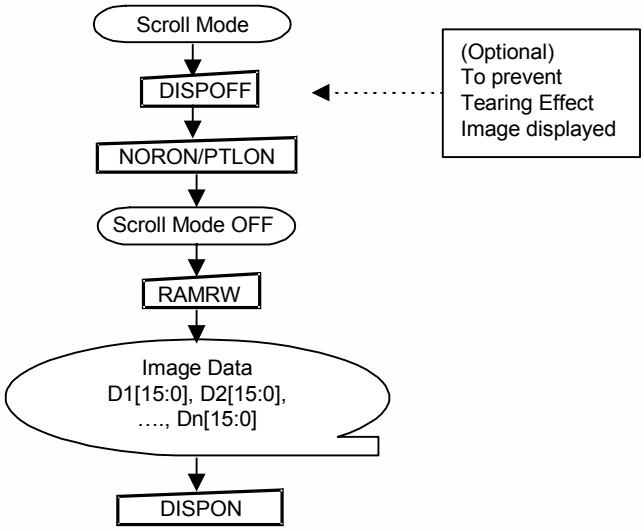


Note: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll:

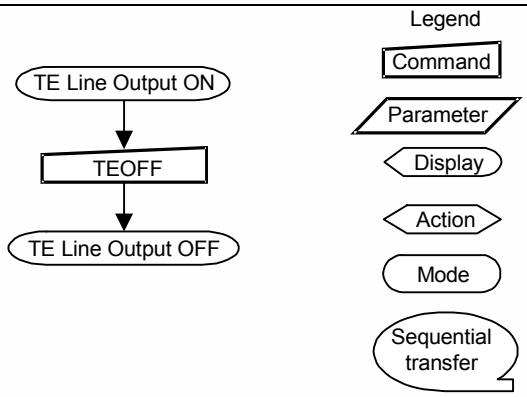


3. To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

6.2.26 Set_tear_off (34h)

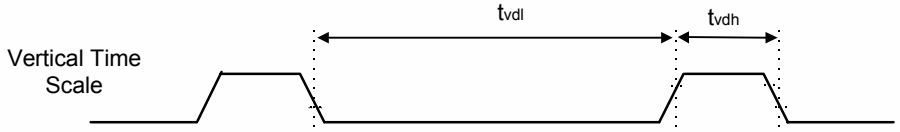
<table>
<tr><td>34 H</td><td colspan="13">TEOFF (Tearing Effect Line OFF)</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17~D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>Off</td></tr><tr><td>S/W Reset</td><td>Off</td></tr><tr><td>H/W Reset</td><td>Off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.27 Set_tear_on (35h)

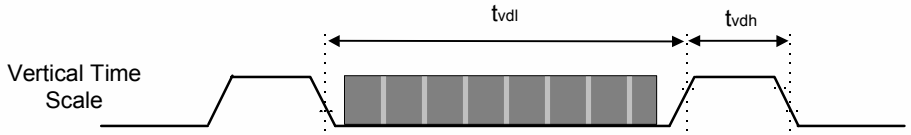
35 H	TEON (Tearing Effect Line ON)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	1	0	1	0	1	35
Parameter	1	1	↑	-	X	X	X	X	X	X	X	M	xx

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal.
This output is not affected by changing MADCTL bit B4.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).
When M=0:
The Tearing Effect Output line consists of V-Blanking information only:



When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

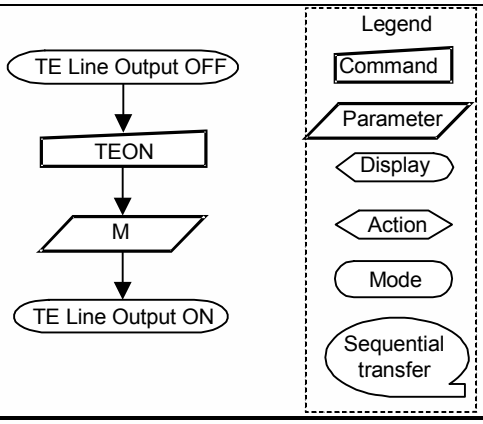
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



6.2.28 Set_address_mode (36h)

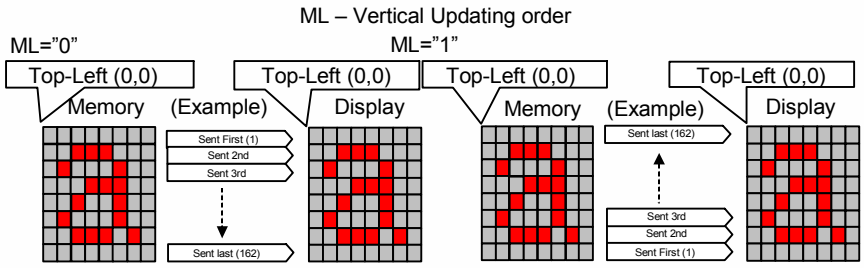
36 H	MADCTL (Memory Access Control)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	1	0	36
1st parameter	1	1	↑	-	B7	B6	B5	B4	B3	0	B1	B0	XX

Description

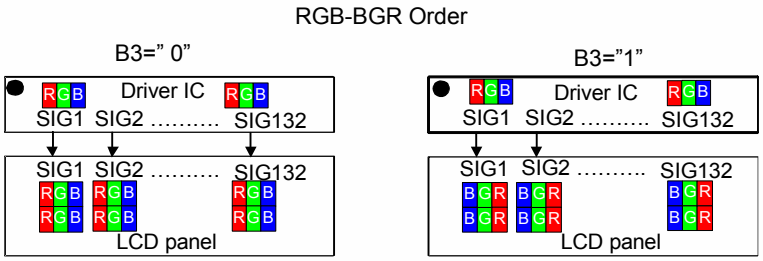
This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

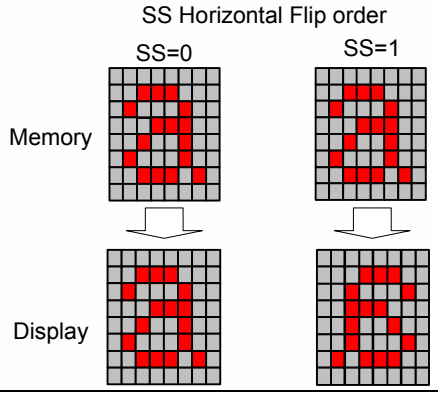
Bit Assignment

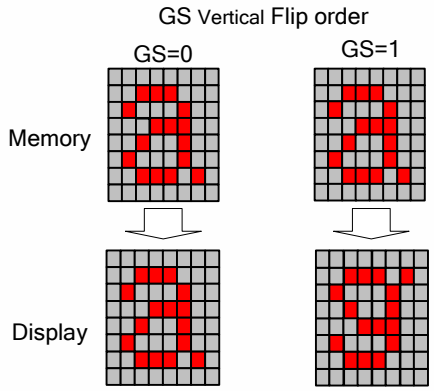
BIT	NAME	DESCRIPTION
B7	PAGE ADDRESS ORDER (MY)	These 3 bits controls MCU to memory write/read direction.
B6	COLUMN ADDRESS ORDER (MX)	
B5	PAGE/COLUMN SELECTION (MV)	
B4	Vertical ORDER (ML)	LCD vertical refresh direction control
B3	RGB-BGR ORDER (BGR)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)
B2		LCD horizontal refresh direction control
B3	Horizontal Flip(SS)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)
B3	Vertical Flip(GS)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)

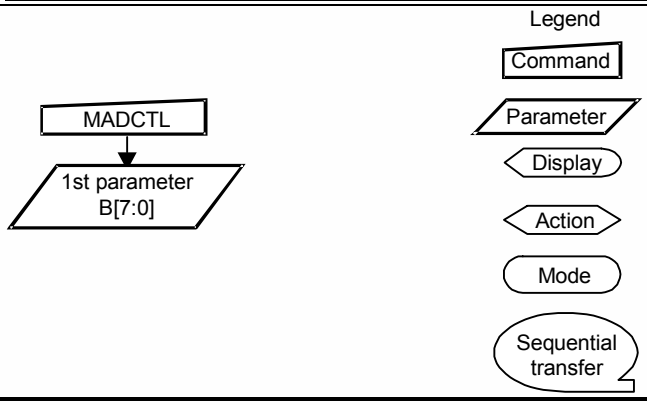


Note: Top-Left (0, 0) means a physical memory location.





<table>
<tr><td></td><td>


</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


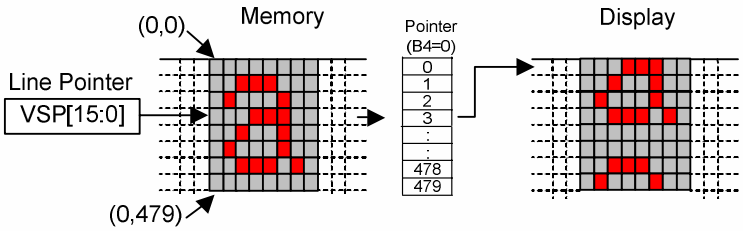
</td></tr>
</table>

6.2.29 Set_scroll_start (37h)

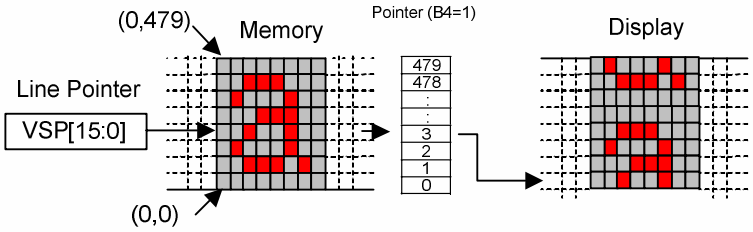
37 H	VSCRSADD (Vertical Scrolling Start Address)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	-	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8	
2nd parameter	0	1	↑	-	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	

Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:
When MADCTL B4=0
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP=3
(Example)



When MADCTL B4=1
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP=3
(Example)



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h), otherwise undesirable image will be displayed on the Panel.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart

See Vertical Scrolling Definition (33h) description.

6.2.30 Exit_idle_mode (38h)

38 H	IDMOFF (Idle mode off)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	1	1	0	0	0	38
Parameter	No Parameter												
	This command is used to recover from Idle mode on.												
Description	In the idle off mode, LCD can display maximum 262K colours.												
Restriction	This command has no effect when module is already in idle off mode.												

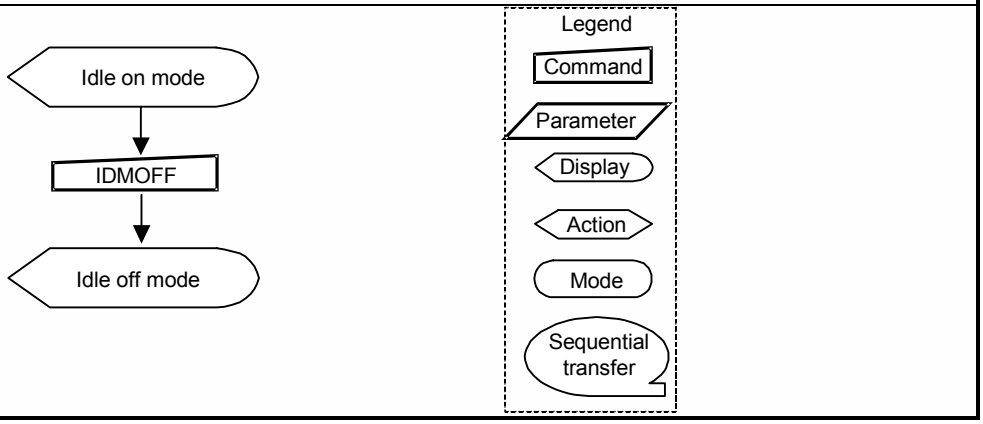
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

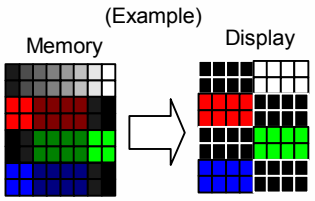
Default

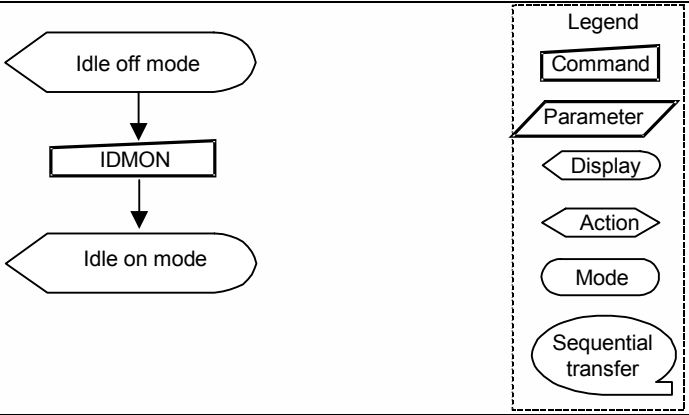
Status	Default Value
Power On Sequence	Idle off mode
S/W Reset	Idle off mode
H/W Reset	Idle off mode

Flow Chart



6.2.31 Enter_Idle_mode (39h)

<table>
<tr><td>39 H</td><td colspan="13">IDMON (Idle mode on)</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB15~DB8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into Idle mode on. In the idle on mode, colour expression is reduced. The primary and the secondary colours using MSB of each R, G and B in the Frame Memory, 8 colour depth data is displayed.
 

Memory contents vs. Display Colour
<table>
<tr><td></td><td>R6 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B2 B1 B0</td></tr>
<tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr>
<tr><td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr>
<tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr>
<tr><td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr>
<tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr>
<tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr>
<tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr>
<tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr>
</table>
X=don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>Idle off mode</td></tr>
<tr><td>S/W Reset</td><td>Idle off mode</td></tr>
<tr><td>H/W Reset</td><td>Idle off mode</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.32 Set_pixel_format (3Ah)

3A H	COLMOD (Interface Pixel Format)												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	1	1	0	1	0	3A
1st parameter	1	1	↑	-	X	D6	D5	D4	X	D2	D1	D0	XX

Description

This command is used to define the format of RGB picture data.
D6~D4: DPI Pixel format Definition.
D2~D0: DBI Pixel format Definition.
The formats are shown in the table:

Pixel Format	D6/D2	D5/D1	D4/D0
Not Defined	0	0	0
3 Bit/Pixel	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

If a particular interface, enter DBI or DPI, is not used then the corresponding bits in the parameter returned from the display module undefined.

Restriction

There is no visible effect until the Frame Memory is written to.

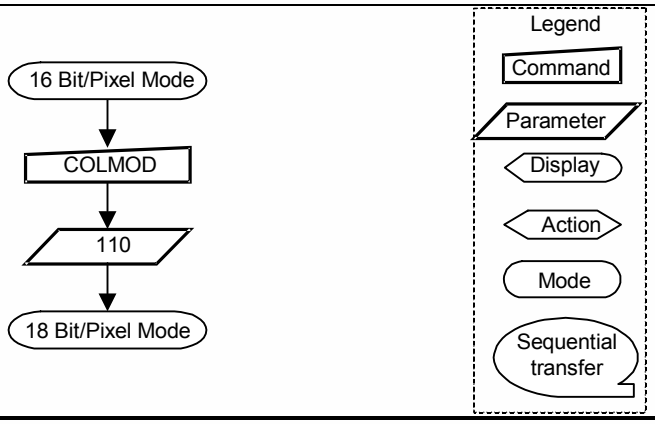
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	18 Bit/Pixel
S/W Reset	18 Bit/Pixel
H/W Reset	18 Bit/Pixel

Flow Chart



6.2.33 Write_memory_contiune (3Ch)

3C H	Write_memory_contiune												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	1	1	1	0	0	3C
1st parameter	1	1	↑	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	1	↑	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
Nth parameter	1	1	↑	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF

Description

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Sending any other command can stop frame Write.

If set_address_mode B5 = 0:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

If set_address_mode B5 = 1:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Restriction

In all colour modes, there is no restriction on length of parameters.

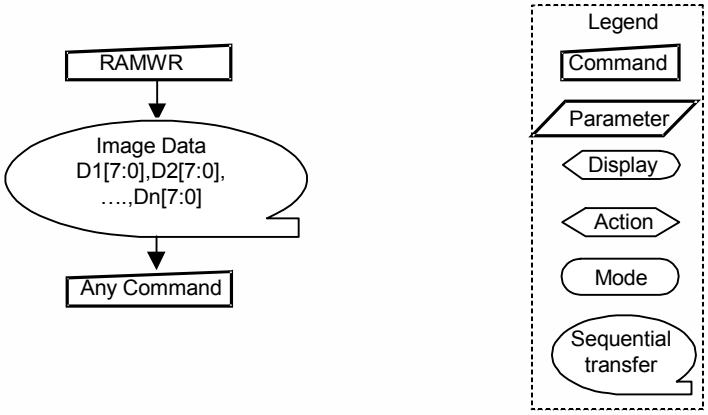
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared

Flow Chart



6.2.34 Raed_memory_continue (3Eh)

3E H	Raed_memory_continue												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	1	1	1	1	0	3E
1st parameter	1	↑	1	-	X	X	X	X	X	X	X	X	Dummy read
2nd parameter	1	↑	1	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	↑	1	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
(n+1)th parameter	1	↑	1	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF

Description

This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command.

If set_address_mode B5 = 0:
Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If set_address_mode B5 = 1:
Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data.
A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.

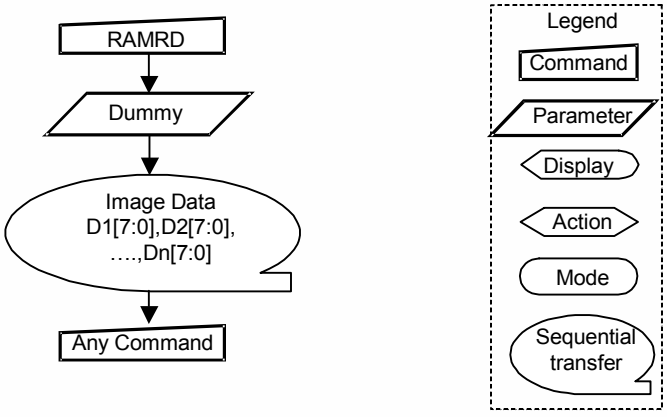
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



6.2.35 Set tear scan lines(44h)

44 H	TEST(Tear Effect Scan Lines)												
	DCX	**NWR**	**NRD**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	1	0	0	0	1	0	0	44
1st parameter	1	1	↑	-	TELINE[15:8](8'b0)								00..FF
2nd parameter	1	1	↑	-	TELINE[7:0](8'b0)								00..FF
Description	This command is turns on the display module's Tearing Effect output signal on the TE signal Line. The TE signal is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. See chapter "5.2 Tearing Effect Output Line".												
Restriction	The command has no effect when Tearing Effect output is already ON.												

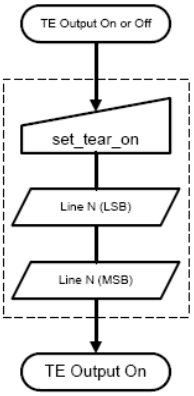
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	TELINE[15:8]=0000h
S/W Reset	TELINE[15:8]=0000h
H/W Reset	TELINE[15:8]=0000h

Flow Chart



6.2.36 Get scan lines(45h)

45H	GETSL(Mipi new Get Scan Lines)												
	DCX	**NWR**	**NRD**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	0	1	1	1	1	1	0	3E
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	↑	1	-	SL[15:8]								00..FF
3rd parameter	1	↑	1	-	SL[7:0]								00..FF
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction													

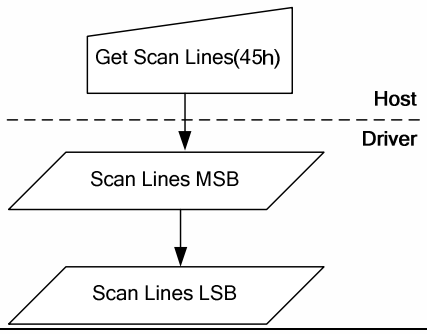
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Undefined
S/W Reset	Undefined
H/W Reset	Undefined

Flow Chart



6.2.37 Read_DDB_start (A1h)

A1 H	Read_DDB_start												
	DCX	**RDX**	**WRX**	**D17~D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	0	1	0	0	0	0	1	A1
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	X	Dummy read
2nd parameter	1	↑	1	-	ID1								
3rd parameter	1	↑	1	-	ID2								
4th parameter	1	↑	1	-	ID3								
5th parameter	1	↑	1	-	ID4								
6th parameter	1	↑	1	-	1	1	1	1	1	1	1	1	0xFF

Description

The format of returned data is as follows:
Parameter 1: Dummy read.
Parameter 2: Supplier ID code ID1.
Parameter 3: Supplier ID code ID2.
Parameter 4: Supplier Elective Data code ID3.
Parameter 5: Supplier Elective Data code ID4.
Parameter 6: single-byte *Escape or Exit Code* (0xFF).

Restrictions

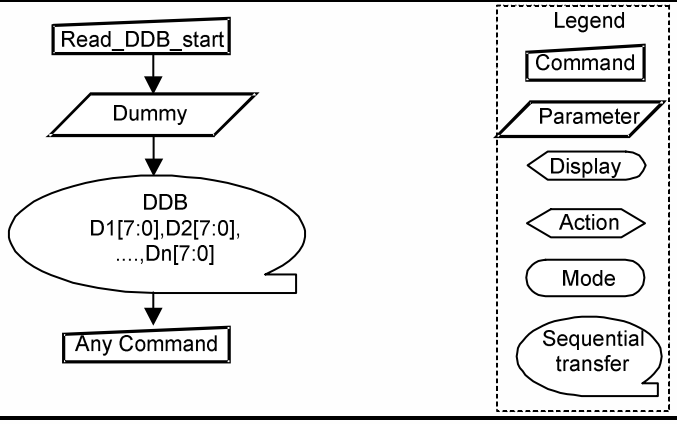
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	OTP Value
S/W Reset	OTP Value
H/W Reset	OTP Value

Flow Chart



6.2.38 Write Display Brightness (51h)

51 H	WRDISBV (Write Display Brightness)												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	1	0	1	0	0	0	1	51
1st parameter	1	1	↑	-	DBV[7:0]								00 ... FF
Description	This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter “7.17.4 Brightness Control Block”.												
Restriction													

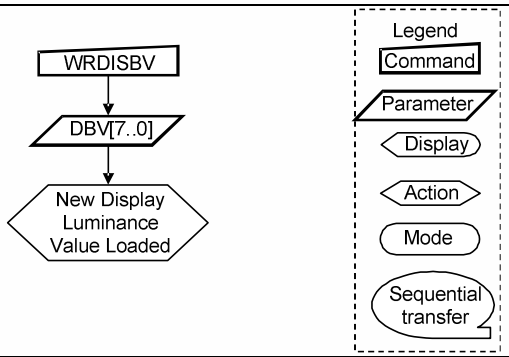
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

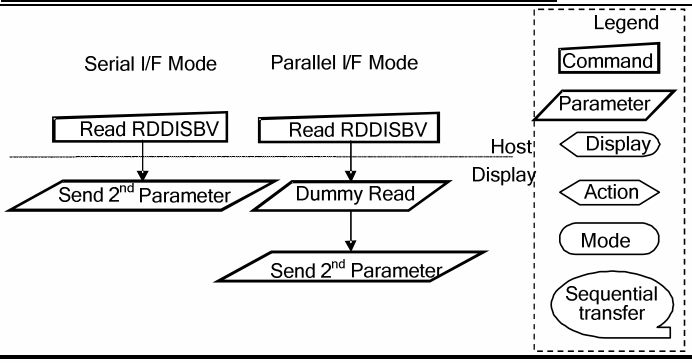
Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

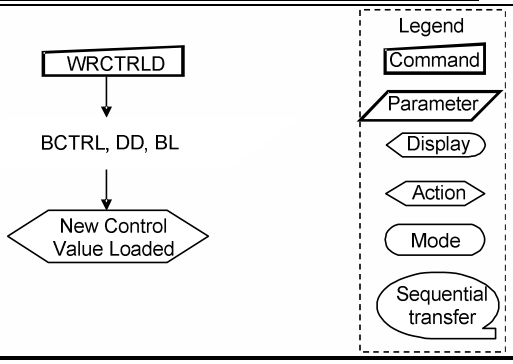
Flow Chart



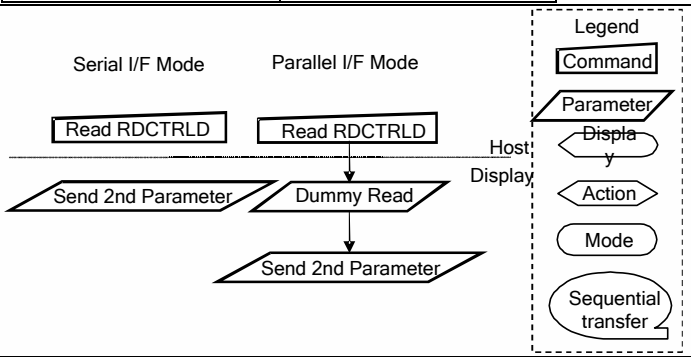
6.2.39 Read Display Brightness Value (52h)

52 H	RDDISBV (Read Display Brightness Value)												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	1	0	1	0	0	1	0	52
1st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd parameter	1	↑	1	-	DBV[7:0]								xx
Description	This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapters: "7.17.4 Brightness Control Block", 7.14.1 Display configuration" and "6.2.39 Write Display Brightness (51h)X" DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is '0' when bit BCTRL of "6.2.41 Write CTRL Display (53h)" command is '0'. DBV[7:0] is manual set brightness specified with "6.2.41 Write CTRL Display (53h)" command when bit BCTRL is '1'. When bit BCTRL of "6.2.41 Write CTRL Display (53h)" command is '1' and bit C1/C0 of "6.2.43 Write Content Adaptive Brightness Control (55h)" are '0', DBV[7:0] output is the brightness value specified with "6.2.39 Write Display Brightness (51h)" command. Refers to "2.8.1 Display configuration" for the function matrix.												
Restriction													
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	Status: Power On Sequence — Default Value: 00h Status: S/W Reset — Default Value: 00h Status: H/W Reset — Default Value: 00h												
Flow Chart													

6.2.40 Write CTRL Display (53h)

53 H	WRCTRLD (Write Control Display)												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	1	0	1	0	0	1	1	53
1st parameter	1	1	↑	-	xx	xx	BCTRL	xx	DD	BL	xx	xx	00.. FF
Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected. X = Don’t care.												
Restriction													
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	Status: Power On Sequence — Default Value: 00h Status: S/W Reset — Default Value: 00h Status: H/W Reset — Default Value: 00h												
Flow Chart													

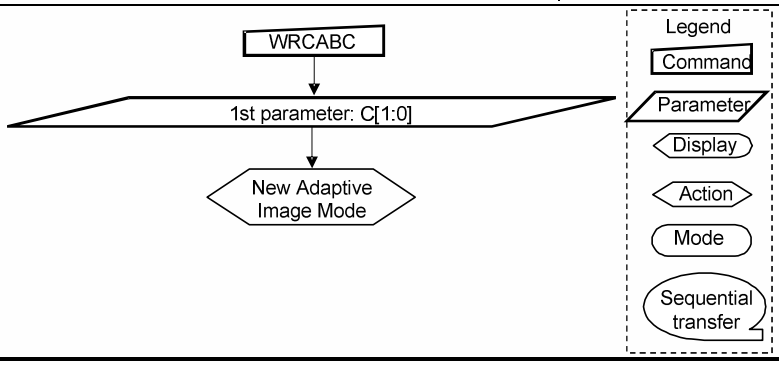
6.2.41 Read CTRL Value Display (54h)

54 H	RDCTRLD (Read Control Value Display)												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	1	0	1	0	0	1	1	54
1st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd parameter	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0	xx
Description	This command returns ambient light and brightness control values, see chapter: "6.2.41 Write CTRL Display (53h)X". BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit and CABC_ON output is VSSD) 1 = On (CABC_ON output is IOVCC)												
Restriction													
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	Status: Power On Sequence — Default Value: 00h Status: S/W Reset — Default Value: 00h Status: H/W Reset — Default Value: 00h												
Flow Chart													

6.2.42 Write Content Adaptive Brightness Control (55h)

<table>
<tr><td>55 H</td><td colspan="13">WRCABC (Write Content Adaptive Brightness Control)</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>55</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td colspan="2">CABC[1:0]</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to set parameters for image content based adaptive brightness control functionality.
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter “7.17 Content Adaptive Brightness Control (CABC)”.

<table>
<tr><td>C1</td><td>C0</td><td>Function</td><td>Note</td></tr>
<tr><td>0</td><td>0</td><td>Off</td><td></td></tr>
<tr><td>0</td><td>1</td><td>User Interface Image</td><td></td></tr>
<tr><td>1</td><td>0</td><td>Still Picture</td><td></td></tr>
<tr><td>1</td><td>1</td><td>Moving Image</td><td></td></tr>
</table>

X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.43 Read Content Adaptive Brightness Control (56h)

56 H	RDCABC (Read Content Adaptive Brightness Control)												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	1	0	1	0	1	1	0	56
1st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	XX
2nd parameter	1	↑	1	-	0	0	0	0	0	0	C1	C0	xx

Description

This command is used to set parameters for image content based adaptive brightness control functionality.
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "7.17 Content Adaptive Brightness Control (CABC)".

C1	C0	Function	Note
0	0	Off	
0	1	User Interface Image	
1	0	Still Picture	
1	1	Moving Image	

Restriction

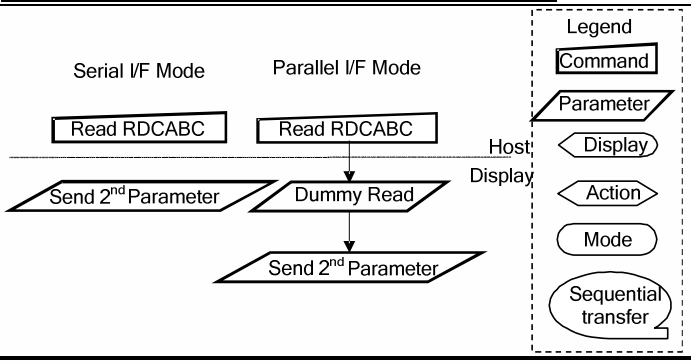
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.44 Write CABC minimum brightness (5Eh)

5E H	WRCABCMB (Write CABC minimum brightness)												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	1	0	1	1	1	1	0	5E
1st parameter	1	1	1	-	CMB[7:0]								00.. FF
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. See chapter “7.17.4 Minimum brightness setting of CABC function”.												
Restriction													

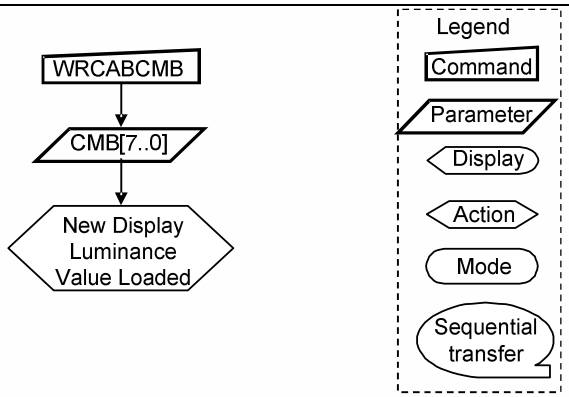
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.45 Read CABC minimum brightness (5Fh)

5F H	RDCABCMB (Read CABC minimum brightness)												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	1	0	1	1	1	1	1	5F
1st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	XX
2nd parameter	1	↑	1	-	CMB[7:0]								XX
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter “7.17.4 Minimum brightness setting of CABC function”. CMB[7:0] is CABC minimum brightness specified with “6.2.45 Write CABC minimum brightness (5Eh)” command.												
Restriction													

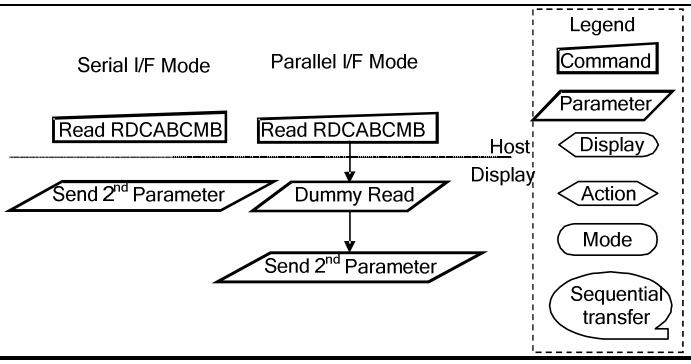
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.46 Read Automatic Brightness Control Self-Diagnostic Result (68h)

68 H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	0	1	1	0	1	0	0	0	68
1st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	XX
2nd parameter	1	↑	1	-	D[7:6]		0	0	0	0	0	0	XX
Description	This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out -command as described in the table below: ● Bit D7 – Register Loading Detection See section “7.15.1 Register loading Detection”. ● Bit D6 – Functionality Detection See section “X7.15.2 Functionality Detection “. ● Bits D5, D4, D3, D2, D1 and D0 are for future use and are set to ‘0’.												
Restriction													

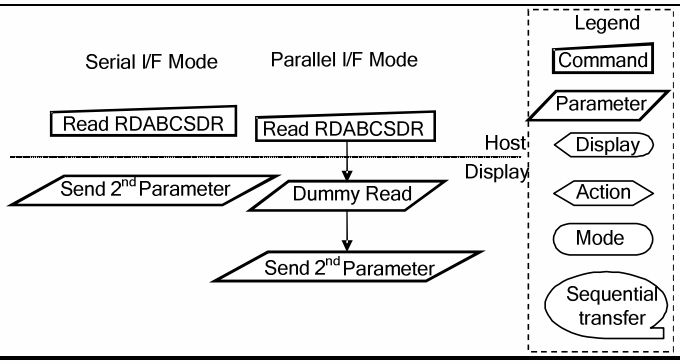
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.47 Set extended command set (B0h)

<table>
<tr><td>B0 H</td><td colspan="13">SETEXTC</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">EXTC[1:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">EXTC[1:0]: This register is select command access protect mode.
<table>
<tr><th rowspan="2">EXTC[1:0]</th><th>User Command</th><th colspan="4">Himax command</th></tr>
<tr><th>00h ~ AFh</th><th>B0h</th><th>B1h~DFh</th><th>E0h~EFh</th><th>F0h~FFh</th></tr>
<tr><td>00</td><td>Yes</td><td>Yes</td><td>Yes</td><td>Yes</td><td>Yes</td></tr>
<tr><td>01</td><td>Yes</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td></tr>
<tr><td>10</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>11</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td><td>No</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>

6.2.48 Set Deep Standby mode (B1h)

B1 H	SETDPSTB												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	0	1	1	0	0	0	1	B1
1st parameter	1	1	↑	-	0	0	0	0	0	0	0	DP_STB	XX
Description	**DP_STB:** Deep standby mode enable bit. See chapter "**5.13 Deep standby mode enter/exit flow**".												
Restriction													
Register Availability	Status: Sleep Out — Availability: No Status: Sleep In — Availability: Yes												
Default	Status: Power On Sequence — Default Value: 00h Status: S/W Reset — Default Value: No change Status: H/W Reset — Default Value: 00h												
Flow Chart													

6.2.49 Set GRAM access and Interface (B3h)

B3 H	SETGRAM												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	0	1	1	0	0	1	1	B3
1st parameter	1	1	↑	-	0	0	0	0	0	0	0	0	00h
2nd parameter	1	1	↑	-	0	0	0	0	0	TEI[2:0]			00h~07h
3rd parameter	1	1	↑	-	0	0	0	0	DENC[3:0]				00h~07h
4th parameter	1	1	↑	-	0	0	EPF[1:0]		0	0	0	DFM	

Description

TEI[2:0]: TE output cycle setting.

TEI[2:0]	TE output cycle
000	1 frame
001	2 frame
011	4 frame
101	6 frame
Others	Prohibited

DENC[2:0]: Select GRAM write cycle in RGB interface.

DENC[2:0]	GRAM write cycle
000	1 frame
001	2 frame
010	3 frame
011	4 frame
100	5 frame
101	6 frame
110	7 frame
111	8 frame

DFM: It is define image data read/write format to GRAM in DBI Type-B 16bit interface and DBI Type-C Interface. See chapter “4.1.5 DBI TYPE-B Interface Data Color Coding” and “4.2.3 DBI TYPE-C Interface Data Color Coding”.

EPF[1:0]: Data format select for 16bbp to 18bbp.

EPF[1:0]	GRAM Data																	
	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
2’h0	R4	R3	R2	R1	R0	0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0
2’h1	R4	R3	R2	R1	R0	1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1
2’h2	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4
2’h3	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Restriction

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

Flow Chart

6.2.50 Set Display mode (B4h)

<table>
<tr><td>B4 H</td><td colspan="13">SETDISPLAY</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>B4</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>0</td><td>0</td><td>RM</td><td>0</td><td>0</td><td colspan="2">DM[1:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">RM: The bit is used to select an interface for the Frame Memory access operation.
The Frame Memory is accessed only via the interface defined by RM bit. Because the interface can be selected separately from display operation mode, writing data to the Frame Memory is possible via system interface when RM = 0, even in the DPI display operation. RM setting is enabled from the next frame. Wait 1 frame to transfer data after setting
<table>
<tr><td>RM</td><td>Interface for RAM Access</td></tr>
<tr><td>0</td><td>DBI Interface (CPU)</td></tr>
<tr><td>1</td><td>DPI Interface (RGB)</td></tr>
</table>
DM[1:0]: The bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, HSYNC or DPI signal.
<table>
<tr><td>DM 1</td><td>DM 0</td><td>Display Mode</td></tr>
<tr><td>0</td><td>0</td><td>Internal oscillation clock</td></tr>
<tr><td>0</td><td>1</td><td>External VSYNC + HSYNC (Display data from GRAM)</td></tr>
<tr><td>1</td><td>0</td><td>External VSYNC (Display data from GRAM)</td></tr>
<tr><td>1</td><td>1</td><td>External DPI (RGB Through mode)</td></tr>
</table>
Note: Switching between VSYNC, HSYNC and DPI operation is prohibited.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>

6.2.51 Get Device ID (BFh)

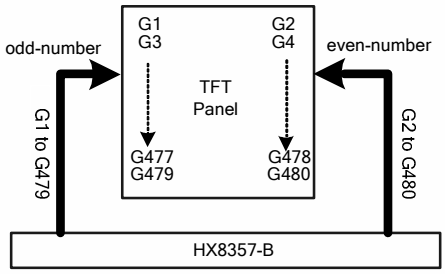
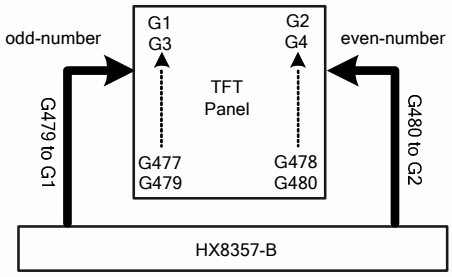
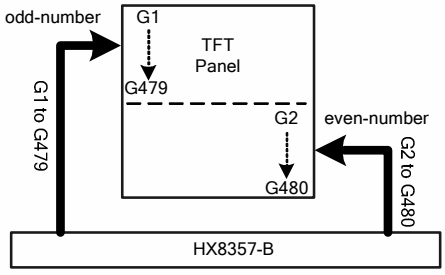
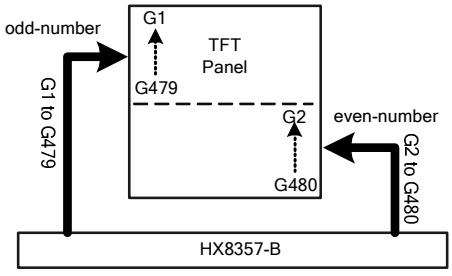
BF H	GETDEVICEID												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	0	1	1	1	1	1	1	BF
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	XX
2nd parameter	1	↑	1	-	0	0	0	0	0	0	0	1	01
3rd parameter	1	↑	1	-	0	1	1	0	0	0	1	0	62
4th parameter	1	↑	1	-	1	0	0	0	0	0	1	1	83
5th parameter	1	↑	1	-	0	1	0	1	0	1	1	1	57
6th parameter	1	↑	1	-	1	1	1	1	1	1	1	1	FF
Description	The format of returned data is as follows: Parameter 1: Dummy read. Parameter 2: MIPI Alliance code. Parameter 3: MIPI Alliance code. Parameter 4: Device ID code. Parameter 5: Device ID code. Parameter 6: single-byte *Escape or Exit Code* (0xFF).												
Restriction													
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	Status: Power On Sequence — Default Value: Status: S/W Reset — Default Value: No change Status: H/W Reset — Default Value:												
Flow Chart													

6.2.52 Set Panel Driving (C0h)

C0 H	SETPANEL												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	0	0	0	0	C0
1st parameter	1	1	↑	-	0	0	0	REV	SM	GS	0	0	XX
2nd parameter	1	1	↑	-	0	0	NL[5:0]						XX
3rd parameter	1	1	↑	-	0	SCN[6:0]							XX
4th parameter	1	1	↑	-	0	0	0	NDL	0	PTS[2:0]			XX
5th parameter	1	1	↑	-	0	0	0	PTG	ISC[3:0]				XX

Description

GS: Select the optimal scan mode for the module.
SM: Sets the gate driver pin arrangement in combination.

SM	GS	Scan direction
0	0	 G1,G2,G3,... G157,G158,... G479,G480
0	1	 G480,G479,G478,... G158,G157,... G2,G1
1	0	 G1,G3... G477,G479, G2,G4,G56.. G480
1	1	 G480,G478... G4,G2, G479,G477,... G1

REV: Enables the grayscale inversion of the image in display area.

REV	GRAM Data	Display area	
		VCOM = "L"	VCOM = "H"
0	18'h00000 : 18'h3FFFF	V63P : V0P	V0N : V63N
1	18'h00000 : 18'h3FFFF	V0P : V63P	V63N : V0N

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0].
The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Driver line number
0x00 ~ 0x3B	8*(NL[5:0]+1) line
Other setting	Inhibited

SCN[6:0]: Scan line start position.

SCN[6:0]	Start position of Gate			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
0x00 ~ 0x3B	G[1+SCN[6:0]*4]	G[480- SCN[6:0]*4]	G[1+SCN[6:0]*8]	G[480- SCN[6:0]*4]
0x3C ~ 0x77	G[1+SCN[6:0]*4]	G[480- SCN[6:0]*4]	G[2+(SCN[6:0]-0x3C)*8]	G[479- (SCN[6:0]-0x3C)*8]
Other setting	Inhibited	Inhibited	Inhibited	Inhibited

PTS[2:0]: Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

PTS[2:0]	Source output level in non-display area			
	VCOM = "L"		VCOM = "H"	
000	V63P	V0N	V0P	V63N
001	V0P	V63N	V63P	V0N
010	GND	GND	GND	GND
011	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Other	Inhibited	Inhibited	Inhibited	Inhibited

NDL: Sets the source output level in non-display area of refresh scan cycle. Settings are different to normally black panels and normally white panels.

NDL	Source output level in non-display area of refresh scan cycle	
	VCOM = "L"	VCOM = "H"
0	V63P	V0N
1	V0P	V63N

ISC[3:0]: Specify the refresh scan cycle of gate driver when **PTG** select in non-display area. Then refresh scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	1 frame	17ms
0	0	0	1	3 frames	50ms
0	0	1	0	5 frames	83ms
0	0	1	1	7 frames	117ms
0	1	0	0	9 frames	150ms
0	1	0	1	11 frames	183ms
0	1	1	0	13 frames	217ms
0	1	1	1	15 frames	250ms
1	0	0	0	17 frames	283ms
1	0	0	1	19 frames	317ms
1	0	1	0	21 frames	350ms
1	0	1	1	23 frames	383ms
1	1	0	0	25 frames	417ms
1	1	0	1	27 frames	450ms
1	1	1	0	29 frames	483ms
1	1	1	1	31 frames	517ms

<table>
<tr><td></td><td>PTG: Specify the scan mode of gate driver in non-display area.
<table>
<tr><th>PTG</th><th>Gate Outputs in Non-display Area</th></tr>
<tr><td>0</td><td>Normal Drive</td></tr>
<tr><td>1</td><td>Interval Drive</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

6.2.53 Set display timing for Normal mode (C1h)

C1 H	SETNORTIM												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	0	0	0	1	C1
1st parameter	1	1	↑	-	0	0	0	BC0	0	0	DIV0[1:0]		XX
2nd parameter	1	1	↑	-	0	0	0	RTN0[4:0]					XX
3rd parameter	1	1	↑	-	FP0[3:0]				BP0[3:0]				XX

Description

BC0: Frame/Line inversion select.

BC0	Inversion mode
0	Frame
1	Line

DIV0[1:0]: Specify the division ratio of internal clocks in Normal mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the RTN1[4:0] bits (1H period clock cycle), FP1[3:0], and BP1[3:0] bits.

DIV0[1:0]	Division ratio
00	1/1
01	1/2
10	1/4
11	1/8

RTN0[4:0]: Specify clock number of one line period in Normal mode for internal operation.
Clock cycles=1/internal operation clock frequency(fosc)

RTN0[4:0]	Clock number per Line
5'b10000	168
5'b10001	169
5'b10010	170
5'b10011	171
5'b10100	172
:	:
5'b11110	182
5'b11111	183
Other	Inhibited

FP0[3:0]: Set the number of lines for a front porch period (a blank period following the end of display).
BP0[3:0]: Set the number of lines for a back porch period (a blank period made before the beginning of display).

FP0[3:0] / BP0[3:0]	Front / Back porch period
4'b0000	Inhibited
4'b0001	Inhibited
4'b0010	2 lines
4'b0011	3 lines
4'b0100	4 lines
:	:
4'b1110	14 lines
4'b1111	15 lines

The condition in setting BP and FP bits are: BP≧2 lines, FP≧2 lines, BP+FP≦30 lines

Formula for the Frame Frequency during internal display mode:
Frame frequency = fosc/(RTN × DIV × (Scan Line+FP+BP)) [Hz]

Restriction

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

Flow Chart

6.2.54 Set display timing for Partial mode (C2h)

C2 H	SETPARTIM												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	1	0	0	0	0	1	0	C2
1st parameter	1	1	↑	-	0	0	0	BC1	0	0	DIV1[1:0]		XX
2nd parameter	1	1	↑	-	0	0	0	RTN1[4:0]					XX
3rd parameter	1	1	↑	-	FP1[3:0]			BP1[3:0]					XX

Description

BC1: Frame/Line inversion select.

BC1	Inversion mode
0	Frame
1	Line

DIV1[1:0]: Specify the division ratio of internal clocks in Normal mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the RTN1[4:0] bits (1H period clock cycle), FP1[3:0], and BP1[3:0] bits.

DIV1[1:0]	Division ratio
00	1/1
01	1/2
10	1/4
11	1/8

RTN1[4:0]: Specify clock number of one line period in Normal mode for internal operation.
Clock cycles=1/internal operation clock frequency(fosc)

RTN1[4:0]	Clock number per Line
5'b10000	168
5'b10001	169
5'b10010	170
5'b10011	171
5'b10100	172
:	:
5'b11110	182
5'b11111	183
Other	Inhibited

FP1[3:0]: Set the number of lines for a front porch period (a blank period following the end of display).
BP1[3:0]: Set the number of lines for a back porch period (a blank period made before the beginning of display).

FP1[3:0] / BP1[3:0]	Front / Back porch period
4'b0000	Inhibited
4'b0001	Inhibited
4'b0010	2 lines
4'b0011	3 lines
4'b0100	4 lines
:	:
4'b1110	14 lines
4'b1111	15 lines

The condition in setting BP and FP bits are: BP≧2 lines, FP≧2 lines, BP+FP≦30 lines

Formula for the Frame Frequency during internal display mode:
Frame frequency = fosc/(RTN × DIV × (Scan Line+FP+BP)) [Hz]

Restriction

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

Flow Chart

6.2.55 Set display timing for Idle mode (C3h)

C3 H	SETIDLTIM												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	1	0	0	0	0	1	1	C3
1st parameter	1	1	↑	-	0	0	0	BC2	0	0	DIV2[1:0]		XX
2nd parameter	1	1	↑	-	0	0	0	RTN2[4:0]					XX
3rd parameter	1	1	↑	-	FP2[3:0]				BP2[3:0]				XX

Description

BC2: Frame/Line inversion select.

BC2	Inversion mode
0	Frame
1	Line

DIV2[1:0]: Specify the division ratio of internal clocks in Normal mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the RTN2[4:0] bits (1H period clock cycle), FP2[3:0], and BP2[3:0] bits.

DIV2[1:0]	Division ratio
00	1/1
01	1/2
10	1/4
11	1/8

RTN2[4:0]: Specify clock number of one line period in Normal mode for internal operation.
Clock cycles=1/internal operation clock frequency(fosc)

RTN2[4:0]	Clock number per Line
5'b10000	168
5'b10001	169
5'b10010	170
5'b10011	171
5'b10100	172
:	:
5'b11110	182
5'b11111	183
Other	Inhibited

FP2[3:0]: Set the number of lines for a front porch period (a blank period following the end of display).
BP2[3:0]: Set the number of lines for a back porch period (a blank period made before the beginning of display).

FP2[3:0] / BP2[3:0]	**Front / Back porch period**
4'b0000	Inhibited
4'b0001	Inhibited
4'b0010	2 lines
4'b0011	3 lines
4'b0100	4 lines
:	:
4'b1110	14 lines
4'b1111	15 lines

The condition in setting BP and FP bits are: BP≧2 lines, FP≧2 lines, BP+FP≦30 lines

Formula for the Frame Frequency during internal display mode:
Frame frequency = fosc/(RTN × DIV × (Scan Line+FP+BP)) [Hz]

Restriction

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

Flow Chart

6.2.56 Set display frame (C5h)

C5 H	SETOSC												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	1	0	0	0	1	0	1	C5
1st parameter	1	1	↑	-	0	0	0	0	UADJ[3:0]				XX
Description	**UADJ[3:0]:** Set the frame rate of full colors normal mode.												
Restriction													
Register Availability													
Default													
Flow Chart													

UADJ[3:0]	Fosc(MHz)
0000	1.7981
0001	2.2366
0010	2.6673
0011	3.0995
0100	3.5198
0101	3.9402
0110	4.3609
0111	4.7758
1000	**5.2000**
1001	5.5791
1010	5.9986
1011	6.4398
1100	6.8374
1101	7.2101
1110	7.6100
1111	8.0426

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

6.2.57 Set RGB Interface (C6h)

C6 H	SETRGB												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	1	0	0	0	1	1	0	C6
1st parameter	1	1	↑	-	SDA_EN	0	0	VPL	HPL	0	EPL	DPL	XX

Description

This command is used to set RGB interface related register

EPL: Specify the polarity of Enable pin in DPI interface mode.

EPL	ENABLE pin	Display image	Operation
0	Low	Enable	Write data to DB17-0
0	High	Disable	Disable
1	Low	Disable	Disable
1	High	Enable	Write data to DB17-0

VPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

SDA_EN: DBI Type-C interface pin selection

SDA_EN	DIN_SDA	DOUT
0	Data Input	Data output
1	Data input/output	Not used

Restriction

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

Flow Chart

6.2.58 Set Gamma (C8h)

C8 H	SETGAMMA												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	1	0	0	1	0	0	0	C8
1st parameter	1	1	↑	-	0	KP1[2:0]			0	KP0[2:0]			XX
2nd parameter	1	1	↑	-	0	KP3[2:0]			0	KP2[2:0]			XX
3rd parameter	1	1	↑	-	0	KP5[2:0]			0	KP4[2:0]			XX
4th parameter	1	1	↑	-	0	RP1[2:0]			0	RP0[2:0]			XX
5th parameter	1	1	↑	-	0	0	0	0	VRP0[3:0]				XX
6th parameter	1	1	↑	-	0	0	0	VRP1[4:0]					XX
7th parameter	1	1	↑	-	0	KN1[2:0]			0	KN0[2:0]			XX
8th parameter	1	1	↑	-	0	KN3[2:0]			0	KN2[2:0]			XX
9th parameter	1	1	↑	-	0	KN5[2:0]			0	KN4[2:0]			XX
10th parameter	1	1	↑	-	0	RN1[2:0]			0	RN0[2:0]			XX
11th parameter	1	1	↑	-	0	0	0	0	VRN0[3:0]				XX
12th parameter	1	1	↑	-	0	0	0	VRN1[4:0]					XX
Description	This command is used for Gamma Curve related Setting. For details, please refer to **"5.7 Gamma Characteristic Correction Function"**												
Restriction													
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	Status: Power On Sequence — Default Value: Status: S/W Reset — Default Value: No change Status: H/W Reset — Default Value:												
Flow Chart													

6.2.59 Set Power (D0h)

D0H	SETPOWER												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	0	0	0	0	D0
1st parameter	1	1	↑	-	0	AP[2:0]			0	VC[2:0]			XX
2nd parameter	1	1	↑	-	0	PON	0	0	0	BT[2:0]			
3rd parameter	1	1	↑	-	0	0	0	0	VRH[3:0]				

Description

AP[2:0]: Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased.
Adjust the fixed current by considering both the display quality and the current consumption.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Operation of the operational amplifier stops
0	0	1	Medium
0	1	0	Medium
0	1	1	Medium
1	0	0	Medium High
1	0	1	Large
1	1	0	Setting Inhibited
1	1	1	Setting Inhibited

VC[2:0]: Set VCI1 voltage

VC[2:0]	VCI1	DDVDH		VCL
		DDVDH_TRI=0	DDVDH_TRI=1	
000	3.24V	6.48V	6.67V	-3.24V
001	3.06V	6.12V	6.48V	-3.06V
010	2.91V	5.82V	6.12V	-2.91V
011	2.77V	5.54V	5.97V	-2.77V
100	2.64V	5.28V	5.67V	-2.64V
101	2.47V	4.94V	5.40V	-2.47V
110	1.92V	3.84V	5.16V	-1.92V
111	VCI	VCIx2	inhibited	-VCI

Note: 1. VCI1 ≤ (VCI-0.15)V.

BT[3:0]: Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT2	BT1	BT0	VGH	VGL
0	0	0	3xDDVDH	-2DDVDH+VCL
0	0	1		-2DDVDH
0	1	0		-DDVDH+VCL
0	1	1	2DDVDH + VCI1	-2DDVDH+VCL
1	0	0		-2DDVDH
1	0	1		-DDVDH+VCL
1	1	0	2DDVDH	-2DDVDH
1	1	1		-DDVDH+VCL

PON: Specify on/off control of step-up circuit 2 for VGH, VGL voltage generation.

PON	Operation of step-up circuit 2
0	OFF
1	ON

VRH[3:0]: Specify the VREG1 voltage adjusting. VREG1 voltage is for gamma voltage setting.
Note: setting restriction: VREG1OUT≦(DDVDH-0.3V)

VRH[3:0]	VREG1
0000	Halt
0001	4.000v
0010	4.125v
0011	4.250v
0100	4.375v
0101	4.500v
0110	4.625v
0111	4.750v

<table>
<tr><td></td><td>
<table>
<tr><td>1000</td><td>4.875v</td></tr>
<tr><td>1001</td><td>5.000v</td></tr>
<tr><td>1010</td><td>5.125v</td></tr>
<tr><td>1011</td><td>5.250v</td></tr>
<tr><td>1100</td><td>5.500v</td></tr>
<tr><td>1101</td><td>5.750v</td></tr>
<tr><td>1110</td><td>6.000v</td></tr>
<tr><td>1111</td><td>6.000v</td></tr>
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</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
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<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

6.2.60 Set VCOM (D1h)

D1H	SETVCOM												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	0	0	0	1	D1
1st parameter	1	1	↑	-	0	VCM[6:0]							XX
2nd parameter	1	1	↑	-	0	0	0	VDV[4:0]					

Description

VCM(6-0): Set the VCOMH voltage (High level voltage of VCOM) It is possible to amplify from 0.492 to 1 times of VREG1OUT voltage.

VCM[6:0]	VCOMH	VCM[6:0]	VCOMH
0 0 0 0 0 0 0	0.492xVREG1OUT	1 0 0 0 0 0 0	0.748xVREG1OUT
0 0 0 0 0 0 1	0.496xVREG1OUT	1 0 0 0 0 0 1	0.752xVREG1OUT
0 0 0 0 0 1 0	0.500xVREG1OUT	1 0 0 0 0 1 0	0.756xVREG1OUT
0 0 0 0 0 1 1	0.504xVREG1OUT	1 0 0 0 0 1 1	0.760xVREG1OUT
0 0 0 0 1 0 0	0.508xVREG1OUT	1 0 0 0 1 0 0	0.764xVREG1OUT
0 0 0 0 1 0 1	0.512xVREG1OUT	1 0 0 0 1 0 1	0.768xVREG1OUT
0 0 0 0 1 1 0	0.516xVREG1OUT	1 0 0 0 1 1 0	0.772xVREG1OUT
0 0 0 0 1 1 1	0.520xVREG1OUT	1 0 0 0 1 1 1	0.776xVREG1OUT
0 0 0 1 0 0 0	0.524xVREG1OUT	1 0 0 1 0 0 0	0.780xVREG1OUT
0 0 0 1 0 0 1	0.528xVREG1OUT	1 0 0 1 0 0 1	0.784xVREG1OUT
0 0 0 1 0 1 0	0.532xVREG1OUT	1 0 0 1 0 1 0	0.788xVREG1OUT
0 0 0 1 0 1 1	0.536xVREG1OUT	1 0 0 1 0 1 1	0.792xVREG1OUT
0 0 0 1 1 0 0	0.540xVREG1OUT	1 0 0 1 1 0 0	0.796xVREG1OUT
0 0 0 1 1 0 1	0.544xVREG1OUT	1 0 0 1 1 0 1	0.800xVREG1OUT
0 0 0 1 1 1 0	0.548xVREG1OUT	1 0 0 1 1 1 0	0.804xVREG1OUT
0 0 0 1 1 1 1	0.552xVREG1OUT	1 0 0 1 1 1 1	0.808xVREG1OUT
0 0 1 0 0 0 0	0.556xVREG1OUT	1 0 1 0 0 0 0	0.812xVREG1OUT
0 0 1 0 0 0 1	0.560xVREG1OUT	1 0 1 0 0 0 1	0.816xVREG1OUT
0 0 1 0 0 1 0	0.564xVREG1OUT	1 0 1 0 0 1 0	0.820xVREG1OUT
0 0 1 0 0 1 1	0.568xVREG1OUT	1 0 1 0 0 1 1	0.824xVREG1OUT
0 0 1 0 1 0 0	0.572xVREG1OUT	1 0 1 0 1 0 0	0.828xVREG1OUT
0 0 1 0 1 0 1	0.576xVREG1OUT	1 0 1 0 1 0 1	0.832xVREG1OUT
0 0 1 0 1 1 0	0.580xVREG1OUT	1 0 1 0 1 1 0	0.836xVREG1OUT
0 0 1 0 1 1 1	0.584xVREG1OUT	1 0 1 0 1 1 1	0.840xVREG1OUT
0 0 1 1 0 0 0	0.588xVREG1OUT	1 0 1 1 0 0 0	0.844xVREG1OUT
0 0 1 1 0 0 1	0.592xVREG1OUT	1 0 1 1 0 0 1	0.848xVREG1OUT
0 0 1 1 0 1 0	0.596xVREG1OUT	1 0 1 1 0 1 0	0.852xVREG1OUT
0 0 1 1 0 1 1	0.600xVREG1OUT	1 0 1 1 0 1 1	0.856xVREG1OUT
0 0 1 1 1 0 0	0.604xVREG1OUT	1 0 1 1 1 0 0	0.860xVREG1OUT
0 0 1 1 1 0 1	0.608xVREG1OUT	1 0 1 1 1 0 1	0.864xVREG1OUT
0 0 1 1 1 1 0	0.612xVREG1OUT	1 0 1 1 1 1 0	0.868xVREG1OUT
0 0 1 1 1 1 1	0.616xVREG1OUT	1 0 1 1 1 1 1	0.872xVREG1OUT
0 1 0 0 0 0 0	0.620xVREG1OUT	1 1 0 0 0 0 0	0.876xVREG1OUT
0 1 0 0 0 0 1	0.624xVREG1OUT	1 1 0 0 0 0 1	0.880xVREG1OUT
0 1 0 0 0 1 0	0.628xVREG1OUT	1 1 0 0 0 1 0	0.884xVREG1OUT
0 1 0 0 0 1 1	0.632xVREG1OUT	1 1 0 0 0 1 1	0.888xVREG1OUT
0 1 0 0 1 0 0	0.636xVREG1OUT	1 1 0 0 1 0 0	0.892xVREG1OUT
0 1 0 0 1 0 1	0.640xVREG1OUT	1 1 0 0 1 0 1	0.896xVREG1OUT
0 1 0 0 1 1 0	0.644xVREG1OUT	1 1 0 0 1 1 0	0.900xVREG1OUT
0 1 0 0 1 1 1	0.648xVREG1OUT	1 1 0 0 1 1 1	0.904xVREG1OUT
0 1 0 1 0 0 0	0.652xVREG1OUT	1 1 0 1 0 0 0	0.908xVREG1OUT
0 1 0 1 0 0 1	0.656xVREG1OUT	1 1 0 1 0 0 1	0.912xVREG1OUT
0 1 0 1 0 1 0	0.660xVREG1OUT	1 1 0 1 0 1 0	0.916xVREG1OUT
0 1 0 1 0 1 1	0.664xVREG1OUT	1 1 0 1 0 1 1	0.920xVREG1OUT
0 1 0 1 1 0 0	0.668xVREG1OUT	1 1 0 1 1 0 0	0.924xVREG1OUT
0 1 0 1 1 0 1	0.672xVREG1OUT	1 1 0 1 1 0 1	0.928xVREG1OUT
0 1 0 1 1 1 0	0.676xVREG1OUT	1 1 0 1 1 1 0	0.932xVREG1OUT
0 1 0 1 1 1 1	0.680xVREG1OUT	1 1 0 1 1 1 1	0.936xVREG1OUT
0 1 1 0 0 0 0	0.684xVREG1OUT	1 1 1 0 0 0 0	0.940xVREG1OUT
0 1 1 0 0 0 1	0.688xVREG1OUT	1 1 1 0 0 0 1	0.944xVREG1OUT
0 1 1 0 0 1 0	0.692xVREG1OUT	1 1 1 0 0 1 0	0.948xVREG1OUT
0 1 1 0 0 1 1	0.696xVREG1OUT	1 1 1 0 0 1 1	0.952xVREG1OUT
0 1 1 0 1 0 0	0.700xVREG1OUT	1 1 1 0 1 0 0	0.956xVREG1OUT
0 1 1 0 1 0 1	0.704xVREG1OUT	1 1 1 0 1 0 1	0.960xVREG1OUT

0 1 1 0 1 1 0	0.708xVREG1OUT	1 1 1 0 1 1 0	0.964xVREG1OUT
0 1 1 0 1 1 1	0.712xVREG1OUT	1 1 1 0 1 1 1	0.968xVREG1OUT
0 1 1 1 0 0 0	0.716xVREG1OUT	1 1 1 1 0 0 0	0.972xVREG1OUT
0 1 1 1 0 0 1	0.720xVREG1OUT	1 1 1 1 0 0 1	0.976xVREG1OUT
0 1 1 1 0 1 0	0.724xVREG1OUT	1 1 1 1 0 1 0	0.980xVREG1OUT
0 1 1 1 0 1 1	0.728xVREG1OUT	1 1 1 1 0 1 1	0.984xVREG1OUT
0 1 1 1 1 0 0	0.732xVREG1OUT	1 1 1 1 1 0 0	0.988xVREG1OUT
0 1 1 1 1 0 1	0.736xVREG1OUT	1 1 1 1 1 0 1	0.992xVREG1OUT
0 1 1 1 1 1 0	0.740xVREG1OUT	1 1 1 1 1 1 0	0.996xVREG1OUT
0 1 1 1 1 1 1	0.744xVREG1OUT	1 1 1 1 1 1 1	1.000xVREG1OUT

VDV(4-0): Specify the VCOM amplitude factors for panel common driving (VCOML = VCOMH –VCOM amplitude, VCOML ≥ VCL+0.5V). It is possible to setup from 0.7 to 1.32 times of VREG1OUT. When VCOMG = 0, the VDV(4-0) setup is invalid and VCOML is output VSSA

VDV[4:0]	VMAG
0 0 0 0 0	0.70xVREG1OUT
0 0 0 0 1	0.72xVREG1OUT
0 0 0 1 0	0.74xVREG1OUT
0 0 0 1 1	0.76xVREG1OUT
0 0 1 0 0	0.78xVREG1OUT
0 0 1 0 1	0.80xVREG1OUT
0 0 1 1 0	0.82xVREG1OUT
0 0 1 1 1	0.84xVREG1OUT
0 1 0 0 0	0.86xVREG1OUT
0 1 0 0 1	0.88xVREG1OUT
0 1 0 1 0	0.90xVREG1OUT
0 1 0 1 1	0.92xVREG1OUT
0 1 1 0 0	0.94xVREG1OUT
0 1 1 0 1	0.96xVREG1OUT
0 1 1 1 0	0.98xVREG1OUT
0 1 1 1 1	1.00xVREG1OUT
1 0 0 0 0	1.02xVREG1OUT
1 0 0 0 1	1.04xVREG1OUT
1 0 0 1 0	1.06xVREG1OUT
1 0 0 1 1	1.08xVREG1OUT
1 0 1 0 0	1.10xVREG1OUT
1 0 1 0 1	1.12xVREG1OUT
1 0 1 1 0	1.14xVREG1OUT
1 0 1 1 1	1.16xVREG1OUT
1 1 0 0 0	1.18xVREG1OUT
1 1 0 0 1	1.20xVREG1OUT
1 1 0 1 0	1.22xVREG1OUT
1 1 0 1 1	1.24xVREG1OUT
1 1 1 0 0	1.26xVREG1OUT
1 1 1 0 1	1.28xVREG1OUT
1 1 1 1 0	1.30xVREG1OUT
1 1 1 1 1	1.32xVREG1OUT

Restriction

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

Flow Chart

6.2.61 Set Power for Normal mode (D2h)

D2H	SETNORPOW												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	1	0	1	0	0	1	0	D2
1st parameter	1	1	↑	-	0	0	0	0	0	SAP0[2:0]			XX
2nd parameter	1	1	↑	-	0	DC10[2:0]			0	DC00[2:0]			XX

Description

SAP0[2:0]: Adjust the amount of fixed current from the fixed current source for the source and gamma driver operational amplifier in the Normal display.

SAP0[2:0]			Gamma Driver Amplifier	Source Driver Amplifier
0	0	0	Operation Stop	Operation Stop
0	0	1	1.00	1.00
0	1	0	1.00	0.75
0	1	1	1.00	0.50
1	0	0	0.75	1.00
1	0	1	0.75	0.75
1	1	0	0.75	0.50
1	1	1	0.5	0.50

DC00[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Normal mode.

DC00[2:0]			**Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1**
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	Setting Inhibited
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

DC10[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Normal mode.

DC10[2:0]			**Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3**
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	Setting Inhibited
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

Note: Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

Restriction

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

Flow Chart

6.2.62 Set Power for Partial mode (D3h)

D3H	SETPARPOW												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	1	0	1	0	0	1	1	D3
1st parameter	1	1	↑	-	0	0	0	0	0	SAP1[2:0]			XX
2nd parameter	1	1	↑	-	0	DC11[2:0]			0	DC01[2:0]			XX

Description

SAP1[2:0]: Adjust the amount of fixed current from the fixed current source for the source and gamma driver operational amplifier in the Normal display.

SAP1[2:0]			Gamma Driver Amplifier	Source Driver Amplifier
0	0	0	Operation Stop	Operation Stop
0	0	1	1.00	1.00
0	1	0	1.00	0.75
0	1	1	1.00	0.50
1	0	0	0.75	1.00
1	0	1	0.75	0.75
1	1	0	0.75	0.50
1	1	1	0.5	0.50

DC01[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Partial mode.

DC01[2:0]			Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	Setting Inhibited
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

DC11[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Partial mode.

DC11[2:0]			Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	Setting Inhibited
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

Note: Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

Restriction

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

Flow Chart

6.2.63 Set Power for Idle mode (D4h)

D4H	SETIDLPOW												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	1	0	1	0	1	0	0	D4
1st parameter	1	1	↑	-	0	0	0	0	0	SAP2[2:0]			XX
2nd parameter	1	1	↑	-	0	DC12[2:0]			0	DC02[2:0]			XX

Description

SAP2[2:0]: Adjust the amount of fixed current from the fixed current source for the source and gamma driver operational amplifier in the Normal display.

SAP2[2:0]			Gamma Driver Amplifier	Source Driver Amplifier
0	0	0	Operation Stop	Operation Stop
0	0	1	1.00	1.00
0	1	0	1.00	0.75
0	1	1	1.00	0.50
1	0	0	0.75	1.00
1	0	1	0.75	0.75
1	1	0	0.75	0.50
1	1	1	0.5	0.50

DC02[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Idle mode.
For details, please refer to “5.6 Oscillator” section.

DC02[2:0]			Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	Setting Inhibited
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

DC12[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Idle mode.

DC12[2:0]			Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	Setting Inhibited
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

Note: Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

Restriction

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

Flow Chart

6.2.64 Set ID (E0h)

E0 H	SETID (Set ID)												
	DCX	**RDX**	**WRX**	**D15-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	1	1	0	0	0	0	0	E0
1st parameter	1	↑	1	-	ID1[7:0]								--
2nd parameter	1	↑	1	-	ID2[7:0]								--
3rd parameter	1	↑	1	-	ID3[7:0]								--
4th parameter	1	↑	1	-	ID4[7:0]								--
Description	**ID1~4:** User can program any value to OTP for module number.												
Restrictions	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All 0x00h
S/W Reset	No Change
H/W Reset	OTP value

Flow Chart

6.2.65 Set OTP Related Setting (E2h)

E2 H	SETOTP(Set OTP Related Setting)												
	DCX	**RDX**	**WRX**	**D15-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	1	1	0	0	0	1	0	E2
1st parameter	1	↑	1	-	OTP_MASK[7:0]								-
2nd parameter	1	↑	1	-	OTP_INDEX[7:0]								-
3rd parameter	1	↑	1	-	OTP_LOAD_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM[1:0]		VPP_SEL	OTP_PROG	-
4th parameter	1	↑	1	-	OTP_DATA[7:0]								-
Description	This command is used to set OTP Related Setting **OTP_MASK[7:0]:** Bit programming mask, if 1, means don't programming this bit **OTP_INDEX[6:0]:** Set location of OTP to be programmed **OTP_LOAD_DISABLE:** When written to 1, auto load from OTP to internal register when SLPOUT command received is disabled, this is used when OTP is not yet programmed **OTP_TEST:** Internal use, not open. Please set "0". **OTP_POR:** OTP read control bit. **OTP_PWE:** Internal use, not open. Please set "0". **OTP_PTM[1:0]:** Internal use, not open. Please set "00". **VPP_SEL:** Internal use, not open. Please set "0". **OTP_PROG:** When set OTP_PROG=1, internal register begin written to OTP. Please refer to "5.14.2 OTP programming flow". **OTP_DATA[7:0]:** OTP data of read OTP index.												
Restrictions	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OTP_MASK[7:0]=8'h00, OTP_INDEX[6:0]=7'h7F, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_TEST=0, OTP_POR=0, OTP_PWE=0, OTP_PTM[1:0]=2'b00, VPP_SEL=0, OTP_PROG=0
S/W Reset	No change
H/W Reset	OTP_MASK[7:0]=8'h00, OTP_INDEX[6:0]=7'h7F, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_TEST=0, OTP_POR=0, OTP_PWE=0, OTP_PTM[1:0]=2'b00, VPP_SEL=0, OTP_PROG=0

Flow Chart

6.2.66 SETOTPKEY (E3h)

<table>
<tr><td>E3 H</td><td colspan="13">SET OTP_KEY</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>E3</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td colspan="8">OTP_KEY[7:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="13">OTP_KEY[7:0]: To enter or leave OTP program mode.
When enter OTP program mode, other user commands can’t be set. Only stop OTP program and set OTP_KEY[7:0]=55h, leave OTP program mode, then the other user commands can be set.
<table>
<tr><td>OTP_KEY[7:0]</td><td>Description</td><td>Note</td></tr>
<tr><td>AAh</td><td>Enter OTP program mode</td><td></td></tr>
<tr><td>55h</td><td>Leave OTP program mode</td><td></td></tr>
<tr><td>Other values</td><td>Invalid</td><td>If OTP is in OTP program mode, then keep OTP program mode
If OTP is in non-OTP program mode, then keep non-OTP program mode.</td></tr>
</table>
OTP_KEY[7:0] can be ignored when user want to do OTP program.</td></tr>
<tr><td>Restrictions</td><td colspan="13">SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>OTP_KEY[7:0]=8’h00</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>OTP_KEY[7:0]=8’h00</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>

6.2.67 SETCABC(E4h)

<table>
<tr><td>E4 H</td><td colspan="13">SETCABC</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>E4</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>0</td><td colspan="2">SEL_PWMCLK[2:0]</td><td colspan="2">SEL_GAIN[1:0]</td><td>INVPULS</td><td>SEL_BLDUTY</td><td>-</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td colspan="8">PWM_PERIOD[7:0]</td><td>-</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>0</td><td colspan="8">DIM_FRAME[6:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="13">
SEL_PWMCLK[2:0]: Internal PWM_CLK divider for CABC clock.
<table>
<tr><td>SEL_PWMCLK[2:0]</td><td>Divider</td></tr>
<tr><td>0</td><td>PWM_CLK/1</td></tr>
<tr><td>1</td><td>PWM_CLK/2</td></tr>
<tr><td>2</td><td>PWM_CLK/4</td></tr>
<tr><td>3</td><td>PWM_CLK/8</td></tr>
<tr><td>4</td><td>PWM_CLK/16</td></tr>
<tr><td>5</td><td>PWM_CLK/32</td></tr>
<tr><td>6</td><td>PWM_CLK/64</td></tr>
<tr><td>7</td><td>PWM_CLK/128</td></tr>
</table>
Note:1. PWM_CLK is OSC frequency in any interface

SEL_GAIN[1:0]: Internal use, not open. Please set to”11”.

INVPULS: The polarity setting of PWM_OUT.
Condition: BL=1, BCTRL=1 and DBV[7:0]=0x00h
INVPULS=1, PWM_OUT will pull Low.
INVPULS=0, PWM_OUT will pull High.

SEL_BLDUTY: Internal use, not open. Please set to”1”.

PWM_PERIOD[7:0]: The backlight PWM output period setting.
Backlight PWM output period =1 / [(PWM_CLK / clock divider (PWM_DIV)) x (255 x PWM_PERIOD[7:0])]

DIM_FRAME[6:0]: Manual brightness setting dimming period.
</td></tr>
<tr><td>Restriction</td><td colspan="13">SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Display On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Display On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td>PWM_PERIOD[7:0]= OTP value, DIM_FRAME[6:0]=OTP value
Others=No Change</td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>

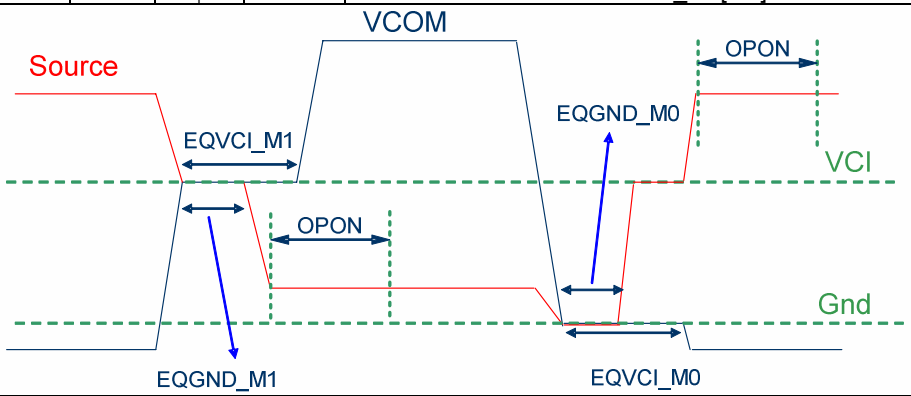
6.2.68 Set Panel related (E9h)

E9 H	SETPANEL												
	DCX	**RDX**	**WRX**	**D17-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	0	1	↑	-	1	1	1	0	1	0	0	1	E9
1st parameter	1	1	↑	-	0	0	0	0	SS_PANEL	0	0	BGR_PANEL	XX
Description	This command is internal use for display panel setting. **SS_PANEL:** The source driver output shift direction selected. When SS_PANEL = 0, the shift direction don't reverse. When SS_PANEL = 1, the shift direction will be reversed. **BGR_PANEL:** The color filter order direction selected.												
Restriction													
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	Status: Power On Sequence — Default Value: Status: S/W Reset — Default Value: No change Status: H/W Reset — Default Value:												
Flow Chart													

6.2.69 Set EQ function (EEh)

EEH	SETEQ												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	1	1	1	0	EE
1st parameter	1	1	↑	-	EQVCI_M1[7:0]								XX
2nd parameter	1	1	↑	-	EQGND_M1[7:0]								XX
3rd parameter	1	1	↑	-	EQVCI_M0[7:0]								XX
4th parameter	1	1	↑	-	EQGND_M0[7:0]								XX

Description



Restriction

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

Flow Chart

7. Layout Recommendation

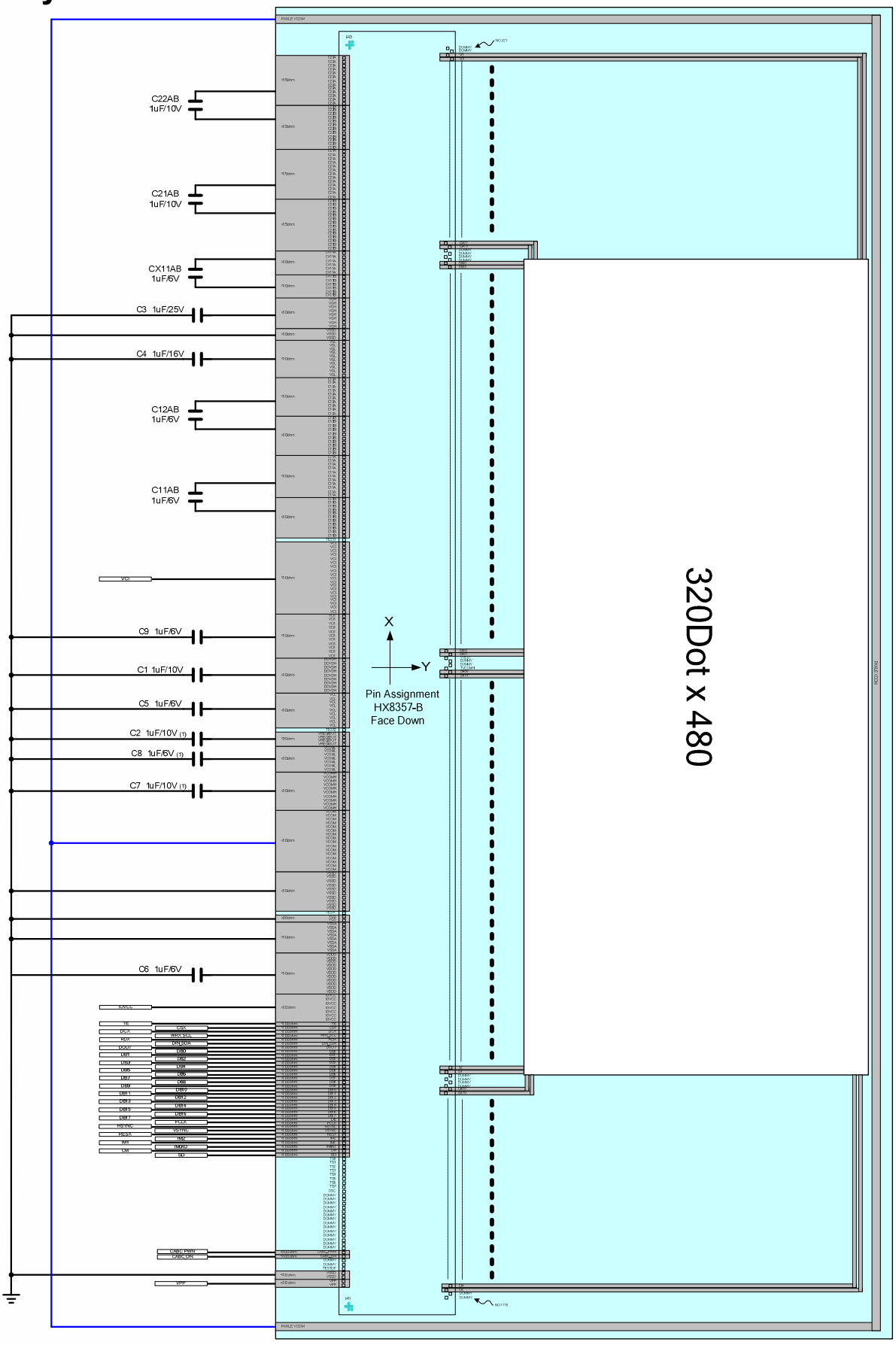


Figure 7.1: Layout Recommendation of HX8357-B

7.1 Maximum layout resistance

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VPP	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
IM[2:0], SD, CM	Input	100	Ω
CSX, DCX, WRX_SCL, RDX, RESX	Input	100	Ω
PCLK, DE, VSYNC, HSYNC	Input	100	Ω
VGS	Input	30	Ω
TEST[3:1]	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCL	Capacitor connection	10	Ω
VCI1	Capacitor connection	10	Ω
DDVDH	Capacitor connection	10	Ω
VDDD	Capacitor connection	10	Ω
VREG1OUT, VREG2OUT, VREG3OUT, VREG4OUT	Capacitor connection	30	Ω
VCOM	Panel connection	10	Ω
VCOMH, VCOML	Capacitor connection	10	Ω
C11A, C11B, CX11A, CX11B	Capacitor connection	10	Ω
C12A, C12B	Capacitor connection	10	Ω
C21A, C21B	Capacitor connection	15	Ω
C22A, C22B	Capacitor connection	15	Ω
TE, DOUT, CABC_ON, CABC_PWM	Output	100	Ω
DIN_SDA, DB[17:0]	Input/Output	100	Ω

Table 7.1: Maximum Layout Resistance

7.2 External Components Connection

Capacitor	Recommended voltage	Capacity	Note
C1 (DDVDH-VSSA)	10V	1μF (B characteristics)	-
C2 (VREG1OUT-VSSA)	10V	1μF (B characteristics)	Note(1)
C3 (VGH-VSSA)	25V	1μF (B characteristics)	-
C4 (VGL-VSSA)	16V	1μF (B characteristics)	-
C5 (VCL-VSSA)	6V	1μF (B characteristics)	-
C6(VDD-VSSA)	6V	1μF (B characteristics)	-
C7 (VCOMH-VSSA)	10V	1μF (B characteristics)	Note(1)
C8 (VCOML-VSSA)	6V	1μF (B characteristics)	Note(1)
C9 (VCI1-VSSA)	6V	1μF (B characteristics)	Note(1)
C11AB (C11A/B)	6V	1μF (B characteristics)	-
CX11AB (CX11A/B)	6V	1μF (B characteristics)	-
C12AB (C12A/B)	6V	1μF (B characteristics)	-
C21AB (C21A/B)	10V	1μF (B characteristics)	-
C22AB (C22A/B)	10V	1μF (B characteristics)	-

Note: (1) If Display quality normal, the C2, C7, C8 and C9 can remove.

8. Electrical Characteristic

8.1 Absolute Maximum Ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3 to +3.6	Note(1),(2)
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3 to +3.6	Note(1),(3)
Power Supply Voltage 3	DDVDH ~ GAND	V	-0.3 to +6.6	Note(4)
Power Supply Voltage 4	VSSA ~ VCL	V	-0.3 to -3.6	Note(5)
Power Supply Voltage 5	DDVDH ~ VCL	V	-0.3 to +9.6	Note(6)
Power Supply Voltage 6	VGH ~ VSSA	V	-0.3 to +18.5	Note(7)
Power Supply Voltage 7	VSSA ~ VGL	V	0 to -16.5	Note(8)
Input Voltage	V_{IN}	V	-0.3 to IOVCC+0.3	-
Operating Temperature	Topr	℃	-40 to +85	Note(9),(10)
Storage Temperature	Tstg	℃	-55 to +110	Note(9),(10)

Note: (1) IOVCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure DDVDH ≥ VSSA.
(5) To make sure VSSA ≥ VCL.
(6) To make sure DDVDH ≥ VCL.
(7) To make sure VGH ≥ VSSA.
(8) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(9) For die and wafer products, specified up to +85℃.
(10) This temperature specifications apply to the TCP package.

8.2 DC Characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70℃)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	IOVCC= 1.65 ~ 3.3V	0.7xIOVCC	-	IOVCC	-
Input low voltage	V_{IL}	V	IOVCC= 1.65 ~ 3.3V	-0.3V	-	0.3xIOVCC	-
Output high voltage(1) (DB17-0 Pins)	V_{OH1}	V	I_{OH} = -0.1 mA	0.8xIOVCC	-	-	-
Output low voltage (DB17-0 Pins)	V_{OL1}	V	IOVCC= 1.65 ~ 2.4V I_{OL} = 0.1mA	-	-	0.2xIOVCC	-
I/O leakage current	I_{Li}	µA	Vin = 0 ~ IOVCC	-1	-	1	-
Current consumption during normal operation (IOVCC – VSSD)	$I_{OP(IOVCC)}$	µA	IOVCC=VCI=2.8V , T_A=25°C , GRAM data = 0000h, Frame rate = 60Hz, REV=0, AP=100, DC0=00, DC01=11, BT=1000, DC=111, VRH=0011, VCM=0100000,VDV=01110, VCOMG=1	-	TBD	-	-
Current consumption during normal operation (VCI – VSSA)	$I_{OP(VCI)}$	mA		-	TBD	-	-
Current consumption during sleep in mode (IOVCC – VSSD)	$I_{SL(IOVCC)}$	µA	IOVCC=VCI=2.8V , T_A =25°C	-	TBD	-	-
Current consumption during sleep in mode (VCI – VSSA)	$I_{SL(VCI)}$	µA		-	TBD	-	
Current consumption during deep-standby mode (IOVCC – VSSD)	$I_{D\_STB(IOVCC)}$	µA	IOVCC=VCI=2.8V , T_A =25°C	-	1	-	-
Current consumption during deep-standby (VCI – VSSA)	$I_{D\_STB(VCI)}$	µA		-	1	-	
Output voltage deviation	-	mV	-	-	TBD	-	-
Dispersion of the Average Output Voltage	V	mV	-	-	TBD	-	-

Table 8.1: DC Characteristic

8.3 AC Characteristics

8.3.1 DBI Type-B interface characteristics

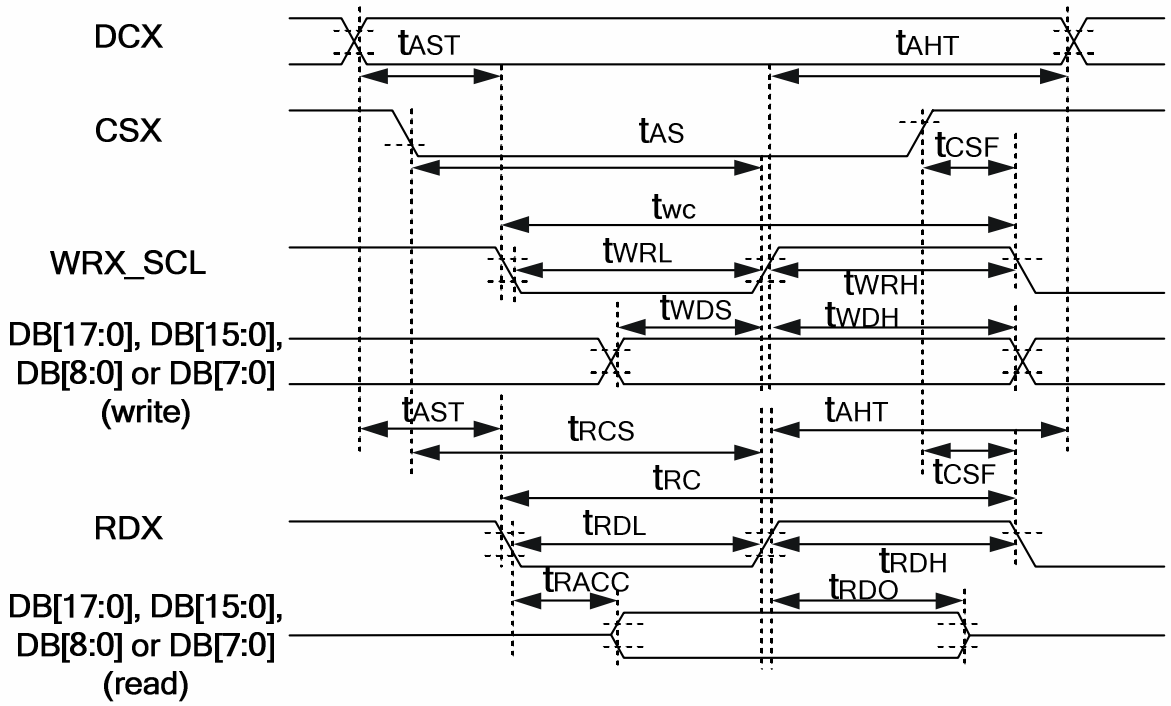


Figure 8.1: DBI Type-B interface characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX	tAST tAHT	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
CSX	tCS tRCS tCSF	Chip select setup time (Write) Chip select setup time (Read) Chip select wait time (Write/Read)	20 20 20	- - -	ns	-
WRX_SCL	tWC tWRH tWRL	Write cycle Control pulse “H” duration Control pulse “L” duration	100 30 25	- - -	ns	-
RDX	tRC tRDH tRDL	Read cycle Control pulse “H” duration Control pulse “L” duration	450 250 170	- - -	ns	-
DB[17:0], DB[15:0], DB[8:0], or DB[7:0]	tWDT tWHT tRACC tROH	Data setup time Data hold time Read access time Output disable time	15 25 10 10	- - 340 -	ns	For maximum CL=30pF For minimum CL=8pF

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 8.2: DBI Type-B Interface Characteristics

8.3.2 DBI Type-C interface characteristics

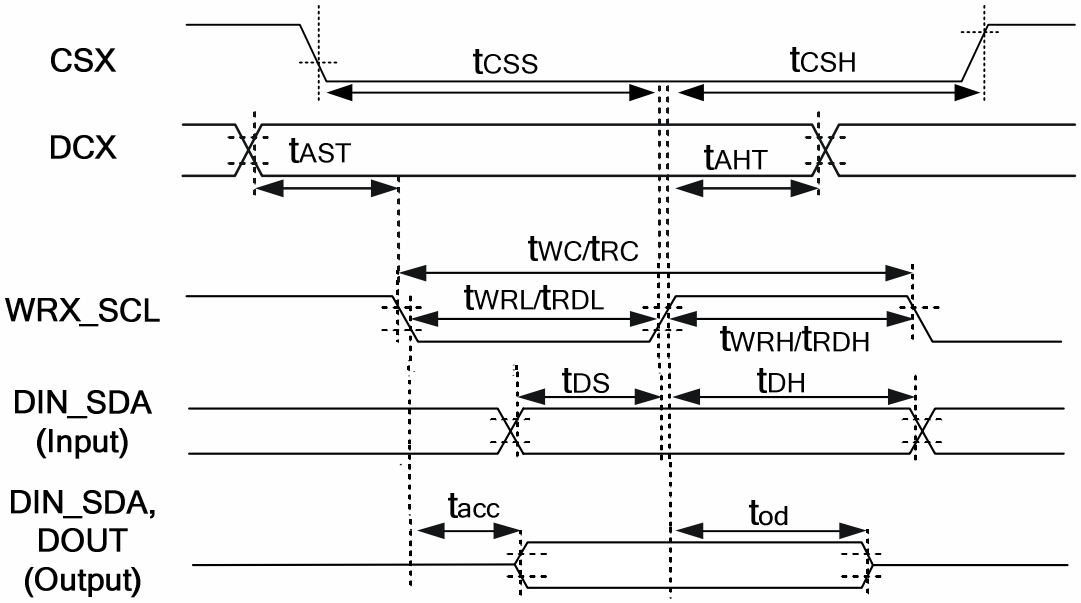


Figure 8.2: DBI Type-C interface characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{CSS} t_{CSH}	Chip select setup time (Write) Chip select setup time (Read)	40 40	- -	ns	-
DCX	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
WRX_SCL (Write)	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse “H” duration Control pulse “L” duration	100 40 40	- - -	ns	-
WRX_SCL (Read)	t_{RC} t_{RDH} t_{RDL}	Read cycle Control pulse “H” duration Control pulse “L” duration	300 120 120	- - -	ns	-
DIN_SDA (Input)	t_{DS} t_{DT}	Data setup time Data hold time	30 30	- -	ns	For maximum C_L=30pF For minimum C_L=8pF
DIN_SDA, DOUT (Output)	t_{RACC} t_{OD}	Read access time Output disable time	- 10	100 -	ns	

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 8.3: DBI Type-C Interface Characteristics

8.3.3 DPI Interface Characteristics

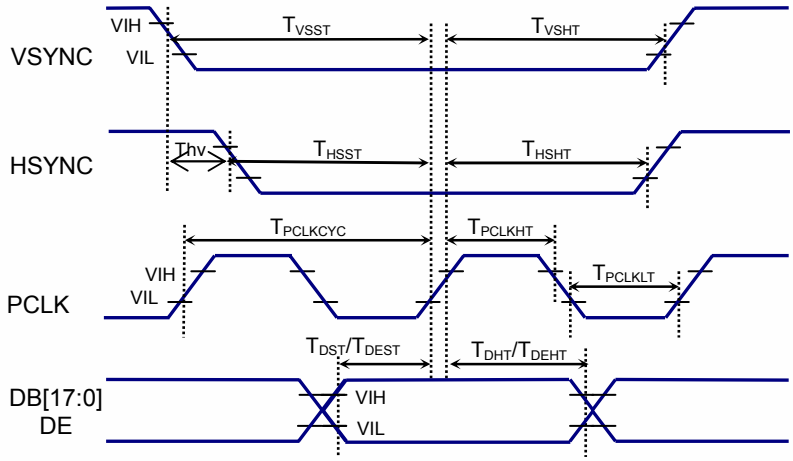


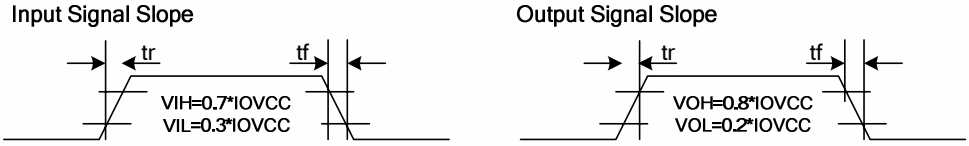
Figure 8.3: DPI Interface Characteristics 1

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70℃)

Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
PCLK cycle time	T_{DCYC}	-	125	-	-	ns
Pixel low pulse width	T_{CLKLT}	-	15	-	-	ns
Pixel high pulse width	T_{CLKHT}	-	15	-	-	ns
Vertical Sync. set-up time	T_{VSST}	-	15	-	-	ns
Vertical Sync. hold time	T_{VSSHT}	-	15	-	-	ns
Horizontal Sync. set-up time	T_{HSST}	-	15	-	-	ns
Horizontal Sync. hold time	T_{VSSHT}	-	15	-	-	ns
Data Enable set-up time	T_{DEST}	-	15	-	-	ns
Data Enable hold time	T_{DEHT}	-	15	-	-	ns
Data setup time	T_{DST}	-	15	-	-	ns
Data hold time	T_{DHT}	-	15	-	-	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Table 8.4: DPI Interface Characteristics 1



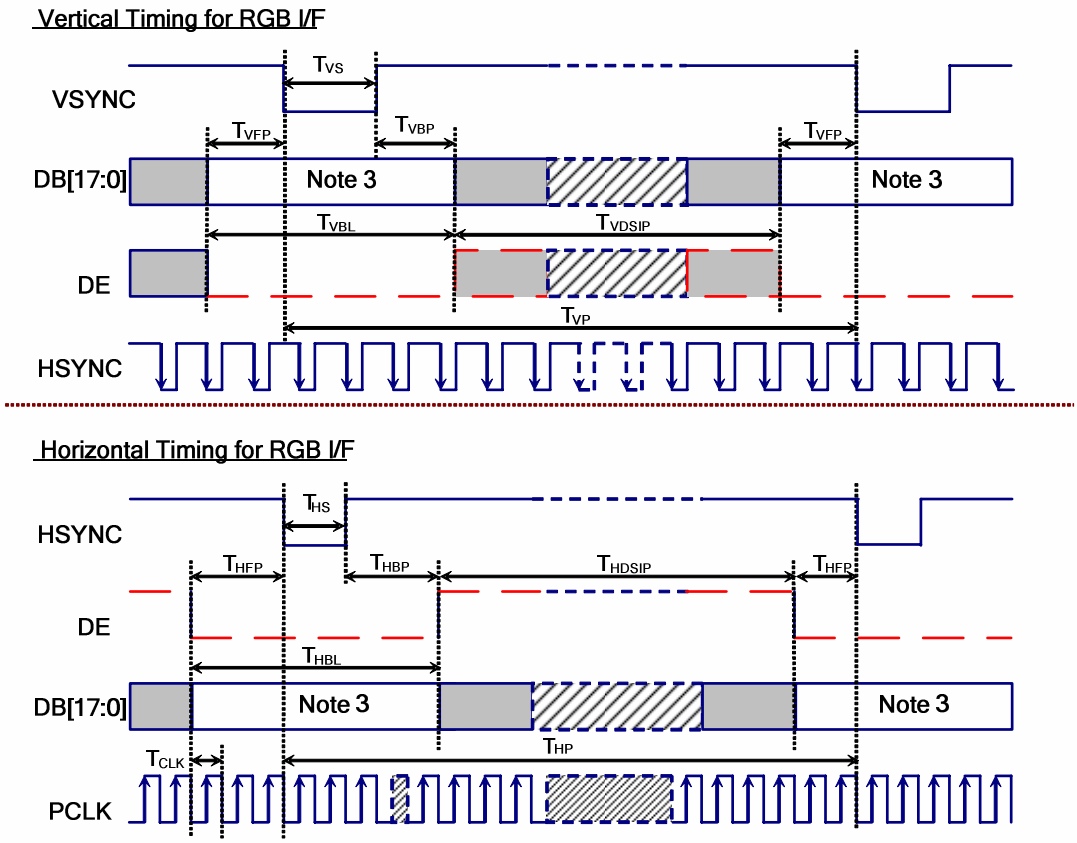


Figure 8.4: DPI Interface Characteristics 2

Item	Symbol	Condition	Specification			Unit
			Min	Typ.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	-	486	-	-	HS
Vertical low pulse width	T_{VS}	-	2	-	-	HS
Vertical front porch	T_{VFP}	-	2	-	-	HS
Vertical back porch	T_{VBP}	-	2	-	-	HS
Vertical blanking period	T_{VBL}	$T_{VS} + T_{VBP} + T_{VFP}$	6	-	-	HS
Vertical active area	T_{VDISP}	-		480		HS
Vertical refresh rate	TVRR	Frame rate	-	60	-	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	-	326	-	-	PCLK
Horizontal low pulse width	T_{HS}	-	2	-	-	PCLK
Horizontal front porch	T_{HFP}	-	2	-	-	PCLK
Horizontal back porch	T_{HBP}	-	2	-	-	PCLK
Horizontal blanking period	T_{HBL}	$T_{HS} + T_{HBP} + T_{HFP}$	6	-	-	PCLK
Horizontal active area	T_{HDISP}	-		320		PCLK
Pixel clock cycle TVRR=60Hz	f_{CLKCYC}	-	-	8	-	MHz

Note: (1) IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, VSSA=VSSD=0V, Ta=-30 to 70℃ (to +85℃ no damage)
(2) Data lines can be set to "High" or "Low" during blanking time – Don't care.
(3) HP is multiples of PCLK.

Table 8.5: DPI Interface Characteristics 2

8.3.4 Reset Input Timing

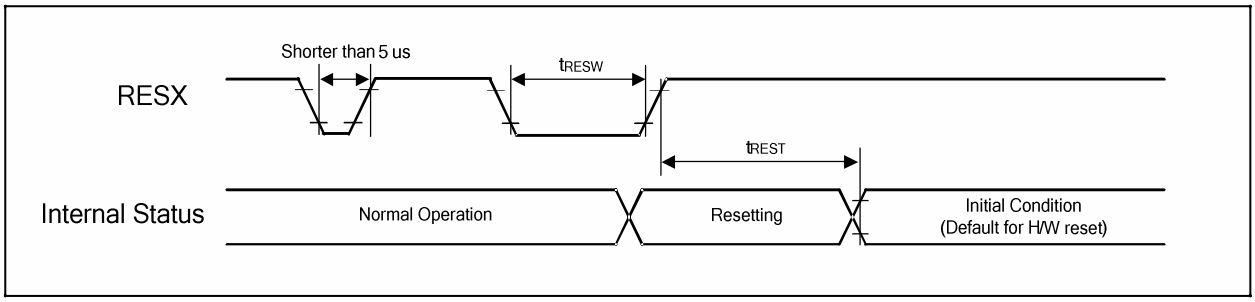


Figure 8.5: Reset Input Timing

Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
tRESW	Reset low pulse width(1)	RESX	10	-	-	-	µs
tREST	Reset complete time(1)	-	-	-	5	When reset applied during Sleep In mode	ms
		-		-	120	When reset applied during Sleep Out mode	ms

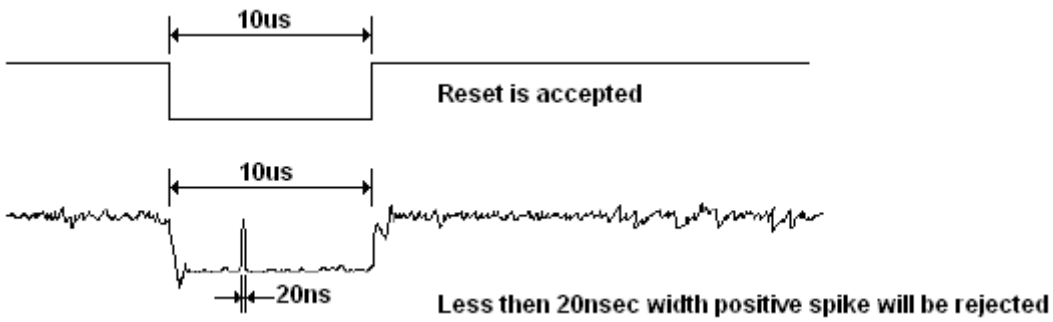
Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the following table. RESET Pulse.

RESET	**Action**
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5 µs and 10µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 1ms after a rising edge of RESX.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Table 8.6: Reset Input Timing

9. Ordering Information

Part No.	Package
HX8357-B000 PDxxx	PD : mean COG xxx : mean chip thickness (μm), (default: 250 μm)

10.Revision History

Version	Date	Description of Changes
01	2010/01/18	1. New setup
01	------	1. Modify the frame rtae of DPI Interface Characteristics 2 (P186) 2. Modify Operation Frequency of Step-up Circuit 1 and 2(P169, 170, 171)