Crystalfontz America, Inc.

SPECIFICATION

CUSTOMER : _____

MODULE NO.: CFAF320240L-035T-CTS

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	**PCB VERSION:** **DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

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	MODLE NO：
RECORDS OF REVISION	**DOC. FIRST ISSUE**

VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	06/21/12		First issue

Contents

1.Module Classification Information

CFA F 320240 L 035 T CTS
① ② ③ ④ ⑤ ⑥ ⑦

①	Brand：**CRYSTALFONTZ AMERICA, INC**		
②	Display Type：H→Character Type, G→Graphic Type **F→TFT Type**		
③	Displays Logical Dimensions: **320 pixels by 240 pixels**		
④	Model PCB Variant: **L**		
⑤	Module's diagonal physical dimension: **3.5”**		
⑥	Backlight Type：	F→CCFL, White	**T→LED, White**
⑦	Touch panel type: **Capacitive touch panel**		

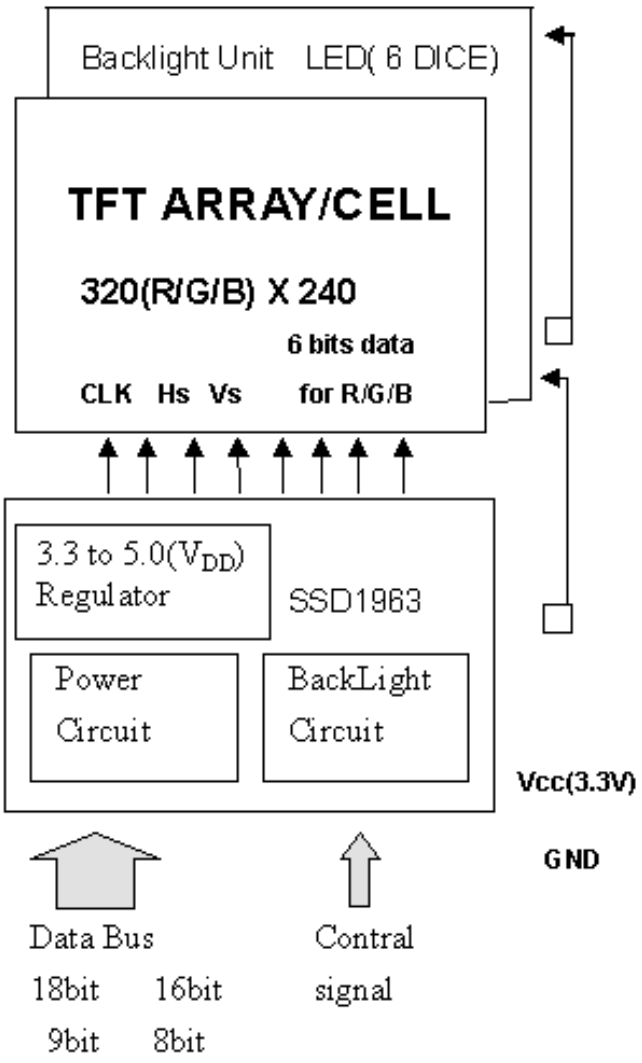
This product is composed of a TFT LCD panel, driver ICs, FPC, Control Board and a backlight unit. The following table described the features of the CFAF320240L-035T-CTS

Item	Dimension	Unit
Dot Matrix	320 x RGBx240(TFT)	dots
Module dimension	93.5 x 66.44 x 9.52	mm
View area	73.1x55.6	mm
Active area	70.08 x 52.56	mm
Dot size	0.073 x 0.219	
Driving IC package	COG	
LCD type	TFT, Negative, Transmissive	
View Direction	12 o’clock	
Gray Scale Inversion Direction	6 o’clock	
Backlight Type	LED,Normally White	
Controller IC	SSD1963	

*Expose the IC number blaze (Luminosity over than 1 cd) when using the LCM may cause IC operating failure.

*Color tone slight changed by temperature and driving voltage.

2.Block Diagram



3.Electrical Characteristics

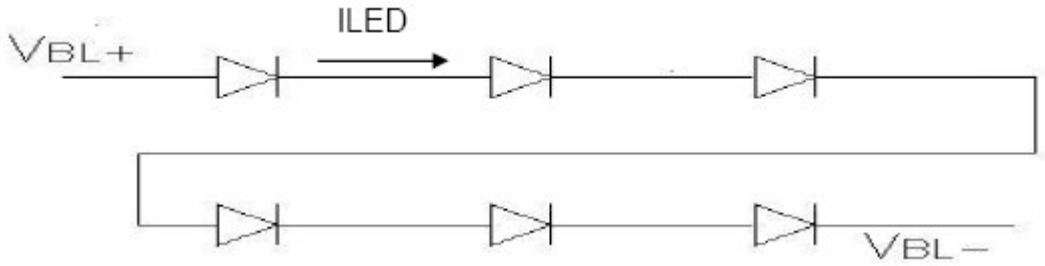
3.1 Operating conditions:

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VCC	—	3.0	3.3	3.6	V
Supply Current	I_{cc}	V_{CC}=3		213		mA

3.3 LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current		-	20	-	mA	
Power Consumption		-	400	420	mW	
LED voltage	VBL+	18.6	19.8	21	V	Note 1
LED Life Time	-		(50,000)-	-	Hr	Note 2,3

Note 1 : There are 1 Groups LED



Note 2 : Ta = 25 _

Note 3 : Brightness to be decreased to 50% of the initial value

4.Absolute Maximum Ratings

Item	Symbol	Condition	Min	Max	Unit	Remark
Power Voltage	DVDD,AVDD	GND=0	-0.3	5.0	V	
Input Signal Voltage	Vin	GND=0	-0.3	VDD+0.3	V	Note
Logic Output Voltage	VOUT	GND=0	-0.3	VDD+0.3	V	Note

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

5.Interface Pin Function

5.1 Pins Connection To Control Board

P/N	Symbol	8BIT Function
1	GND	Ground
2	VCC	Power supply for Logic
3	BL_E	Backlight control (H: On \ L: Off)
4	RS	Command/Data select
5	WR	8080 family MPU interface : Write signal
6	RD	8080 family MPU interface: Read signal
7	DB0	Data bus
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15	CS	Chip select
16	RES	REST
17	NC	No connection
18	FGND	Frame Gnd
19	NC	No connection
20	NC	No connection

5.2 CTP PIN Definition:

PIN NO.	SYMBOL	FUNCTION
1	VSS	GROUND
2	VDD	POWER SUPPLY VOLTAGE
3	SCL (SSEL)	I2C CLOCK INPUT (ACTIVE LOW SELECT SIGNAL)
4	NC (SCK)	NC (SERIAL DATA CLOCK)
5	SDA (MOSI)	I2C DATA INPUT AND OUTPUT (DATA LINE FROM MASTER TO SLAVE)
6	NC (MISO)	NC (DATA LINE FROM SLAVE TO MASTER)
7	/RST	EXTERNAL RESET, LOW IS ACTIVE
8	/WAKE	EXTERNAL INTERRUPT FROM THE HOST
9	/INT	EXTERNAL INTERRUPT TO THE HOST
10	VSS	GROUND

NOTE1: PIN NAMES IN () IS FOR SPI TYPE INTERFACE INTERNAL PULL UP ON PIN 3~6(100K Ω)

NOTE2:Control signal Voltage:3V~3.3V

6. DC CHARATERISTICS

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PSTY	Quiescent Power			300	500	uW
IIZ	Input leakage current		-1		1	uA
IOZ	Output leakage current		-1		1	uA
VOH	Output high voltage		0.8VDDIO			V
VOL	Output low voltage				0.2VDDIO	V
VIH	Input high voltage		0.8VDDIO		VDDIO + 0.5	V
VIL	Input low voltage				0.2VDDIO	V

7. AC Characteristics

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

CL = 50pF (Bus/CPU Interface)

CL = 0pF (LCD Panel Interface)

7.1 Clock Timing

Table 7-1:Clock Input Requirements for CLK (PLL-bypass)

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)		110	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 7-2:Clock Input Requirements for CLK

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)	2.5	50	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 7-3:Clock Input Requirements for crystal oscillator XTAL

Symbol	Parameter	Min	Max	Units
FXTAL	Input Clock Frequency	2.5	10	MHz
TXTAL	Input Clock period	1/fXTAL		ns

7.2 MCU Interface Timing

7.2.1 Parallel 6800-series Interface Timing

Table 7-4: Parallel 6800-series Interface Timing Characteristics (Use CS# as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tPWCSL	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 7-1: Parallel 6800-series Interface Timing Diagram (Use CS# as Clock)

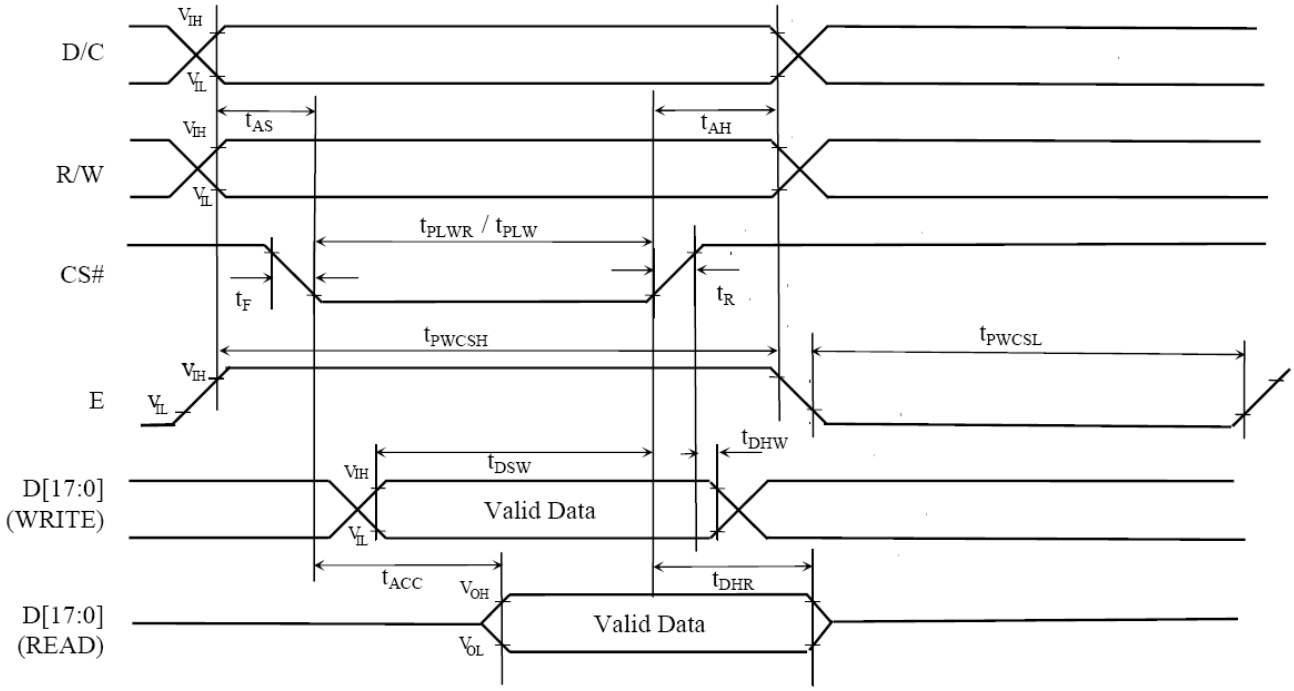
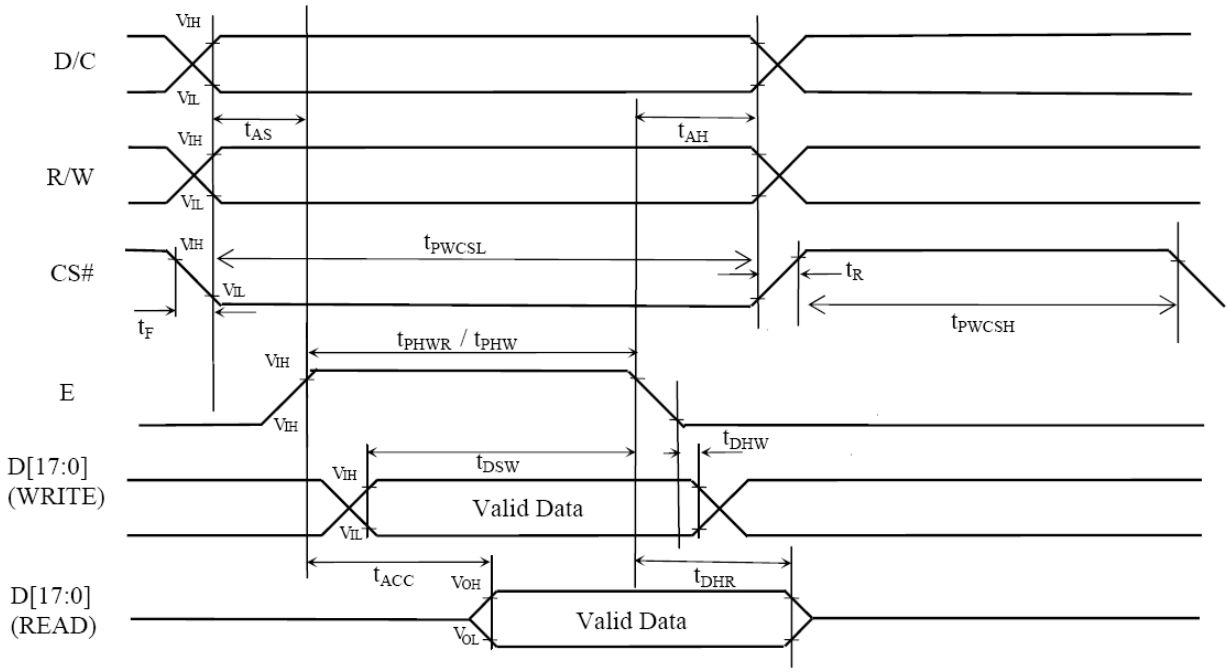


Table 7-5: Parallel 6800-series Interface Timing Characteristics (Use E as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tPWCSL	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure7-2: Parallel 6800-series Interface Timing Diagram (Use E as Clock)



7.2.2 Parallel 8080-series Interface Timing

Table 7-6: Parallel 8080-series Interface

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSL	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tAS	Address Setup Time		1	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Write Data Setup Time		4	-	-	ns
tDHW	Write Data Hold Time		1	-	-	ns
tPWLW	Write Low Time		12	-	-	ns
tDHR	Read Data Hold Time		1	-	-	ns
tACC	Access Time		32	-	-	ns
tPWLR	Read Low Time		36	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns
tCS	Chip select setup time		2	-	-	ns
tCSH	Chip select hold time to read signal		3	-	-	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 7-3: Parallel 8080-series Interface Timing Diagram (Write Cycle)

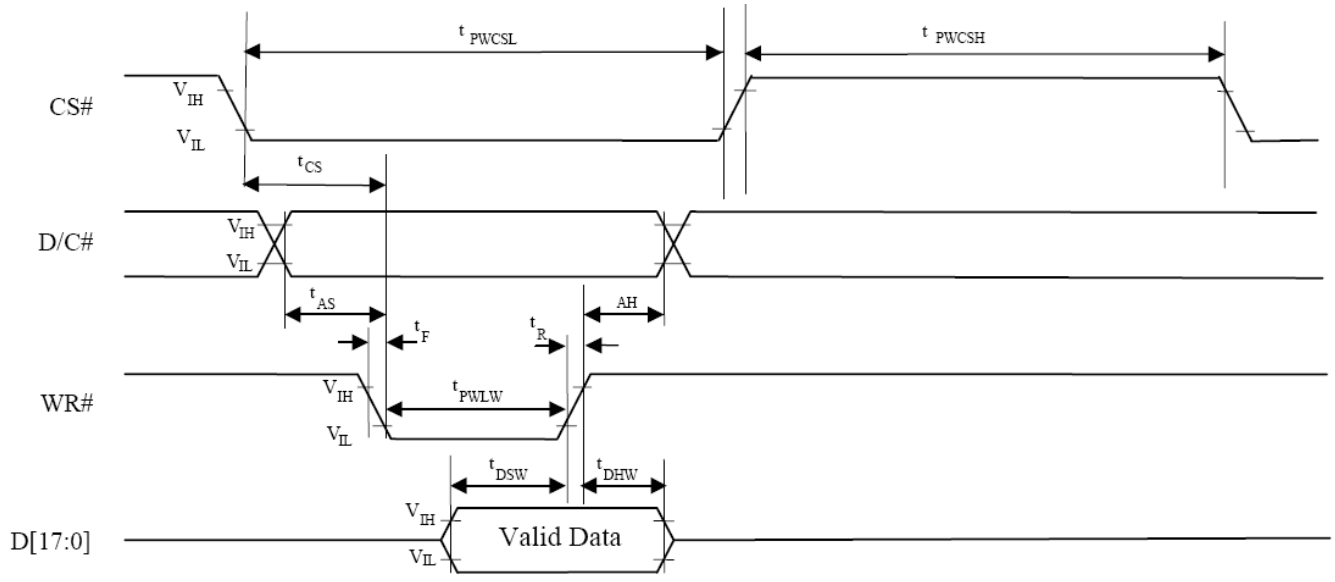
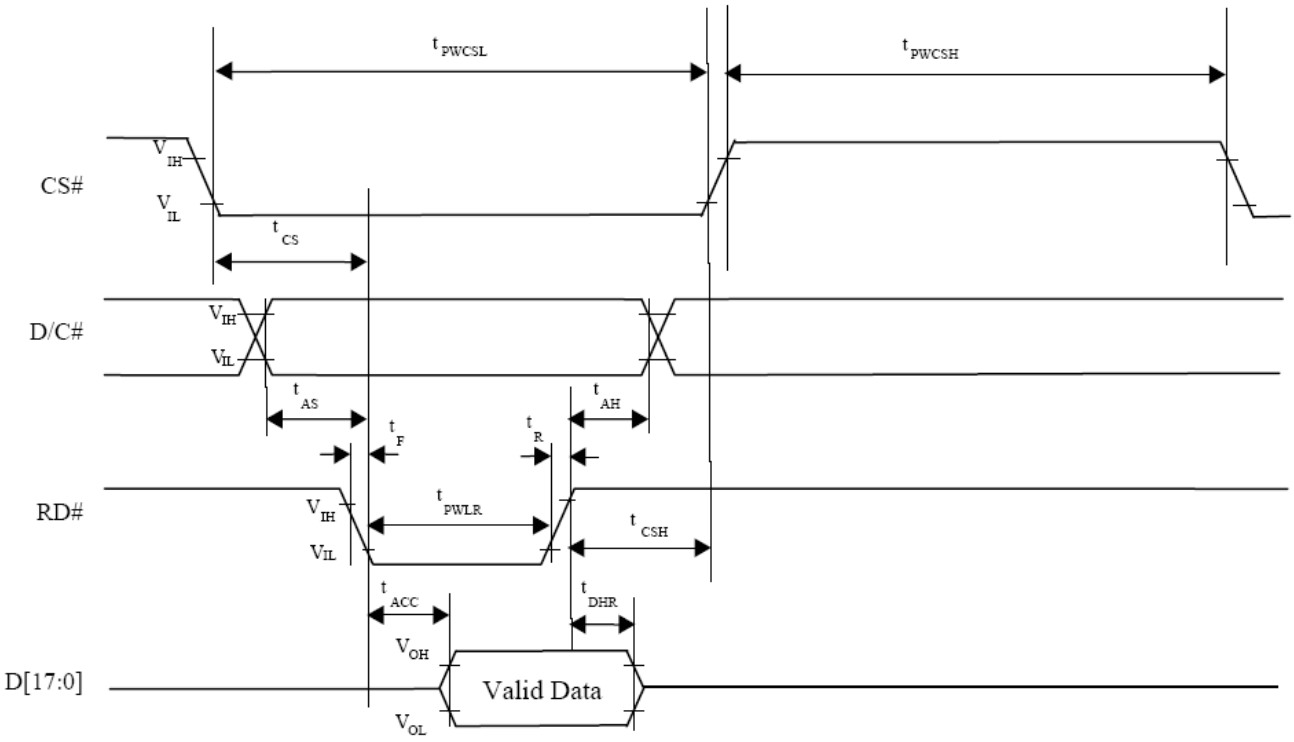
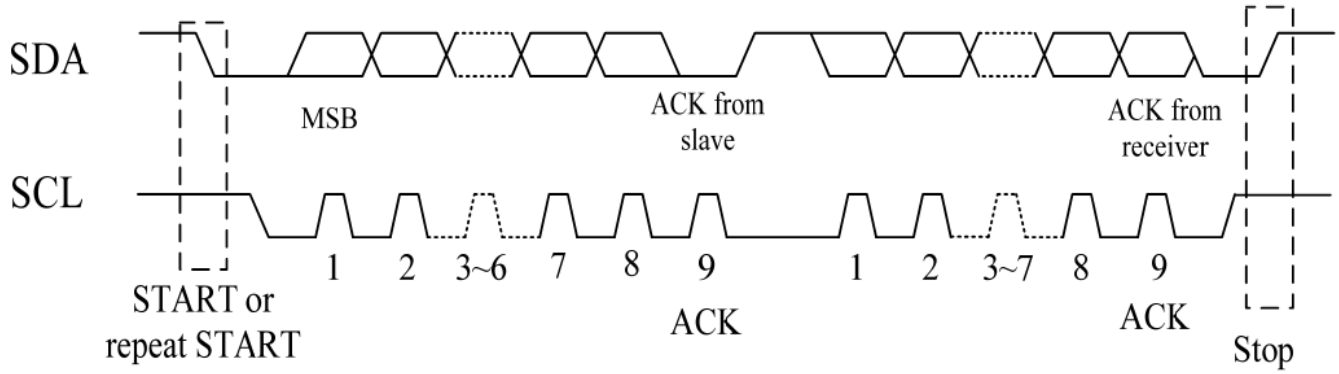


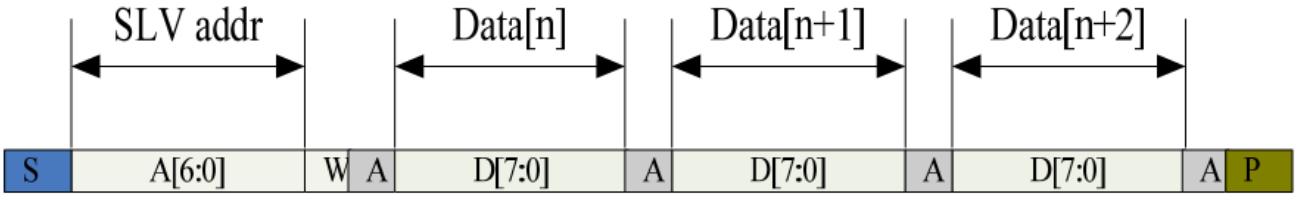
Figure 7-4: Parallel 8080-series Interface Timing Diagram (Read Cycle)



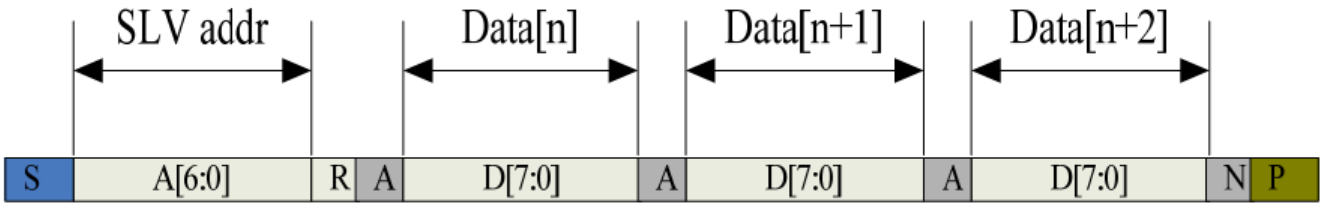
7.3 CTP I2C Timing:



I2C Serial Data Transfer Format



I2C master write, slave read



I2C master read, slave write

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address A[6:4]: 3'b011 A[3:0]: data bits are identical to those of I2CCON[7:4] register.
W	1'b0: Write
R	1'b1: Read
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

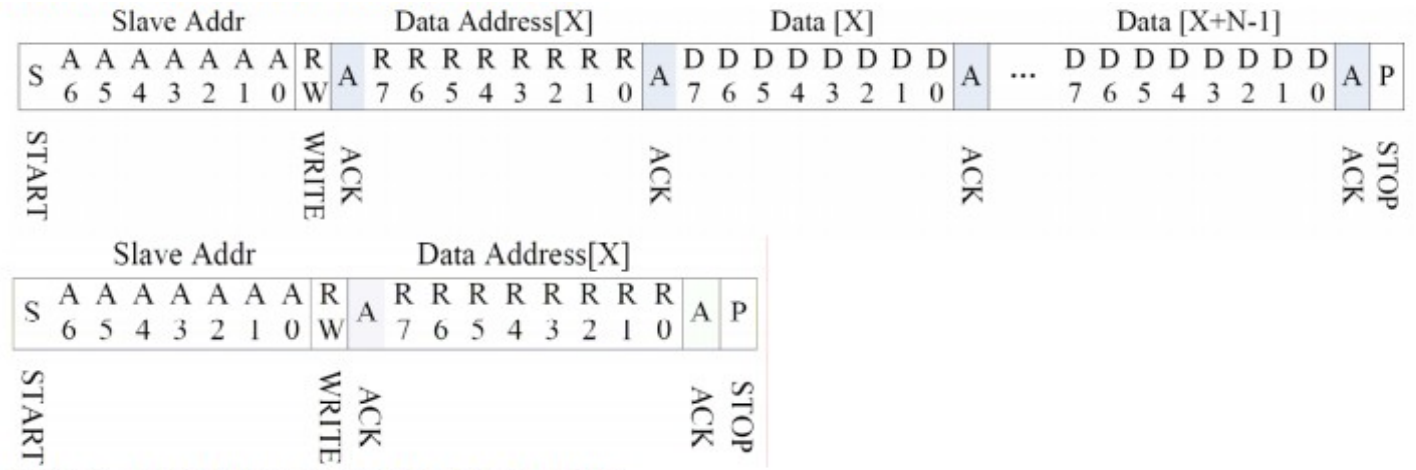
Lists the meanings of the mnemonics used in the above figures

Parameter	Unit	Min	Max
SCL frequency	KHz	0	400
Bus free time between a STOP and START condition	us	4.7	\
Hold time (repeated) START condition	us	4.0	\
Data setup time	ns	250	\
Setup time for a repeated START condition	us	4.7	\
Setup Time for STOP condition	us	4.0	\

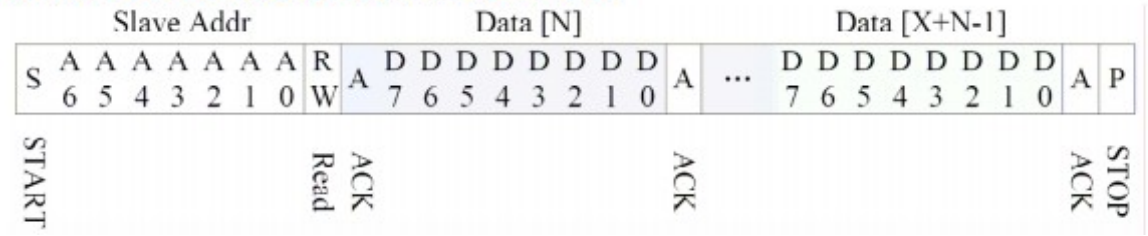
Interface Timing Characteristics

AS FOR STANDARD CTPM, HOST NEED TO USE BOTH INTERRUPT CONTROL SIGNAL AND SERIAL DATA INTERFACE TO GET THE TOUCH DATA.
HERE IS THE TIMING TO GET TOUCH DATA.

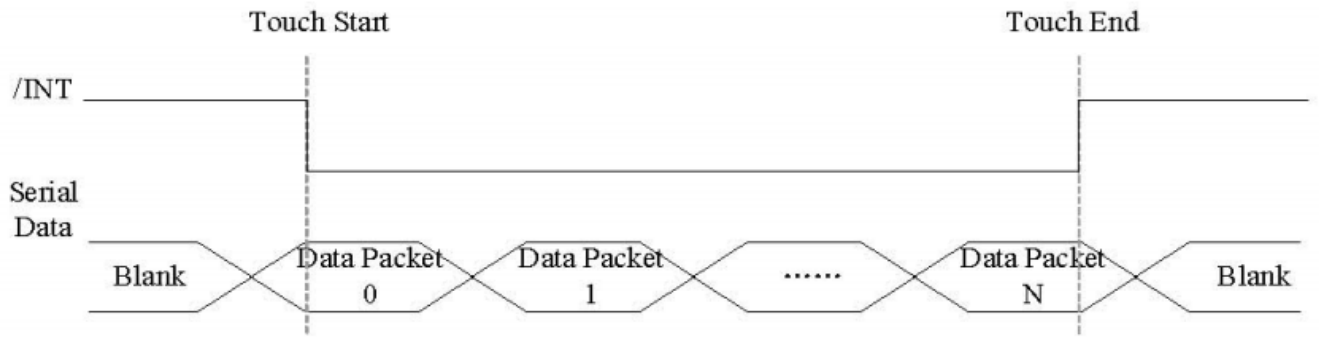
WRITE BYTES TO I2C SLAVE



READ X BYTES FROM I2C SLAVE



AS FOR STANDARD CTPM, HOST NEED TO USE BOTH INTERRUPT CONTROL SIGNAL AND SERIAL DATA INTERFACE TO GET THE TOUCH DATA, HERE IS THE TIMING TO GET TOUCH DATA.



TOUCH DATA READ PROTOCOL

NAME	VALUE	DESCRIPTION
START CH	0xF9	START COMMAND FOR CTPM TOUCH DATA PACKET, HOST MUST SEND CTPM A START CH COMMAND BEFORE READ TOUCH DATA
1st READ BYTE ~ LAST READ BYTE		TOUCH DATA PACKET SENT BY CTPM, EACH BYTE HAS 8-BIT DATA, A TOUCH DATA PACKET CONSISTS OF N BYTE.

A DATA PACKET STARTS EITH A HEADER AND ENDS WITH CRC CODE. AS FOR 5 POINTS DATA PACKET, THE LENGTH OF THE PACKET IS ALWAYS 26 BYTES IN SPITE OF ACTUAL TOUCH POINTS.

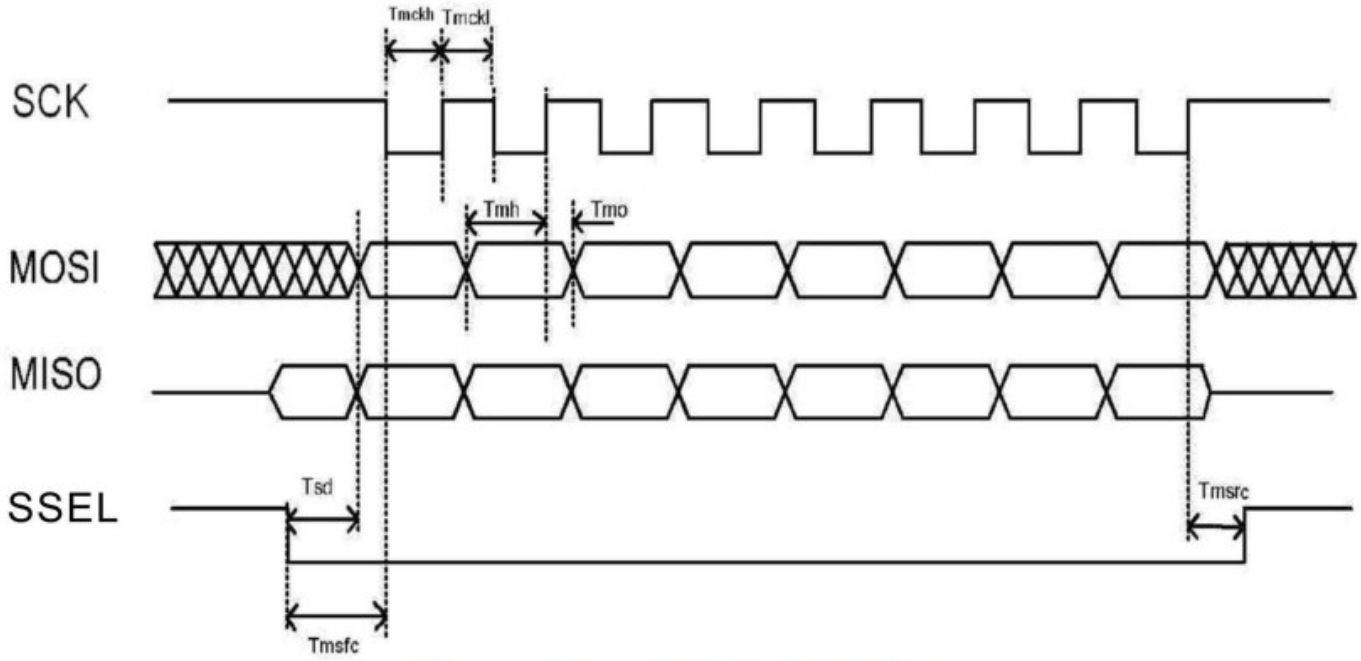
NAME	LENGTH (BYTE)	VALUE	DESCRIPTION
HEAD	2	0xAAAA	HEADER OF TOUCH DATA
BYTE0	1	0b00xx_xxxx	THE PACKET LENGTH WHICH STORES IN THE LOWER 6 BIT, 26 HERE.
BYTE1	1	0b0000_xxxx	ACTUAL TOUCH POINTS WHICH STORES IN THE LOWER 4 BIT.
BYTE2	1	0x00	RESERVED.
X1	2	0x0XXX	HORIZONTAL COORDINATE OF TOUCH POINT 1(12 BIT), CORRESPONDING TO THE HORIZONTAL CORRDINATE OF DISPLAY SCREEN.
Y1	2	0x0XXX	VERTICAL COORDINATE OF TOUCH POINT 1(12 BIT), CORRESPONDING TO THE HORIZONTAL CORRDINATE OF DISPLAY SCREEN.
X2	2	0x0XXX	HORIZONTAL COORDINATE OF TOUCH POINT 2
Y2	2	0x0XXX	VERTICAL COORDINATE OF TOUCH POINT 2
X3	2	0x0XXX	HORIZONTAL COORDINATE OF TOUCH POINT 3
Y3	2	0x0XXX	VERTICAL COORDINATE OF TOUCH POINT 3
X4	2	0x0XXX	HORIZONTAL COORDINATE OF TOUCH POINT 4
Y4	2	0x0XXX	VERTICAL COORDINATE OF TOUCH POINT 4
X5	2	0x0XXX	HORIZONTAL COORDINATE OF TOUCH POINT 5
Y5	2	0x0XXX	VERTICAL COORDINATE OF TOUCH POINT 5
CRC	1	0xXXX	CRC CODE FOR PREVIOUS N-1 DATA, FOR THE DATA VALIDATION. CRC CODE IS EQUAL TO THE XOR RESULT OF PREVIOUS 25 BYTE.

7.4 SPI INTERFACE TIMING CHARACTERISTICS:

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
SCK HIGH TIME	Tmckh	4×Tsysclk	—	—	ns
SCK LOW TIME	Tmckl	4×Tsysclk	—	—	ns
SCK SHIFT EDGE TO MOSI DATA CHANGE	Tmo	0	—	—	ns
MOSI DATA VALID TO SCK SHIFT EDGE	Tmh	3×Tsysclk	—	—	ns
SSEL FALLING EDGE TO MOSI DATA VALID	Tsd	4×Tsysclk	—	—	ns
SSEL FALLING EDGE TO FIRST SCK EDGE	Tmsfc	(Tmckh+ Tmckl) /2	—	—	ns
LAST SCK EDGE TO SSEL RISING EDGE	Tmsrc	(Tmckh+ Tmckl) /2	—	—	ns

NOTE(1):Tsysclk IS EQUAL TO ONE PERIOD OF THE DEVICE SYSTEM CLOCK(24MHz)

SPI TIMING



SPI master Timing PHASE=0, POLCK=1

8. Data transfer order Setting

Pixel Data Format

Both 6800 and 8080 support 8-bit, 9-bit, 16-bit, 18-bit and 24-bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in different ways.

Table 8-1: Pixel Data Format

Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
24 bits	1st	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18 bits	1st							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits (565 format)	1st									R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1
16 bits	1st									R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0
	2nd									B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0
	3rd									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
12 bits	1st													R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
	2nd													G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
9 bits	1st																R5	R4	R3	R2	R1	R0	G5	G4	G3
	2nd																G2	G1	G0	B5	B4	B3	B2	B1	B0
8 bits	1st																	R7	R6	R5	R4	R3	R2	R1	R0
	2nd																	G7	G6	G5	G4	G3	G2	G1	G0
	3rd																	B7	B6	B5	B4	B3	B2	B1	B0

9 Register Depiction

Please consult the spec of SSD1963 Version 1.2
Please consult the spec of FOCALTECH FT5x06

10. OPTICAL CHARATERISTIC

Ta=25±2℃, ILED=20mA

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr	θ =0° 、Φ=0°	-	10		ms	Note 3,5
		Tf		-	15		ms	
Contrast ratio		CR	At optimized viewing angle	300	400	-	-	Note 4,5
Color Chromaticity	White	Wx	θ =0° 、Φ=0	(0.26)	(0.31)	(0.36)		Note 2,6,7
		Wy		(0.28)	(0.33)	(0.38)		
	Red	Rx	θ =0° 、Φ=0					
		Ry						
	Green	Gx	θ =0° 、Φ=0					
		Gy						
	Blue	Bx	θ =0° 、Φ=0					
		By						
Viewing angle	Hor.	ΘR	CR≧10	(50)	(60)		Deg.	Note 1
		ΘL		(50)	(60)			
	Ver.	ΦT		(40)	(50)			
		ΦB		(45)	(55)			
Brightness		-	-	200	250	-	cd/m^2	Center of display

Ta=25±2℃, I_L=20mA

Note 1: Definition of viewing angle range

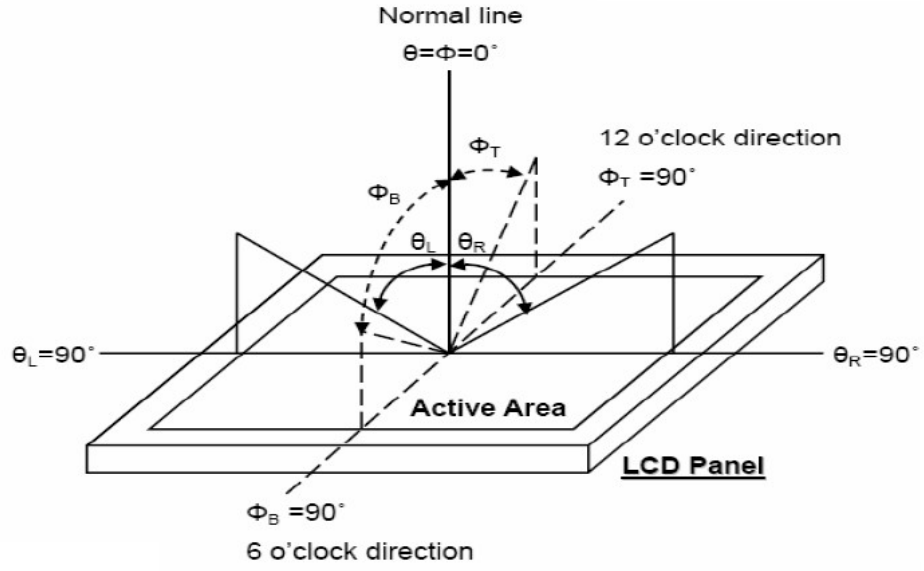


Fig. 8-1 Definition of viewing angle

Note 2: Test equipment setup:
After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

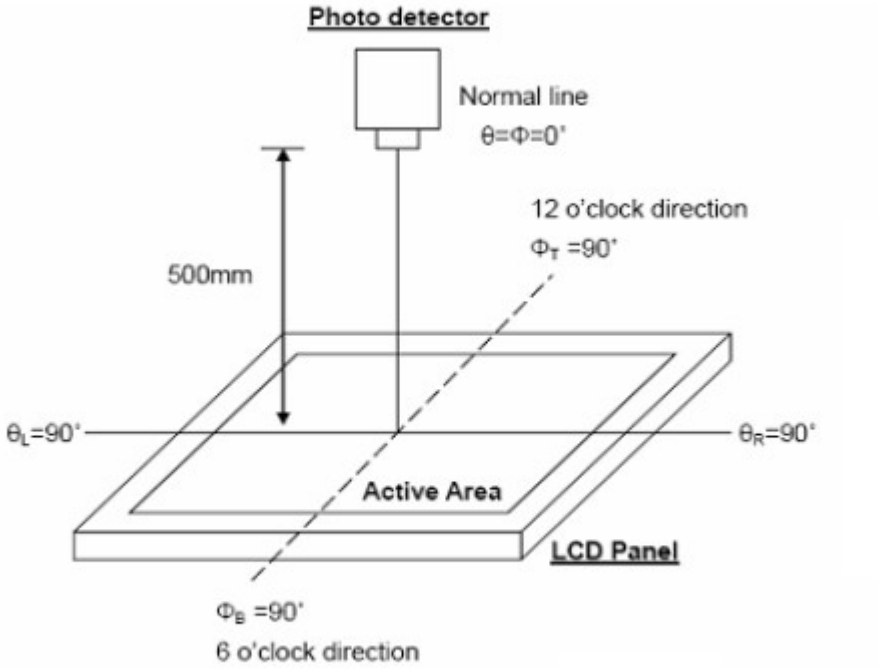


Fig. 8-2 Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, Tr, is the time between photo detector output intensity changed from 90% to 10% . And fall time, Tf, is the time between photo detector output intensity changed from10% to 90% .

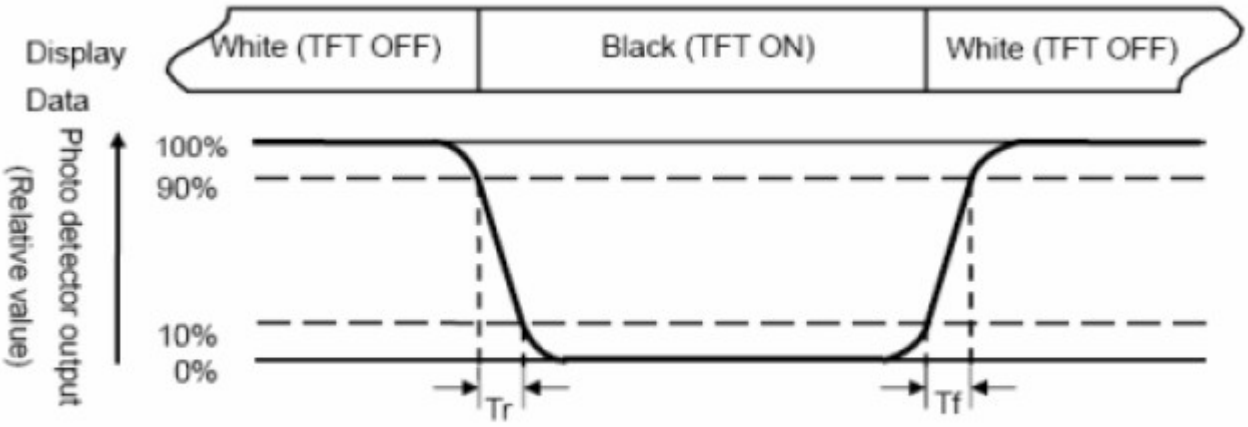


Fig. 3-3 Definition of response time

Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: White Vi = Vi50 ± 1.5V
Black Vi = Vi50 ± 2.0V
"±" means that the analog input signal swings in phase with VCOM signal.
"±" means that the analog input signal swings out of phase with VCOM signal.
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of

module are electrically opened.

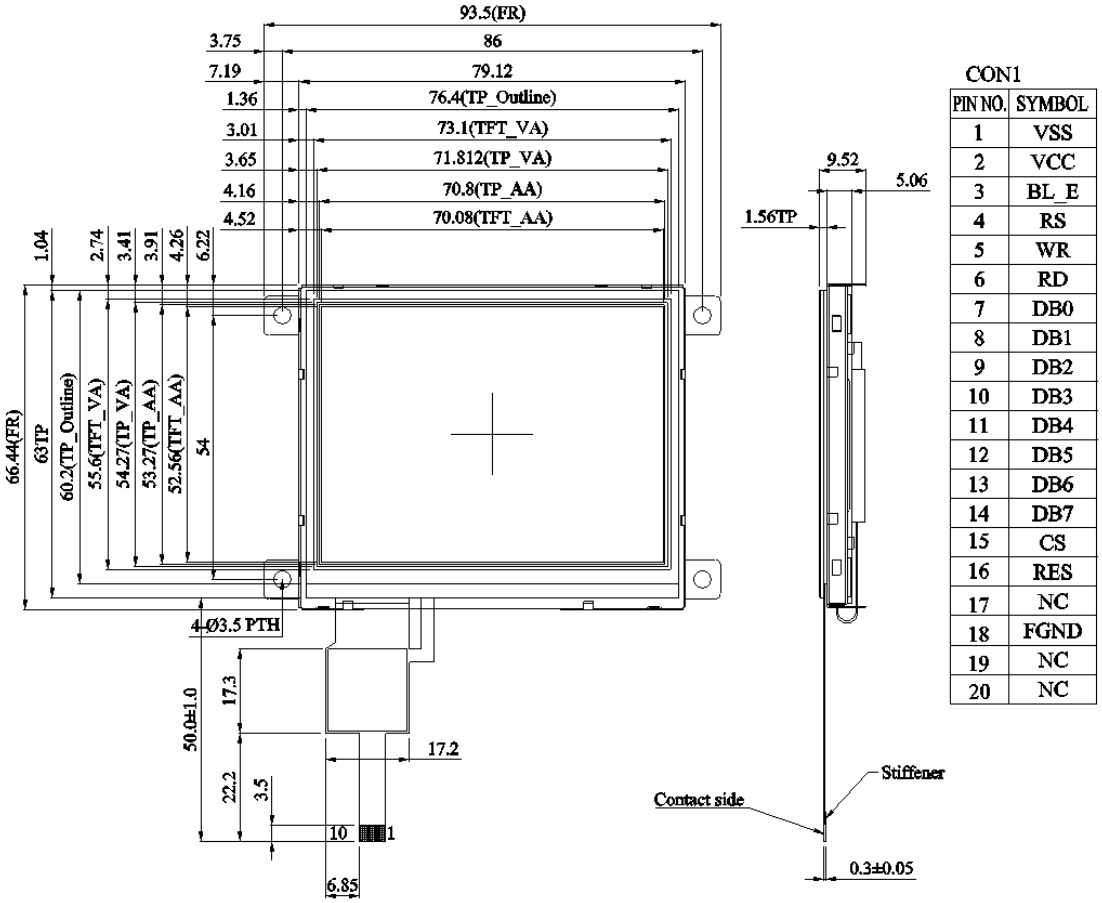
Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

$$\text{Note 8 : Uniformity (U)} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\%$$

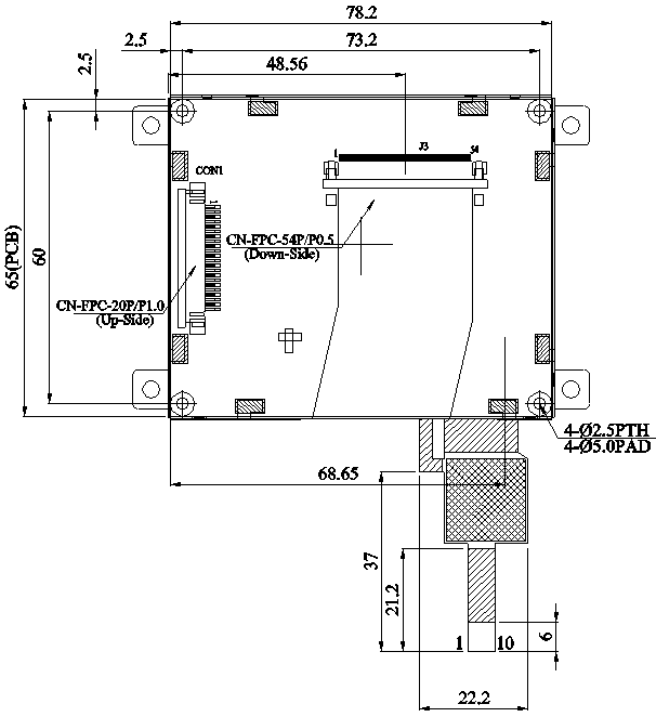
11.Contour Drawing

PIN NO.	SYMBOL
1	VSS
2	VDD
3	SCL
4	NC
5	SDA
6	NC
7	/RST
8	/WAKE
9	/INT
10	VSS



CON1

PIN NO.	SYMBOL
1	VSS
2	VCC
3	BL_E
4	RS
5	WR
6	RD
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	CS
16	RES
17	NC
18	FGND
19	NC
20	NC



12. RELIABILITY TEST

WIDE TEMPERATURE RELIABILITY TEST

NO.	ITEM	CONDITION			STANDARD	NOTE
1	High Temp. Storage	80℃	240 Hrs		Appearance without defect	
2	Low Temp. Storage	-30℃	240 Hrs		Appearance without defect	
3	High Temp. & High Humi. Storage	60 ℃ 90%RH	240 Hrs		Appearance without defect	
4	High Temp. Operating Display	70℃	240 Hrs		Appearance without defect	
5	Low Temp. Operating Display	-20℃	240 Hrs		Appearance without defect	
6	Thermal Shock	-20 ℃, 30min. → 70℃, 30min. (1cycle)			Appearance without defect	10 cycles

Inspection Provision

1.Purpose

The Crystalfontz America inspection provision provides outgoing inspection provision and its expected quality level based on our outgoing inspection of Crystalfontz America LCD produces.

2.Applicable Scope

The Crystalfontz America inspection provision is applicable to the arrangement in regard to outgoing inspection and quality assurance after outgoing.

3.Technical Terms

3-1 Crystalfontz America Technical Terms

4.Outgoing Inspection

4-1 Inspection Method

MIL-STD-105E Level Ⅱ Regular inspection

4-2 Inspection Standard

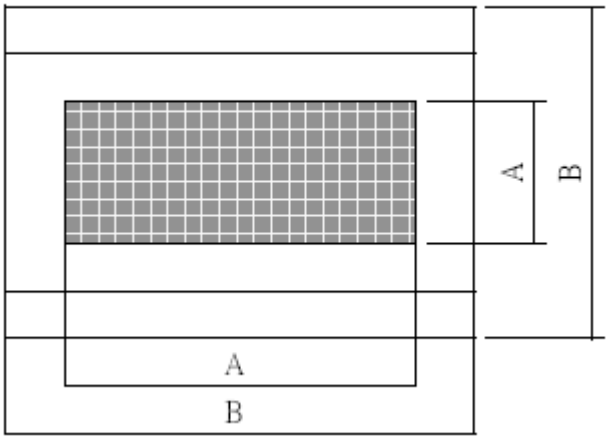
	Item		AQL(%)	Remarks
Major Defect	Dots	Opens Shorts Erroneous operation	0.4	Faults which substantially lower the practicality and the initial purpose difficult to achieve
	Solder appearance	Shorts Loose		
	Cracks	Display surface cracks		

	Dimensions	External from Dimensions	0.4	
Minor Defect	Inside the glass	Black spots	0.65	Faults which appear to pose almost no obstacle to the practicality, effective use, and operation
	Polarizing plate	Scratches, foreign Matter, air bubbles, and peeling		
	Dots	Pinhole, deformation		
	Color tone	Color unevenness		
	Solder appearance	Cold solder Solder projections		

4-3 Inspection Provisions

*Viewing Area Definition

Fig. 1



A : Zone Viewing Area
B : Zone Glass Plate Outline

*Inspection place to be 500 to 1000 lux illuminance uniformly without glaring.
The distance between luminous source(daylight fluorescent lamp and cool white fluorescent lamp) and sample to be 30 cm to 50 cm.

*Test and measurement are performed under the following conditions, unless otherwise specified.
Temperature 20 ± 15℃
Humidity 65 ± 20%R.H.
Pressure 860~1060hPa(mmbar)
In case of doubtful judgment, it is performed under the following conditions.
Temperature 20 ± 2℃
Humidity 65 ±5%R.H.
Pressure 860~1060hPa(mmbar)

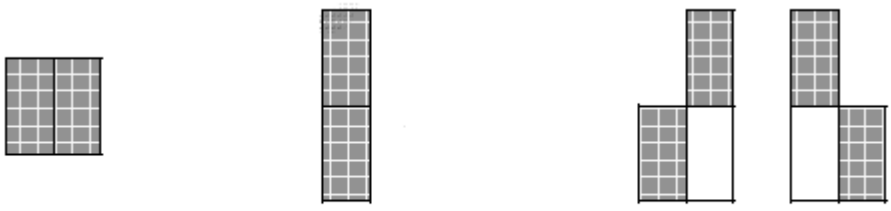
5.Specification for quality check
5-1-1 Electrical characteristics :

NO.	Item	Criterion
1	Non operational	Fail
2	Miss operating	Fail
3	Contrast irregular	Fail
4	Response time	Within Specified value

5-1-2 Components soldering :
Should be no defective soldering such as shorting, loose terminal cold solder, peeling of printed circuit board pattern, improper mounting position, etc.

5-2 Inspection Standard for TFT panel
5-2-1 The environmental condition of inspection :
The environmental condition and visual inspection shall be conducted as below.
(1) Ambient temperature : 25±5℃
(2) Humidity : 25~75% RH
(3) External appearance inspection shall be conducted by using a single 20W fluorescent lamp or equivalent illumination.
(4) Visual inspection on the operation condition for cosmetic shall be conducted at the distance 30cm or more between the LCD panels and eyes of inspector. The viewing angle shall be 90 degreeto the front surface of display panel.
(5) Ambient Illumination : 300~500 Lux for external appearance inspection.
(6) Ambient Illumination : 100~200 Lux for light on inspection.

5-2-2 Inspection Criteria
(1) Definition of dot defect induced from the panel inside
a) The definition of dot : The size of a defective dot over 1/2 of whole dot is regarded as one defective dot
b) Bright dot : Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
c) Dark dot : Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.
d) 2 dot adjacent = 1 pair = 2 dots
Picture :



(2) Display Inspection

NO.	Item			Acceptable Count
1	Dot defect	Bright Dot	Random	N ≦ 2
			2 dots adjacent	N ≦ 0
		Dark Dot	Random	N ≦ 3
			2 dots adjacent	N ≦ 1
		Total bright and dark dot		N ≦ 4
	Functional failure (V-line/ H-line/Cross line etc.)			Not allowable
	Mura	It's OK if mura is slight visible through 6% ND filter. (Judged by limit sample if it is necessary)		
2	Newton ring (touch panel)	Orbicular of interference fringes is not allowed in the optimum contrast within the active area under viewing angle.		

(3) Appearance inspection

NO.	Item	Standards
1	Panel Crack	Not allow. It is shown in Fig.1.
2	Broken CF Non -lead Side of TFT	The broken in the area of W > 2mm is ignored, L is ignored. It is shown in Fig.2.
3	Broken Lead Side of TFT	FPC lead, electrical line or alignment mark can't be damaged. It is shown in Fig.3.
4	Broken Corner of TFT at Lead Side	FPC lead. electrical line or alignment mark can't be damaged. It is shown in Fig.4.
5	Burr of TFT / CF Edge	The distance of burr from the edge of TFT / CF, W ≦ 0.3mm. It is shown in Fig.5.
6	Foreign Black / White/Bright Spot	(1) 0.15 < D ≦ 0.5 mm, N≦ 4 ; (2) D ≦ 0.15mm, Ignore. It is shown in Fig.6.
7	Foreign Black / White/Bright Line	(1) 0.05<W≦ 0.1 mm, 0.3<L≦2 mm, N≦ 4.
		(2) W ≦ 0.05mm and L≦ 0.3mm Ignore.
		It is shown in Fig.7.
8	Color irregular	Not remarkable color irregular.

Fig 1.

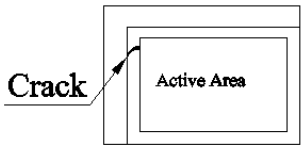


Fig 2.

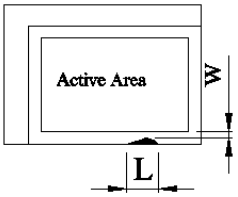


Fig 3.

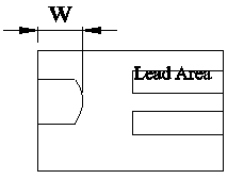


Fig 4.

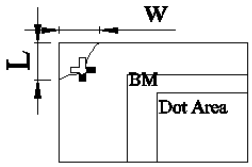


Fig 5.

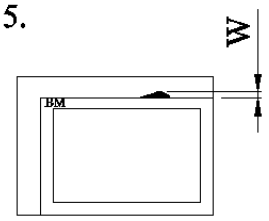
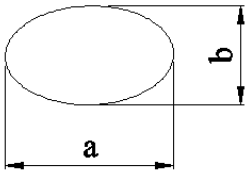


Fig 6.



D=(a+b)/2

Fig 7.

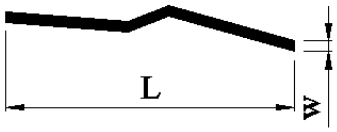
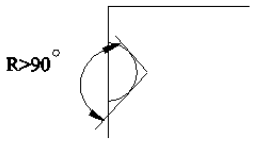


Fig8.



Notes
1.W:Widh
2.Lengh
3.D:Average Diameter
4.N:Count
5.All the anhle of the broken must be larger than 90°.It is shown in Fig.8.(R>90°)

NOTICE:

- SAFETY

1. If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
2. If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

- HANDLING

1. Avoid static electricity which can damage the CMOS LSI.
2. Do not remove the panel or frame from the module.
3. The polarizing plate of the display is very fragile. So, please handle it very carefully.
4. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
5. Do not use ketosis solvent & Aromatic solvent. Use a soft cloth soaked with a cleaning naphtha solvent.

- STORAGE

1. Store the panel or module in a dark place where the temperature is 25±5℃ and the humidity is below 65% RH.
2. Do not place the module near organics solvents or corrosive gases.
3. Do not crush, shake, or jolt the module.