ePAPER DISPLAY MODULE DATASHEET

Datasheet Release 2019-10-16
for
CFAP640384A0-0750

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CONTENTS

1. General Information

Datasheet Revision History
Datasheet Release Date: **2019-10-16** Datasheet for the CFAP640384A0-0750 ePaper display module.

Product Change Notifications
You can check for or subscribe to Part Change Notices for this display module on our website.

Variations
Slight variations between lots are normal (e.g., contrast, color, or intensity).

Volatility
This display module has volatile memory.

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2. Description Overview

This large ePaper display offers a crisp, high-contrast, easily readable display. The 7.5” active area contains 640x384 pixels and has 1-bit white/black full display capabilities. The display includes an integrated circuit containing a gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border.

3. Features

- High Contrast
- High Reflectance
- Ultra-Wide Viewing Angle
- Ultra-Low Power Consumption
- Pure Reflective Mode
- Bi-Stable Display
- Commercial Temperature Range
- Landscape or Portrait Mode
- Antiglare Hard-Coated Front-Surface
- Low Current Deep Sleep Mode
- On-Chip Display RAM
- Waveform Stored in On-Chip OTP
- Serial Peripheral Interface Available
- On-Chip Oscillator
- On-Chip Booster and Regulator Control for Generating VCOM, Gate and Source Driving Voltage
- I^2C Signal Master Interface to Read External Temperature Sensor

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	7.5	in	-
Display Resolution	640 (W) × 384 (H)	pixel	ppi: 100
Active Area	163.2(W) × 97.92(H)	mm	-
Pixel Pitch	0.255 × 0.255	mm	-
Pixel Configuration	Rectangle	-	-
Outline Dimension	170.2 (W) × 111.2(W) × 1.18 (D)	mm	-
Weight (typical)	43.75	g	-

5. Input/Output Terminals

5.1. Pin Out List

Pin #	Type	Symbol	Description	Remark
1	I	MFCSB	Serial Communication Chip Select Bypasses the MFCSB by R61H command.	
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate Driving Voltage	
5	C	VGH	Positive Gate Driving Voltage	
6	O	TSCL	I^2C Interface to Digital Temperature Sensor Clock Pin	
7	I/O	TSDA	I^2C Interface to Digital Temperature Sensor Data Pin	
8	I	BS1	Bus Selection Pin	Note 5-5
9	O	BUSY	Busy State Output Pin	Note 5-4
10	I	RES#	Reset	Note 5-3
11	I	D/C#	Command / Data Control Pin	Note 5-2
12	I	CS#	Chip Select Input Pin	Note 5-1
13	I/O	D0	Serial Clock Pin (SPI - SLCK)	
14	I/O	D1	Serial Data Pin (SPI - SDIN)	
15	I	VDDIO	Power for Interface Logic Pins	
16	I	VCI	Power Supply Pin for Chip	
17	-	VSS	Ground	
18	C	VDD	Core Logic Power Pin	
19	O	FMSDO	Serial Communication Data Output. Bypasses to FMSDO by R61H command.	
20	C	VSH	Positive Source Driving Voltage	
21	C	PREVGH	Positive Supply Pin for VGH and VSH	
22	C	VSL	Negative Source Driving Voltage	
23	C	PREVGL	Power Supply Pin for VCOM, VGL, and VSL	
24	O	VCOM	VCOM Driving Voltage	

Note (5-1): This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note (5-2): This pin (D/C#) is the Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note (5-3): This pin (RES#) is the reset signal input. The reset is active LOW.

Note (5-4): This pin (BUSY) is the Busy state output pin. When busy is LOW, the operation of chip should not be interrupted and no commands should be issued to the module. The driver IC will put Busy pin LOW when the driver IC is working such as

- Outputting Display Waveform; or
- Communicating with Digital Temperature Sensor

Note (5-5): This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “LOW”, 4-line SPI is selected. When it is “HIGH”, 3-line SPI (9 bits SPI) is selected. Please refer to the table below.

Table: Bus Interface Selection

BS1	MPU Interface
L	4-Lines Serial Peripheral Interface (SPI)
H	3-Lines Serial Peripheral Interface (SPI) – 9 bits SPI

6. Command Table

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data D7~D0:-: Don't care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	-	#	#	#	#	RES[1], RES[0], LUT_EN, UD, SHL, SHD_N, RST_N	0Fh
		0	1	-	-	-	#	-	-	-	-	VCM_HZ	00h
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	-	-	#	#	-	#	#	#	EDATA_SEL, EDATA_SET, VSource_LV_EN, VSource _EN, VGate_EN	07h
		0	1	-	-	-	-	-	#	#	#	VGHL_LV[1:0]	01h
		0	1	-	-	#	#	#	#	#	#	VDPS_LV[5:0]	05h
		0	1	-	-	#	#	#	#	#	#	VDNS_LV[5:0]	05h
3	Power OFF(POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	-	-	#	#	-	-	-	-	T_VDS_OFF[1:0]	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	00h
		0	1			#	#	#	#	#	#	BT_PHC[5:0]	00h
7	Deep Sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1	Check Code	A5h
8	Data Start Transmission 1 (DTM1) (x-byte command)	0	0	0	0	0	1	0	0	0	0		10h
		0	1	-	#	#	#	-	#	#	#	Kpixel1[2:0], KPixel2[2:0]	00h
		0	1	..	..	..	..	..	..	..	..	..	..
		0	1	-	#	#	#	-	#	#	#	Kpixel[2M-1][2:0] Kpixel[2M][2:0]	00h
9	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	-	-	-	-	-	-	-	Data_flag	-
10	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
11	Image Process Command (IPC)	0	0	0	0	0	1	0	0	1	1		13h
		0	1	-	-	-	#	-	#	#	#	IP_EN_IP_SEL[2:0]	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
12	VCOM LUT (LUTC) (221-byte command, bytes 2-12 repeated 20 times)	0	0	0	0	1	0	0	0	0	0		20h
13	LUT Black (LUTB) (261-byte command, bytes 2-14 repeated 20 times)	0	0	0	0	1	0	0	0	0	1		21h
14	LUT White (LUTW) (261-byte command, 2-14 repeated 20 times)	0	0	0	0	1	0	0	0	1	0		22h
15	LUT Gray1 (LUTG1) (261-byte command, bytes 2-14 repeated 20 times)	0	0	0	0	1	0	0	0	1	1		23h
16	LUT Gray2 (LUTG2) (261-byte command, bytes 2-14 repeated 20 times)	0	0	0	0	1	0	0	1	0	0		24h
17	LUT Red0 (LUTR0) (261-byte command, bytes 2-14 repeated 20 times)	0	0	0	0	1	0	0	1	0	1		25h
18	LUT Red1 (LUTR1) (261-byte command, bytes 2-14 repeated 20 times)	0	0	0	0	1	0	0	1	1	0		26h
19	LUT Red2 (LUTR2) (261-byte command, bytes 2-14 repeated 20 times)	0	0	0	0	1	0	0	1	1	1		27h
20	LUT Red3 (LUTR3) (261-byte command, bytes 2-14 repeated 20 times)	0	0	0	0	1	0	1	0	0	0		28h
21	LUT XON (LUTXON) (201-byte command, bytes 2-11 repeated 20 times)	0	0	0	0	1	0	1	0	0	1		29h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
22	PLL Control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	-	-	#	#	#	#	#	#	M[2:0], N[2:0]	3Ch
23	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	D10:3]/TS[7:1]	00h
		1	1	#	#	#	-	-	-	-	-	D[2:0]/TS[0]	00h
24	Temperature Sensor Select (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	-	-	-	-	-	-	-	TSE	00h
25	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
26	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
27	VCOM and Data Interval Setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	#	#	#	#	VBD[2:0],DDX,CDI[3:0]	F7h
28	Low Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	-	-	-	-	-	-	-	-	#	LPD	01h
29	TCON Setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0],G2S[3:0]	22h
30	TCON Resolution Setting (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	#	#	#	#	#	#	#	#	HRES[9:0]	00h
		0	1	-	-	-	-	-	-	#	#		00h
		0	1	-	-	-	-	-	-	-	#	VRES[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
31	SPI Flash Control (DAM)	0	0	0	1	1	0	0	1	0	1		65h
		0	1	-	-	-	-	-	-	-	#	DAM	00h
32	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70h
		0	1	-	-	#	#	#	#	#	#	MAN_SHRK_LUT_REV[3:0]	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
33	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	-	#	#	#	#	#	#	#	I^2C,ERR,I^2C_BUSY, DATA_ FLAG,PON,POF,BUSY	02h
34	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80h
		0	1	-	-	#	#	#	#	#	#	AMVT[1:0], AMVX, AMVS, AMV,AMVE	10h
35	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	-	#	#	#	#	#	#	#	VV[6:0]	00h
36	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	-	#	#	#	#	#	#	#	VDCS[6:0]	02h

(1) Panel Setting (PSR) (Register: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the Panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	LUT_EN	-	UD	SHL	SHD_N	RST_N

RES [1:0]: Display Resolution setting (source x gate)
00b: 640x480 (Default)
01b: 600x450
10b: 640x448
11b: 600x448
LUT_EN: LUT selection
0: Using LUT from external Flash.
1: Using LUT from register.
UD: Gate Scan Direction
0: Scan down. First line to last line: Gn→……→ G1
1: Scan up. (Default) First line to last line: G1→……→ Gn
SHL: Source Shift direction
0: Shift left. First data to last data: Sn→……S1
1: Shift right. (Default) First data to last data: S1→ ……→ Sn
SHD_N: Booster Switch
0: DC-DC converter OFF.
1: DC-DC converter ON (Default).
When SHD_N becomes LOW, DC-DC will turn OFF. Register and SRAM data will keep until VDD is OFF. SD output and VCOM will be based on previous condition. It may have two conditions: 0V or floating.

RST_N: Soft Reset
0: The controller is reset. All registers are reset to their default value.
1: Normal operation (Default). Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V.
When RST_N becomes LOW, the driver will be reset; all registers will be reset to their default value. All driver functions will be disabled. SD output and VCOM will be based on previous condition. It may have two conditions: 0V and floating.

VCM_HZ: VCOM Hi-Z function
0: VCOM normal output (Default)
1: VCOM floating.

(2) Power Setting (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1
	0	1	-	-	EDATA_SEL	EDATA_SET	-	VSource_LV_EN	VSource_EN	VGate_EN
	0	1	-	-	-	-	-	-	VGHL_LVL[1:0]	
	0	1	-	-	VDPS_LV[5:0]					
	0	1	-	-	VDNS_LV[5:0]					

EDATA_SEL: EDATA selection for pure driver mode

0: When EDATA_SET=1, pixel bit = 2`b11 VDPS_L level

1: When EDATA_SET=1, pixel bit = 2`b11 VDNS_L level (Default)

EDATA_SET: EDATA setting for pure driver mode

0: 3-bit data mode for pure driver

1: 2-bit data mode for pure driver (Default)

VSource_LV_EN: VSource LV power selection

0: External source power from VSH_LV and VSL_LV pin.

1: Internal DCDC function for generate source power. (Default)

VSource_EN: VSource power selection

0: External source power from VSH and VSL pin.

1: Internal DCDC function for generate source power. (Default)

VGate_EN: VGate power selection

0: External gate power from VGH and VGL pin.

1: Internal DCDC function for generate gate power. (Default)

VGHL_LVL [1:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
00	VGH=20V, VGL= -20V
01(Default)	VGH=19V, VGL= -19V
10	VGH=18V, VGL= -18V
11	VGH=17V, VGL= -17V

VDPS_LV [5:0]: Internal VDH power selection for RED LUT.

VDPS_LV	VDH_V
000000	3.0V
000001	3.2V
000010	3.4V
000011	3.6V
000100	3.8V
000101	4.0V (Default)
...	..
111100	15.0V

VDNS_LV [5:0]: Internal VDL power selection for RED LUT.

VDNS_LV	VDL_V
000000	-3.0V
000001	-3.2V
000010	-3.4V
000011	-3.6V
000100	-3.8V
000101	-4.0V (Default)
...	..
111100	-15.0V

(3) Power OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the Power	0	0	0	0	0	0	0	0	1	0

After the Power Off command, the driver will power off based on the Power Off Sequence, and the BUSY signal will become “0”. The Power Off command will turn off DCDC, T-CON, source driver, gate driver, VCOM, and temperature sensor, but register and SRAM data will be kept until VDD becomes OFF.

SD output and VCOM will be based on the previous condition. It may have 2 conditions: 0V or floating.

(4) Power OFF Sequence Setting (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF Sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-

T_VDS_OFF [1:0]: Power OFF Sequence of VDH and VDL

00b:1 frame (Default) 01b:2 frames 10b: 3 frames 11b:4 frames

(5) Power ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the Power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will power on based on the Power ON Sequence.

After power on command and all power sequences are ready, the BUSY signal will become “1”.

(6) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Booster Soft Start	0	0	0	0	0	0	0	1	0	1
	0	1	BTPHA7	BTPHA6	BTPHA5	BTPHA4	BTPHA3	BTPHA2	BTPHA1	BTPHA0
	0	1	BTPHB7	BTPHB6	BTPHB5	BTPHB4	BTPHB3	BTPHB2	BTPHB1	BTPHB0
	0	1			BTPHC5	BTPHC4	BTPHC3	BTPHC2	BTPHC1	BTPHC0

Name	Control	Value	Description
BT_PHA[7:6] BT_PHB[7:6]	Soft Start Phase Period	00	10ms
		01	20ms
		10	30ms
		11	40ms
BT_PHA[5:3] BT_PHB[5:3] BT_PHC[5:3]	Driving Strength	000	1
		001	2
		010	3
		011	4
		100	5
		101	6
		110	7
		111	8

Name	Control	Value	Description
BT_PHA[2:0] BT_PHB[2:0] BT_PHC[2:0]	Min. OFF Time	000	0.26μs
		001	0.31μs
		010	0.36μs
		011	0.52μs
		100	0.77μs
		101	1.61μs
		110	3.43μs
		111	6.77μs

(7) Deep Sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

This command causes the chip to enter the deep-sleep mode to save power.

The deep sleep mode will return to standby by hardware reset.

The only parameter is a check code, the command will execute if the check code is A5h.

(8) Data Start Transmission 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting Data Transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Dummy	Kpixel12	Kpixel11	Kpixel10	Dummy	Kpixel22	Kpixel21	Kpixel20
	0	1	..	..	..	..	..	..	..	..
	0	1	Dummy	Kpixel (2M-1)2	Kpixel (2M-1)1	Kpixel (2M-1)0	Dummy	Kpixel (2M)2	Kpixel (2M)1	Kpixel (2M)0

This command starts transmitting data and writing data to SRAM. To complete data transmission, command Data Transmission Stop (R11H) must be issued. Then the chip will start to send data/VCOM for panel.

Kpixel[1~2M][2:0]

Kpixel[2:0]	Source Driver Output	
	DDX=1(default)	DDX=0
	LUT	LUT
000	Black	White
001	Gray1	Gray2
010	Gray2	Gray1
011	White	Black
100	Red0	Red3
101	Red1	Red2
110	Red2	Red1
111	Red3	Red0

(9) Data Stop (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping Data Transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data_flag	-	-	-	-	-	-	-

To stop data transmission, this command must be issued to check the data_flag.

data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (R10H) or "Data Stop" (R11H) commands, BUSY signal will become "0" until display update is finished.

(10) Display Refresh Command (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the Display	0	0	0	0	0	1	0	0	1	0

After this command is issued, the driver will refresh the display (data/VCOM) according to SRAM data and LUT.
After Display Refresh command, BUSY signal will become "0" until display update is finished.

(11) Image Process Command (IPC) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Image Process Setting	0	0	0	0	1	0	0	0	1	1
	0	1	-	-	-	IP_EN	-	IP_SEL[2:0]		

After this command is issued, image process engine will find thin lines/pixels from frame SRAM and update the frame SRAM for applying new gray level waveform.

IP_EN: Image process enabled.

0: No action

1: Image process enabled (auto return to "0" after image process is finished)

IP_SEL[2:0]: Image process selection.

000: Deal with 1-pixel width

001: Deal with 2-pixel width

010: Deal with 3-pixel width

011: Deal with 1-pixel and 2-pixel width

100: Deal with 1-pixel, 2-pixel, and 3-pixel width

Others: Deal with 1-pixel width

After "Image Process Command" (13H), BUSY signal will be low until image process is finished.

(12) VCOM LUT (LUTC) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for VCOM (221-byte command, bytes 2-12 repeated 20 times.	0	0	0	0	1	0	0	0	0	0

This command builds the VCOM Look-up Table (LUT).

(13) Black LUT (LUTB) (R21H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Black (261-byte command, bytes 2-14 repeated 20 times.	0	0	0	0	1	0	0	0	0	1

This command builds LUTB.

(14) White LUT (LUTW) (R22H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for White (261-byte command, bytes 2-14 repeated 20 times.	0	0	0	0	1	0	0	0	1	0

This command builds LUTW.

(15) Gray1 LUT (LUTG1) (R23H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Gray1 (261-byte command, bytes 2-14 repeated 20 times.	0	0	0	0	1	0	0	0	1	1

This command builds LUTG1.

(16) Gray2 LUT (LUTBB / LUTB) (R24H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Gray2 (261-byte command, bytes 2-14 repeated 20 times.	0	0	0	0	1	0	0	1	0	0

This command builds LUTG2.

(17) Red0 LUT (LUTR0) (R25H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Red0 (261-byte command, bytes 2-14 repeated 20 times.	0	0	0	0	1	0	0	1	0	1

This command builds LUTR0.

(18) Red1 LUT (LUTR1) (R26H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Red1 (261-byte command, bytes 2-14 repeated 20 times.	0	0	0	0	1	0	0	1	0	1

This command builds LUTR1.

(19) Red2 LUT (LUTR2) (R27H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Red2 (261-byte command, bytes 2-14 repeated 20 times.	0	0	0	0	1	0	0	1	1	1

This command builds LUTR2.

(20) Red3 LUT (LUTR3) (R28H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Red3 (261-byte command, bytes 2-14 repeated 20 times.	0	0	0	0	1	0	1	0	0	0

This command builds LUTR3.

(21) XON LUT (LUTXON) (R29H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for XON (201-byte command, bytes 2-11 repeated 20 times.	0	0	0	0	1	0	1	0	0	1

This command builds LUTXON.

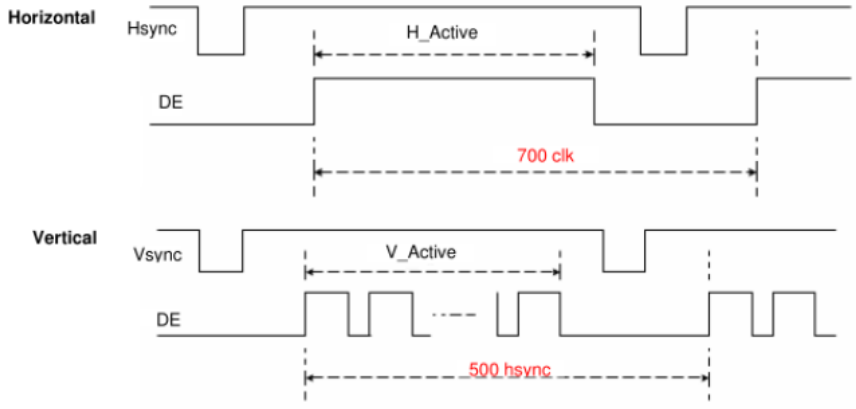
(22) PLL Control (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	M[2:0]			N[2:0]		

This command controls the PLL clock frequency.

The PLL structure must support the following frame rates:

M	N	Frame Rate	M	N	Frame Rate	M	N	Frame Rate	M	N	Frame Rate
1	1	29 Hz	3	1	86 Hz	5	1	143 Hz	7	1	200 Hz
	2	14 Hz		2	43 Hz		2	71 Hz		2	100 Hz
	3	10 Hz		3	29 Hz		3	48 Hz		3	67 Hz
	4	5 Hz		4	21 Hz		4	36 Hz		4	50 Hz (Default)
	5	7 Hz		5	17 Hz		5	29 Hz		5	40 Hz
	6	6 Hz		6	14 Hz		6	24 Hz		6	33 Hz
	7	5 Hz		7	12 Hz		7	20 Hz		7	29 Hz
2	1	57 Hz	4	1	114 Hz	6	1	171 Hz			
	2	29 Hz		2	57 Hz		2	86 Hz			
	3	19 Hz		3	38 Hz		3	57 Hz			
	4	14 Hz		4	29 Hz		4	43 Hz			
	5	11 Hz		5	23 Hz		5	34 Hz			
	6	10 Hz		6	19 Hz		6	29 Hz			
	7	8 Hz		7	16 Hz		7	24 Hz			



(23) Temperature Sensor Calibration (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10	D9/TS7	D8/TS6	D7/TS5	D6/TS4	D5/TS3	D4/TS2	D3/TS1
	1	1	D2/TS0	D1	D0	-	-	-	-	-

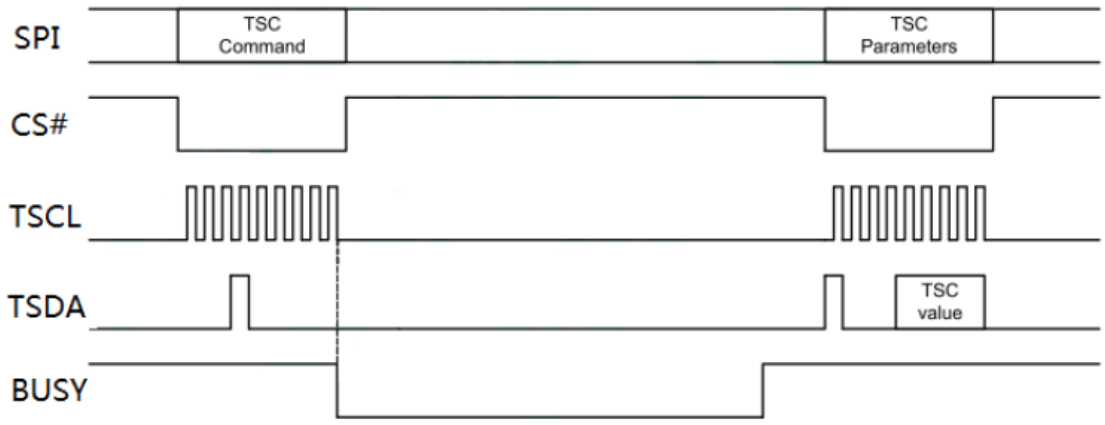
This command reads the temperature sensed by the temperature sensor.

TS [7:0]: When TSE (R41H) is set to 0, this command reads the internal temperature sensor value.

D [10:0]: When TSE (R41H) is set to 1, this command reads the external LM75 temperature sensor value.

Bit 7~0	Temperature (°C)
0000 0000b	0
0000 0001b	0.5
0000 0010b	1
..	..
0101 1010b	45
..	..
0110 0100b	50
..	..
1100 1110b	-25
..	..
1111 1110b	-1
1111 1111b	-0.5

BUSY becomes low after TSC command. When BUSY becomes high, parameter can be read.



(24) Temperature Sensor Select (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Sensor Selection	0	0	0	1	0	0	0	0	0	1
	0	1	TSE	-						

This command selects the Internal and External temperature sensor.

TSE: Internal temperature sensor switch

0: Select internal temperature sensor (Default) 1: Select external temperature sensor.

(25) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Sensor Write	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	1	WLSB[7:0]							

This command writes data to the external temperature sensor.

WATTR: D[7:6] I^2C Write Byte Number

00: 1 byte (head byte only)
01: 2 bytes (head byte + pointer)
10: 3 bytes (head byte + pointer + 1st parameter)
11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)
D[5:3]: User-defined address bits (A2, A1, A0)
D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor.

WLSB[7:0]: LSByte of write-data to external temperature sensor.

(26) Temperature Sensor Read (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Sensor Read	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the data from the external temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor.

RLSB[7:0]: LSByte read data from external temperature sensor.

(27) VCOM and Data Interval Setting (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval Between VCOM and Data	0	0	0	1	0	1	0	0	0	0
	0	1	VBD[2:0]			DDX	CDI[3:0]			

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 H_{SYNC}).

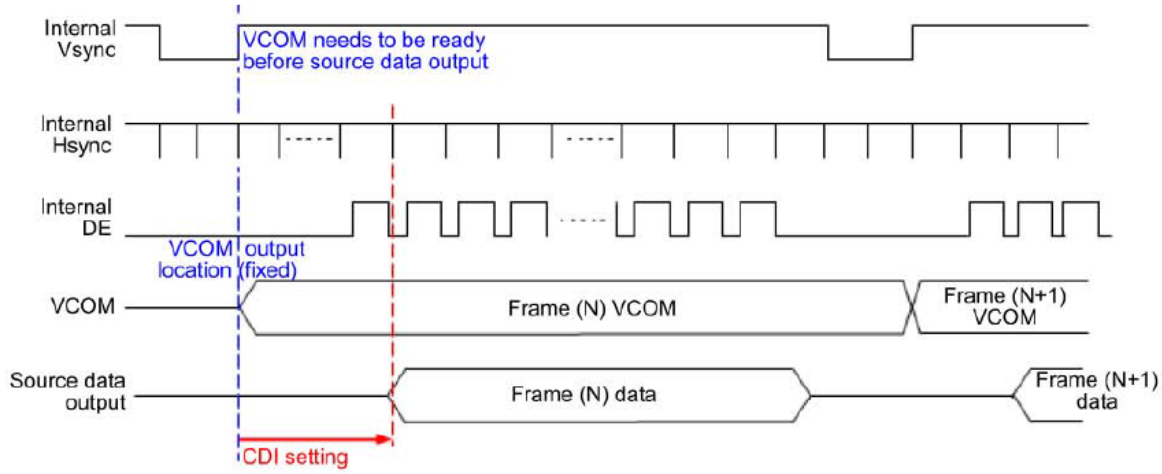
VBD[2:0]: Border output selection

DDX: Data polarity.

VBD[2:0]	Border Output	
	DDX=1(default)	DDX=0
	LUT	LUT
000	Black	White
001	Gray1	Gray2
010	Gray2	Gray1
011	White	Black
100	Red0	Floating
101	Red1	Red2
110	Red2	Red1
111	Floating	Red0

CDI[3:0]: VCOM and Data Interval

CDI[3:0]	VCOM and Data Interval	CDI[3:0]	VCOM and Data Interval
0000 b	17 H_{SYNC}	1000	9
0001	16	1001	8
0010	15	1010	7
…	…	…	…
0110	11	1110	3
0111	10(Default)	1111	2



(28) Low Power Detection (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the condition of the battery.

LPD: Interval temperature sensor switch

0: Low Power Input (VDD<2.5V)

1: Normal Status (Default)

(29) TCON Setting (TCON) (R60H)

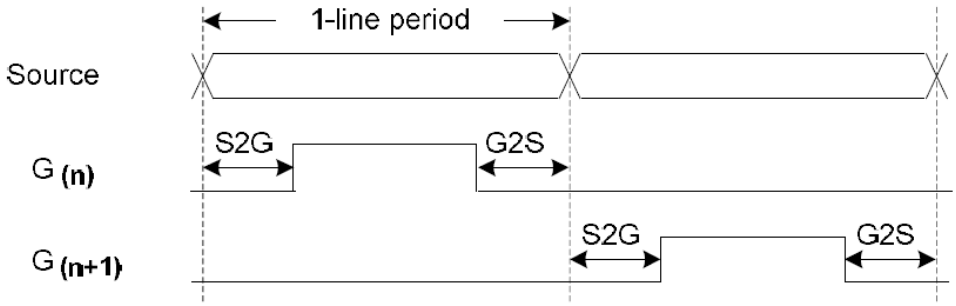
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Timing definition	0	0	0	1	1	0	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

This command defines the non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap Period

S2G[3:0] or G2S[3:0]	Period		S2G[3:0] or G2S[3:0]	Period
0000 b	4		…	…
0001	8		1011	48
0010	12 (Default)		1100	52
0011	16		1101	56
0100	20		1110	60
0101	24		1111	64

Period = 660 nS.



(30) TCON Resolution Setting (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	0	1	1	0	0	0	0	1
	0	1	HRES[7:0]							
	0	1	-	-	-	-	-	-	HRES[9:8]	
	0	1	VRES[7:0]							
	0	1	-	-	-	-	-	-	-	VRES[8]

This command defines the alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR). Resolution should be an even number.

HRES[9:0]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

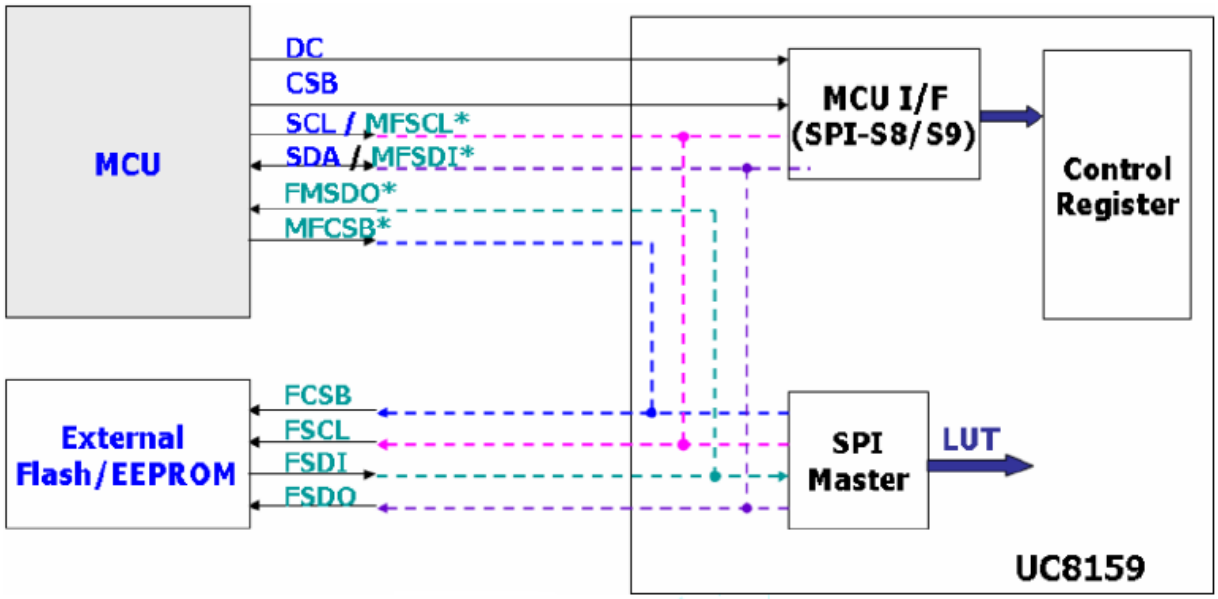
(31) SPI Flash Control (DAM) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Define MCU memory mode	0	0	0	1	1	0	0	0	0	1
	0	1	-	-	-	-	-	-	-	DAM

This command defines MCU host direct access external memory mode.

DAM: 0: Disable (Default)

1: Enable. Bypass MFSCL*, MFSDI*, MFSDO*, and MFCSB* to external flash.



(32) Revision (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
LUT/Chip Revision	0	0	0	1	1	1	0	0	0	0
	1	1	LUTVER[7:0]							
	1	1	LUTVER[15:8]							
	1	1	0	0	0	0	CHREV[3:0]			

The LUTVER[15:0] is read from OTP address = 25001 and 25000.

LUTVER[15:0]: LUT version.

CHREV[3:0]: Chip revision.

(33) Get Status (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	-	I^2C_ERR	I^2C_BUSY	Data_flag	PON	POF	BUSY

This command reads the IC status.

I^2C_ERR: I^2C master error status
I^2C_BUSY: I^2C master BUSY status (low active)
Data_flag: Driver has already received all the one frame data
PON: Power ON status
POF: Power OFF status
BUSY: Driver busy status (low active)

(34) Auto Measure VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically Measure VCOM	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		AMVX	AMVS	AMV	AMVE

This command implements related VCOM sensing setting.

AMVT[1:0]: Auto Measure VCOM Time
00b: 3s 01b: 5s (Default)
10b: 8s 11b:10s
AMVX: Auto Measure VCOM without XON Function
0: Measure VCOM without XON function. (Default)
1: Measure VCOM without XON function. (All Gate ON)
AMVS: Source Output of AMV
0: Set source output to 0V during Auto Measure VCOM period. (Default)
1: Set source output to 3V (or VDPS_L) during Auto Measure VCOM period.
AMV: Analog Signal
0: Get VCOM value with the VV command (R18h) (Default)
1: Get VCOM value in analog signal. (external analog to digital converter)
AMVE: Auto Measure VCOM Enable (Disable)
0: Disabled
1: Enabled

(35) Read VCOM Value (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically Measure VCOM	0	0	1	0	0	0	0	0	0	1
	1	1	-	VV[6:0]						

This command gets the VCOM value.

VV[6:0]: VCOM Value Output

VV[6:0]	VCOM Value
00 0000b	0V
00 0001b	-0.05V
00 0010b	-0.10V
000 0011b	-0.15V
:	:
101 0000b	-4.0V
(Others)	-4.0V

(36) VCOM-DC Setting (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	VDCS[6:0]						

This command sets VCOM_DC value.

VDCS[6:0]: VCOM-DC Setting

VDCS[6:0]	VCOM_DC Value
00 0000b	(Reserved)
00 0001b	(Reserved)
00 0010b	-0.10V
00 0011b	-0.15V
11 1010b	-0.20V
..	..
101 0000b	-4.0V
(Others)	-4.0V

7. Electrical Characteristics

7.1. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.3 to +6.0	V
Logic Input Voltage	V_{IN}	-0.3 to V_{CI} +0.3	V
Operating Temp. range	T_{OPR}	0 to +50	°C
Storage Temp. range	T_{STG}	-25 to +70	°C
IMPORTANT: It is recommended that you use a UV protective film when operating the module in direct sunlight.			

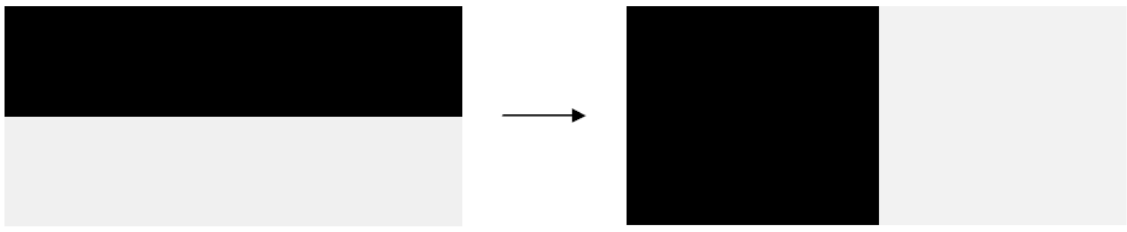
7.2. Panel DC Characteristics

The following specifications apply for: V_{SS} = 0V, V_{CI} = 3.3V, T_A = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V_{SS}	-	-	0	-	V
Logic Supply Voltage	V_{CI}	-	2.3	3.3	3.6	V
High Level Input Voltage	V_{IH}	Digital Input Pins	0.7V_{CI}	-	V_{CI}	V
Low Level Input Voltage	V_{IL}	Digital Input Pins	GND	-	0.3V_{CI}	V
High Level Output Voltage	V_{OH}	I_{OH}= 400uA	V_{CI}-0.4	-	-	V
Low Level Output Voltage	V_{OL}	I_{OL}= -400uA	GND	-	GND +0.4	V
Image Update Current	I_{UPDATE}	-	8.0	11.5	15.0	mA
Standby Panel Current	$I_{STANDBY}$	-	0	2.0	4.0	µA
Power Panel (Update)	P_{UPDATE}	-	24	38	54	mW
Standby Power Panel	P_{STBY}	-	-	-	0.018	mW
Operating Temperature	-	-	0	-	50	°C
Storage Temperature	-	-	-25	-	70	°C
Image update Time at 25°C	-	-	3	4	5	sec
POF	V_{CI}	DC/DC Off No Clock No Input Load Ram Data Not Retain	25	30	35	µA

The typical power consumption is measured with the following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern, shown below.

Note: The standby power is the consumed power when the panel controller is in standby mode. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Crystalfontz. V_{COM} is recommended to be set in the range of assigned value ±0.1V.



7.3. Panel AC Characteristics

7.3.1. MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with the MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is low, 4-wire SPI is selected. When it is high, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus Interface	D1	D0	CS#	D/C#	RES#
SPI4	SDIN	SCLK	CS#	D/C#	RES#
SPI3	SDIN	SCLK	CS#	Low	RES#

Table 7-1: MCU Interface Assignment Under Different Bus Interface Mode

Note: Low is connected to V_{SS}. High is connected to V_{CI}.

4-Wire SPI

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, data/command D/C#, and chip select CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCLK
Write Command	Low	Low	↑
Write Data	Low	High	↑

Table 7-2: Control Pins of 4-Wire Serial Peripheral Interface

Note: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order: D7, D6…D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

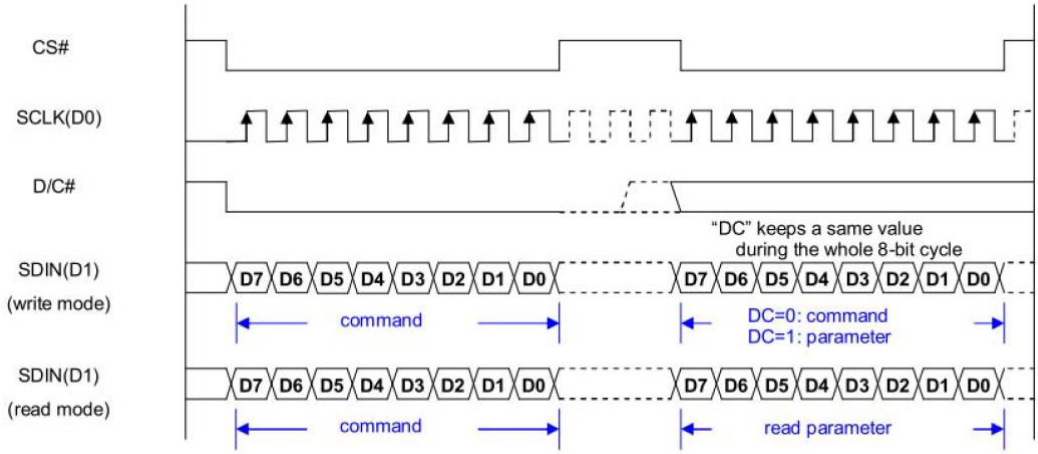


Figure 7-1: Write Procedure in 4-Wire Serial Peripheral Interface Mode

3-Wire SPI

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and chip select CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. The pin D/C# should be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are 9-bits that will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	Low	Tie LOW	↑
Write Data	Low	Tie LOW	↑

Table 7-3: Control Pins of 3-Wire Serial Peripheral Interface

Note: ↑stands for rising edge of signal

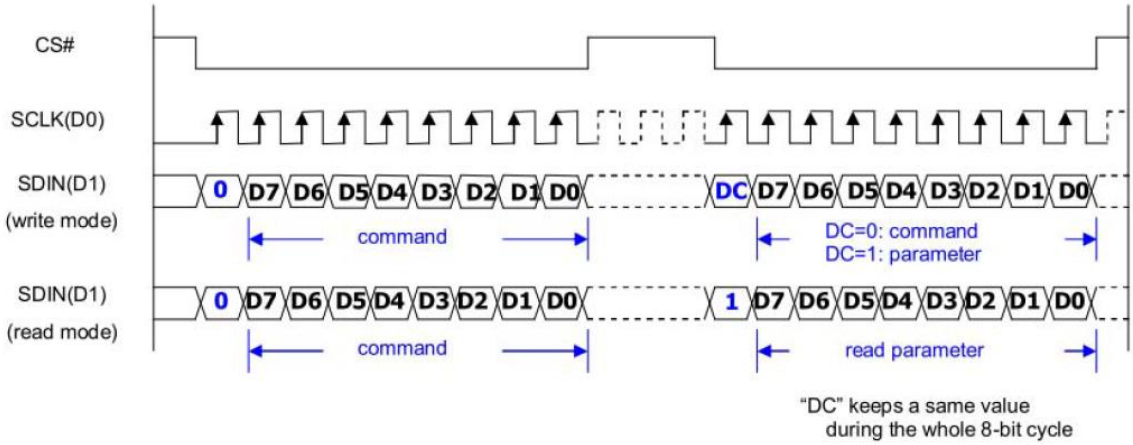
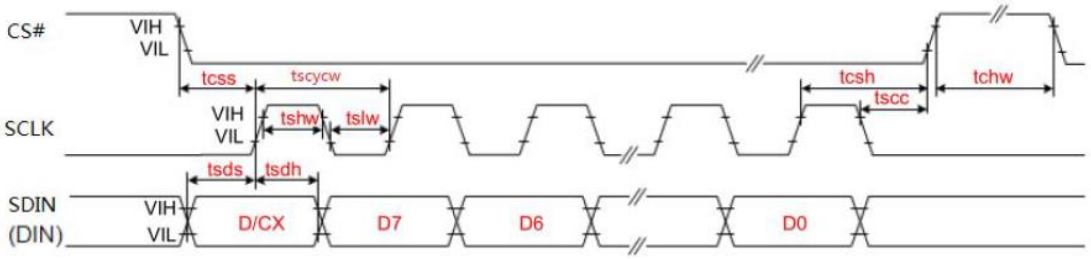
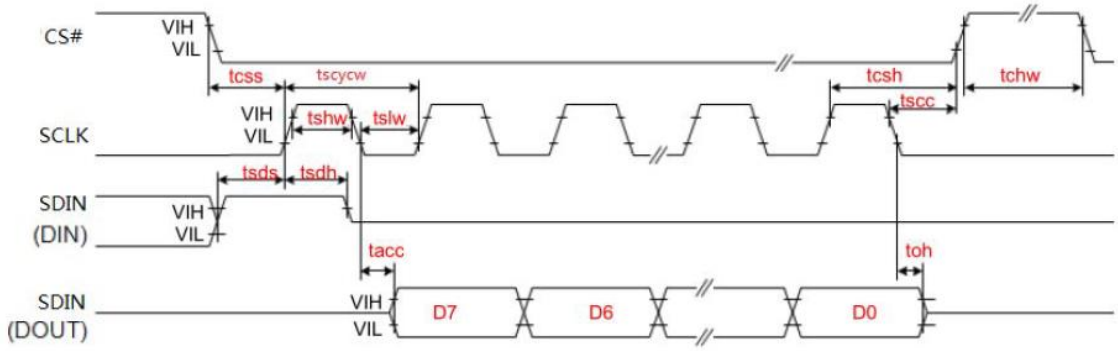


Figure 7-2: Write Procedure in 3-Wire Serial Peripheral Interface Mode

7.3.2. Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CS#	Chip Select Setup Time	60	-	-	ns
tcsh		Chip Select Hold Time	65	-	-	ns
tscc		Chip Select Setup Time	20	-	-	ns
tchw		Chip Select Setup Time	40	-	-	ns
tscycw	SCLK	Serial Clock Cycle (Write)	100	-	-	ns
tshw		SCLK “H” Pulse Width (Write)	35	-	-	ns
tslw		SCLK “L” Pulse Width (Write)	35	-	-	ns
tscycr		Serial Clock Cycle (Read)	150	-	-	ns
tshr		SCLK “H” Pulse Width (Read)	60	-	-	ns
tslr		SCLK “L” Pulse Width (Read)	60	-	-	ns
tsds	SDIN (DIN) (DOUT)	Data Setup Time	30	-	-	ns
tsdh		Data Hold Time	30	-	-	ns
tacc		Access Time	10	-	-	ns
toh		Output Disable Time	15	-	-	ns

7.4. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel Power Consumption During Update	-	25°C	26.4	40	mW	-
Power Consumption in Standby Mode	-	25°C	-	0.0165	mW	-

7.5. Reference Circuit

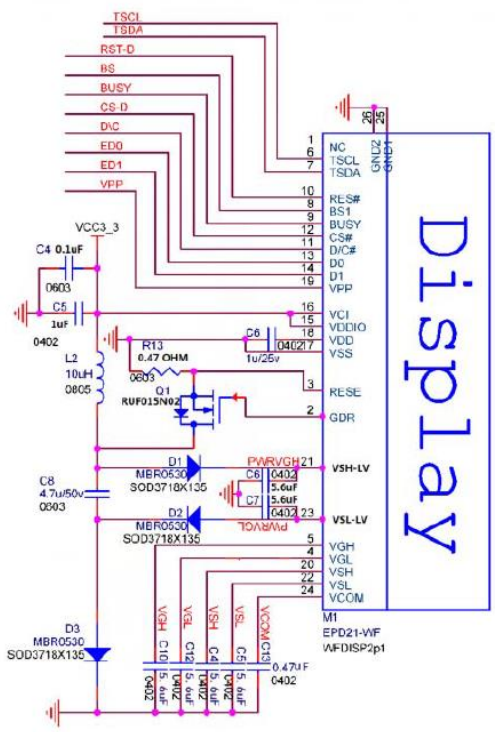


Figure 7-5 (1)

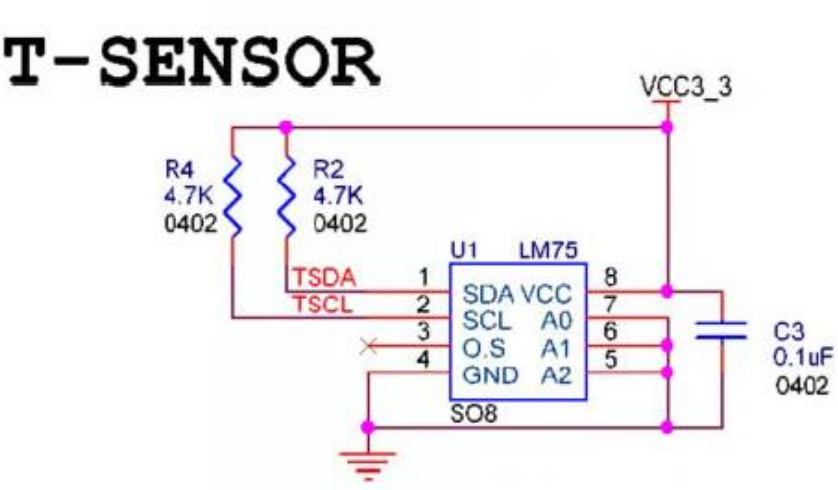
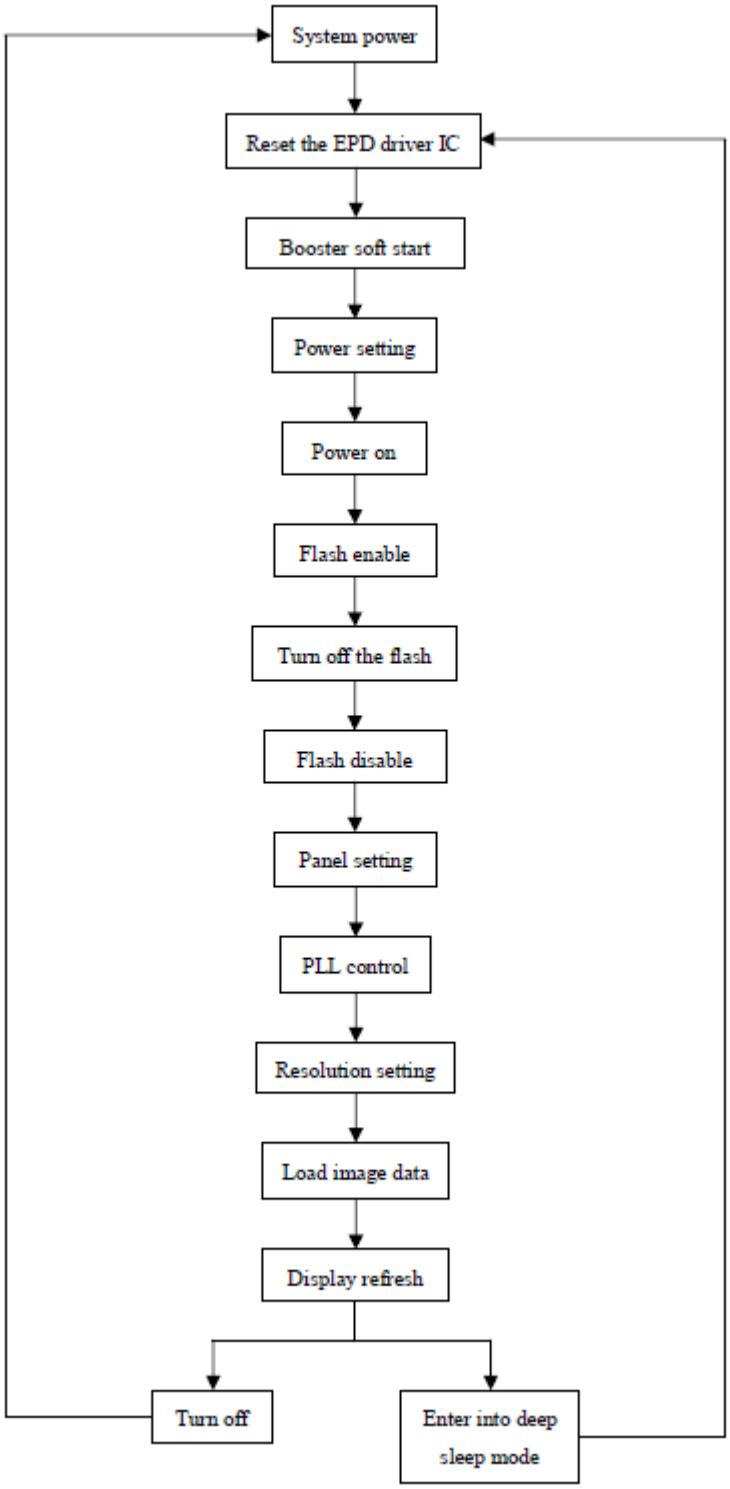


Figure 7-5 (2)

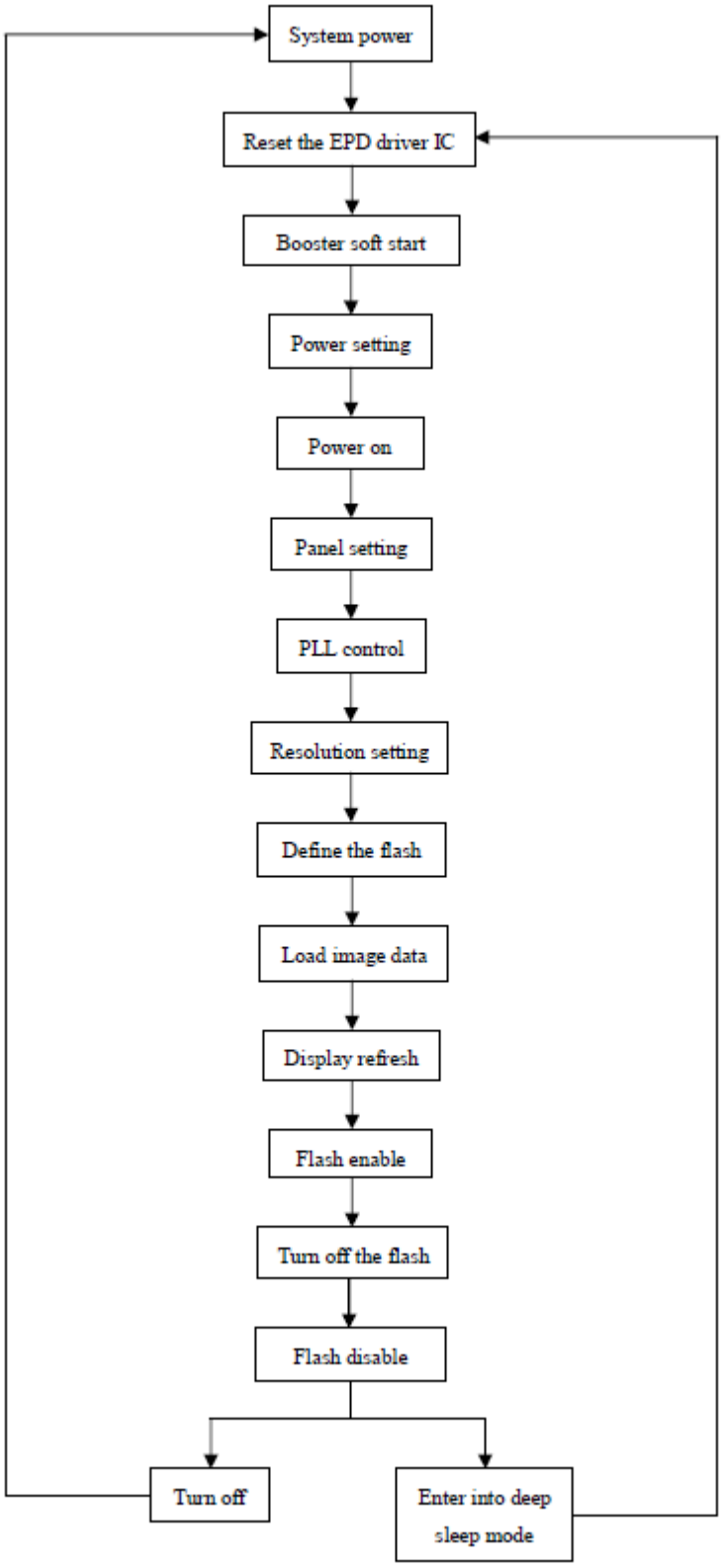
8. Typical Operating Sequence

8.1. Normal Operation Flow

8.1.1. LUT from Register

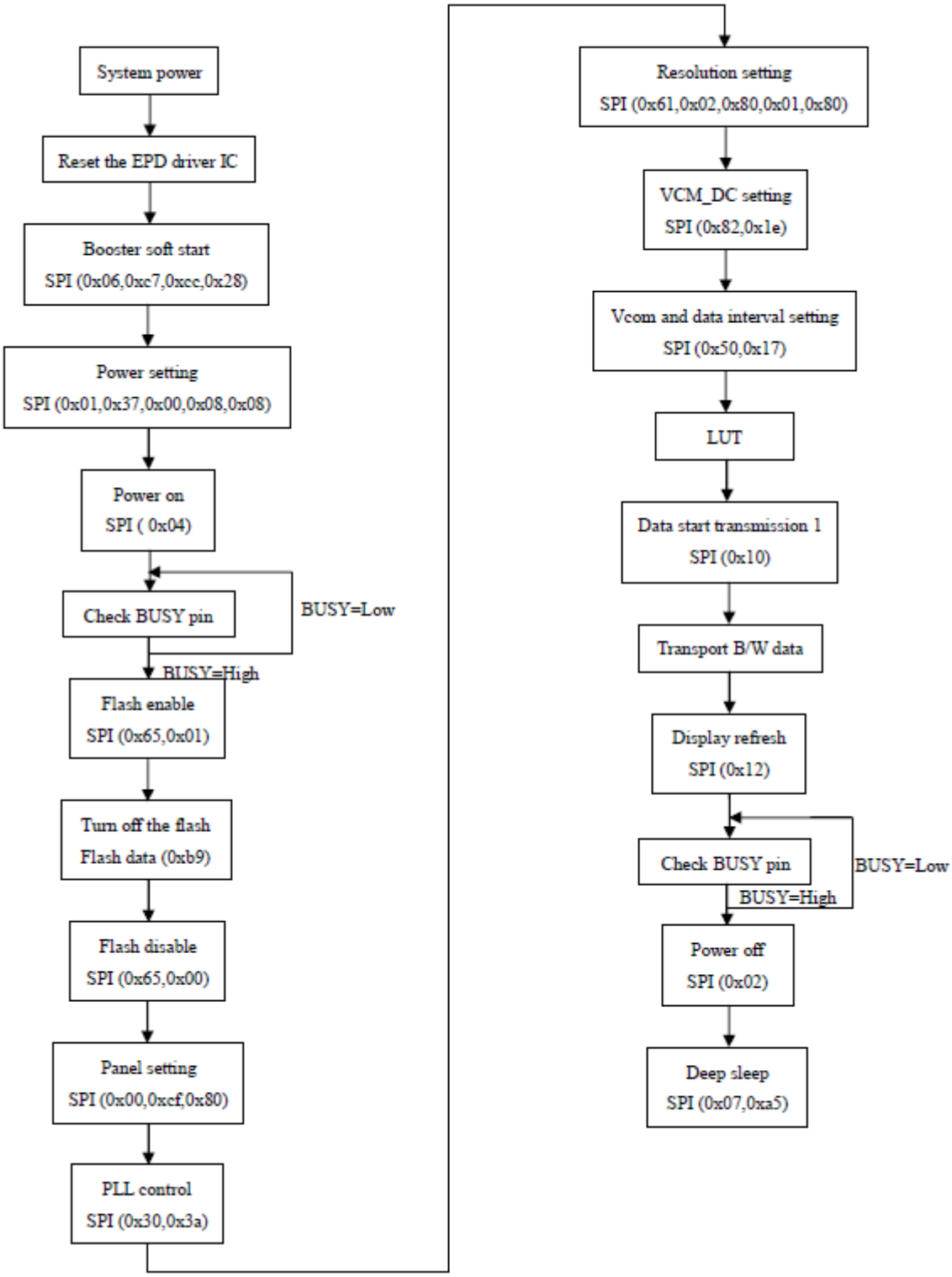


8.1.2. LUT from Flash

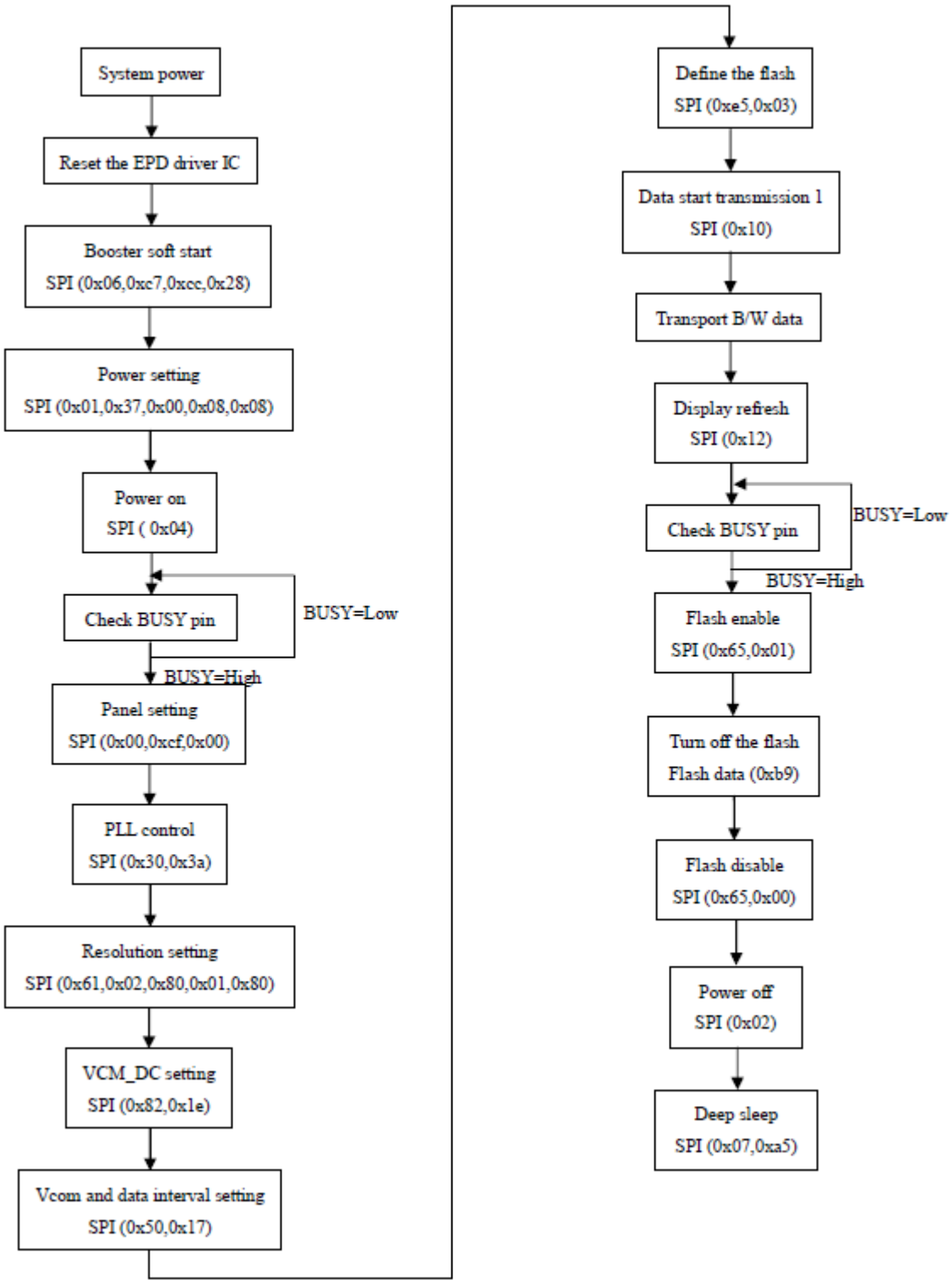


8.2. Reference Program Code

8.2.1. LUT from Register



8.2.2. LUT from Flash



9. Optical Characteristics

9.1. Specifications

Measurements are made with the illumination under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

Symbol	Parameter	Conditions	Min	Type	Max	Unit	Note
R	Reflectance	White	30	35	-	%	Note 9-1
Gn	2Gray Level	-	-	DS＋(WS-DS) x n (m-1)	-	L*	-
CR	Contrast Ratio	Indoor	8		-	-	-
Panel's Life	-	0°C~50°C	-	1,000,000 times or 5 years	-	-	Note 9-2

WS: White State, DS: Dark State

Gray State from Dark to White: DS, WS

m: 2

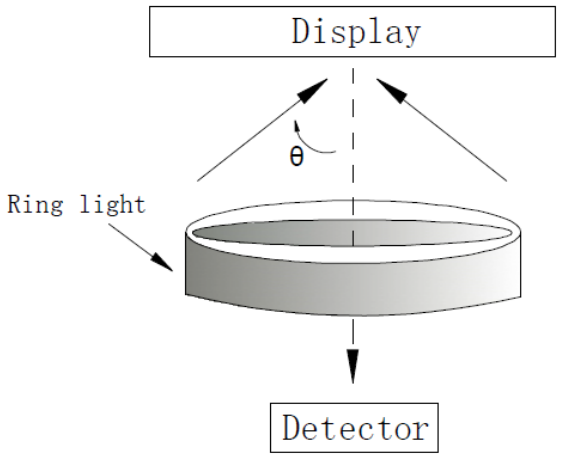
Note (9-1): Luminance meter: Eye – One Pro Spectrophotometer
Note (9-2): Panel life is not guaranteed when worked in temperatures below 0 degrees or above 50 degrees. Each update interval time should be at a minimum of 180 seconds.

9.2. Definition of Contrast Ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) ():

R1: White Reflectance Rd: Dark Reflectance

CR = R1/Rd

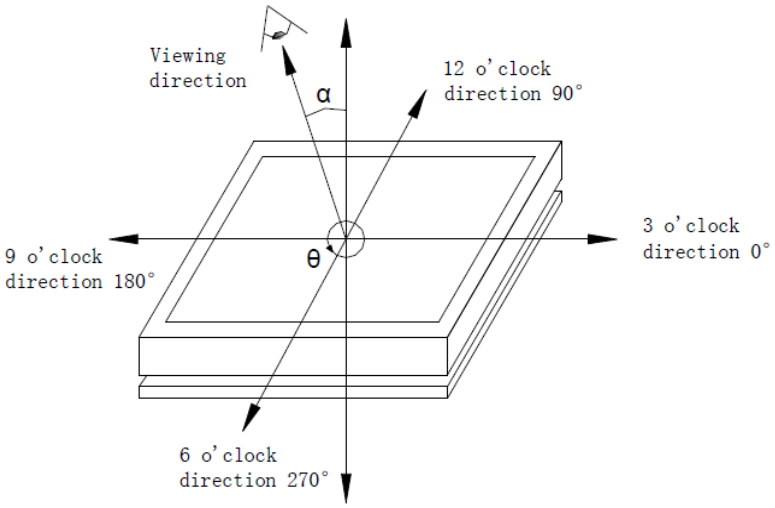


9.3. Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{CENTER} / $L_{WHITE\ BOARD}$)

L_{CENTER} is the luminance measured at center in a white area (R=G =B=1). $L_{WHITE\ BOARD}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

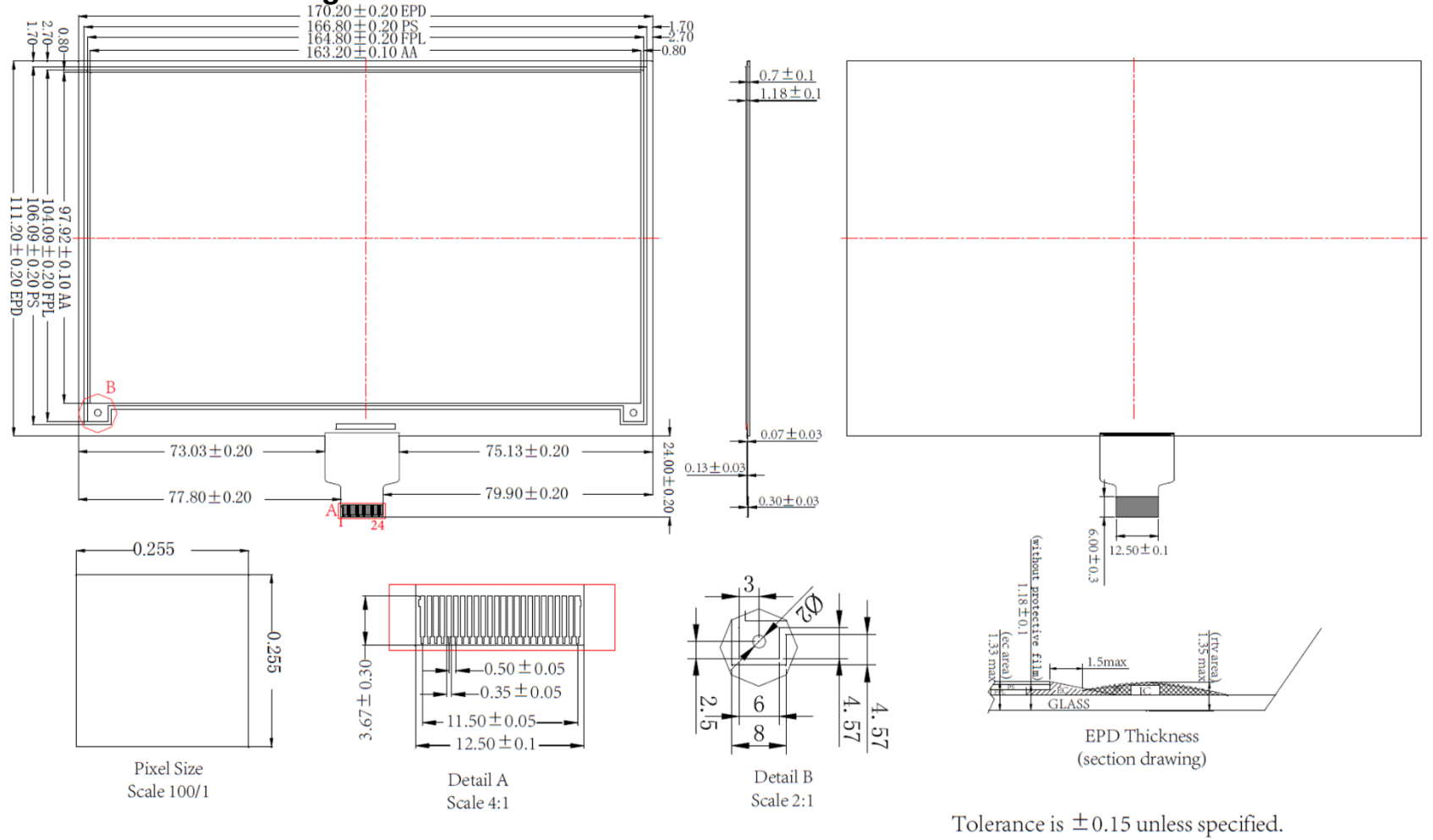


9.4. Bi-Stability

The Bi-Stability standard is as follows:

Bi-Stability	Result		
24-Hour Luminance Drift		AVG	MAX
	White state △L*	-	3
	Black state △L*	-	3

10. Mechanical Drawing



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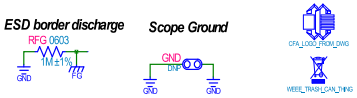
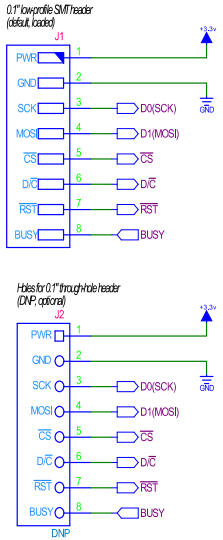
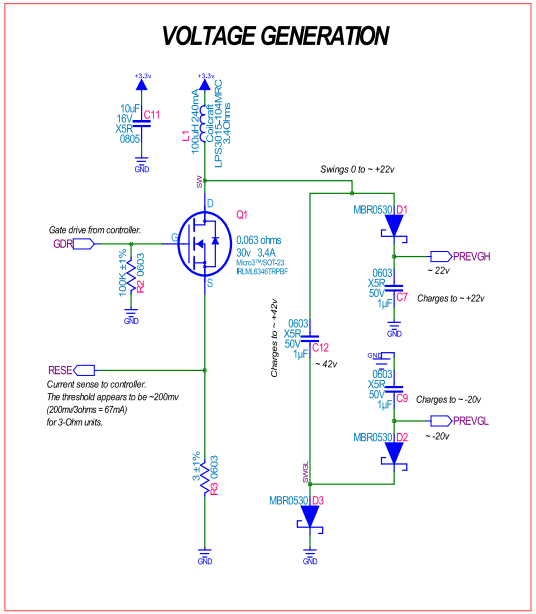
	Location: Datasheet		Sheet: 1 of 1

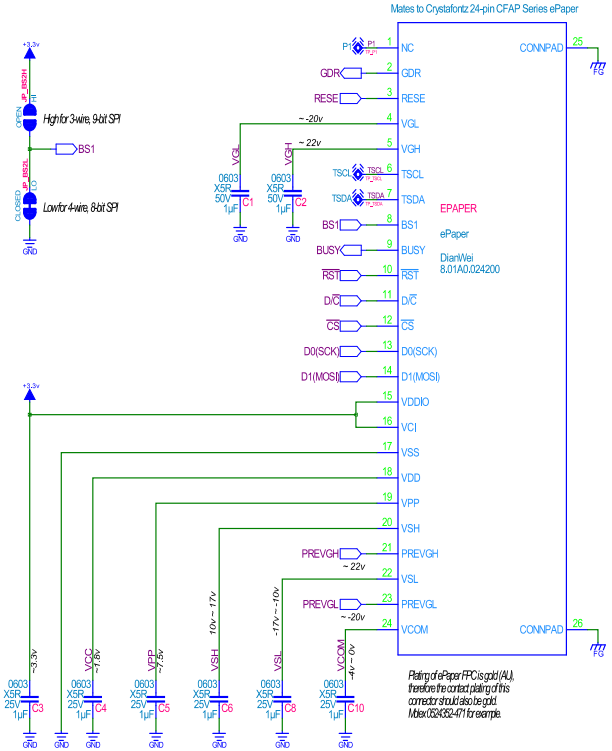
11. ePaper Breakout Board Schematic



REV	ENGINEER	DATE	REMARKS
0v0	BAC	2018-04-04	Initial Creation
0v1	BAC	2018-05-17	Ind val, C12 val, JP_0P47 open, CN FPC
-	-	-	-
-	-	-	-
-	-	-	-







Crystalfontz America, Inc

CFA-10084: ePaper Adapter Board 24-pin (3-ohm)

Page 1 / 1 : Schematic

PRODUCT NAME:	PRODUCT REVISION:	PCB NUMBER:	PCB REVISION:
CFA-10084	0v1	PCB-10084	0v1